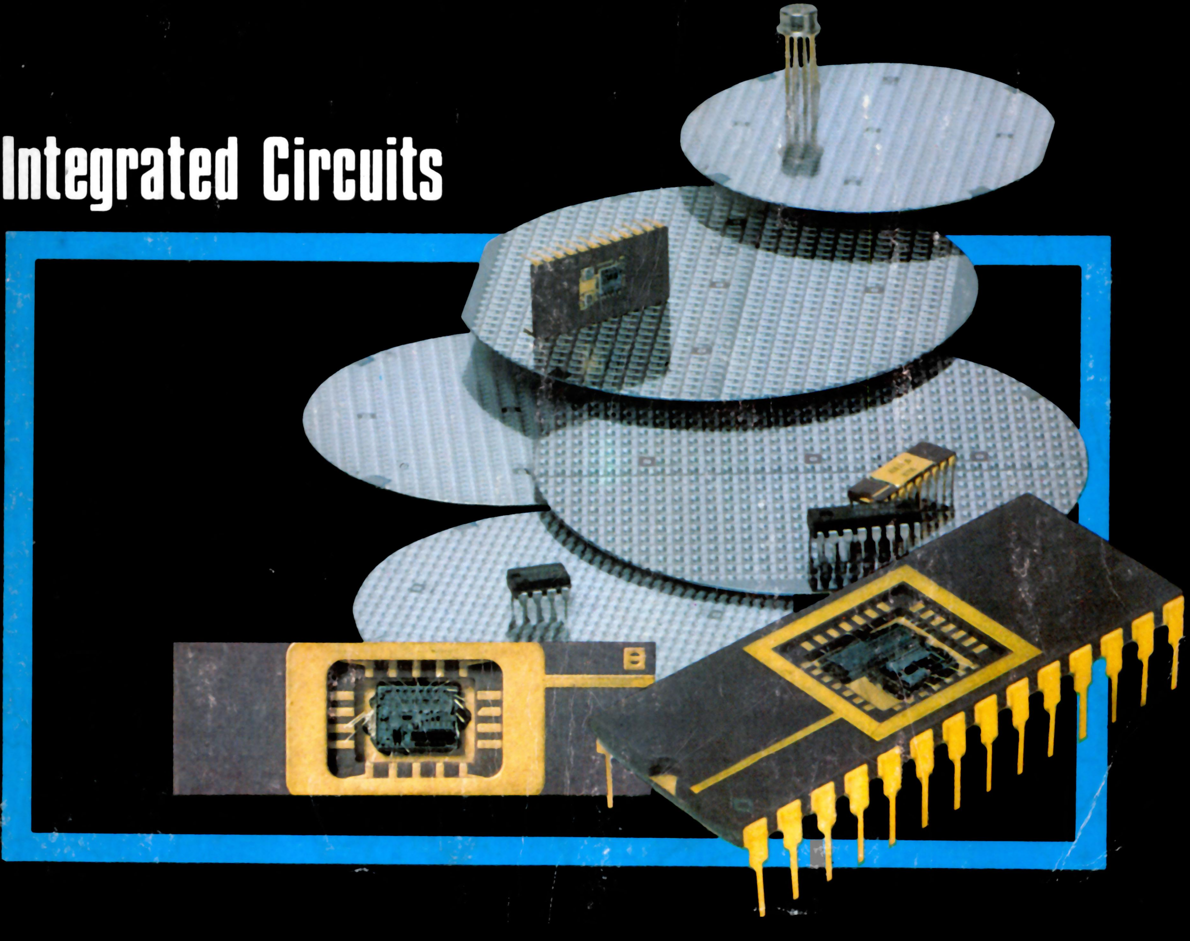
ANALOG
DEVICES

Data-Acquisition Databook 1982

Integrated Circuits



How to Find Product Data in this Databook

HOW TO FIND PRODUCT DATA IN THIS DATABOOK

The Databook contains Data Sheets for all products recommended for new designs, lists of Available Products not databooked here (data sheets upon request), and a Substitution Guide for products no longer available, plus a wealth of background information.

THERE ARE TWO VOLUMES

VOLUME I contains technical data on our *integrated circuits and hybrids* for data acquisition, plus abbreviated data on certain Volume II products that are well-suited to new designs and do not yet have integrated-circuit equivalents.

VOLUME II has all data-acquisition products manufactured in the form of *modules, cards, instruments, and discrete-assembly subsystems*.

DO YOU KNOW THE MODEL NUMBER?

If it's an Analog Devices model number, look it up in the alphanumeric Index (Section 2) to find the Volume, Section, and Page numbers.

If you're looking for a form-and-function-compatible version of a product originally brought to market by some other manufacturer (second source), add our "AD" prefix and look it up in the Index.

IF YOU DON'T KNOW THE MODEL NUMBER

There are two ways to find a device to perform your function:

1. **FIND YOUR FUNCTION IN THE LIST ON THE OPPOSITE PAGE**
   Use the "bleed tabs" to turn directly to the appropriate Section. You will find one or more functional Selection Guides at the beginning of the Section. The Selection Guide will help you find the products that are closest to satisfying your need, and their Volume-Section-Page locations. Use it to compare all products in the category by salient criteria, no matter which Volume their technical data resides in.

2. **IF THE FUNCTION IS NOT LISTED BY A NAME THAT YOU RECOGNIZE**
   Find it in the diagram (opposite page) or in the Index (Section 2). The Index will help you find the Selection Guides for products in that functional category. Then use the Selection Guide(s) to find the Volume-Section-Page locations of products that will come closest to satisfying your need.

A RELATED PRODUCT MAY BE WHAT YOU REALLY WANT

Text in each section often mentions related or complementary product categories having a greater or lesser degree of functional integration.

IF YOU CAN'T FIND IT HERE . . . ASK!

See Worldwide Service Directory in last pages of this Volume.

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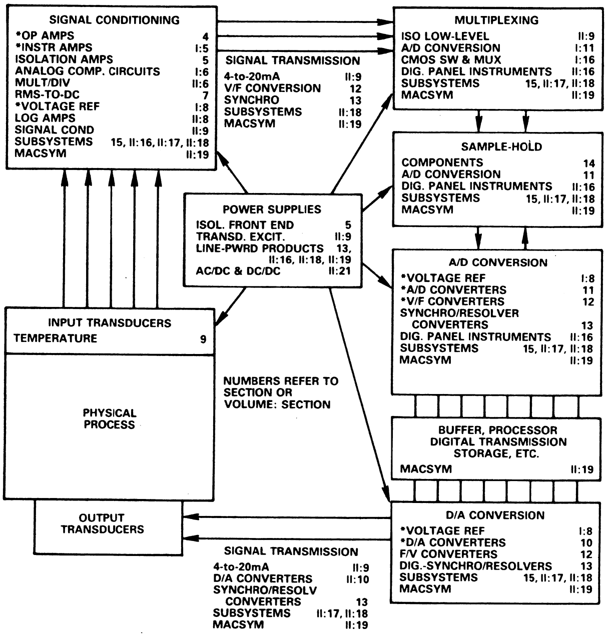
DATA-ACQUISITION DATABOOK 1982

VOLUME I
INTEGRATED CIRCUITS

General Information 1
Comprehensive Index to Both Volumes 2
Ordering Guide 3
Operational Amplifiers 4
Instrumentation & Isolation Amplifiers 5
Analog Computational Circuits 6
RMS-to-DC Converters 7
Voltage References 8
Transducers 9
Digital-to-Analog Converters 10
Analog-to-Digital Converters 11
Voltage-Frequency Converters 12
Synchro & Resolver Converters 13
Sample/Track-Hold Amplifiers 14
Data-Acquisition Subsystems 15
CMOS Switches & Multiplexers 16
Monolithic Chips 17
Linear IC Test Systems 18
Quality Assurance Program 19
Package Information 20
Application Notes 21

PICTORIAL GUIDE TO PRODUCT CATEGORIES

LINEAR IC TEST SYSTEMS–I:18, II:20
MACSYM MEASUREMENT AND CONTROL SYSTEM–II:19



*Automatic Test Instrumentation Available (I:18, II:20)

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DATA-ACQUISITION DATABOOK 1982

VOLUME I: INTEGRATED CIRCUITS

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Specifications and prices shown in this Databook are subject to change without notice.

Products in this book may be covered by one or more of the following patents. Additional patents are pending. See individual data sheets for further information:

U.S.: 3,007,114, 3,278,736, 3,355,670, 3,441,913, 3,467,908, 3,500,218, 3,530,390, 3,533,002, 3,685,045, 3,729,660, 3,747,088, 3,793,563, 3,803,590, 3,842,412, 3,868,583, 3,872,466, 3,887,863, 3,890,611, 3,906,486, 3,909,908, 3,932,863, 3,940,760, 3,942,173, 3,946,324, 3,950,603, 3,961,326, 3,978,473, 3,979,688, 4,016,559, 4,020,486, 4,029,974, 4,034,366, 4,092,698, 4,123,698, 4,136,349, 4,141,004, 4,213,806, 4,250,445, 4,270,118, 4,268,759, 4,054,829, 4,286,225. U.K.: 1,310,591, 1,310,592, 1,364,233, 1,470,673, 1,470,674, 1,537,542, 1,531,931, 1,571,869, 1,590,136, 1,590,137. France: 70.10561, 71.28952, 74.25263, 76 08238. West Germany: 20 14 034, 21 39 560. Italy: 933,798. Canada: 1,025,558, 1,035,464, 984,015, 1,006,236, 1,054,248. Sweden: 7603320-8.

Contents

Page

Contents 1-1
General Introduction 1-2
Contents of Volume II (back) 1-3

Selection Guides for Product Categories Not Included in this Volume

  Signal Conditioners (back) 1-4
  Digital Panel Instruments (back) 1-6
  Microcomputer Analog I/O Subsystems (back) 1-9
  AC/DC and DC/DC Power Supplies (back) 1-11
Product Families Not Included in the Databook But Still Available (back) 1-13
Substitution Guide for Product Families No Longer Available (back) 1-14
Technical Publications (back) 1-15
Worldwide Service Directory (back) 1-16

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General Introduction

Analog Devices designs, manufactures, and sells worldwide sophisticated electronic components and subsystems for use in precision measurement and control. More than six hundred standard products are produced in manufacturing facilities located throughout the world. These facilities encompass all relevant technologies, including bipolar, I^2L, CMOS, and hybrid integrated circuits–and assembled products in the form of potted modules, printed-circuit boards, and instrument packages.

State-of-the-art technologies have been utilized (and, in many cases, invented) to provide timely, reliable, easy-to-use advanced designs at realistic prices. More than fifteen years of successful applications experience and continuing vertical integration insure that these products are oriented to user needs. The continuing application of present state-of-the-art and the invention of future state-of-the-art processes strengthens the leadership position of Analog Devices in data-acquisition products.

MAJOR PROGRESS

Since the publication of our one-volume Databook, *Data Acquisition Components and Subsystems Catalog*, in 1980, more than 60 significant new products have been introduced. They are identified by bullets (●) in the Index and in the table of contents for each section of this Databook. The sheer mass of new products, the impressive volume of technical data on our large and rapidly growing line of precision integrated circuits, and the increasing diversity of our modular and subsystem product lines for precision data acquisition and control have led us to take the logical step of dividing the Databook into two Volumes, retaining within each the functional organization that our customers have found so useful.

INTEGRATED CIRCUITS

The list of product-category "bleed tabs" opposite the "How to Find It" Guides on the inside front cover of this Volume is a functional summary of our integrated-circuit and hybrid component and subsystem product classes. The complete Index, starting on page 2-1, provides a detailed alphanumeric panorama of products and functions, irrespective of technology, appearing in either or both Volumes of this Databook.

Among the most significant of our new products, in terms of both user applications and advancement of the technology, are the monolithic 16-bit AD7581 CMOS D/A converter; the monolithic 8-channel 8-bit AD7581 CMOS data-acquisition system with data continuously available in 8 channels of on-board memory; the AD547 family of monolithic drift-trimmed high-performance FET-input op amps and its AD647 matched-dual version; the AD7528 monolithic dual D/A converter; the high-performance AD293/294 hybrid isolation amplifiers, based on an ingenious thick-film printed transformer and a significant advance in isolator circuit design; and the µMAC-4000 Intelligent Single-Board Data-Acquisition System and its high-performance plug-in analog signal conditioners–with available software for using popular micro- and minicomputers as host computers.

TECHNICAL SUPPORT

Analog Devices offers extensive technical literature, which discusses the technology and applications of products for precision measurement and control. Besides comprehensive data sheets, of which there are many outstanding examples in this book, we offer Application Notes, Application Guides, Technical Handbooks (at reasonable prices), and two serial publications: *Analog Productlog* which provides brief information on new products being introduced, and *Analog Dialogue*, our technical journal, which provides-in-depth discussions of new developments in analog and digital circuit technology as applied to data-acquisition and control. We maintain a mailing list of engineers, scientists, and technicians with a serious interest in our products. In addition to data-book catalogs–such as this one–we also publish several short-form catalogs, including a *Short-Form Guide* to our entire product line. You will find our publications described on page 1-15 at the back of the book.

SALES OFFICES

Backing up our design and manufacturing capabilities and our extensive array of publications is a network of sales offices and representatives throughout the United States and most of the world. They are staffed by experienced sales and applications engineers, and many of them maintain a local stock of Analog Devices products. Our Worldwide Service Directory appears on pages 1-16 and 1-17 at the back of the book.

STANDARDS

Many products comply with MIL-STD-883B and/or other customer requirements. Analog Devices Semiconductor has complete capabilities for 100% screening of devices per Methods 5004 and 5005 of MIL-STD-883B; generic data is available on many of our products. Our CMOS facility in the Republic of Ireland has received plant approval from the European standardization authority; its quality-assurance procedures and capabilities have met the standards of CECC (CENELEC Electronic Components Committee), which are essentially compatible with what are known in the U.S.A. as MIL-M-38510 and MIL-STD-883B. A summary of our IC quality assurance procedures appears in Section 19 of Volume I.

PRODUCTS NOT CATALOGUED HERE

On page 1-3, at the back of this book, you will find a table listing the sections (bleed tabs) to be found in the other Volume of the Databook. In the pages that follow it, you will find Selection Guides listing salient characteristics of products in categories that are to be found exclusively in that volume.

For maximum usefulness to designers of new equipment, without unwieldy size, we have limited the contents of the Databook to products most likely to be used for the design of new circuits and systems. If the data sheet for a product you are interested in is not in either Volume turn to page 1-13, at the back of this book, where you will find a list of older products for which data sheets are available upon request. On page 1-14 you will find a guide to substitutions for products no longer available.

PRICES

At Analog Devices, we recognize that accurate, up-to-date prices of our products are an important consideration in making a choice among the many available product families. However, since prices are subject to change, current price lists and/or quotations are available upon request from our sales offices.

(this section continues at the back of the book)

Comprehensive Index to Both Volumes

Alphanumerically by Product
Alphabetically by Function

PRODUCT OR FUNCTION†	Vol. I	Vol. II
AC2626 General-Purpose Temperature Probe		9 – 5
AD 101A General-Purpose Low-Cost MIL-Temp IC Op Amp	4 – 17	
AD 201A General-Purpose Low-Cost Industrial-Temp IC Op Amp	4 – 17	
•AD293 Hybrid Industrial Isolation Amplifier	5 – 27	5 – 7*
•AD294 Hybrid Medical Isolation Amplifier	5 – 27	5 – 7*
AD 301A General-Purpose Low-Cost Commercial-Temp IC Op Amp	4 – 17	
AD 301AL Low-Drift, Low-Cost Commercial-Temp IC Op Amp	4 – 17	
•AD 346 High-Speed Sample-and-Hold Amplifier	14 – 7	
AD362 Precision Sample-and-Hold with 16-Channel Multiplexer	15 – 5*	15 – 5
AD363 Complete 16-Channel 12-Bit Integrated-Circuit DAS	15 – 13*	15 – 9
AD364 Fast, Complete 16-Channel μP-Compatible 12-Bit DAS	15 – 25*	15 – 13
AD 370/371 Complete Low-Power 12-Bit D/A Converter	10 – 11	
•AD 380 Wideband Fast-Settling FET-Input Op Amp	4 – 21	
•AD 381 High-Speed Low-Drift FET-Input Op Amp	4 – 23	
•AD 382 High-Speed Low-Drift FET-Input Op Amp	4 – 25	
•AD 390 Quad 12-Bit μP-Compatible D/A Converter	10 – 15	
AD503 High Accuracy Low-Offset FET-Input IC Op Amps	4 – 27	
AD504 High-Accuracy IC Operational Amplifier	4 – 31	
AD506 High-Accuracy Low-Offset FET-Input IC Op Amps	4 – 27	
AD507 IC Wideband Fast-Slewing, General-Purpose IC Op Amp	4 – 39	
•AD509 High-Speed Fast-Settling IC Op Amp	4 – 43	
AD510 Low-Cost, Laser-Trimmed, Precision IC Op Amp	4 – 47	
AD515 Precision, Low-Power FET-Input Electrometer Op Amp	4 – 51	
AD517 Low-Cost, Laser-Trimmed Precision IC Op Amp	4 – 57	
AD518 Low-Cost, High-Speed, IC Operational Amplifier	4 – 63	
AD521 IC Precision Instrumentation Amplifier	5 – 9	
AD522 High-Accuracy Data-Acquisition Instrumentation Amplifier	5 – 15	
AD524 Precision Instrumentation Amplifier	5 – 19	
AD532 Internally Trimmed Integrated Circuit Multiplier	6 – 11	
AD533 Low-Cost IC Multiplier, Divider, Squarer, Square-Rooter	6 – 17	
AD534 Internally Trimmed Precision IC Multiplier	6 – 21	
AD535 Internally Trimmed Integrated-Circuit Divider	6 – 29	
AD536A Integrated-Circuit True-RMS-to-DC Converter	7 – 7	
AD537 Integrated-Circuit Voltage-to-Frequency Converter	12 – 7	
•AD539 Wideband 2-Channel, 2-Quadrant, Log-Linear Multiplier	6 – 35	
AD540 High-Accuracy, Low-Cost, FET-Input Op Amp	4 – 67	
AD542 Precision Low-Cost BIFET Op Amp	4 – 71	
AD544 High-Speed Implanted FET-Input Op Amp	4 – 77	
AD545 Precision, Low-Drift FET-Input Op Amp	4 – 83	
•AD547 Ultra-Low-Drift BIFET Operational Amplifier	4 – 87	
AD558 DACPORT™ Low-Cost Complete μP-Compatible 8-Bit DAC	10 – 17	
Interfacing the AD558 to Microprocessors (Application Note)	21 – 31	
AD561 Low-Cost 10-Bit Monolithic D/A Converter	10 – 25	
AD562 IC 12-Bit D/A Converter	10 – 33	
AD563 IC 12-Bit D/A Converter with Reference	10 – 33	
AD565 Complete High-Speed 12-Bit Monolithic D/A Converter	10 – 39	
•AD565A Complete High-Speed 12-Bit Monolithic D/A Converter	10 – 43	
AD566 Low-Cost High-Speed 12-Bit Monolithic D/A Converter	10 – 51	
•AD566A Low-Cost High-Speed 12-Bit Monolithic D/A Converter	10 – 55	
AD567 Microprocessor Compatible 12-Bit D/A Converter	10 – 63	
AD570 Low-Cost Complete IC 8-Bit A/D Converter	11 – 11	
AD571 Integrated-Circuit 10-Bit A/D Converter	11 – 15	
AD572 12-Bit Successive-Approximation IC A/D Converter	11 – 23	
•AD573 Fast, Complete 10-Bit A/D Converter with μP Interface	11 – 31	
•AD574A Fast, Complete 12-Bit A/D Converter with μP Interface	11 – 39	
AD578 Very Fast, Complete 12-Bit A/D Converter	11 – 47	
•AD579 Very Fast Complete 10-Bit A/D Converter	11 – 53	
AD580 High Precision 2.5-Volt IC Reference	8 – 5	
AD581 High Precision 10-Volt IC Reference	8 – 9	
AD582 Low-Cost Sample/Hold Amplifier	14 – 9	
AD583 IC Sample-and-Hold, Gated Op Amp	14 – 13	
AD584 Pin-Programmable Precision Voltage Reference	8 – 15	
AD589 Two-Terminal IC 1.2-Volt Reference	8 – 21	
AD590 Two-Terminal IC Temperature Transducer	9 – 5*	9 – 7
AD612/614 Self-Contained Wideband High-Performance Instrumentation Amplifier	5 – 23	
AD636 Low-Level True-RMS-to-DC Converter	7 – 13	
AD642 Precision Low-Cost Dual BIFET Op Amp	4 – 93	

†Functions are listed alphabetically and are intermixed with products listed in alphanumeric order. Products with numerical model numbers or prefixes follow at the end of the alphabetic listing.
•New product since *1980 Data-Acquisition Components and Subsystems Catalog*
*Principal Listing

	Vol. I	Vol. II
•AD644 Dual High-Speed Implanted FET-Input Op Amp	4 – 99	
•AD647 Ultra-Low-Drift Dual BIFET Op Amp	4 – 105	
AD650 Voltage-to-Frequency and Frequency-to-Voltage Converter	12 – 15	
•AD673 Fast, Complete 8-Bit ADC, with µP Interface	11 – 59	
AD 741J/K/L/S Lowest Cost High-Accuracy IC Op Amps	4 – 111	
AD 1403/1403A Low-Cost Precision 2.5-Volt IC Reference	8 – 25	
AD 1408 8-Bit Monolithic Multiplying D/A Converter	10 – 71	
AD 1508 8-Bit Monolithic Multiplying D/A Converter	10 – 71	
AD2004 4 1/2-Digit DPM for System Applications		16 – 13
AD2006 AC-Powered 3 1/2-Digit DPM with Sperry Display		16 – 15
AD2009 3 1/2-Digit Line-Powered Digital Panel Meter		16 – 19
AD2010 Low-Cost 3 1/2-Digit DPM for OEM Applications		16 – 23
AD2016 Low-Cost 3 1/2-Digit Line-Powered DPM with LED Display		16 – 27
AD2021 Low-Cost 3 1/2-Digit Logic-Powered DPM with LED Display		16 – 31
AD2024 Line-Powered 4 1/2-Digit DPM with LED Displays		16 – 33
AD2025 Line-Powered 4 3/4-Digit DPM with LED Displays		16 – 37
AD2026 Low-Cost 3-Digit Analog-Panel-Meter Replacement		16 – 41
AD2027 Logic-Powered 4 1/2-Digit DPM with LED Displays		16 – 33
AD2028 Logic-Powered 4 3/4-Digit DPM with LED Displays		16 – 37
AD2033 True-rms/dB Multirange Line-Powered 3 1/2-Digit DPM		16 – 43
AD2036 6-Channel Scanning Digital Thermocouple Thermometer		16 – 47
AD2037 6-Channel Scanning Digital Voltmeter		16 – 49
AD2038 6-Channel Scanning Digital Thermometer		16 – 49
AD2040 Low-Cost Temperature Indicator for AD590 Sensor		16 – 51
•AD2050 Intelligent Thermocouple Meter for User-Specified Sensor		16 – 55
•AD2051 Intelligent Thermocouple Meter for User-Selected Sensor		16 – 55
AD2700/2702 ±10-Volt Precision Reference Series	8 – 29	
•AD2710 ±10.000-Volt Ultra-High Precision Reference Series	8 – 33	
•AD 3554 Wideband, Fast-Settling, FET-Input Op Amp	4 – 115	
•AD 3860 Complete Voltage-Output 12-Bit DAC	10 – 75	
AD 5200 12-Bit Successive-Approximation High-Accuracy ADC	11 – 63	
•AD 5210 12-Bit Successive-Approximation High-Accuracy ADC	11 – 67	
•AD 5240 Very Fast Complete 12-Bit A/D Converter	11 – 73	
AD7110 CMOS Digitally Controlled Audio Attenuator	10 – 79	
•AD7111 LOGDAC™ CMOS Logarithmic D/A Converter	10 – 85	
•AD7118 LOGDAC™ CMOS Logarithmic D/A Converter	10 – 91	
AD7501 CMOS 8-Channel Multiplexer	16 – 5	
AD7502 CMOS Dual 4-Channel Multiplexer	16 – 5	
AD7503 CMOS 8-Channel Multiplexer	16 – 5	
AD7506 CMOS 16-Channel Multiplexer	16 – 9	
AD7507 CMOS Dual 8-Channel Multiplexer	16 – 9	
AD7510DI Dielectrically Isolated CMOS Quad SPST Switches	16 – 13	
AD7511DI Dielectrically Isolated CMOS Quad SPST Switches	16 – 13	
AD7512DI Dielectrically Isolated CMOS Dual SPDT Switches	16 – 13	
AD7520 CMOS 10-Bit Monolithic Multiplying D/A Converter	10 – 97	
AD7521 CMOS 12-Bit Monolithic Multiplying D/A Converter	10 – 97	
AD7522 CMOS 10-Bit Buffered Multiplying D/A Converter	10 – 105	
AD7523 CMOS 8-Bit Multiplying D/A Converter	10 – 111	
AD7524 CMOS 8-Bit Buffered Multiplying DAC	10 – 115	
AD7525 3 1/2-BCD Monolithic CMOS Digitally Controlled Pot	10 – 121	
•AD7527 CMOS 10-Bit (Systems) D/A Converter	10 – 127	
•AD7528 CMOS Dual-8-Bit Buffered Monolithic Multiplying DAC	10 – 139	
AD7530 CMOS 10-Bit Monolithic Multiplying D/A Converter	10 – 147	
AD7531 CMOS 12-Bit Monolithic Multiplying D/A Converter	10 – 147	
AD7533 CMOS Low-Cost 10-Bit Multiplying DAC	10 – 151	
AD7541 CMOS 12-Bit Monolithic Multiplying DAC	10 – 157	
•AD7541A CMOS 12-Bit Monolithic Multiplying DAC	10 – 163	
AD7542 Microprocessor-Compatible 12-Bit DAC	10 – 165	
AD7543 CMOS Serial-Input 12-Bit DAC	10 – 173	
•AD7544 CMOS 12-Bit 6-Word FIFO D/A Converter	10 – 181	
•AD7545 CMOS 12-Bit Buffered Multiplying DAC	10 – 189	
•AD7546 CMOS 16-Bit Multiplying DAC	10 – 197	
AD7550 CMOS 13-Bit Monolithic A/D Converter	11 – 81	
•AD7552 CMOS 12-Bit-Plus-Sign Monolithic A/D Converter	11 – 89	
AD7555 CMOS 4 1/2 – 5 1/2-Digit ADC Subsystem	11 – 101	
AD7574 CMOS Microprocessor-Compatible 8-Bit A/D Converter	11 – 113	
•AD7581 CMOS µP-Compatible 8-Bit 8-Channel DAS	11 – 121	
•AD7590DI DI CMOS Latched Quad SPST Switch	16 – 21	
•AD7591DI DI CMOS Latched Quad SPST Switch	16 – 21	
•AD7592DI DI CMOS Latched Dual SPDT Switch	16 – 21	
AD ADC80 12-Bit Successive-Approximation IC A/D Converter	11 – 129	
•AD ADC84/85 Fast, Complete 12-Bit A/D Converters	11 – 137	

•New product since *1980 Data-Acquisition Components and Subsystems Catalog*

	Vol. I	Vol. II
ADC1130/1131 14-Bit High-Speed Analog-to-Digital Converters	11 – 145	11 – 11*
•ADC1140 Low-Cost 16-Bit A/D Converter	11 – 147	11 – 15*
A/D Conversion, see A/D Converters		
A/D Converters		
as Components	11 – 1	11 – 1
in Data-Acquisition Subsystems	15 – 1	15 – 1
in Digital Panel Instruments		16 – 1
in Intelligent Single-Board Data Acquisition Subsystems		18 – 1
in MACSYM		19 – 1
in Microcomputer Analog I/O Cards (RTIs)		17 – 1
Monolithic Chips	17 – 1	
Sample/Track-Hold Amplifiers for	14 – 1	14 – 1
Test Systems for	18 – 1	20 – 1
Voltage References for	8 – 1	
ADCs, see A/D Converters		
AD DAC-08-Bit Monolithic High-Speed Multiplying D/A Converter	10 – 205	
•AD DAC71/72 High-Resolution 16-Bit D/A Converters	10 – 211	
AD DAC80 Low-Cost 12-Bit IC D/A Converter	10 – 215	
AD DAC85 High-Performance 12-Bit IC D/A Converter	10 – 223	
AD DAC87 Wide-Temperature-Range 12-Bit IC D/A Converter	10 – 231	
•AD DAC100 10-Bit Monolithic D/A Converter	10 – 235	
ADG 200 DI CMOS Protected Dual SPST Analog Switch	16 – 29	
ADG 201 DI CMOS Protected Quad SPST Analog Switch	16 – 33	
•AD LH0032 Ultra-Fast FET Operational Amplifier	4 – 117	
•AD LH0033 High-Speed Buffer Amplifiers	4 – 121	
AD OP-07 Ultra-Low Offset-Voltage Op Amp	4 – 125	
•AD SHC85 Fast 0.01% Track/Sample-Hold Amplifiers	14 – 17	
•AD SHM-5 Ultra Fast 0.01% Track/Sample-Hold Amplifiers	14 – 21	14 – 7*
AD VFC32 V/F and F/V Converter	12 – 17	
Amplifiers, Instrumentation		
Applications	21 – 21	
as Components	5 – 1*	1 – 4
in Data-Acquisition Subsystems	15 – 1	15 – 1
in Digital Panel Instruments		16 – 1
in Intelligent Data Acquisition Systems		18 – 1
in MACSYM Measurement And Control SYsteMs		19 – 4
in Microcomputer Analog I/O Subsystems (RTIs)		17 – 1
Monolithic Chips	17 – 1	
in Signal Conditioners		9 – 1
Test Systems for	18 – 1	20 – 1
Amplifiers, I.C., Guide to Decoupling, Grounding, etc.	21 – 13	
Amplifiers, Isolation		
as Components	5 – 1	5 – 1
in Data-Acquisition Subsystems	15 – 1	15 – 1
in Digital Panel Instruments		16 – 1
in Intelligent Data Acquisition Systems		18 – 1
Isolated Op Amp, see 277		
in MACSYM Measurement And Control SYsteMs		19 – 4
in Signal Conditioners		9 – 1
Amplifiers, Operational	4 – 1	4 – 1
How to Select (Application Note)	21 – 3	
How to Test Basic Parameters (Application Note)	21 – 9	
Isolated, see 277		
Monolithic Chips	17 – 1	
Test Systems for	18 – 1	20 – 1
Amplifier, Power, Synchro/Resolver		13 – 1
Analog Computational ICs	6 – 1	
Analog Devices Sales Offices	1 – 16	1 – 10
Analog Devices Technical Publications	1 – 15	1 – 9
Analog I/O Subsystems		
Data-Acquisition Subsystems as Components	15 – 1	15 – 1
Digital Panel Instruments		16 – 1
Intelligent Measurement and Control Subsystems (μMAC-4000)		18 – 1
MACSYM I/O Cards		19 – 4
Microcomputer Analog I/O Boards (RTIs)		17 – 1
Analog-to-Digital Converters, see A/D Converters		
Antilog Amplifiers	6 – 1	8 – 1
see also Logarithmic D/A Converters	10 – 1	
•API1620/1718 Synchro/Resolver Angle-Position Indicator Displays		13 – 5
Application Notes, Linear ICs	21 – 1	
Chips, Monolithic	17 – 1	

•New product since *1980 Data-Acquisition Components and Subsystems Catalog*
*Principal Listing

	Vol. I	Vol. II
CMOS D/A Converters	10 – 1	
Application Notes	21 – 41	
CMOS Switches and Multiplexers	16 – 1*	1 – 6
Application Note	21 – 41	
Cold-Junction Compensators, Thermocouple		
in Signal Conditioners		9 – 1
in Digital Panel Instruments		16 – 1
in MACSYM Measurement And Control SYsteMs		19 – 4
in µMAC Intelligent Measurement and Control Systems		18 – 1
Compensators, Cold-Junction, Thermocouple, see Cold-Junction		
Computational Circuits, Analog, see also:	6 – 1	
Antilog Amplifiers	6 – 1	8 – 1
Dividers, Analog	6 – 1	6 – 1
Logarithmic Amplifiers	6 – 1	8 – 1
Multipliers, Analog	6 – 1	6 – 1
Powers and Roots	6 – 1	6 – 1
Squaring	6 – 1	6 – 1
Square Rooting	6 – 1	6 – 1
Computer-Based		
Data Acquisition (µMAC-4000)		18 – 1
Measurement And Control SYsteMs (MACSYM)		19 – 1
Test Systems for Linear ICs	18 – 1	20 – 1
Conditioners, Signal, as Components, see also:	1 – 4	9 – 1*
Instrumentation Amplifiers	5 – 1	
Isolation Amplifiers	5 – 1	5 – 1
Data-Acquisition Subsystems	15 – 1	15 – 1
Digital Panel Instruments		16 – 1
µMAC Intelligent Single-Board Meas. & Control Subsystem		18 – 1
MACSYM Computer-Based Measurement And Control SYsteM		19 – 4
Converters, Analog-to-Digital	11 – 1	11 – 1
Converters, DC/DC	1 – 11	21 – 1*
Converters, Digital-to-Analog	10 – 1	10 – 1
Converters, Digital-to-Angle	13 – 1	13 – 1
Converters, Digital-to-Resolver	13 – 1	13 – 1
Converters, Digital-to-Synchro	13 – 1	13 – 1
Converters, Frequency-to-Voltage	12 – 1	12 – 1
Converters, Inductosyn-to-Digital	13 – 1	13 – 1
Converters, Resolver-to-Digital	13 – 1	13 – 1
Converters, RMS-to-DC	7 – 1	7 – 1
Converters, Synchro-to-Digital	13 – 1	13 – 1
Converters, Voltage-to-Current, see Signal Conditioners		
Converters, Voltage-to-Frequency	12 – 1	12 – 1
DAC-08 (see AD DAC-08)		
DAC71/72 (see AD DAC71/72)		
DAC80 (see AD DAC80)		
DAC85 (see AD DAC85)		
DAC87 (see AD DAC87)		
DAC100 (see AD DAC100)		
DAC1106 8/10-Bit-Resolution High-Speed D/A Converter		10 – 11
DAC1108 12-Bit-Resolution High-Speed D/A Converter		10 – 11
DAC1136 High-Resolution 16-Bit Digital-to-Analog Converter	10 – 243	10 – 15*
DAC1138 High-Resolution 18-Bit Digital-to-Analog Converter	10 – 243	10 – 15*
DAC1420 8-Bit D/A Converter with 4-to-20mA Output	10 – 245	10 – 23
DAC1422 10-Bit D/A Converter with 4-to-20mA Output	10 – 245	10 – 23
DAC1423 4-to-20mA Output 10-Bit Isolated D/A Converter	10 – 247	10 – 27*
DACs, see D/A Converters		
D/A Converters		
Application Notes for CMOS DACs	21 – 41	
as Components	10 – 1	10 – 1
Interfacing the AD558 DACPORT™ to Microprocessors	21 – 31	
Logarithmic DACs	10 – 1	
MACSYM Measurement And Control SYsteM (Analog Output Cards)		19 – 4
Microcomputer Analog I/O (Output) Subsystems		17 – 1
Monolithic Chips	17 – 1	
DAS1128 Low-Cost High-Speed Data-Acquisition Subsystem	15 – 37	15 – 17*
•DAS1152 14-Bit Sampling A/D Converter	15 – 39	15 – 25*
•DAS1153 15-Bit Sampling A/D Converter	15 – 39	15 – 25*
•DAS1155 14-Bit Low-Level Data-Acquisition System	15 – 41	15 – 29*
•DAS1156 15-Bit Low-Level Data-Acquisition System	15 – 41	15 – 29*
Data-Acquisition Cards		
Microcomputer Analog I/O Subsystems (RTIs)	1 – 9	17 – 1*
µMAC Intelligent Measurement and Control Subsystems		18 – 1

•New product since *1980 Data-Acquisition Components and Subsystems Catalog*
*Principal Listing

	Vol. I	Vol. II
MACSYM Measurement And Control SYsteMs		19 – 4
Data-Acquisition ICs, see Vol. I listings of: A/D Converters, Analog Computational Circuits, CMOS Switches and Multiplexers, D/A Converters, Data-Acquisition Subsystems, Instrumentation and Isolation Amplifiers, Operational Amplifiers, RMS-to-DC Converters, Sample/Track-Hold Amplifiers, Synchro & Resolver Converters, Transducers, V/F Converters, Voltage References		
Data-Acquisition Subsystems as Components	15 – 1	15 – 1
DC/DC Converters	1 – 11	21 – 1*
DG200, DG201 (see ADG 200, ADG 201)		
Digital Panel Instruments	1 – 6	16 – 1*
Digital Thermometers	1 – 8	16 – 1*
Digital-to-Analog Converters	10 – 1	10 – 1
Digital-to-Resolver Converters	13 – 1	13 – 1
Digital-to-Synchro Converters	13 – 1	13 – 1
Digital Vector Generator	13 – 1	13 – 1
see also Application Note (Generating Waveforms & Vectors)	21 – 43	
Digital Voltmeters, Scanning	1 – 6	16 – 1*
Dividers, Analog	6 – 1	6 – 1
DSC1705 14-Bit Digital-to-Synchro/Resolver Converter		13 – 9
DSC1706 12-Bit Digital-to-Synchro/Resolver Converter		13 – 9
DTM1716 14-Bit Digital-to-Analog Vector Generator		13 – 13
DTM1717 12-Bit Digital-to-Analog Vector Generator		13 – 13
Frequency-to-Voltage Converters	12 – 1	12 – 1
HAS Series Ultra-Fast Hybrid Analog-to-Digital Converters	11 – 149	
•HDD Series Hybrid Video Low-Glitch D/A Converters	10 – 249	
•HDD1206 12-Bit Deglitched Voltage-Output D/A Converter	10 – 255	
HDG Series Hybrid Video Digital-to-Analog Converters	10 – 259	
HDH Series 8-,10-,12-Bit Video-Speed Hybrid Voltage-Out DACs	10 – 265	
HDS Series 8-,10-,12-Bit Video-Speed Hybrid Current-Out DACs	10 – 265	
•HDS-0810E Ultra-High-Speed ECL Hybrid 8-Bit D/A Converter	10 – 269	
HDS-1015E Ultra-High-Speed ECL Hybrid 10-Bit D/A Converter	10 – 269	
•HDS-1240E Ultra-High-Speed ECL Hybrid 12-Bit D/A Converter	10 – 271	
HOS050/050A/050C Fast-Settling Video Operational Amplifier	4 – 131	
•HOS100 Wide-Bandwidth High-Speed Buffer Amplifiers	4 – 137	
HTC Series Ultra-High-Speed Track-and-Hold Amplifiers	14 – 23	
HTS Series Ultra-High-Speed Track-and-Hold Amplifiers	14 – 23	
Inductosyn™-to-Digital Converters	13 – 1	13 – 1
Instrumentation Amplifiers	5 – 1*	1 – 4
Integrated Circuits (see Volume I)		
Application Notes	21 – 1	
Monolithic Chips	17 – 1	
Package Information	20 – 1	
Quality Assurance	19 – 1	
Test System, Computer-Based	18 – 1	20 – 1
Interface Boards, Microcomputer		
Microcomputer Analog I/O Subsystems (RTIs)	1 – 9	17 – 1*
μMAC Intelligent Measurement and Control Subsystem		18 – 1
•IRDC1730 Inductosyn/Resolver-to-Digital (Binary) Converter		13 – 17
•IRDC1731 Inductosyn/Resolver-to-Digital (Pulses) Converter		13 – 23
Isolated Op Amps, see 277		
Isolated Signal Conditioners		
Isolators	5 – 1	5 – 1
Signal Conditioners	1 – 4	9 – 1*
see also sections 16, 17, 18, 19 in Volume II		
Isolation Amplifiers, Isolators	5 – 1	5 – 1
see also sections 9, 16, 17, 18, 19 in Volume II		
Linear-Circuit Testers, Computer-Based	18 – 1	20 – 1
Log Amplifiers	6 – 1	8 – 1
Log-Antilog Amplifiers	6 – 1	8 – 1
see also Logarithmic DACs in D/A Converter Section	10 – 1	10 – 1
Log-Ratio Modules	6 – 1	8 – 1
LTS-2000 Computer-Based Automatic Test System for Linear ICs	18 – 3	20 – 1
LTS-2010 Computer-Based Automatic Test System for Linear ICs	18 – 4	20 – 1
MACSYM Computer-Based Measurement And Control SYsteMs		
ADIO Analog-Digital Input/Output Cards		19 – 4
MACSYM 2 Fully Integrated Measurement and Control SYsteM		19 – 1
MACSYM 10 Measurement and Control SYsteM for Industrial Applications		19 – 2
MACSYM 20 Low-Cost Intelligent Front End		19 – 3
MAH-0801 Ultra-High-Speed 8-Bit A/D Converter	11 – 153	11 – 19*
MAH-1001 Ultra-High-Speed 10-Bit A/D Converter	11 – 153	11 – 19*

•New product since *1980 Data-Acquisition Components and Subsystems Catalog*
*Principal Listing

	Vol. I	Vol. II
MAS-0801 Ultra-High-Speed 8-Bit A/D Converter	11 – 155	11 – 23*
MAS-1001 Ultra-High-Speed 10-Bit A/D Converter	11 – 155	11 – 23*
MAS-1202 Ultra-High-Speed 12-Bit A/D Converter	11 – 155	11 – 23*
MATV Series 8-Bit Video Analog-to-Digital Converters	11 – 157	11 – 27*
MDD Series Ultra-High-Speed Deglitched D/A Converters		10 – 23
MDMS Series Ultra-High-Speed Multiplying D/A Converters	10 – 275	10 – 37
MDS/MDSE/MDSL/MDH Series 8-,10-,12-Bit Video-Speed Current-Output DACs		10 – 39
Microcomputer Analog I/O Boards	1 – 9	17 – 1*
"Micromac"(μMAC-4000) Intelligent Single Board Measurement and Control Subsystem		18 – 1
MOD-1005 10-Bit Video A/D Converter	11 – 159	11 – 31*
MOD-1020 10-Bit Video A/D Converter	11 – 161	11 – 35*
MOD-1205 12-Bit Video A/D Converter	11 – 163	11 – 39*
Monolithic Chips	17 – 1	
Multichannel A/D Converters	11 – 1	
see also all listings under A/D Converters		
Multichannel Signal Conditioners	1 – 4	9 – 1*
see also Sections 16, 17, 18, 19 in Volume II		
Multifunction Devices	6 – 1	6 – 1
Multifunction Modules		6 – 1
Multiplexed Signal Conditioners (see Signal Conditioners)	1 – 4	9 – 1*
Multiplexers, CMOS	16 – 1*	1 – 6
Multiplier/Dividers	6 – 1	6 – 1
Multipliers, Analog	6 – 1	6 – 1
μMAC-4000 Intelligent Measurement and Control Subsystem		18 – 1
Operational Amplifiers (Op Amps)	4 – 1	4 – 1
Operational Amplifiers, Isolated, see 277		
Package Information, Integrated Circuits	20 – 1	
Power Amplifier, Synchro/Resolver		13 – 1
Powers and Roots	6 – 1	6 – 1
Power Supplies	1 – 11	21 – 1*
see also Self-Powered		
Power Supplies, AC/DC	1 – 11	21 – 1*
Power Supplies, DC/DC	1 – 11	21 – 1*
Power Supplies, Transducer Excitation		9 – 1
Publications, Technical, of Analog Devices	1 – 15	1 – 9
Quality Assurance, Integrated Circuits	19 – 1	
RDC1727 High-Resolution Resolver-to-Digital (18 Bits)		13 – 49
RDC1740/1741/1742 Resolver-to-Digital Converters	13 – 5	13 – 53*
References, Voltage	8 – 1*	1 – 5
Resolver Power Amplifier	13 – 1	13 – 1
Resolver-to-Digital Converters	13 – 1	13 – 1
Resolver-to-Linear Converters	13 – 1	13 – 1
RMS-to-DC Converters	7 – 1	7 – 1
RTD Signal Conditioners, see Signal Conditioners		
RTI-1200 MULTIBUS-Compatible Combination Analog I/O Subsystem		17 – 5
RTI-1201 MULTIBUS-Compatible Analog Output Subsystem		17 – 7
RTI-1202 MULTIBUS-Compatible Analog Input Subsystem		17 – 9
RTI-1225 STD-Bus-Compatible Analog Input/Output Subsystem		17 – 11
•RTI-1226 STD-Bus-Compatible Analog Input Subsystem		17 – 11
RTI-1230 Motorola-Compatible Analog Input Subsystem		17 – 13
RTI-1231 Motorola-Compatible Analog I/O Subsystem		17 – 13
RTI-1232 Motorola-Compatible Analog Output Subsystem		17 – 13
RTI-1240 TM990/100M-Compatible Analog Input Subsystem		17 – 15
RTI-1241 TM990/100M-Compatible Analog I/O Subsystem		17 – 15
RTI-1242 TM990/100M-Compatible Analog Output Board (4 DACs)		17 – 15
RTI-1243 TM990/100M-Compatible Analog Output Board (8 DACs)		17 – 15
RTI-1250 DEC-Compatible Analog Input Subsystem		17 – 17
RTI-1251 DEC-Compatible Analog I/O Subsystem		17 – 17
RTI-1252 DEC LSI-Compatible Analog Output Subsystem		17 – 17
•RTI-1260 High-Performance Analog-Input Card for STD Bus		17 – 19
•RTI-1261 High-Performance Analog-Output Card for STD Bus		17 – 19
RTM Series 5VA Resolver Output Transformers		13 – 27
SAC1763 Synchro/Resolver-to-Analog Converter		13 – 31
Sales Offices of Analog Devices	1 – 16	1 – 10
Sample-Hold Amplifiers, see also A/D Converters	14 – 1	14 – 1
Sample/Track-Hold Amplifiers, see also A/D Converters	14 – 1	14 – 1
SBCD1752 Synchro/Resolver-to-Digital (13 BCD + Sign), 0°C to ± 180°C		13 – 35
SBCD1753 Synchro/Resolver-to-Digital (14 BCD), 0°C to ± 180°C		13 – 35
SBCD1756 Synchro/Resolver-to-Digital (13 BCD + Sign), 0°C to 360°C		13 – 35
SBCD1757 Synchro/Resolver-to-Digital (14 BCD), 0°C to 360°C		13 – 35
SDC1700 Synchro/Resolver-to-Digital (12 Bits)		13 – 39

•New product since *1980 Data-Acquisition Components and Subsystems Catalog*
*Principal Listing

	Vol. I	Vol. II
SDC1702 Synchro/Resolver-to-Digital (10 Bits)		13 – 39
SDC1704 Synchro/Resolver-to-Digital (14 Bits)		13 – 39
SDC1725 Synchro/Resolver-to-Digital (12 Bits), Low Profile		13 – 45
SDC1726 Synchro/Resolver-to-Digital (10 Bits), Low Profile		13 – 45
•SDC1727 High-Resolution Synchro-to-Digital (18 Bits)		13 – 49
•SDC1740/1741/1742 Synchro-to-Digital Converters	13 – 5	13 – 53*
Self-Powered Instruments, Subsystems, and Systems		
Digital Panel Instruments		16 – 1
Signal Conditioners		9 – 1
Microcomputer Analog I/O Subsystems		17 – 1
μMAC Measurement and Control Subsystems		18 – 1
MACSYM Measurement And Control SYsteMs		19 – 1
Linear-IC Test Systems		20 – 1
SHA1144 High-Resolution 14-Bit Sample-and-Hold Amplifier	14 – 29	14 – 11*
Signal Conditioners as Components, see also:	1 – 4	9 – 1*
Instrumentation Amplifiers	5 – 1	
Isolation Amplifiers	5 – 1	5 – 1
Data-Acquisition Subsystems	15 – 1	15 – 1
Digital Panel Instruments		16 – 1
μMAC Intelligent Single-Board Meas. & Control Subsystem		18 – 1
MACSYM Computer-Based Measurement And Control SYsteM		19 – 1
SPA1695 5VA-Output Power Amplifier for Synchros/Resolvers		13 – 57
Squaring (Analog Multipliers)	6 – 1	6 – 1
Square Rooting (Analog Dividers)	6 – 1	6 – 1
STM Series 5VA Synchro Output Transformers		13 – 27
Strain Gage Signal Conditioners see also Signal Conditioners	1 – 4	9 – 1*
Switches, CMOS	16 – 1*	1 – 6
Switches, Dielectrically Isolated	16 – 1	
Switches, Dual	16 – 1	
Switches, Quad	16 – 1	
Synchro Power Amplifiers	13 – 1	13 – 1
Synchro-to-Digital Converters	13 – 1	13 – 1
Synchro-to-Linear Converters	13 – 1	13 – 1
Technical Publications of Analog Devices	1 – 15	1 – 9
Temperature Indicators		16 – 1
Temperature Transducers	9 – 1	9 – 1
Temperature Transmitters, see Signal Conditioners	1 – 4	9 – 1*
Testers, Linear Integrated Circuits	18 – 1	20 – 1
THC Series Fast Sample/Track-and-Hold Amplifiers		14 – 15
Thermocouple Cold-Junction Compensators, see Signal Conditioners		
Thermocouple Signal Conditioners, see Signal Conditioners		
Thermometers, Digital, see Digital Panel Instruments	1 – 8	16 – 1*
THS Series Ultra-Fast Sample/Track-and-Hold Amplifiers		14 – 15
Track-Hold Amplifiers, see also A/D Converters	14 – 1	14 – 1
Transducers	9 – 1	9 – 1
Transducers, Temperature-to-Current (AC2626, AD590)	9 – 1	9 – 1
Transmitters, 4-to-20mA, see Signal Conditioners	1 – 4	9 – 1*
Transmitters, Temperature, see Signal Conditioners	1 – 4	9 – 1*
TSL1612 2-Speed Processor for Coarse/Fine Synchros/Resolvers		13 – 59
UMAC-4000, see μMAC-4000 or "Micromac"		
Vector Generator, Digital	13 – 1	13 – 1
see also App. Note: Generating Waveforms and Vectors	21 – 43	
V/F Converters	12 – 1	12 – 1
Voltage References	8 – 1*	1 – 5
Voltage-to-Current Converters, see Signal Conditioners	1 – 4	9 – 1*
Voltage-to-Frequency Converters	12 – 1	12 – 1
Voltmeters, Digital, Scanning, (Digital Panel Instruments)	1 – 6	16 – 1*
2B20 4-to-20mA-Voltage-to-Current Converter		9 – 9
2B22 Isolated 4-to-20mA Voltage-to-Current Converter		9 – 13
•2B24 Loop-Powered Isolator		9 – 17
2B30 Strain-Gage/RTD Signal Conditioner		9 – 19
2B31 Strain-Gage/RTD Signal Conditioner with X'ducer Excitation		9 – 19
•2B34 Four-Channel RTD/Strain-Gage Conditioner		9 – 25
2B35 Precision Triple-Output Transducer Power Supply		9 – 29
•2B50 Isolated Thermocouple Signal-Conditioner		9 – 31
•2B52 Isolated Two-Wire Thermocouple Temperature Transmitter		9 – 35
•2B53 Two-Wire Thermocouple Temperature Transmitter		9 – 35
2B54 Low-Level 4-Channel Multiplexed Isolated Conditioner		9 – 37
2B55 4-Channel Multiplexed Isolated Conditioner		9 – 37
2B56 High-Accuracy Thermocouple Cold-Junction Compensator		9 – 43
2B57 Low-Cost Two-Wire Temperature Transmitter for AD590		9 – 47

•New product since *1980 Data-Acquisition Components and Subsystems Catalog*
*Principal Listing

	Vol. I	Vol. II
•2B58 Two-Wire Linearized RTD Temperature Transmitter		9 – 51
•2B59 Low-Cost 2-Wire RTD Temperature Transmitter		9 – 53
48 Fast-Settling Differential FET-Input Op Amp		4 – 17
50/51 Fast-Settling, Wideband, 100mA Output FET-Input Op Amp		4 – 19
52 Low-Noise, Low-Drift Precision FET-Input Amplifier	4 – 139	4 – 21
171 High-Voltage Differential FET-Input Amplifier	4 – 141	4 – 23
234 Low-Noise Wideband Chopper-Stabilized Amplifier	4 – 143	4 – 25
235 Economy, Guaranteed Low-Noise Chopper-Stabilized Amplifier	4 – 143	4 – 25
261 Low-Noise, Non-Inverting Chopper Amplifier	4 – 145	4 – 27
277 Precision Isolation Amplifier with Op-Amp Front End		5 – 15
281 100kHz Isolator Excitation Oscillator		5 – 17
284J Economy High-Performance Self-Contained Isolation Amplifer		5 – 17
286J High-CMV, High-Performance Synchronized Isolation Amplifier		5 – 17
289 Precision Wide-Bandwidth Synchronized Isolation Amplifier	5 – 35	5 – 23*
290A Low-Cost Single-Channel Isolation Amplifier		5 – 27
292A Low-Cost Multi-Channel Isolation Amplifier		5 – 27
429 Accurate Wideband, Multiplier, Divider, Square-Rooter	6 – 37	6 – 7*
433 Programmable Multifunction Amplifier	6 – 39	6 – 11*
436 High-Accuracy Two-Quadrant Analog Divider		6 – 15
442 Wideband, High-Accuracy True-RMS-to-DC Converter	7 – 19	7 – 7
450 High-Performance 10kHz Voltage-to-Frequency Converter		12 – 7
451 Low-Cost, Versatile 10kHz Frequency-to-Voltage Converter	12 – 21	12 – 11*
453 Low-Cost, Versatile 100kHz F/V Converter	12 – 21	12 – 11*
454 Versatile 20kHz Voltage-to-Frequency Converter		12 – 7
456 Low-Cost 10kHz Full-Scale Voltage-to-Frequency Converter		12 – 7
458 100kHz-Full-Scale High-Accuracy V/F Converter		12 – 17
460 1MHz-Full-Scale High-Accuracy V/F Converter		12 – 17
755N/P 6-Decade High-Accuracy Log/Antilog Amplifiers	6 – 41	8 – 7*
757N/P 6-Decade High-Accuracy Log-Ratio Amplifiers	6 – 43	8 – 11*
759N/P Economy Wideband Log/Antilog Amplifiers	6 – 41	8 – 7*
902/902-2 Dual 15V 100mA AC/DC Power Supply module	1 – 11	21 – 2*
903 Single 5V 500mA AC/DC Power Supply module	1 – 11	21 – 2*
904 Dual 15V 50mA AC/DC Power Supply module	1 – 11	21 – 2*
905 Single 5V 1A AC/DC Power Supply module	1 – 11	21 – 2*
906 Single 5V 250mA AC/DC Power Supply module	1 – 11	21 – 2*
915 Dual 15V 25mA AC/DC Power Supply module	1 – 11	21 – 2*
920 Dual 15V 200mA AC/DC Power Supply module	1 – 11	21 – 2*
921 Dual 12V 240mA AC/DC Power Supply module	1 – 11	21 – 2*
922 Single 5V 2A AC/DC Power Supply module	1 – 11	21 – 2*
923 Triple ± 15V 100mA, 5V 500mA AC/DC Power Supply module	1 – 11	21 – 2*
925 Dual 15V 350mA AC/DC Power Supply module	1 – 11	21 – 2*
•926 Triple ± 15V 150mA, 5V 300mA AC/DC Power Supply module	1 – 11	21 – 2*
•927 Triple ± 15V 150mA, 5V 1A AC/DC Power Supply module	1 – 11	21 – 2*
•928 Single 5V 3A AC/DC Power Supply module	1 – 11	21 – 2*
940 5V to ± 15V 150mA DC/DC Converter module	1 – 11	21 – 2*
941 5V to ± 12V 150mA DC/DC Converter module	1 – 11	21 – 2*
943 5V to 5V 1A DC/DC Converter module	1 – 11	21 – 2*
945 28V to ± 15V 150mA DC/DC Converter module	1 – 11	21 – 2*
949 5V to ± 15V 60mA DC/DC Converter module	1 – 11	21 – 2*
951 5V to ± 15V 410mA DC/DC Converter module	1 – 11	21 – 2*
952 Dual 15V 100mA AC/DC Power Supply (chassis)	1 – 11	21 – 2*
953 12V to ± 15V 150mA DC/DC Converter module	1 – 11	21 – 2*
955 Single 5V 1A AC/DC Power Supply (chassis)	1 – 11	21 – 2*
•957 5V to 5V 100mA DC/DC Converter module	1 – 11	21 – 2*
•958 5V to 5V 100mA DC/DC Converter module	1 – 11	21 – 2*
•959 5V to ± 12V 40mA DC/DC Converter module	1 – 11	21 – 2*
•960 5V to ± 12V 40mA DC/DC Converter module	1 – 11	21 – 2*
•961 5V to ± 15V 33mA DC/DC Converter module	1 – 11	21 – 2*
•962 5V to ± 15V 33mA DC/DC Converter module	1 – 11	21 – 2*
•963 12V to ± 15V 33mA DC/DC Converter module	1 – 11	21 – 2*
•964 12V to ± 15V 33mA DC/DC Converter module	1 – 11	21 – 2*
•965 5V to ± 15V 190mA DC/DC Converter module	1 – 11	21 – 2*
•966 12V to ± 15V 190mA DC/DC Converter module	1 – 11	21 – 2*
•967 24V to ± 15V 190mA DC/DC Converter module	1 – 11	21 – 2*
•968 28V to ± 15V 190mA DC/DC Converter module	1 – 11	21 – 2*
970 Dual 15V 200mA AC/DC Power Supply (chassis)	1 – 11	21 – 2*
•972 Triple ± 15V 150mA, 5V 300mA AC/DC Power Supply (chassis)	1 – 11	21 – 2*
973 Dual 15V 350mA AC/DC Power Supply (chassis)	1 – 11	21 – 2*
•974 Triple ± 15V 150mA, 5V 1A AC/DC Power Supply (chassis)	1 – 11	21 – 2*
975 Dual 15V 500mA AC/DC Power Supply (chassis)	1 – 11	21 – 2*
•976 Single 5V 3A AC/DC Power Supply (chassis)	1 – 11	21 – 2*

•New product since *1980 Data-Acquisition Components and Subsystems Catalog*
*Principal Listing

Ordering Guide

Contents

	Page
Introduction	3–2
Model Numbering	3–2
Second Source	3–3
Ordering from Analog Devices	3–3
Warranty and Repair Charge Policies	3–3

INTRODUCTION

This Ordering Guide should make it easy to order Analog Devices products, whether you're buying one IC op amp, a multi-option subsystem, or 1000 each of 15 different items. It will help you:

1. Find the correct part number for the options you want.
2. Get a price quotation and place an order with us.
3. Know our warranty for components and subsystems.

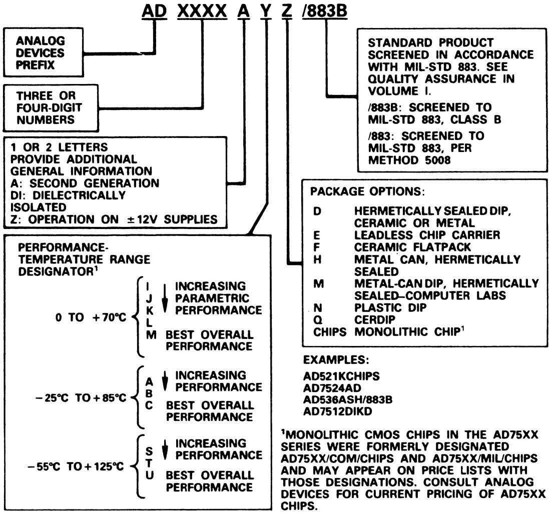
For answers to further questions, call the nearest sales office (listed at the back of the book) or our main office in Norwood, Mass. U.S.A. (617-329-4700).

MODEL NUMBERING

Many of the data sheets in the Databook have an Ordering Guide. Use it to specify the correct part number for the exact combination of options you want. I.C. and hybrid part numbers are created using one of these two systems:

Figure 1 shows the form of model number used for our proprietary standard monolithic ICs and many of our hybrids. It consists of an "AD" (Analog Devices) prefix, a 3- or 4-digit model number, an alphabetic performance/temperature-range designator, a package designator, and a MIL-screening designator (where applicable). One or two additional letters may immediately follow the digits ("A" for second-generation redesigned ICs, "DI" for dielectrically isolated CMOS switches, e.g., AD536AJH, AD7512DIKD).

Figure 2 shows the somewhat different numbering scheme used by our Computer Labs Division for hybrid circuits. The number starts with a three-character alphabetic prefix, followed by a hyphen, a three- or four-digit number, and alphabetic designators (as applicable) to indicate additional functional designations or options, packaging options, and MIL-screening options.


AD XXXX A Y Z /883B
ANALOG DEVICES PREFIX
THREE OR FOUR-DIGIT NUMBERS
1 OR 2 LETTERS PROVIDE ADDITIONAL GENERAL INFORMATION
A: SECOND GENERATION
DI: DIELECTRICALLY ISOLATED
Z: OPERATION ON ±12V SUPPLIES
PERFORMANCE-TEMPERATURE RANGE DESIGNATOR¹
0 TO +70°C
I J K L M
INCREASING PARAMETRIC PERFORMANCE
M BEST OVERALL PERFORMANCE
−25°C TO +85°C
A B C
INCREASING PERFORMANCE
C BEST OVERALL PERFORMANCE
−55°C TO +125°C
S T U
INCREASING PERFORMANCE
U BEST OVERALL PERFORMANCE
STANDARD PRODUCT SCREENED IN ACCORDANCE WITH MIL-STD 883. SEE QUALITY ASSURANCE IN VOLUME I.
/883B: SCREENED TO MIL-STD 883, CLASS B
/883: SCREENED TO MIL-STD 883, PER METHOD 5008
PACKAGE OPTIONS:
D HERMETICALLY SEALED DIP, CERAMIC OR METAL
E LEADLESS CHIP CARRIER
F CERAMIC FLATPACK
H METAL CAN, HERMETICALLY SEALED
M METAL-CAN DIP, HERMETICALLY SEALED–COMPUTER LABS
N PLASTIC DIP
Q CERDIP
CHIPS MONOLITHIC CHIP¹
EXAMPLES:
AD521KCHIPS
AD7524AD
AD536ASH/883B
AD7512DIKD

[1] MONOLITHIC CMOS CHIPS IN THE AD75XX SERIES WERE FORMERLY DESIGNATED AD75XX/COM/CHIPS AND AD75XX/MIL/CHIPS AND MAY APPEAR ON PRICE LISTS WITH THOSE DESIGNATIONS. CONSULT ANALOG DEVICES FOR CURRENT PRICING OF AD75XX CHIPS.

Figure 1. Model-Number Designations for Standard Analog Devices Monolithic and Hybrid IC Products

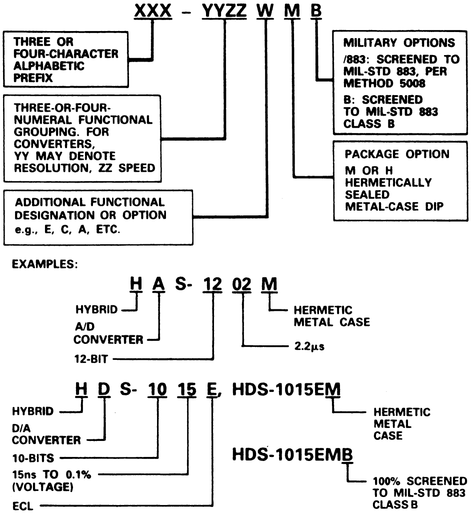

XXX - YYZZ W M B
THREE OR FOUR-CHARACTER ALPHABETIC PREFIX
THREE-OR-FOUR-NUMERAL FUNCTIONAL GROUPING. FOR CONVERTERS, YY MAY DENOTE RESOLUTION, ZZ SPEED
ADDITIONAL FUNCTIONAL DESIGNATION OR OPTION e.g., E, C, A, ETC.
MILITARY OPTIONS
/883: SCREENED TO MIL-STD 883, PER METHOD 5008
B: SCREENED TO MIL-STD 883 CLASS B
PACKAGE OPTION
M OR H HERMETICALLY SEALED METAL-CASE DIP
EXAMPLES:
H A S- 12 02 M
HYBRID
A/D CONVERTER
12-BIT
2.2µs
HERMETIC METAL CASE
H D S- 10 15 E, HDS-1015EM
HYBRID
D/A CONVERTER
10-BITS
15ns TO 0.1% (VOLTAGE)
ECL
HERMETIC METAL CASE
HDS-1015EMB
100% SCREENED TO MIL-STD 883 CLASS B

Figure 2. Computer Labs Video Hybrid Product Designations

SECOND SOURCE

In addition to our many proprietary products, we also manufacture devices that are fit-, form-, and function-compatible (and often superior in performance and reliability) to popular products that originated elsewhere. For such products, we add the prefix "AD" to the familiar model number. (Example: ADDAC85MIL-CBI-V/883).

ORDERING FROM ANALOG DEVICES

When placing an order, please provide specific information regarding model type, number, option designations, quantity, ship-to and bill-to address. Prices quoted are list; they do not include applicable taxes, customs, or shipping charges. All shipments are F.O.B. factory. Please specify if air shipment is required.

Place your orders with our local sales office or representative, or directly with our customer service group located in the Norwood facility. Orders and requests for quotations may be telephoned, sent via TWX or TELEX, or mailed. Orders will be acknowledged when received; billing and delivery information is included.

Payments for new accounts, where open-account credit has not yet been established, will be C.O.D. or prepaid. On all orders under fifty dollars ($50.00), a five-dollar ($5.00) processing charge is required.

When prepaid, orders should include $2.50 additional for packaging and postage (and a 5% sales tax on the price of the goods if you are ordering for delivery to a destination in Massachusetts).

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Operational Amplifiers

Contents

Page

Selection Guides

General Purpose Op Amps 4-2
High Accuracy Op Amps 4-3
Fast/Wideband Op Amps 4-4
Selection Principles and Definitions of Specifications 4-5
AD101A/201A/301A/301AL General-Purpose IC Op Amps 4-17
•AD380J/K/L/S Wideband, Fast-Settling FET Operational Amplifier 4-21
•AD381J/K/L/S High Speed, Low Drift FET Operational Amplifier 4-23
•AD382J/K/L/S High Speed, Low Drift FET Operational Amplifier 4-25
AD503J/K/S FET-Input IC Op Amps 4-27
AD504J/K/L/M/S High-Accuracy Low-Drift IC Op Amps 4-31
AD506J/K/L/S FET-Input IC Op Amps 4-27
AD507J/K/S Wideband General-Purpose IC Op Amps 4-39
AD509J/K/S High-Speed Fast-Settling IC Op Amps 4-43
AD510J/K/L/S High-Accuracy Low-Drift IC Op Amps 4-47
AD515J/K/L Electrometer IC Op Amps 4-51
AD517J/K/L/S High-Accuracy Low Drift IC Op Amps 4-57
AD518J/K/S Fast Wideband IC Op Amps 4-63
AD540J/K/S FET-Input IC Op Amps 4-67
AD542J/K/L/S Trimmed Implanted FET (TRIFET) IC Op Amps 4-71
AD544J/K/L/S Trimmed Implanted FET (TRIFET) IC Op Amps 4-77
AD545J/K/L/M Low Bias Current FET IC Op Amps 4-83
•AD547J/K/L/S Ultra Low Drift BIFET Operational Amplifiers 4-87
AD642J/K/L/S Dual AD542 Trimmed Implanted FET (TRIFET) Op Amps 4-93
•AD644J/K/L/S Dual High-Speed Implanted FET-Input Operational Amplifiers 4-99
•AD647JH/KH/LH/SH Ultra-Low Drift BIFET Operational Amplifiers 4-105
AD741/C/J/K/L/S Internally Compensated IC Op Amps 4-111
•AD3554A/B/S Wideband, Fast-Settling FET-Input Op Amps 4-115
•ADLH0032G/CG Ultra Fast FET Operational Amplifiers 4-117
•ADLH0033G/CG High-Speed Buffer Amplifiers 4-121
AD OP-07/A/D/C/E High-Accuracy Low-Drift IC Op Amps 4-125
HOS-050/050A/050C Ultra Fast Hybrid IC Op Amps 4-131
•HOS-100AH/SH Wide Bandwidth, High-Speed Buffer Amplifiers 4-137
52J/K High-Accuracy Low-Bias FET-Input Op Amps 4-139
171J/K High-Output Op Amps 4-141
234J/K/L Low Noise-Wideband Chopper Stabilized Amplifier 4-143
235J/K/L Inverting Chopper-Stabilized Op Amps 4-143
261J/K Noninverting Chopper Op Amps 4-145

•New product since the *1980 Data-Acquisition Components and Subsystems Catalog*

Selection Guide
Operational Amplifiers

FEATURE SELECTION CHART

		GENERAL PURPOSE								
			FET INPUT						WIDEBAND	
		AD741	AD503	AD506	AD540	AD542	AD642	AD644	AD544	AD101 Series
Monolithic Technology	Bipolar Input	●								●
	J-FET				●	●			●	
	Dual J-FET						●	●		
Multi-Device Technology	Hybrid		●	●	●					
	Module									
High Open Loop Gain	≥100dB					●	●			
	≥140dB									
High CMR	>100dB									
Low Offset Voltage	≤5mV	●		●		●	●	●	●	●
	≤1mV					●	●	●	●	
	≤50µV									
Low Offset V, vs. Temp	≤5µV/°C					●	●	●	●	
	≤1µV/°C									
	≤0.6µV/°C									
Low Bias Current	≤50pA		●	●	●	●	●	●	●	
	≤5pA									
	≤0.5pA									
Fast Settling	≤1µs to 0.1%							●	●	
	≤5µs to 0.01%									
Wideband (Unity Gain)	≥2MHz							●	●	●
	≥10MHz									
High Slew Rate	≥10V/µs							●	●	●
	≥30V/µs									
	≥100V/µs									
	≥1000V/µs									
Low Noise (0.1 to 10Hz) 2µV p-p						●	●	●	●	●
High Voltage Out	≥100V									
High Current Out	≥20mA									
Low Power	≤75mW	●				●	●	●	●	●
Second Source		●								●
Temperature Range										
0 to +70°C		●	●	●	●	●	●	●	●	●
-25°C to +85°C										●
-55°C to +125°C		●	●	●	●	●	●	●	●	●
Dice Availability					●	●	●	●	●	
Volume I Page		4-111	4-27	4-27	4-67	4-71	4-93	4-99	4-77	4-27
Volume II Page		–	–	–	–	–	–	–	–	–

HIGH ACCURACY

LOW V_{OS} DRIFT

LOW BIAS CURRENT

FET INPUT

		AD504	AD510	AD OP-07	AD517	234	235[1]	261[1]	AD545	AD547	AD647	52	AD515	171
Monolithic Technology	Bipolar Input	●	●	●	●									
	J-FET													
	Dual J-FET									●	●			
Multi-Device Technology	Hybrid								●				●	
	Module					●	●	●				●		●
High Open Loop Gain	≥100dB	●	●	●	●	●	●	●		●	●	●		●
	≥140dB					●	●	●						
High CMR	>100dB	●	●	●	●			●				●		●
Low Offset Voltage	≤5mV	●	●	●	●	●	●	●	●			●	●	●
	≤1mV					●	●	●		●	●	●		●
	≤50µV			●	●	●	●	●						
Low Offset V, vs. Temp	≤5µV/°C	●	●	●	●	●	●	●	●	●	●	●		
	≤1µV/°C					●	●	●		●	●	●		
	≤0.6µV/°C	●	●	●		●	●	●						
Low Bias Current	≤50pA						●		●	●	●	●	●	●
	≤5pA								●			●	●	
	≤0.5pA												●	
Fast Settling	≤1µs to 0.1%													
	≤5µs to 0.01%					●								
Wideband (Unity Gain)	≥2MHz					●								●
	≥10MHz													
High Slew Rate	≥10V/µs													●
	≥30V/µs					●								
	≥100V/µs													
	≥1000V/µs													
Low Noise (0.1 to 10Hz) 2µV p-p		●	●	●	●	●		●		●	●	●		
High Voltage Out	≥100V													●
High Current Out	≥20mA													
Low Power	≤75mW								●	●	●		●	
Second Source				●										
Temperature Range	0 to +70°C	●	●	●	●		●	●	●	●	●	●	●	●
	-25°C to +85°C													
	-55°C to +125°C	●	●	●	●					●	●			
Dice Availability				●	●					●				
Volume I Page		4-31	4-47	4-125	4-57	4-143	4-143	4-145	4-83	4-87	4-105	4-139	4-51	4-141
Volume II Page		–	–	–	–	4-25	4-25	4-27	–	–	–	4-21	–	4-23

[1] Chopper Stabilized

		FAST/WIDEBAND												
					FET INPUT								UNITY GAIN BUFFER	
		AD507	AD509	AD518	48	AD380	AD381	AD382	AD3554	50, 51	HOS-050	ADLH0032	ADLH0033	HOS-100
Monolithic Technology	Bipolar Input	●	●	●										
	J-FET													
	Dual J-FET													
Multi-Device Technology	Hybrid					●	●	●	●		●	●	●	●
	Module				●					●				
High Open Loop Gain	⩾100dB	●			●		●	●	●		●			
	⩾140dB													
High CMR	>100dB													
Low Offset Voltage	⩽5mV	●	●		●	●		●	●	●		●	●	
	⩽1mV						●							
	⩽50µV													
Low Offset V, vs. Temp	⩽5µV/°C						●	●						
	⩽1µV/°C													
	⩽0.6µV/°C													
Low Bias Current	⩽50pA				●		●	●	●			●	●	
	⩽5pA													
	⩽0.5pA													
Fast Settling	⩽1µs to 0.1%	●	●	●			●	●		●	●	●	●	●
	⩽5µs to 0.01%				●	●			●	●	●	●		
Wideband (Unity Gain)	⩾2MHz	●	●	●			●	●			●	●	●	●
	⩾10MHz	●	●	●	●	●			●	●	●	●	●	●
High Slew Rate	⩾10V/µs	●	●	●							●	●	●	●
	⩾30V/µs						●	●						
	⩾100V/µs		●		●	●				●	●	●	●	●
	⩾1000V/µs								●					
Low Noise (0.1 to 10Hz) 2µV p-p							●	●						
High Voltage Out	⩾100V													
High Current Out	⩾20mA	●			●	●		●	●	●	●		●	●
Low Power	⩽75mW													
Second Source		●	●						●			●	●	
Temperature Range	0 to +70°C	●	●	●	●	●	●	●		●				
	-25°C to +85°C								●	●		●	●	
	-55°C to +125°C	●	●	●		●	●	●	●		●	●	●	●
Dice Availability				●										
Volume I Page		4-39	4-43	4-63	–	4-21	4-23	4-25	4-115	–	4-131	4-117	4-121	4-137
Volume II Page		–	–	–	4-17	–	–	–	–	4-19	–	–	–	–

Orientation

Operational Amplifiers

The amplifiers listed in this catalog are intended to provide cost-effective solutions to the bulk of op-amp requirements in precision measurement and control, as well as to more-general requirements in electronic circuits. The technical data included here* cover the properties of some 36 op-amp families, comprising about 100 distinct types. Some are general purpose, others provide near-optimum performance for specific classes of applications.

They differ in a variety of ways, for example, circuit technology, circuit architecture, input properties, output properties, operating temperature range and in terms of the many performance specifications.

BACKGROUND

The operational amplifier is today the most-widely used analog subassembly. It is safe to say that its *basic* properties and applications are sufficiently understood by most circuit designers and builders. However, the basis for choice, the subtleties of using op amps in circuits for best results (especially in precision measurement and control), and the varieties of possible applications are less clearly understood by op amp users, in varying degrees.

In these few pages, we shall address the question of making a proper choice of op amp type for an application, in relation to the extensive array of device properties presented in the data sheets that follow.

For those users requiring basic tutorial material, and detailed information on getting the most out of op amps, we have provided on page 4-16 a bibliography that should make available up to 99% of information needed now and then, with "fanout" to the vast body of literature that – with some redundancy – will provide the remainder. It should come as no surprise to successful users of Analog Devices op amps that a number of the references are to the applications sections of data sheets included in this catalog.

SELECTION PRINCIPLES

In selecting the right device for a specific application, you should have clearly in mind your design objectives and a firm understanding of what published specifications mean. Beyond this, you should detail the significant variables that are pertinent to your application. The purpose of this section is to put these many decision factors into perspective to help you make the most meaningful buying decisions.

To properly choose an operational amplifier for any given set of requirements, the designer must have:

> 1. *A complete definition of the design objectives.* Signal levels, accuracy desired, bandwidth requirements, circuit impedance, environmental conditions and other factors must be well defined before selection can be effectively undertaken.
>
> 2. *Firm understanding of what the manufacturer means by the numbers published for the parameters.* Frequently, any two manufacturers may have comparable published specifications, which may have been arrived at using differing measurement techniques. This creates a pitfall in op amp selection. To avoid these difficulties, the designer must know what the published specifications mean and how these parameters are measured and then must be able to translate these published specifications in terms meaningful to the design requirements.

There are three fundamental aspects to the rational selection of an operational amplifier for a given application: (1) establishing the circuit architecture, (2) defining the performance levels, and (3) choosing the amplifier(s).

1. To obtain a circuit building block to implement a defined functional job, the principal choices are either to purchase a committed functional device or to design a circuit employing op amps to perform the function. For example, to obtain a difference between two voltages, one may either purchase an instrumentation or isolation amplifier, or design a suitable subtraction circuit using op amps. If a committed functional building block, with appropriate specs and price, is not available, the circuit designer must start by developing schematic diagrams of circuits that will perform the function simply using "ideal" operational amplifiers. Many commonly used circuits can be found in textbooks, "cookbooks", and linear circuit books, as well as in application notes and data sheets.

2. Recognizing that the choice of an op amp depends on both the overall circuit requirements and the characteristics of available op amps, the designer should interpret the desired overall performance in terms of the parameters of op amps, and establish acceptable ranges of parameters, and their variation with time, temperature, supply voltage, etc. Examples of the key parameters are the input offset voltage, input bias and offset currents, and the high-frequency performance and transient behavior of the op-amp block (and its effect on the closed-loop circuit) for large and small signals. It will be helpful to develop an application checklist, which includes such considerations as the character of the input signals and their impedance, the output load, the desired accuracy – static and dynamic – and the environmental conditions.

3. The designer must then relate acceptable performance of the op-amp building block to the specifications and prices of available devices from preferred suppliers, bearing in mind a firm understanding of the way in which manufacturers define their specifications, and how definitions can differ in a way that may be misleading. A set of definitions used by Analog Devices follows the next section.

APPLICATION CHECKLIST

By way of an application checklist, the designer will need to account for the following:

> *Character of the application:* The character of the application (inverter, follower, differential amplifier, etc.) will often influence the choice of amplifier.

---

*In addition to the products listed here, which are recommended for new designs, a number of older products are still available; data sheets are available upon request.

Accurate description of the input signal: It is extremely important that the input signal be thoroughly characterized. Is the input a voltage source or current source? Range of amplitude? Source impedance? Time/frequency characteristics?

Environmental conditions: What is the maximum range of temperature, time, and supply voltage over which the circuits must operate (to the required accuracy) without readjustment?

Accuracy desired: The accuracy requirement determines the extent to which the foregoing considerations are critical, and ultimately points the way to a device (or series of devices) which are acceptable. Accuracy must, of course, be defined in terms meaningful to the application with regard to bandwidth, DC offset, and other parameters.

SELECTION PROCESS

In general, the objective of amplifier selection should be to choose the least expensive device which will meet the physical, electrical, and environmental requirements imposed by the application. This suggests that a "General Purpose" amplifier will be the best choice in all applications where the desired performance requirements can be met. Where this is not possible, it is generally because of limitations encountered in two areas – bandwidth requirements, and/or offset and drift parameters.

To make it easier to relate bandwidth requirements with the drift and offset characteristics, a capsule view of bandwidth considerations precedes the DC discussions below. The reader is then returned to an expanded discussion of gain-bandwidth considerations.

Gain Bandwidth Considerations, A Capsule View

Although all selection criteria must be met simultaneously, determination of the bandwidth requirements is a logical starting point because:

A) If DC information is not of interest, a suitable blocking capacitor can be connected at the amplifier input and all of the "drift" specifications may usually be ignored, and

B) Where high frequency (>10MHz) characteristics are of primary importance, the choice will be limited to those amplifiers designated "Wide Bandwidth/Fast Settling."

Where DC information is required and where frequency requirements are relatively modest (full power response below 100kHz, unity gain of less than 1.5MHz) other criteria will probably influence the final choice. It is important, however, to choose an amplifier with which an adequate value of loop gain is assured (at the maximum frequency of interest) to obtain the desired accuracy. Loop gain is the excess of open loop gain over closed loop gain, and is responsible for the diminishing error due to fluctuations in the open loop gain due to time, temperature, etc. For example, if the closed-loop gain is 1000, the open-loop gain must be at least 100,000 to yield an error of no more than 1%, and 1,000,000 to yield an error no greater than 0.1%. Where undistorted response is required, the specifications for full linear response and slewing rate should be chosen such that they are not exceeded at the highest frequency of operation.

Offset and Drift Considerations

In the majority of op-amp applications, final selection is determined by the DC offset and drift characteristics. To undertake amplifier selection in these cases, it is necessary to translate the requirements listed above as follows. (It is assumed that bandwidth requirements and temperature range have been established at this point.)

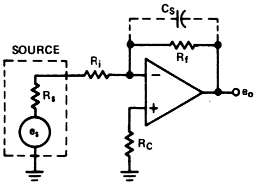
1. *What input impedance must the circuit present to the signal source?* This depends primarily on the source impedance, R_s, and the amount of loading error which is acceptable. Most amplifier circuits are designed around either the inverting or noninverting circuit of Figure 1. The choice is often made between the two to accommodate the impedance requirement. Input impedance for the inverting circuit is approximately equal to the summing impedance, R_i and the upper limit on the magnitude of R_i is determined by the allowable drift error because of input bias current as discussed below. The noninverting circuit offers inherently higher input impedance than the inverting circuit (due to "bootstrapping" feedback) and in this case input impedance is approximately equal to the common mode impedance of the amplifier R_{cm}.

2. *How much drift error can be tolerated?* The question is related to the input signal level, e_s, and the required accuracy. For example, to amplify or otherwise manipulate a DC input signal of one volt with an accuracy of 0.1%, the offset drift error, V_d, must be one millivolt or less. (This assumes that other sources of error such as input loading, noise and gain error have already been allowed for.) By the same reasoning, the allowable drift error for a 1 volt signal and 0.01% accuracy would be 100μV.

When this has been defined, the allowable limits of offset voltage (e_{os}), bias current (i_b), and difference current can be calculated by the equations of Figure 1.

Figure 1 gives the equations which relate offset voltage (e_{os}), bias current (i_b), difference current (i_d) and the external circuit impedances to the drift error, V_d, for both the inverting and the noninverting circuits. From these equations it can be seen how the input impedance requirements of the foregoing paragraphs are related to the drift error.

For example, in the case of the inverting circuit, an offset error voltage, i_bR_i, is generated by the bias current flowing through the summing impedance. This error increases for increasing R_i. Since R_i also sets the input impedance, there is a conflict between high input impedance and low offset errors. Likewise, for a given offset error, higher values for R_i can be used with an amplifier which has lower bias current.



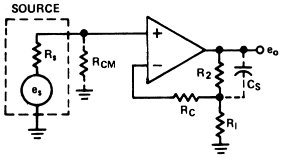
$$e_o = -\frac{R_f}{R_i}\Big[\underbrace{e_s}_{\text{Signal}} + \underbrace{e_{os}\left(\frac{R_f + R_i}{R_f}\right) + I_b R_i}_{\text{Input Drift Error} = V_d}\Big] \quad \text{For } R_C = 0 \text{ and } R_s << R_i$$

$$e_o = -\frac{R_f}{R_i}\Big[\underbrace{e_s}_{\text{Signal}} + \underbrace{e_{os}\frac{R_f + R_i}{R_f} + i_d R_i}_{\text{Input Drift Error} = V_d}\Big] \quad \text{For } R_C = R_i R_f/(R_i + R_f) \text{ and } R_s << R_i$$

Input Impedance $R_{IN} \approx R_i$

$$\% \text{ Drift Error} = \frac{100V_d}{e_s}$$

Figure 1A. Inverting Configuration



$$e_o = \frac{R_2 + R_i}{R_i}\Big[\underbrace{e_s}_{\text{Signal}} + \underbrace{e_{os} + i_b R_s}_{\text{Drift Error} = V_d}\Big] \text{ for } R_C = 0$$

$$e_o = \frac{R_2 + R_i}{R_i}\Big[\underbrace{e_s}_{\text{Signal}} + \underbrace{e_{os} + i_d R_s}_{\text{Drift Error} = V_d}\Big] \text{ for } R_C = R_s - \frac{R_i R_2}{R_i + R_2}$$

Input Impedance $R_{IN} \approx R_{CM}$

$$\% \text{ Drift Error} = \frac{100V_d}{e_s}$$

Figure 1B. Noninverting Configuration

Where it will otherwise function properly, the noninverting circuit generally makes a better choice for high input impedance circuits. Also, for the same source and input impedance requirement, a given amplifier will generate lower offset errors for the noninverting circuit than for the inverting circuit. This is so because the bias current flows only through R_s for the noninverter and this will always be less than the input impedance, R_i, of the inverter. Input impedance of the noninverter (approximately R_{CM}) is typically 10^7 ohms even for the least expensive bipolar amplifiers and up to 10^{11} ohms for FET types.

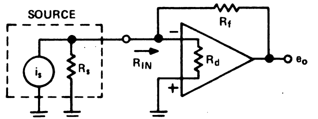
Unfortunately, however, the noninverting configuration cannot always be used since it is not convenient to use for many circuit functions such as integration or summation. A further limitation occurs in high accuracy applications, where common mode errors may rule out this circuit configuration.

Initial offsets can usually be zeroed at room temperature so that only the maximum temperature excursion (ΔT) from +25°C need be considered. For example, over the range of -25°C to +85°C, the maximum temperature excursion (ΔT) from +25°C would be 60°C. As a practical matter, offset errors due to supply voltage and time drift can generally be neglected since errors due to temperature drift are usually much greater.

Current Amplifier Considerations

Before leaving the subject of offset errors, we shall discuss briefly the current amplifier configuration which is shown in Figure 2A. The obvious approach to measuring current is to develop a voltage drop across a load resistor, R_f, and to measure this potential with a high impedance amplifier as shown in Figure 2B.

This approach has several disadvantages as compared to the circuit of Figure 2A. First the noninverting amplifier introduces common mode errors which do not occur for Figure 2A. Second, an ideal current meter would have zero impedance whereas, R_f in Figure 2B may become very large since this resistor determines the sensitivity of the measurement. Third, the changes of input impedance, R_{cm},

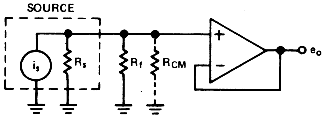


$$e_o = -R_f\Big[\underbrace{i_s}_{\text{Signal}} + \underbrace{e_{os}\left(\frac{R_f + R_s}{R_s R_f}\right) + i_b}_{\text{Drift error} = I\epsilon}\Big]$$

$$\text{Input Impedance } R_{IN} = \left(\frac{R_f R_d}{R_f + R_d}\right)\left(\frac{1}{1 + A\beta}\right)$$

$$\text{where } 1/\beta = 1 + \frac{R_f (R_s + R_d)}{R_s \quad R_d} \qquad \% \text{ Drift Error} = \frac{100\ I\epsilon}{i_s}$$

Figure 2A. Current Amplifier



$$e_o = \underbrace{R_f i_s}_{\text{Signal}} + \underbrace{e_{os} + i_b R_f}_{\text{Drift Error} = V_d} \text{ for } R_s > R_f$$

Input Impedance $R_{IN} \approx R_f$

$$\% \text{ Drift Error} = \frac{100V_d}{R_f i_s}$$

Figure 2B. Voltage Amplifier with Sampling Resistor

for the noninverting amplifier with temperature will cause variable loading on R_f and hence a change in sensitivity.

The current amplifier of Figure 2A circumvents all of these difficulties and approaches an ideal current meter; that is, there is essentially no voltage drop across the measuring circuit, since with enough open loop gain, A, the input impedance R_{IN} becomes very small.

In selecting a current amplifier, the most important consideration is current noise, and bias current drift. Measuring accuracy is largely the ratio of current noise and drift to signal current, i_s. To obtain the drift of error current I_ϵ referred to the input, use the following expression.

$$\Delta I_\epsilon = \left[\frac{\Delta e_{os}}{\Delta T}\left(\frac{R_f + R_s}{R_f R_s}\right) + \frac{\Delta i_B}{\Delta T}\right]\Delta T$$

Now, to make a proper selection you must pick an amplifier with an error current, I_ϵ, over the operating temperature which is small compared to the signal current, i_s. Do not overlook current noise which may be more important than current drift in many applications.

Gain Bandwidth Considerations, Expanded Discussion

From the previous discussion, it is apparent that most general purpose operational amplifiers will usually give adequate performance for the DC and audio frequency range applications. However, to obtain unity gain bandwidth above 2MHz, full power response above 20kHz and slewing rate above 6V/μsec, in general, requires special design techniques. All amplifiers with wideband, fast response characteristics have been listed in the wide bandwidth group to simplify the selection for higher frequency applications.

One factor often overlooked is that stray capacitance and impedance levels of the external feedback circuit can be the major limitation in high frequency applications. For example, in Figure 1A, if R_f were one megohm, and stray capacitance, C_S, were one picofarad then the closed loop bandwidth would be limited to 160kHz ($1/(2\pi R_F C_S)$) regardless of how fast the amplifier is. Moreover, output slewing rate will be limited by how fast C_S can be charged which in turn is related to signal level, e_s, and input impedance, R_i, by $de_o/dt = -e_s/R_iC_s$. For these reasons it is usually not possible to obtain both fast response and high input impedance for an inverting circuit since both R_i and R_f must be large to obtain high input impedance.

Another advantage of the noninverting circuit (Figure 1B) is that input impedance, being determined by potentiometric feedback, does not depend on the impedance levels for R_1 and R_2. Therefore, a low impedance can be used for R_2 so that stray capacitance of C_s will not limit the circuit's bandwidth. In this case the minimum value for R_2 is constrained only by the output current rating of the amplifier. Again the trade-off between the frequency response and input impedance of the inverting and noninverting circuits must be evaluated in light of the common mode rejection error introduced by the noninverter.

For greater emphasis wideband applications can be separated into two categories – steady state and transient. Since the amplifier requirements for the two are somewhat different, these categories will be discussed separately.

A. Steady State Applications

Steady state applications involve amplifying or otherwise manipulating *continuous* sinusoidal, complex or random waveforms. In these applications the significant issues in choosing an amplifier are as follows:

1. *Is DC coupling required?* If DC information is of no consequence, then the offset drift errors are not usually important and a capacitor can be used if necessary to block the output DC offset. Your only concern here is that DC offset at the output does not become so large, as might be the case with a high gain stage, that the output is saturated or the dynamic swing for AC signals is limited. One way to circumvent the latter problem is to use feedback to limit the gain at DC as shown in Figure 3. The gain of these circuits can be small at DC but large at high frequencies.

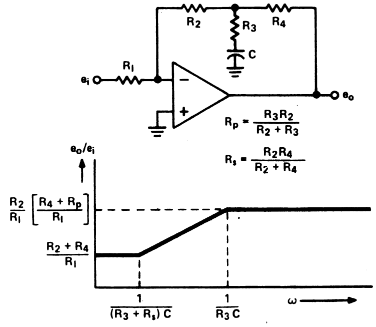

R2
R3
R4
C
R1
e_i
e_o
−
+
$R_p = \frac{R_3R_2}{R_2 + R_3}$
$R_s = \frac{R_2R_4}{R_2 + R_4}$
e_o/e_i
$\frac{R_2}{R_1}\left[\frac{R_4 + R_p}{R_1}\right]$
$\frac{R_2 + R_4}{R_1}$
$\frac{1}{(R_3 + R_s)C}$
$\frac{1}{R_3C}$
ω

Figure 3. DC Feedback Minimizes Output Offset for AC Applications

2. *What closed loop gain and bandwidth are required?* Closed loop gain, G, is dictated by the application. To a first approximation the intersection of the open and closed loop gain curves in Figure 4 gives the closed loop bandwidth, f_{c1}(−3dB). For high gain, wideband requirements, it may be necessary, or more economical, to use two amplifiers in cascade each at lower gain.

3. *What loop gain is required or alternatively what gain stability, output impedance and/or linearity are necessary?* The available loop gain at a particular frequency or over a range of frequencies is very often more important than closed loop bandwidth in selecting an amplifier. Loop gain as illustrated in Figure 4, is defined as the difference, in dB, or as the ratio, arithmetically, of the open to closed loop gain ($A\beta$ = A/G). You will find in most of the equations defining the closed loop characteristic of a feedback amplifier that the loop gain ($A\beta$) is the determining factor in performance. Some of the more notable examples of this point are as follows:

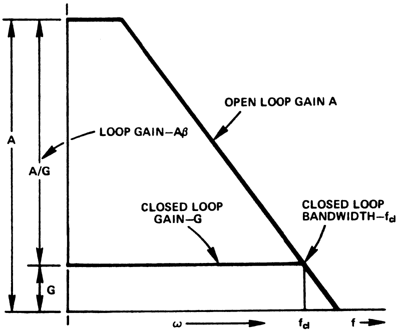


Figure 4. Closed Loop Bandwidth and Loop Gain

a. Closed loop gain stability = ΔG/G
$\Delta G/G = (\Delta A/A)\ [1/(1 + A\beta)]$ where $\Delta A/A$ is the open loop gain stability, usually about 1%/°C.

b. Closed loop output impedance = $Z_{ocl} = Z_o/(1 + A\beta)$, where Z_o is the open loop output impedance, usually 200 to 5000 ohms.

c. Closed loop nonlinearity = $L_{cl} = L_{ol}/(1 + A\beta)$, where L_{ol} is the open loop linearity, usually less than 5%.

Loop gain of 100, or 40dB, is adequate for most applications and this is readily achievable at DC and low frequencies. But note that loop gain decreases with increasing frequency which makes it difficult to obtain large loop gains at high frequencies. For this reason it may be necessary to use a 10MHz unity gain amplifier in order to obtain adequate feedback over a 10kHz bandwidth.

4. *What full power response and/or slew rate are required?* You should examine your expected output waveform and select an amplifier whose slewing rate exceeds the maximum rate of change of output signal. For a sinusoidal waveform with a peak voltage output equal to the rated amplifier output the frequency should not exceed f_p, the full power response of the amplifier. As the output signal voltage is reduced below the rated output voltage, the usable maximum frequency can be extended proportionately. If you do not observe these restrictions you will get distortion and unexpected DC offsets at the output of the amplifier.

For some monolithic amplifier designs available today their frequency response is not a simple 6dB roll-off; the response may be shaped with external RC components for improved performance. Using feedforward or phase lag compensation networks, gain-bandwidth product and/or full power response may be shaped to meet varying design requirements. Most internally compensated op amps offer a stable 6dB per octave roll-off with specified unity gain-bandwidth and slew rate thereby limiting maximum speed and response to those published specifications.

B. Transient Applications

In applications such as A/D and D/A converters and pulse amplifiers, the *transient response* of the wideband amplifier is generally more important than the *gain bandwidth* characteristic described above. Slewing rate, overload recovery and settling time are the specifications which determine the transient response.

When applying the high frequency amplifier, it is important to understand how amplifier performance is affected by component selection as well as impedance levels used around the amplifier.

Settling Time

Settling time is defined as the time elapsed from the application of a perfect step input to the time when the amplifier output has entered and remained within a specified error band symmetrical about the final value (Figure 5). Settling time therefore includes the time required for the amplifier to slew from the initial value, recover from slew rate limited overload, and settle to a given error in the linear range.

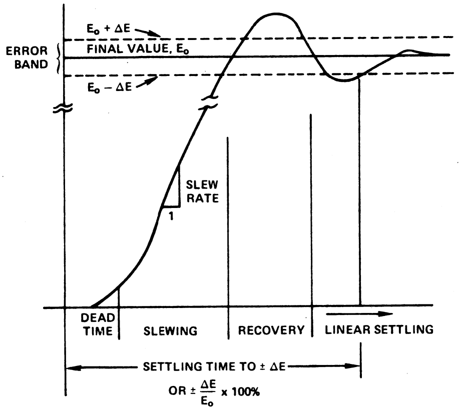


Figure 5. Typical Settling Time Characteristics

The time and frequency response of a linear, bilateral network or amplifier are related by well known mathematics. For example, the step response for a well behaved, ideally linear, 6dB/octave amplifier with a closed loop bandwidth of ω_{cl} is shown in Figure 6.

However, since settling time is determined by a combination of amplifier characteristics (both linear and nonlinear) and because it is a closed loop parameter, it cannot be readily predicted from the open loop specifications such as slew rate, small signal bandwidth, etc.

Analog Devices specifies settling time for the condition of unity gain, relatively low impedance levels, and no capacitive loading. A full-scale step input is used to determine settling time and the step is generally unipolar – i.e.: from zero to plus or minus full scale. The settling time indicated is generally the longest time resulting from a step of either polarity and is given as a percentage of the full scale step transition.

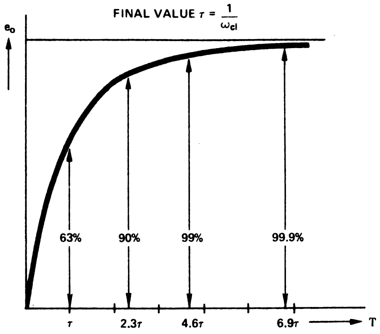


Figure 6. Step Response for Linear 6dB/Octave Amplifier

Settling time is a nonlinear function. It varies with the input signal level and it is greatly affected by impedances external to the amplifier.

ERRORS DUE TO NOISE

A major criterion in the selection of an amplifier for low level signals is the amplifier input noise, since this is usually the limiting factor on system resolution. In the general case, amplifier noise can be characterized by a voltage source in series with the summing junction and a current source in parallel with the summing junction. Whenever high source impedance is encountered, current noise flowing through the source impedance will appear as an additional voltage noise, combining with the amplifier voltage noise. The sum of these noise sources will then be amplified along with the desired signal. For this reason, selection of a particular amplifier must consider both the amplifier noise performance as well as the source impedance.

Consideration must also be given to noise sources other than the amplifier whenever determining total system noise. RF noise may be fed into an amplifier through any connecting wire, including power supply and output leads. Adequate shielding and low-pass filters on all incoming leads will usually prevent noise pick-up.

Thermal noise is generated in any conductor or resistor as a result of thermal agitation of the electrons. This noise voltage source, sometimes referred to as "Johnson Noise", is generated in the resistive component of any impedance and has a value:

$e_n = \sqrt{4KTBR}$

where e_n = the rms value of the noise voltage
K = Boltzman's Constant (1.38×10^{23} joules/°K)
T = absolute temperature of the resistance, °K
B = the bandwidth in which the noise is measured

Since noise is related to the bandwidth over which the measurement is made, no noise specification is meaningful unless the bandwidth for the specification is given. Although the Thermal Noise equation may appear unwieldy for practical noise calculations, all that is required to enable rapid approximations is to apply a few simple rules of thumb.

Rules of Thumb

(1) Remember that a 100kΩ resistor generates 40nV rms in a 1Hz bandwidth. The noise voltages generated by other values of resistances in other bandwidths can be calculated by remembering that the noise is proportional to the square root of the resistance and the bandwidth; i.e.

$$e_n\,(\text{rms}) = (40\text{nV}/\sqrt{\text{Hz}})\left(\sqrt{\frac{R}{100\text{k}\Omega}\,(\text{BW})}\right)$$

(2) To convert the rms noise to a p-p value, a conversion factor of 6.6μV p-p/μV rms is applied for less than 0.1% probability of noise peaks exceeding calculated limits.

(3) The total rms noise contribution due to several noise sources is determined by the square root of the sum of the squares:

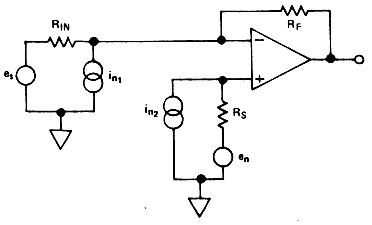
$$e_t = \sqrt{e_a^2 + e_b^2 + e_c^2 + \ldots e_n^2}$$

If any noise source is less than a third of another, it may be neglected. The resulting error will be approximately 5%.

(4) Restricting the bandwidth of a system to the minimum usable and using the lowest impedances possible are ways to reduce noise.

DESIGN EXAMPLE

Figure 7A illustrates a typical circuit with noise calculations shown for each noise source. The total of the noise sources is obtained by adding each of the individual sources in a RMS fashion.



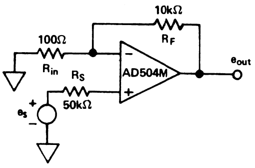
COMPONENT	CAUSE	OUTPUT CONTRIBUTION
R_{IN}	Johnson Noise	$\sqrt{4KTBR_{IN}}\,(R_F/R_{IN})$
R_S	Johnson Noise	$\sqrt{4KTBR_S}\,(R_F/R_{IN} + 1)$
R_F	Johnson Noise	$\sqrt{4KTBR_F}$
i_{n_1}	Amp. Current Noise	$i_{n_1} R_F$
i_{n_2}	Amp. Current Noise	$(i_{n_2} R_S)\,(R_F/R_{IN} + 1)$
e_n	Amp. Voltage Noise	$e_n\,(R_F/R_{IN} + 1)$

$$\text{TOTAL NOISE} = \sqrt{(e_{R_{IN}}\,G)^2 + [e_{R_S}\,(G+1)]^2 + e^2{}_{R_F} + (i_{n_1}\,R_F)^2 + [(i_{n_2}\,R_S)\,(G+1)]^2 + [e_n\,(G+1)]^2}$$

Figure 7A. Noise Components

Figure 7B illustrates how the Rules of Thumb may be applied in a practical case to approximate the total output noise. In this example, AD504, or a low noise type amplifier is being used with a 50kΩ source impedance. The two major noise sources, in addition to the AD504M input voltage noise of 0.6μV p-p, are the Johnson noise (58μV p-p) and current noise (100μV p-p).

GAIN = 100
BW = 0.01 TO 10Hz
R_S = 50kΩ
R_F = 10kΩ
R_{IN} = 100Ω



1) RESISTOR NOISE: $R_F \to 13nV/\sqrt{Hz}$
$R_{IN} \to (1.3nV/\sqrt{Hz})\ 100$
$R_S \to (28nV/\sqrt{Hz})\ 101 = 2.8\mu V/\sqrt{Hz}$

TOTAL RESISTOR NOISE IN 10Hz BW =
$(2.8\mu V/\sqrt{Hz})\ (\sqrt{10Hz})\ 6.6\mu V$ p-p/μV rms = $58\mu V$ p-p

2) AMPLIFIER CURRENT NOISE: (50pA p-p) (50k) (101) = $252\mu V$
(50pA p-p) (10k) = $0.5\mu V$

3) AMPLIFIER VOLTAGE NOISE: $(0.6\mu V$ p-p) (101) = $60.6\mu V$ p-p

TOTAL OUTPUT NOISE = $\sqrt{(252)^2 + (60.6)^2 + (58)^2} \approx 265\mu V$ p-p

Figure 7B. Design Example

HOW THE OPERATIONAL AMPLIFIERS ARE CLASSIFIED

To assist the designer in distinguishing among the many types available from Analog Devices, we have provided a Selection Guide, in which amplifiers are grouped in terms of common properties which have been optimized in order to satisfy the needs of specific classes of applications. Once the choice has been narrowed to the manageable number of types in any group, distinctions can be drawn in terms of other requirements or considerations.

Temperature Range and Nomenclature. Analog Devices operational-amplifier nomenclature uses suffixes to permit ready identification of the temperature range for which device operation to meet critical specifications has been designed or selected. The most popular range comprises the "commercial" temperatures from 0 to 70°C; it is designated by suffixes such as J, K, L, M, in order of increasingly tighter specs (e.g., AD741L). Also popular is the "military" range, -55°C to +125°C, designated by S, T, U, (e.g., AD510S); not all families have types with specified performance in this range. There are a few types designed for operation in the "industrial" range, -25°C to +85°C, designated by A, B (e.g., model 51B). Wide-range types will generally meet the same or better specs in a narrower temperature range. A few types are second-sources for products originally introduced by other manufacturers. In those instances, the generic nomenclature is used (AD741C) or enlarged upon, if superior selections are offered (e.g., AD301AL).

There are nine divisions by class of application, based on optimization of one or more key specifications. Versions of many devices in this class are available to meet requirements of MIL-STD-883B; the availability of such devices will be noted on the data sheets.

1. *General-Purpose ICs.* Amplifiers in this group include our lowest-cost devices. They are best-suited for general purpose designs with moderate drift requirements, down to 5μV/°C max (AD301AL), and gain-bandwidth to 8MHz (AD301A). Typical applications include summing, inverting, impedance buffering (followers), and active filtering. They are also useful for developing nonlinear transfer functions, with appropriate external circuitry.

Bipolar monolithic technology is used for all types. The AD741 is internally compensated; it does not require external capacitance for frequency compensation. On the other hand, the AD301A's ability to be externally compensated, by either lag or feedforward circuitry, permits circuits with a wide range of dynamic performance characteristics to be handled. Extended-temperature-range equivalents are the AD101A, AD201A, and AD741.

2. *Low Bias-Current, High Input-Impedance, FET-Input ICs.* These types use the inherently high impedance and low leakage current of junction field-effect transistors (FET's) to deal with configurations that either provide the measurement of low currents or require the use of high-resistance circuitry.

Typical applications range from general-purpose high-impedance circuitry to integrators, current-to-voltage converters, and log-function generation, to measurements with high-impedance transducers, such as photomultipliers, flame detectors, pH cells, and radiation detectors.

The performance range is from the 75fA (75×10^{-15}A) maximum bias current of the AD515L electrometer to the 50pA max of the general purpose, lowest-cost AD540J. The AD542 is a low-cost, laser-wafer-trimmed (LWT) monolithic implanted FET input amplifier with low offset and drift. The AD544 is similar, but has higher speed. Low bias current does not necessarily imply large voltage offsets; the AD515K combines a 150fA (0.15pA) max bias current with 1.0mV max offset and 15μV/°C max voltage drift; comparable figures for the AD547L are 25pA, 0.25mV and 1μV/°C.

The types of amplifiers in this group either are completely monolithic or employ matched FET's and a special bipolar amplifier chip designed to accommodate the input FET's electrically. In nearly all the IC's, thin-film resistors are deposited on the chip at critical circuit locations to ensure stability; low offsets and drift are achieved by laser-trimming of circuit balance. All FET-input op amps from Analog Devices are manufactured to meet their published bias-current specifications *after full warmup* (some manufacturers specify *initial* current, which is lower than warmed-up bias current). Our published max bias-current specification applies to either input (some manufacturers call "bias current" the *average* of the two input currents). Bias current of junction FET's approximately doubles for every 10°C increase of temperature.

3. *FET-Input Dual ICs.* The AD642, AD644, and AD647 are a single-chip pair of trimmed implanted-FET-input (TRIFET) op amps similar to the AD542, AD644, and AD547 with low warmed-up bias current (35pA max – K, L, S), low offset voltage (0.5mV max – L), low offset-voltage drift (2.5μV/°C max – L), and excellent V_{OS} matching (0.25mV max – L). Besides applications calling for more than one FET-input op amp at low cost per function, the AD647 is especially useful

in applications calling for matched duals, such as log-ratio amplifiers, FET-input instrumentation amplifiers, and buffering of differential signals. The AD644, a wideband version, was designed for fast DAC amplifiers, sample and hold, filters and wideband instrument amplifiers.

4. *Electrometers.* This class comprises the lowest bias-current devices, the AD515. The AD515L, with its 75fA input bias current, 1mV max offset, and 25µV/°C offset tempco, has differential inputs, and can be used in voltage measurements at high impedance, as a follower, or in current measurements, as an inverter, or even differentially.

5. *High-Accuracy Low-Drift Differential-Input ICs.* "Chopperless" low-drift designs with differential inputs, optimized for voltage offset and drift, dc open-loop gain, and CMR, should be considered for high-accuracy instrumentation, low-level transducer bridge circuits, precision voltage comparators, and for impedance buffer designs.

Performance of internally compensated premium amplifiers in this group ranges from the ADOP-07A's 25µV max offset voltage and 0.6µV/°C drift, and the AD517L's 50µV max offset voltage and 1.3µV/°C drift, combined with 1nA max bias current (1.5nA max over the temperature range), and CMR of 110dB min, to the low-cost AD741L's maximum offset of 0.5mV and max offset tempco of 5µV/°C, with 100nA max bias current over the temperature range, and CMR of 90dB min.

The ADOP-07 is a superior second source to other OP-07 families; for example, ADOP-07AH has minimum gain of 3×10^6 V/V compared to 3×10^5 V/V.

Among *uncompensated* op amps, the premium range is from the AD504M, with 0.5mV maximum offset voltage, 0.5µV/°C max drift, 100nA max bias current over the temperature range, and 110dB CMR, to the low-cost AD301AL, with max offset of 0.5mV, max drift of 5µV/°C, max bias current of 45nA over the temperature range, and minimum CMR of 90dB. For applications in which low noise is essential, the AD504M has 100%-tested guaranteed maximum voltage noise of 0.6µV p-p, for the frequency range 0.1 to 10Hz, and maximum spot noise of 13, 10, and 9nV/$\sqrt{\text{Hz}}$ and 0.6, and 0.3pA/$\sqrt{\text{Hz}}$, at 100Hz, and 1000Hz, respectively.

External dynamic compensation permits considerably greater bandwidths, at higher gains, than are available with the compensated AD517 and AD510 families. For example, with a 3.9pF compensating capacitor, the AD504's typical small-signal bandwidth is 100kHz at a gain of 200, vs. 1.5kHz for the internally compensated AD510; under the same conditions, the full-power bandwidth of the AD504 is 30kHz, vs. 1.5kHz for the AD510. With feedforward compensation, the AD301AL has a full-power bandwidth in excess of 150kHz, for inverting applications.

The AD741J/K/L and the AD301AL are selected from production lots of the generic AD741 and AD101A types. The AD504, AD510, and AD517 are thermally balanced for low drift and high gain (independent of output loading), with inputs that are bootstrapped for high CMR and protected against overloads to prevent bias-current degradation due to reverse breakdown. Thin-film resistors, deposited on the chip, are another key to the stability of these amplifiers. The AD510 and the AD517 employ super-beta input transistors to achieve low bias current, and they are laser-trimmed at the wafer-probe stage (LWT) to achieve their excellent offset-voltage specifications at low cost. Since the bias currents are always of one polarity, they can be nulled at a given temperature with simple circuitry; and the change over the temperature range will be considerably less than for low-cost FET-input amplifiers having comparable specifications.

Extended-temperature-range equivalents are AD504S, AD510S, AD714S, and AD517S.

6. *Wide Bandwidth, Fast-Settling ICs.* High-speed op amps are characterized by high slewing rates, fast settling time, and wide bandwidth. Fast settling time is especially important in applications with rapidly changing or switched analog data, in buffers, d/a converters, and multiplexer circuitry; wide small-signal bandwidth is important in preamplification and in handling low-level wideband ac signals; high slewing rate is associated with fast settling time and is also important in handling ac signals having large magnitudes with minimal distortion, since the large-signal bandwidth is closely related to the slewing rate.

The products in this category with outstanding specifications are models HOS-050, AD3554 and AD380. Settling of the hybrid HOS-050 is to within 0.01% in 300ns in the inverting connection. Model AD3554 max slewing rate is 1000V/µs inverting, and small-signal unity-gain bandwidth is 70MHz; full-power bandwidth is 16MHz, min. In addition, all of these devices will deliver ±100mA of output current at ±10V, an important factor in video and line-driver circuitry, and in driving capacitive loads. For example, the current required to sustain 500V/µs in a 100pF load is $I = C\,dV/dt = 50\text{mA}$. AD380 is optimized for settling time: 250ns maximum to 0.01%, inverting or noninverting, with output of ±50mA at ±10V.

There are three families of monolithic ICs listed in this category, with slewing rates ranging from 25V/µs min to 100V/µs min. The AD509S is the fastest slewing (100V/µs min) and settling (500ns min to 0.1% and 2.5µs min to 0.01%). The AD507K is the best all-around performer, with small-signal bandwidth of 35MHz, slewing rate of 25V/µs min, and typical settling to 0.1% within 900ns, in addition to open-loop dc gain of 10^5 min, drift of 15µV/°C max, and bias current of 15nA max. The AD518J is the lowest in cost, yet it slews at 50V/µs min, and typically settles to within 0.1% in 800ns, with single-capacitor compensation.

Extended-temperature-range equivalents are models AD507S, AD509S and AD518S.

DEFINITIONS OF SPECIFICATIONS

Absolute Maximum Differential Voltage
Under most operating conditions, feedback maintains the error voltage between inputs to nearly zero volts. However, in some applications, such as voltage comparators, the voltage between the inputs can become large. This specification defines the maximum voltage which can be applied between inputs without causing permanent damage to the amplifier.

Common-Mode Rejection
An ideal operational amplifier responds only to the difference voltage between inputs ($e^+ - e^-$) and produces no output for a *common-mode voltage*, that is, when both inputs are at the same potential. However, due to slightly different gains between the plus and minus inputs, or variations in offset voltage as a function of common-mode level, common-mode input voltages are not eliminated at the output. If the output error voltage, due to a known magnitude of common-mode voltage, is referred to the input (dividing by the closed-loop gain), it reflects the equivalent *common-mode error voltage* (CME) between the inputs. Common-mode rejection ratio (CMRR) is defined as the ratio of common-mode voltage to the resulting common-mode error voltage. Common-mode rejection is often expressed logarithmically: CMR (in dB) = $20 \log_{10}$ (CMRR).

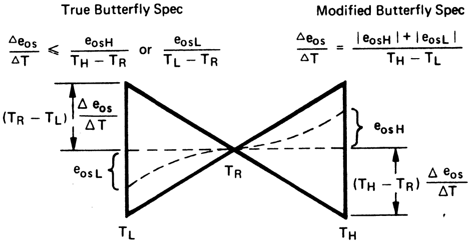
The precise specification of CMR is complicated by the fact that the common-mode voltage error can be a highly nonlinear function of common-mode voltage and also varies with temperature. As a consequence, CMR data published by Analog Devices are average figures, assuming an end-point measurement over the common-mode range specified. The incremental CMR about small values of common-mode voltage may be greater than the average CMR specified (on the other hand, the incremental CMR may be less in the neightborhood of large CMV). Published CMR specifications for op amps pertain to very low-frequency voltages, unless specified otherwise; CMR decreased with increasing frequency.

Common-Mode Voltage, Maximum
For differential-input amplifiers, the voltage at both inputs can swing about ground (power-supply common) level. *Common-mode voltage* is defined as any voltage (above or below ground) that could be observed at both inputs. The maximum common-mode voltage is defined as that voltage which will produce less than a specified value of common-mode error. This establishes the maximum input voltage for the voltage-follower connection.

Drift vs. Supply
Offset voltage, bias current, and difference current vary as supply voltage is varied. Usually, dc errors due to this effect are negligible compared to drift with temperature. No inference may be drawn from this low-frequency specification concerning the effects of rapid variation of voltage at the supply terminals.

Drift vs. Temperature
Offset voltage, bias current, and difference current all change, or "drift", from their initial values with temperature. This is by far the most important source of error in most precision applications. The temperature coefficients (tempcos) of those parameters are all defined as the average slope over a specified temperature range. Drift can be a nonlinear function of temperature (though it is often quite linear over limited temperature ranges); the slopes generally are greater at the extremes of temperature than around normal ambient (+25°C), which generally means that for small temperature excursions in the vicinity of +25°C, the specification is conservative.

Analog Devices precision operational amplifiers are specified by three- (or more-) point measurements, at 25°C and at the high and low extremes of the range (T_H, T_L), with the amplifier adjusted to zero at room temperature. The sum of the magnitudes of the drifts in the two ranges must be less than the specified drift rate (μV/°C or nA/°C) multiplied by the total temperature range (modified "butterfly"), or, in some cases, the magnitude of the drifts in both ranges must be less than the specified drift rate multiplied by the respective temperature ranges ("true butterfly").


True Butterfly Spec
$\frac{\Delta e_{os}}{\Delta T} \leq \frac{e_{osH}}{T_H - T_R}$ or $\frac{e_{osL}}{T_L - T_R}$
Modified Butterfly Spec
$\frac{\Delta e_{os}}{\Delta T} = \frac{|e_{osH}| + |e_{osL}|}{T_H - T_L}$
$(T_R - T_L)\frac{\Delta e_{os}}{\Delta T}$
e_{osL}
e_{osH}
T_R
$(T_H - T_R)\frac{\Delta e_{os}}{\Delta T}$
T_L
T_H

$\frac{\Delta e_{os}}{\Delta T}$ is the max. drift coefficient permissible

The lowest-cost second-source IC amplifiers are specified only in terms of the maximum value of the parameter (e.g., offset voltage) over temperature in the specified range.

Drift vs. Time
Offset voltage, bias current, and difference current change with time as components age. It is important to realize that drift with time is random, and rarely – if ever – accumulates linearly for healthy devices. For example, voltage drift for a chopper-stabilized amplifier might be quoted at 1μV/day, whereas cumulative drift over 30 days might not exceed 5μV, or 15μV in a year (e.g., model 235). A convenient rule of thumb for extrapolation is to divide the drift for a stated interval by the square root of its ratio to any other interval of interest.

Full-Power Response
The large-signal and small-signal response characteristics of operational amplifiers differ substantially. An amplifier's output will not respond to large signal changes as fast as the small-signal bandwidth characteristics would predict, primarily because of slew-rate limiting in the output stages. Full-power response is specified in two ways: full linear response and full peak response. Full linear response is specified in terms of the maximum frequency, at unity closed-loop gain, for which a

sinusoidal input signal will produce full output at rated load without exceeding a pre-determined distortion level. There is no industry-wide accepted value for the distortion level which determines the full-linear-response limitation, but we use 3% as a maximum acceptable limit for modules.

In many applications, the distortion caused by exceeding the full linear response can be comfortably ignored, but a more-serious effect (often overlooked) is an effect equivalent to a dc offset voltage that can be generated when full linear response is exceeded, due to rectification of the asymmetrical feedback waveform or overloading of the input stage by large distortion signals at the summing junction.

Another frequency response that is often if interest is the maximum frequency at which full output swing may be obtained, irrespective of distortion. This is termed "full peak response" and can often be found in a plot of output voltage swing vs. frequency.

Initial Bias Current
Bias current is defined as the current required at either input from an infinite source impedance to drive the output to zero (assuming zero common-mode voltage). For differential amplifiers, bias current is present at both the negative and the positive input. All Analog Devices specifications pertain to the *larger* of the two, *not the average.* For single-ended amplifiers (i.e., chopper types), bias current refers to the current at the input terminal.

Analog Devices specifies initial bias current, I_b, as the bias current at either input, specified at +25°C ambient with the input junctions *at normal operating temperature* (some manufacturers specify initial bias current at power turn-on. Such specifications may be misleading. For example, in FET-input amplifiers, bias current is doubled for each 10°C increase; since junction temperatures may warm up to 20°C or more above ambient, the "initial bias current" spec used by some manufacturers may be met only during a brief interval after the power is burned on, and I_b may be quadrupled under ordinary operation conditions.)

Initial Difference Current
Difference current is defined as the difference between the bias currents at the two inputs. The input circuitry of differential amplifiers is generally symmetrical, so that bias currents at both inputs tend to be equal and tend to track with changes in temperature and supply voltage. Therefore, difference current is often about 0.1 times the bias current at either input, assuming that initial bias current has not been compensated at the input terminals. For amplifiers in which bias currents track, it is often possible to reduce voltage errors due to bias current and its variations by the use of equal resistance loads at both inputs.

Input Impedance
Differential input impedance is defined as the impedance between the two input terminals at +25°C, assuming that the error voltage is nulled or very near zero volts. To a first approximation, dynamic impedance can be represented by a capacitor in parallel with a resistor.

Common-mode impedance, expressed as a resistance in parallel with a capacitance, is defined as the impedance between each input and power-supply common, specified at +25°C. For most circuits, common-mode impedance on the negative input has little significance, except for the capacitance which it adds at the summing junction (one exception is electrometer circuitry). However, common-mode impedance on the plus input sets the upper limit on closed-loop input impedance for the non-inverting configuration. Common-mode impedance is a nonlinear function of both temperature and common-mode voltage. For FET-input amplifiers, common-mode resistance is reduced by a factor of two for each 10° of temperature rise. As a function of common-mode voltage, the resistive component is defined as the average resistance for a common-mode change from zero to the maximum common-mode voltage. Incremental resistance may be less than the specified average value, especially at full-scale for some FET-input amplifiers.

Input Offset Voltage
Offset voltage is defined as the voltage required at the input from zero source impedance to drive the output to zero; its magnitude is measured by closing the loop (using low values of resistance) to establish a large fixed gain, measuring the amplified error at the output, and dividing the measured value by the gain.

The initial offset voltage is specified at +25°C and rated supply voltage. In most amplifiers, provisions are made to adjust initial offset to zero with an external trim potentiometer.

Input Noise
Input voltage- and current-noise characteristics can be specified and analyzed in much the same way as offset-voltage and bias-current characteristics. In fact, long-term drift can be considered as noise which occurs at very low frequencies. The primary difference is that, when evaluating noise performance, bandwidth must be considered. Also rms noise from different sources is summed by root-sum-of-squares, rather than linear, addition. Depending on the amplifier design, noise may have differing characteristics as a function of frequency, being dominated by "1/f noise", resistor noise, or junction noise, at various frequencies.

For this reason, several noise specifications are given. Low-frequency noise in the band 0.01 to 1Hz (or 0.1 to 10Hz) is specified as peak-to-peak, with a 3.3σ uncertainty, signifying that 99.9% of the observed peak-to-peak excursions will fall within the specified limits. Wideband noise is specified as rms. For some types, spectral-density plots or "spot noise", at specific frequencies, in $\mu V/\sqrt{Hz}$ or $pA/\sqrt{Hz}$, are provided.

Open-Loop Gain
Open-loop gain is defined as the ratio of a change of output voltage to the voltage applied between the amplifier inputs to produce the change. Gain is specified at dc. In many applications, the frequency dependence of gain is important; for this reason, the typical open-loop gain as a function of frequency is published for each amplifier type. See also *unity gain small-signal response.*

Overload Recovery
Overload recovery is defined as the time required for the output voltage to recover to the rated output voltage from a saturated condition caused by a 50% overdrive. Published specifications apply for low impedances and contain the assumption that overload recovery is not degraded by stray capacitance in the feedback network.

Rated Output
Rated output *voltage* is the minimum peak output voltage which can be obtained at rated current or a specified value of resistive load before clipping or out-of-spec nonlinearity occurs. Rated output *current* is the minimum guaranteed value of current supplied at the rated output voltage (or other specified voltage). Load impedances less than the specified (or implied) value can be used, but the maximum output voltage will decrease, distortion may increase, and the open-loop gain will be reduced. (All models are short-circuit protected to ground, and many are safe against shorts to the supplies.)

Settling Time
Settling time is defined as the time elapsed from the application of a perfect step input to the time when the amplifier output has entered and remained within a specified error band symmetrical about the final value. Settling time, therefore, includes the time required: for the signal to propagate through the amplifier, for the amplifier to slew from the initial value, recover from slew-rate-limited overload (if it occurs), and settle to a given error in the linear range. It may also include a "long tail" due to the time required to reach thermal equilibrium, or the settling time of compensation circuits. Settling time is usually specified for the condition of unity gain, relatively low impedance levels, and no (or a specified value of) capacitive loading, and any specified compensation. A full-scale unipolar step input is used, and both polarities are tested.

Although settling time can generally be grossly inferred from the other amplifier specifications (an amplifier that has extra-wide small-signal bandwidth, extra-fast slewing, and excellent full-power response may reasonably – but not always – be expected to have fast settling), the settling time cannot usually be rationally predicted from the other dynamic specifications.

Slewing Rate
The slewing rate of an amplifier, usually in volts per microsecond (V/μs), defines the maximum rate of change of output voltage for a large input step change.

Unity-Gain Small-Signal Response
Unity-gain small-signal response is the frequency at which the open-loop gain falls to 1V/V, or 0dB under a specified compensation condition. "Small signal" indicates that, in general, it is not possible to obtain large output voltage swing at high frequencies because of distortion due to slew-rate limiting or signal rectification. For amplifiers with symmetrical response for signals applied to either input, the dynamic behavior will be consistent for both inverting and non-inverting configurations. However, if feedforward compensation is used, fast response will be available only on the negative input, restricting fast applications of the device to the inverting mode.

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Operational Amplifiers, Theory and Practice, by J. K. Roberge, J. Wiley & Sons, 1975. Authoritative book on op amp principles and circuitry; contains extensive material on compensation to optimize dynamic performance

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ARTICLES AND APPLICATION NOTES (Available Upon Request; ask for specific issue of Analog Dialogue)

"Analog Signal Handling for High Speed and Accuracy" by A. P. Brokaw, ANALOG DIALOGUE 11-2

"Current Inverter with Wide Dynamic Range" by Barrie Gilbert, ANALOG DIALOGUE 9-1, 1975

"How to Select Operational Amplifiers", Application Note Section 21 of Volume I

"An IC-Amplifier User's Guide to Decoupling, Grounding, and Making Things Go Right for a Change," by A. P. Brokaw, Application Note Section 21 of Volume I

"Laser-Trimming on the Wafer, A Powerful New Tool for IC's" by R. Wagner, ANALOG DIALOGUE 9-3, 1975

"Noise and Operational Amplifier Circuits" by L. Smith and D. Sheingold, ANALOG DIALOGUE 3-1, 1969

"Op Amps as Electrometers," ANALOG DIALOGUE 5-2, 1971

"Settling Time of Operational Amplifiers" by R. Demrow, ANALOG DIALOGUE 4-1, 1970

"Simple Rules for Choosing Resistance Values in Adder-Subtractor Circuits" by D. Sheingold, ANALOG DIALOGUE 10-1, 1976

"Specifying and Measuring a Low-Noise FET-Input IC Op Amp" by Bill Maxwell, ANALOG DIALOGUE 8-2, 1974

"How to Test Operational Amplifier Parameters", Application Note Section 21 of Volume I

USEFUL TUTORIAL MATERIAL IN DATA SHEETS

Electrometer Circuitry, see AD515 and Models 310/311

High-Speed Amplifiers, see AD518 and Models 50/51

Low-Drift Differential Op Amp Performance, see AD504

Low-Level Applications of Chopper-Stabilized Amplifiers:
Inverting, see Models 234, 235
Non-Inverting, see Model 261

ANALOG DEVICES

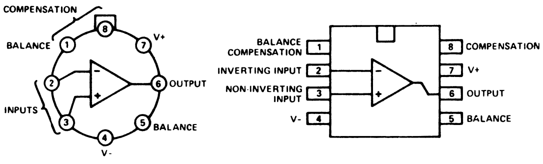
General Purpose Low Cost IC Operational Amplifier

AD101A, AD201A, AD301A, AD301AL

FEATURES

Low Bias and Offset Current
Single Capacitor External Compensation for Operating Flexibility
Nullable Offset Voltage
No Latch-Up
Fully Short Circuit Protected
Wide Operating Voltage Range

AD101 SERIES FUNCTIONAL BLOCK DIAGRAMS



TO-99 MINI DIP

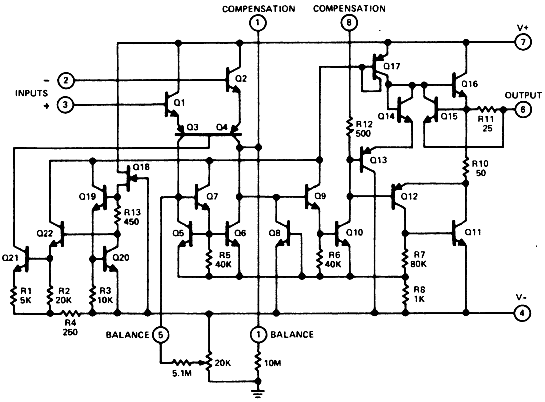
TOP VIEW

GENERAL DESCRIPTION

The Analog Devices AD101A, AD201A, AD301A and AD301AL are high performance monolithic operational amplifiers. All the circuits feature full short circuit protection, external offset voltage nulling, wide operating voltage range, and the total absence or "latch-up". Because frequency compensation is performed externally with a single capacitor (30pF maximum), the AD101A, AD201A, AD301A and AD301AL provide greater flexibility than internally compensated amplifiers since the degree of compensation can be fitted to the specific system application.

The AD101A and AD201A have identical specifications in the TO-99 package; the former guaranteed over the -55°C to +125°C temperature range, and the latter over -25°C to +85°C. The AD201A is also available in the mini-DIP package for high performance operation over the 0 to +70°C temperature range. The AD301A is specified for operation over the 0 to +70°C temperature range in both the TO-99 and mini-DIP packages. The AD301AL is the highest accuracy version of this series. Improved processing and additional electrical testing allow the user to achieve precision performance at low cost. The device provides substantially increased accuracy by reducing errors due to offset voltage (0.5mV max), offset voltage drift (5.0μV/°C max), bias current (30nA max), offset current (5nA max), voltage gain (80,000 min), PSRR (90dB min), and CMRR (90dB min). The AD301AL is also specified from 0 to +70°C and is available in the TO-99 can or 8-pin mini-DIP.

SCHEMATIC DIAGRAM



SPECIFICATIONS (typical @ +25°C and ±15V dc, unless otherwise specified)

ABSOLUTE MAXIMUM RATINGS	AD101A, AD201A, AD301A, AD301AL unless otherwise specified
Supply Voltage	
AD101A, AD201A	±22V
AD301A, AD301AL	±18V
Power Dissipation[1]	
TO-99 (Metal Can)	500mW
Dual In-Line (Mini-DIP)	500mW
Differential Input Voltage	±30V
Input Voltage[2]	±15V
Output Short Circuit Duration[3]	Indefinite
Operating Temperature Range	
AD101A	-55°C to +125°C
AD201A (TO-99)	-25°C to +85°C
AD201A (Mini-DIP)	0 to +70°C
AD301A, AD301AL	0 to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 60sec)	300°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise specified)[4]

		AD101A/AD201A			AD301A			AD301AL			
Parameter	Conditions	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
Input Offset Voltage	$R_S \leqslant 10k\Omega$		0.7	2.0		2.0	7.5		0.3	0.5	mV
Input Offset Current			1.5	10		3	50		3	5	nA
Input Bias Current			30	75		70	250		15	30	nA
Input Resistance		1.5	4		0.5	2		1.5	4		MΩ
Supply Current	$V_S = \pm 20V$		1.8	3.0							mA
	$V_S = \pm 15V$					1.8	3.0		1.8	3	mA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \geqslant 2k\Omega$	50	160		25	160		80	300		V/mV
The Following Specifications Apply Over the Operating Temperature Ranges[4]											
Input Offset Voltage	$R_S \leqslant 10k\Omega$			3.0			10		0.5	1	mV
Input Offset Current				20			70		5	10	nA
Average Temp. Coefficient of Input Offset Voltage	$T_A(\min) \leqslant T_A \leqslant T_A(\max)$		3.0	15		6.0	30		2	5	µV/°C
Average Temp. Coefficient of Input Offset Current	$+25°C \leqslant T_A \leqslant T_A(\max)$		0.01	0.1		0.01	0.3		0.01	0.1	nA/°C
	$T_A(\min) \leqslant T_A \leqslant +25°C$		0.02	0.2		0.02	0.6		0.01	0.1	nA/°C
Input Bias Current				100			300		30	45	nA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \geqslant 2k\Omega$	25			15			40	100		V/mV
Input Voltage Range	$V_S = \pm 20V$	±15									V
	$V_S = \pm 15V$				±12			±12			V
Common Mode Rejection Ratio	$R_S \leqslant 50k\Omega$	80	96		70	90		90	100		dB
Supply Voltage Rejection Ratio	$R_S \leqslant 50k\Omega$	80	96		70	96		90	100		dB
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10k\Omega$	±12	±14		±12	±14		±12	±14		V
	$V_S = \pm 15V$, $R_L = 2k\Omega$	±10	±13		±10	±13		±10	±13		V
Supply Current	$T_A = T_A(\max)$, $V_S = \pm 20V$		1.2	2.5					1.8	3	mA

[1] The maximum desirable junction temperature of the AD101A is +150°C; that of the AD201A, AD301A and AD301AL is +100°C. For operating at elevated temperatures, devices must be derated based upon a thermal resistance of +150°C/W, junction to ambient, or +45°C/W, junction to case. The thermal resistance of the Dual In-Line package is +160°C/W, junction to ambient.

[2] For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

[3] For the AD301A and AD301AL continuous short circuit is allowed for case temperatures to +70°C and ambient temperatures to +55°C.

[4] Unless otherwise specified, these specifications apply for supply voltages and ambient temperatures of ±5V to ±20V and -55°C to +125°C for the AD101A, ±5V to ±20V and -25°C to +85°C for the AD201AH (0 to +70°C for the AD201AN), and ±5V to ±15V and 0 to +70°C for the AD301A and AD301AL.

Specifications subject to change without notice.

ORDERING GUIDE

MODEL	TEMP RANGE	ORDER NUMBER*	PACKAGE OPTION**
AD301AL	0 to +70°C	AD301AL	TO-99, N8A
AD201A	−25°C to +85°C	AD201A	TO-99, N8A
AD301A	0 to +70°C	AD301A	TO-99, N8A
AD101A	−55°C to +125°C	AD101AH	TO-99

*Add package type letter: H = TO-99, N = Mini DIP.
**See Section 20 for package outline information.

FREQUENCY COMPENSATION CIRCUITS

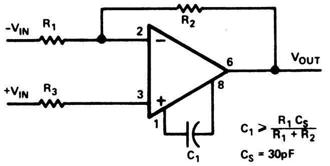


Figure 1. Single Pole Compensation

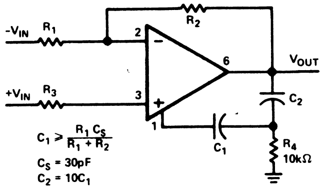


Figure 2. Two Pole Compensation

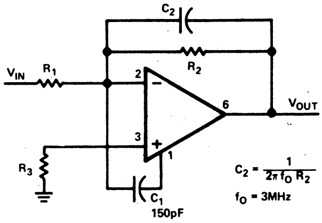
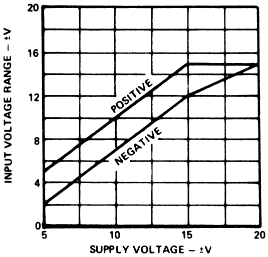
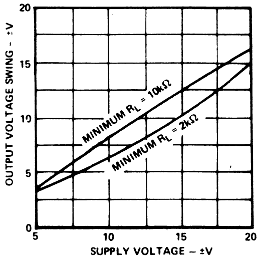


Figure 3. Feedforward Compensation

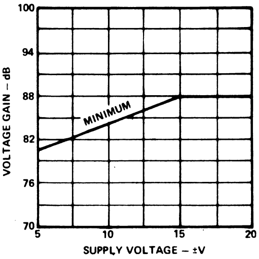
GUARANTEED PERFORMANCE CURVES (Curves apply over the Operating Temperature Ranges)



Input Voltage Range

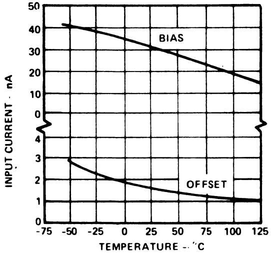


Output Swing

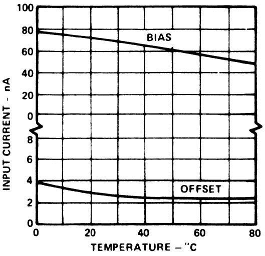


Voltage Gain

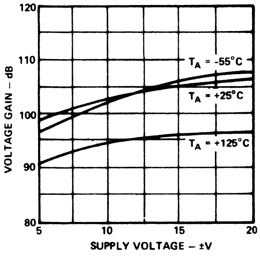
TYPICAL PERFORMANCE CURVES[4]



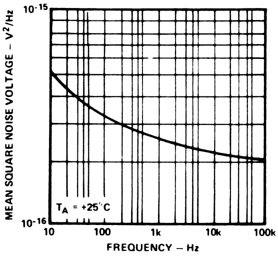
Input Current AD101A, AD201A



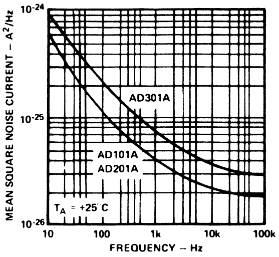
Input Current – AD301A



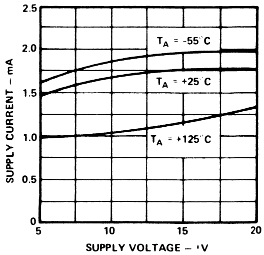
Voltage Gain



Input Noise Voltage

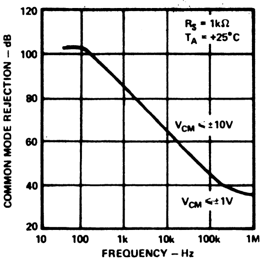


Input Noise Current

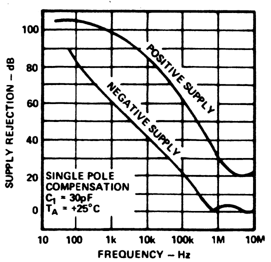


Supply Current

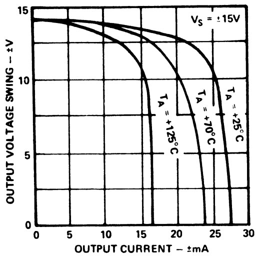
TYPICAL PERFORMANCE CURVES



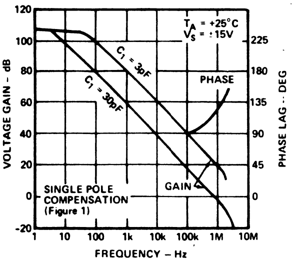
Common Mode Rejection



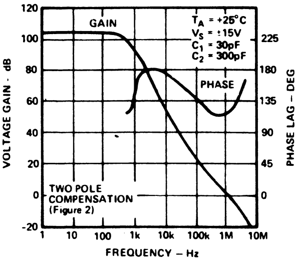
Power Supply Rejection



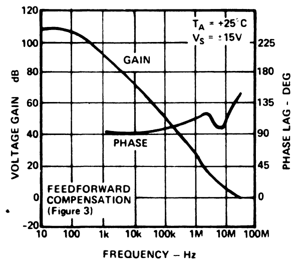
Current Limiting



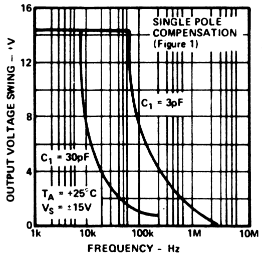
Open Loop Frequency Response



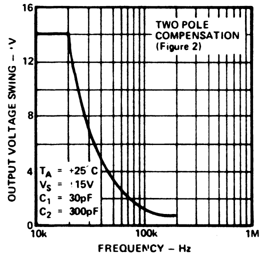
Open Loop Frequency Response



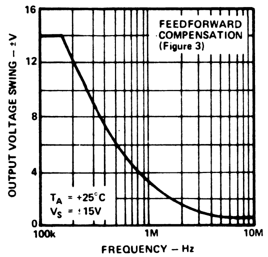
Open Loop Frequency Response



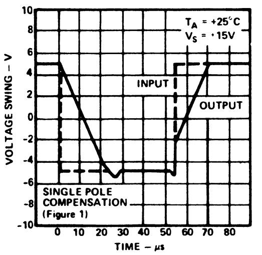
Large Signal Frequency Response



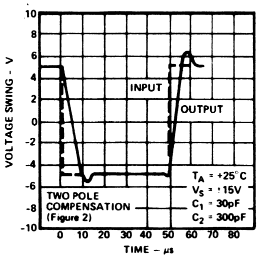
Large Signal Frequency Response



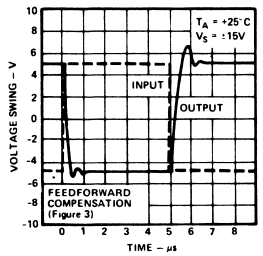
Large Signal Frequency Response



Voltage Follower Pulse Response



Voltage Follower Pulse Response



Inverter Pulse Response

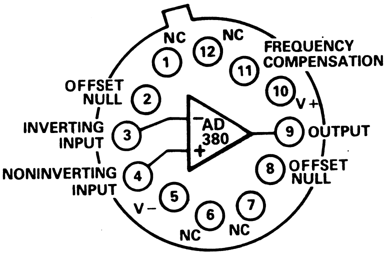
ANALOG DEVICES

Wideband, Fast-Settling FET Operational Amplifier

AD380

FEATURES
High Output Current: 50mA @ ±10V
Fast Settling to 0.1%: 130ns
High Slew Rate: 330V/μs
High Gain-Bandwidth Product: 350MHz
High Unity Gain Bandwidth: 40MHz
Low Offset Voltage (1mV for AD380K, L, S)

AD380 FUNCTIONAL BLOCK DIAGRAM



12-PIN TO-8 STYLE
TOP VIEW

PRODUCT DESCRIPTION

The AD380 is a hybrid operational amplifier that combines the low input bias current advantages of a FET input stage with the high slew rate and line driving capability of a fast, high power output amplifier.

The AD380 has a slew rate of 330V/μs and will output ±10V and ±50mA. A single external compensation capacitor allows the user to optimize the bandwidth slew rate, or settling time for the given application.

A true differential input ensures equally superior performance in all system designs whether they are inverting, noninverting, or differential.

The AD380 is especially designed for use in applications, such as fast A/D, D/A and sampling circuits, that require fast and smooth settling and FET input parameters.

The AD380 is offered in three commercial versions, J, K and L specified from 0 to +70°C and one military version, the S, specified from −55°C to +125°C. All grades are packaged in hermetically sealed TO-8 style cans. The S grade is available screened to MIL-STD-883, Level B.

PRODUCT HIGHLIGHTS

1. The AD380's high output current (50mA @ ±10V) makes it suitable for driving terminated 200Ω twisted pair outputs.
2. The fast settling output (250ns to 0.01%) makes the AD380 an ideal choice for video A/D and D/A converters and sample and hold applications.
3. The settling wave forms are not only fast but are also very smooth. The absence of large overshoot and oscillations makes the AD380 a very predictable and dependable system element.
4. The high gain-bandwidth product (350MHz) ensures low distortion in high frequency applications.
5. Laser trimming techniques reduce offset voltage to 1mV on the AD380K, L and S grades.

SPECIFICATIONS (typical @ +25°C and V_S = ±15V dc unless otherwise specified)

MODEL	AD380J	AD380K	AD380L	AD380S[1]
OPEN LOOP GAIN				
V_{OUT} = ±10V, $R_L \geq 200\Omega$	25,000 min	*	*	*
OUTPUT CHARACTERISTICS				
Voltage @ $R_L = 200\Omega$, T_A = min to max	±12V (±10V min)	*	*	*
Output Impedance (Open Loop)	100Ω	*	*	*
Short Circuit Current	100mA	*	*	*
DYNAMIC RESPONSE				
Unity Gain, Small Signal	40MHz	*	*	*
Gain-Bandwidth Product[2]	350MHz	*	*	*
Full Power Response	6MHz	*	*	*
Slew Rate	330V/µs	*	*	*
Settling Time: 10V Step to 1%	90ns	*	*	*
10V step to 0.1%	130ns	*	*	*
10V step to 0.01%	250ns	*	*	*
INPUT OFFSET VOLTAGE[3]	2.0mV max	1.0mV max	**	**
vs. Temperature[4]	50µV/°C max	20µV/°C max	10µV/°C max	20µV/°C max
vs. Supply, T_A = min to max	1mV/V max	*	*	*
INPUT BIAS CURRENT				
Either Input[5]	200pA max	100pA max	**	**
Input Offset Current	20pA	*	*	*
INPUT IMPEDANCE				
Differential	$10^{10}\|\|6pF$	*	*	*
Common Mode	$10^{10}\|\|6pF$	*	*	*
INPUT VOLTAGE RANGE				
Differential[6]	±20V	*	*	*
Common Mode	±12V (±10V min)	*	*	*
Common Mode Rejection, V_{IN} = ±10V	60dB min	*	*	*
POWER SUPPLY				
Rated Performance	±15V	*	*	*
Operating	±(10 to 20)V	*	*	*
Quiescent Current	12mA (15mA max)	*	*	*
VOLTAGE NOISE				
0.1Hz to 100Hz	4µV p-p (0.5µV rms)	*	*	*
100Hz to 10kHz	5µV p-p (1µV rms)	*	*	*
10kHz to 1MHz	50µV p-p (6µV rms)	*	*	*
TEMPERATURE RANGE				
Operating, Rated Performance	0 to +70°C	*	*	−55°C to +125°C
Storage	−65°C to +150°C	*	*	*
PACKAGE OPTION[7]				
TO-8 Style (H12A)	AD380JH	AD380KH	AD380LH	AD389SH

NOTES

[1] The AD380SH is offered screened to MIL-STD-883, Level B.

[2] Gain-Bandwidth Product measured at f = 10MHz, C_F = 0pF.

[3] Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[4] Input Offset Voltage Drift is specified with the offset voltage unnulled. Nulling will induce an additional 3µV/°C/mV of nulled offset.

[5] Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

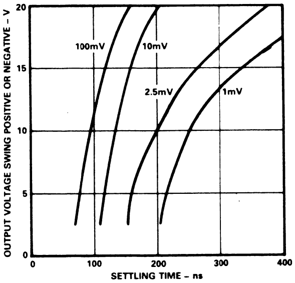
[6] Defined as the maximum safe voltage between inputs, such that neither exceeds ±10V from ground.

[7] See Section 20 for package outline information.

*Specifications same as AD380J.

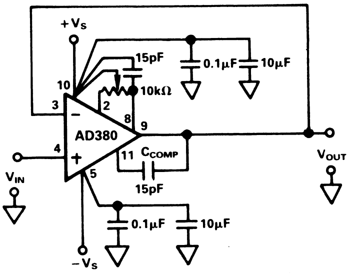
**Specifications same as AD380K.

Specifications subject to change without notice.



Output Settling Time vs. Output Voltage Swing and Error

TYPICAL APPLICATION



Noninverting Unity Gain Amplifier

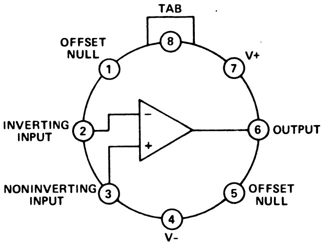
ANALOG DEVICES

High Speed, Low Drift FET Operational Amplifier

AD381

FEATURES
High Slew Rate: 30V/μs
Fast Settling to 0.01%: 700ns
High Output Current: 10mA
Low Drift (5μV/°C–AD381L)
Low Offset Voltage (0.25mV–AD381L)
Low Input Bias Currents (25pA–AD381L, K)
Low Noise (2μV p-p)

AD381 FUNCTIONAL BLOCK DIAGRAM



TO-99 STYLE
TOP VIEW

PRODUCT DESCRIPTION

The AD381 is a hybrid operational amplifier combining the very low input bias current advantages of a FET input stage with a high speed output stage.

The offset voltage (0.25mV maximum for AD381L) and offset voltage drift (5μV/°C maximum for AD381L) are exceptionally low for a high speed operational amplifier.

In addition to superior low drift performance, the AD381 offers the lowest guaranteed input bias currents of any wideband FET amplifier with 50pA max for the J grade and 25pA max for the K and L grades. Since Analog Devices, unlike most other manufacturers, specifies input bias currents with the amplifiers warmed-up, our FET amplifiers are specified under actual operating conditions

The AD381 is especially designed for use in applications, such as precision, high speed data acquisition systems and signal conditioning circuits that require excellent input parameters and a fast output.

The AD381 if offered in three commercial versions, J, K and L specified from 0 to +70°C and two military versions, the S and T, specified from -55°C to +125°C. All grades are packaged in hermetically sealed TO-99 style cans. The S and T grades are available screened to MIL-STD-883, Level B.

PRODUCT HIGHLIGHTS

1. Advanced laser trimming techniques reduce offset voltage drift to 5μV/°C max and offset voltage to only 0.25mV max on the AD381L.
2. Analog Devices FET processing provides 25pA max (10pA typical) bias currents, specified after 5 minutes of warm-up.
3. The AD381's high slew rate (30V/μs) and high gain-bandwidth product (5MHz) makes it an ideal choice for sample and hold and high speed integrator circuits.
4. The fast settling time (700ns + 0.01%) makes the AD381 ideal for D/A and A/D converter applications.
5. The AD381 is capable of driving 1kΩ loads over the commercial temperature range.

SPECIFICATIONS (typical @ +25°C and V_S = ±15V dc unless otherwise specified)

MODEL	AD381J	AD381K	AD381L	AD381S[1]	AD381T[1]
OPEN LOOP GAIN					
V_{OUT} = ±10V, $R_L \geq 2k\Omega$	60,000 min	100,000 min	**	**	**
OUTPUT CHARACTERISTICS					
Voltage @ R_L = 1kΩ, T_A = min to max	±12V (±10V min)	*	*	*[2]	*[2]
Voltage @ R_L = 2kΩ, T_A = min to max	±12V (±10V min)	*	*	*	*
Voltage @ R_L = 10kΩ, T_A = min to max	±13V (±12V min)	*	*	*	*
Short Circuit Current	20mA	*	*	*	*
DYNAMIC RESPONSE					
Unity Gain, Small Signal	5MHz	*	*	*	*
Full Power Response	500kHz	*	*	*	*
Slew Rate, Unity Gain	30V/µs	*	*	*	*
Settling Time: 10V Step to 0.1%	700ns	*	*	*	*
10V Step to 0.01%	1.2µs	*	*	*	*
INPUT OFFSET VOLTAGE[3]	1.0mV max	0.5mV max	0.25mV max	*	**
vs. Temperature[4]	15µV/°C max	10µV/°C max	5µV/°C max	10µV/°C max	5µV/°C max
vs. Supply	200µV/V max	100µV/V max	**	**	**
INPUT BIAS CURRENT[5]					
Either Input	10pA (50pA max)	10pA (25pA max)	**	**	**
Input Offset Current	5pA	2pA	**	**	**
INPUT IMPEDANCE					
Differential	$10^{12}\Omega \| 7pF$	*	*	*	*
Common Mode	$10^{12}\Omega \| 7pF$	*	*	*	*
INPUT VOLTAGE RANGE					
Differential[6]	±20V	*	*	*	*
Common Mode	±12V (±10V min)	*	*	*	*
Common Mode Rejection, V_{in} = ±10V	76dB	80dB min	**	**	**
POWER SUPPLY					
Rated Performance	±15V	*	*	*	*
Operating	±(5 to 18)V	*	*	*	*
Quiescent Current	3.3mA (5mA max)	*	*	*	*
VOLTAGE NOISE					
0.1-10Hz	2µV p-p	*	*	*	*
10Hz	$70nV/\sqrt{Hz}$	*	*	*	*
100Hz	$45nV/\sqrt{Hz}$	*	*	*	*
1kHz	$30nV/\sqrt{Hz}$	*	*	*	*
10kHz	$25nV/\sqrt{Hz}$	*	*	*	*
TEMPERATURE RANGE					
Operating, Rated Performance	0 to +70°C	*	*	-55°C to +125°C	***
Storage	-65°C to +150°C	*	*	*	*
PACKAGE OPTION[7]					
TO-99 Style (H08B)	AD381JH	AD381KH	AD381LH	AD381SH	AD381TH

NOTES

[1] The AD381SH and AD381TH are offered screened to MIL-STD-883. Level B.

[2] The AD381S, T have an output voltage of ±12V (±10V min) for a 1kΩ load from T_{min} to +100°C. From +100°C to +125°C the output current is 7mA.

[3] Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[4] Input Offset Voltage Drift is specified with the offset voltage unnulled. Nulling will induce an additional 3µV/°C/mV of nulled offset.

[5] Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

[6] Defined as the maximum safe voltage between inputs, such that neither exceeds ±10V from ground.

[7] See Section 20 for package outline information.

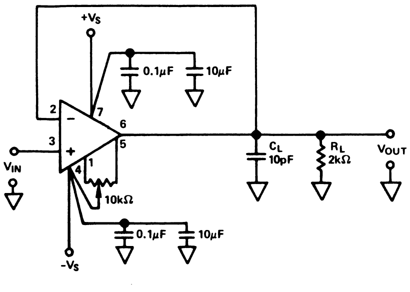
*Specifications same as AD381J.

**Specifications same as AD381K.

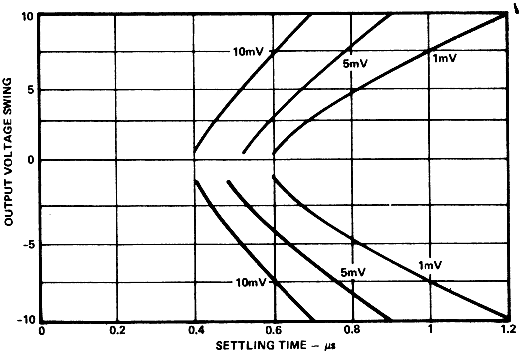
***Specifications same as AD381S.

Specifications subject to change without notice.

TYPICAL APPLICATION



Unity Gain Follower



Output Settling Time vs. Output Voltage Swing and Error

ANALOG DEVICES

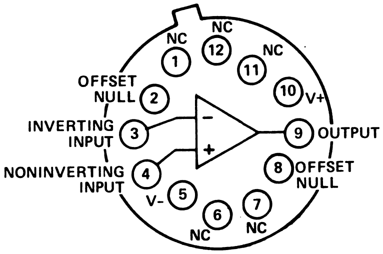
High Speed, Low Drift FET Operational Amplifier

AD382

FEATURES

High Slew Rate: 30V/μs
Fast Settling to 0.1%: 750ns
High Output Current: 50mA min
Low Drift (5μV/°C–AD382L)
Low Offset Voltage (0.25mV–AD382L)
Low Input Bias Currents (25pA–AD382L, K)
Low Noise (2μV p-p)

AD382 FUNCTIONAL BLOCK DIAGRAM



12-PIN, TO-8 STYLE
TOP VIEW

PRODUCT DESCRIPTION

The AD382 is a hybrid operational amplifier combining the very low input bias current advantages of a FET input stage with high slew rate and line driving capability of a high power output stage.

The offset voltage (0.25mV maximum for AD382L) and offset voltage drift (5μV/°C maximum for AD382L) are exceptionally low for a high speed operational amplifier.

In addition to superior low drift performance, the AD382 offers the lowest guaranteed input bias currents of any wideband FET amplifier with 50pA max for the J grade and 25pA max for the L grade. Since Analog Devices, unlike most other manufacturers, specifies input bias current with the amplifiers warmed-up, our FET amplifiers are specified under actual operating conditions.

The AD382 is especially designed for use in applications, such as precision high speed data acquisition systems and signal conditioning circuits, that require excellent input parameters and a fast, high power output.

The AD382 is offered in three commercial versions, J, K and L specified from 0 to +70°C and two military versions, the S and T specified from -55°C to +125°C. All grades are packaged in hermetically sealed TO-8 style cans. The S and T grades are available screened to MIL-STD-883, Level B.

PRODUCT HIGHLIGHTS

1. Laser trimming techniques reduce offset voltage drift to 5μV/°C max and reduce offset voltage to only 0.25mV max on the AD382L.
2. Analog Devices FET processing provides 25pA max (10pA typical) bias currents specified after 5 minutes of warm-up.
3. Low voltage noise and outstanding offset performance make the AD382 a true precision FET amplifier.
4. The fast settling output (750ns to 0.1%) makes the AD382 an ideal choice for D/A and A/D converter amplifier applications.
5. The AD382's high output current (50mA minimum at ±10 volts for commercial temperature range versions makes it suitable for driving terminated (200Ω) twisted pair outputs.

SPECIFICATIONS (typical @ +25°C and V_S = ±15V dc unless otherwise specified)

MODEL	AD382J	AD382K	AD382L	AD382S[1]	AD382T[1]
OPEN LOOP GAIN					
V_{OUT} = ±10V, R_L = 200Ω	30,000 min	40,000 min	**	**	**
R_L = 1kΩ	100,000 min	150,000 min	**	**	**
OUTPUT CHARACTERISTICS					
Voltage @ R_L = 200Ω, T_A = min to max	±12V (±10V min)	*	*	*[2]	*[2]
Voltage @ R_L = 10kΩ, T_A = min to max	±13V (±12V min)	*	*	*	*
Short Circuit Current	80mA	*	*	*	*
FREQUENCY RESPONSE					
Unity Gain, Small Signal	5MHz	*	*	*	*
Full Power Response	500kHz	*	*	*	*
Slew Rate, Unity Gain	30V/μs	*	*	*	*
Settling Time to 0.01%	1.3μs	*	*	*	*
INPUT OFFSET VOLTAGE[3]	1.0mV max	0.5mV max	0.25mV max	*	**
vs. Temperature[4]	15μV/°C max	10μV/°C max	5μV/°C max	10μV/°C max	5μV/°C max
vs. Supply, T_A = min to max	200μV/V max	100μV/V max	**	**	**
INPUT BIAS CURRENT[5]					
Either Input	10pA (50pA max)	10pA (25pA max)	**	**	**
Input Offset Current	5pA	2pA	**	**	**
INPUT IMPEDANCE					
Differential	10^{12}Ω‖7pF	*	*	*	*
Common Mode	10^{12}Ω‖7pF	*	*	*	*
INPUT VOLTAGE RANGE					
Differential[6]	±20V	*	*	*	*
Common Mode	±12V (±10V min)	*	*	*	*
Common Mode Rejection, V_{IN} = ±10V	76dB min	80dB min	**	**	**
POWER SUPPLY					
Rated Performance	±15V	*	*	*	*
Operating	±(5 to 18)V	*	*	*	*
Quiescent Current	3.5mA (6mA max)	*	*	*	*
VOLTAGE NOISE					
0.1-10Hz	2μV p-p	*	*	*	*
10Hz	70nV/√Hz	*	*	*	*
100Hz	45nV/√Hz	*	*	*	*
1kHz	30nV/√Hz	*	*	*	*
10kHz	25nV/√Hz	*	*	*	*
TEMPERATURE RANGE					
Operating, Rated Performance	0 to +70°C	*	*	-55°C to +125°C	***
Storage	-65°C to +150°C	*	*	*	*
PACKAGE OPTION[7]					
TO-8 Style (H12A)	AD382JH	AD382KH	AD382LH	AD382SH	AD382TH

NOTES:

[1] The AD382S and AD382T are offered screened to MIL-STD-883, Level B.

[2] The AD382S, T have an output voltage of ±12V (±10V min) for a 200Ω load from T_{min} to +100°C. From +100°C to +125°C the output current is 7mA.

[3] Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[4] Input Offset Voltage Drift is specified with the offset voltage unnulled. Nulling will induce an additional 3μV/°C/mV of nulled offset.

[5] Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

[6] Defined as the maximum safe voltage between inputs, such that neither exceeds ±10V from ground.

[7] See Section 20 for package outline information.

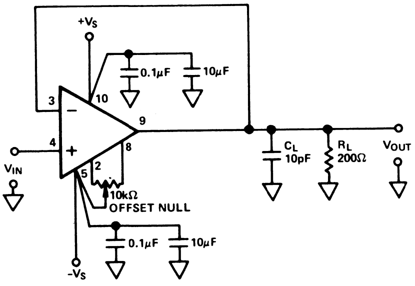
*Specifications same as AD382J.

**Specifications same as AD382K.

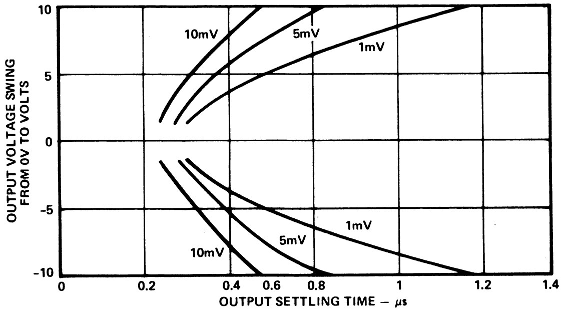
***Specifications same as AD382S.

Specifications subject to change without notice.

TYPICAL APPLICATION



Unity Gain Follower



Output Settling Time vs. Output Voltage Swing and Error

ANALOG
DEVICES

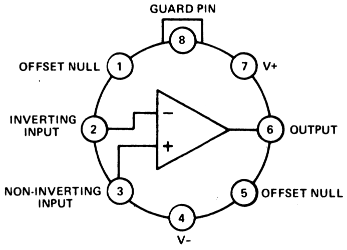
High Accuracy Low Offset IC FET-Input Op Amps

AD503, AD506

FEATURES

Low I_b: 15pA max (AD503J, AD506J)
5pA max (AD506L)
Low V_{OS}: 1mV max (AD506L)
Low Drift: 25μV/°C max (AD503K, AD506K)
10μV/°C max (AD506L)

AD503, AD506 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW

PRODUCT DESCRIPTION

The AD503J/AD506J, AD503K/AD506K, AD506L and AD503S/AD506S are IC FET input op amps that provide the user with input currents of a few pA, high overall performance, low cost, and accurately specified, predictable operation. The devices achieve maximum bias currents as low as 5pA, minimum gain of 75,000, CMRR of 80dB, and a minimum slew rate of 3V/μs. They are free from latch-up and are short circuit protected. No external compensation is required as the internal 6dB/octave rolloff provides stability in closed loop applications.

The AD503 is suggested for all general purpose FET input amplifier requirements where low cost is of prime importance. The AD506, with specifications otherwise similar to the AD503, offers significant improvement in offset voltage and nulled offset voltage drift by supplementing the AD503 configuration with internal laser trimming of thin film resistors to provide typical offset voltages below 1mV.

The AD503 and AD506 are especially designed for applications involving the measurement of low level currents or small voltages from high impedance sources, in which bias current can be a primary source of error. Input bias current contributes to error in two ways: (1) in current measuring configurations, the bias current limits the resolution of a current signal; (2) the bias current produces a voltage offset which is proportional to the value of input resistance (in the case of an inverting configuration) or source impedance (when the non-inverting "buffer" connection is used). The AD503 and AD506 IC FET input amplifiers, therefore, are of use where small currents are to be measured or where relatively low voltage drift is necessary despite large values of source resistance.

All the circuits are supplied in the TO-99 package; the AD503J, K and AD506J, K and L are specified for 0 to +70°C temperature range operation; the AD503S and AD506S for operation from −55°C to +125°C.

PRODUCT HIGHLIGHTS

1. The AD503 and AD506 op amps meet their published input bias current and offset voltage specs after full warmup. Conventional high speed IC testing does not allow for self-heating of the chip due to internal power dissipation under operating conditions.
2. The bias currents of the AD503 and AD506 are specified as a maximum for *either* input. Conventional IC FET op amps generally specify bias currents as the average of the two input currents.
3. Offset voltage nulling of the AD503 and AD506 is accomplished without affecting the operating current of the FET's and results in relatively small changes in temperature drift characteristics. The additional drift induced by nulling is only ±0.8μV/°C per millivolt of nulled offset for the AD506 and ±2.0μV/°C per millivolt of nulled offset for the AD503, compared to several times this for other IC FET op amps.
4. The gain of the AD503 and AD506 is measured with the offset voltage nulled. Nulling a FET input op amp can cause the gain to decrease below its specified limit. The gain of the AD503 and AD506 is fully guaranteed with the offset voltage both nulled and unnulled.
5. Bootstrapping of the input FET's achieves a superior CMRR of 80dB, while reducing bias currents and maintaining them constant through the CMV range.

SPECIFICATIONS (typical @ +25°C and ±15V dc, unless otherwise noted)

PARAMETER	AD503J	AD503K	AD503S
OPEN LOOP GAIN[1]			
V_{OUT} = ±10V, $R_L \geqslant 2k\Omega$	20,000 min (50,000 typ)	50,000 min (120,000 typ)	**
T_A = min to max	15,000 min	40,000 min	25,000 min
OUTPUT CHARACTERISTICS			
Voltage @ $R_L = 2k\Omega$, T_A = min to max	±10V min (±13V typ)	*	*
@ $R_L = 10k\Omega$, T_A = min to max	±12V min (±14V typ)	*	*
Load Capacitance[2]	750pF	*	*
Short Circuit Current	25mA	*	*
FREQUENCY RESPONSE			
Unity Gain, Small Signal	1.0MHz	*	*
Full Power Response	100kHz	*	*
Slew Rate, Unity Gain	3.0V/μs min (6.0V/μs typ)	*	*
Settling Time, Unity Gain (to 0.1%)	10μs	*	*
INPUT OFFSET VOLTAGE[3]	50mV max (20mV typ)	20mV max (8mV typ)	**
vs. Temperature, T_A = min to max	75μV/°C max (30μV/°C typ)	25μV/°C max (10μV/°C typ)	50μV/°C max (20μV/°C typ)
vs. Supply, T_A = min to max	400μV/V max (200μV/V typ)	200μV/V max (100μV/V typ)	**
INPUT BIAS CURRENT			
Either Input[4]	15pA max (5pA typ)	10pA max (2.5pA typ)	**
INPUT IMPEDANCE			
Differential	$10^{11}\,\Omega \| 2pF$	*	*
Common Mode	$10^{12}\,\Omega \| 2pF$	*	*
INPUT NOISE			
Voltage, 0.1Hz to 10Hz	15μV (p-p)	*	*
5Hz to 50kHz	5.0μV (rms)	*	*
f = 1kHz (spot noise)	$30.0nV/\sqrt{Hz}$	*	*
INPUT VOLTAGE RANGE			
Differential[5]	±3.0V	*	*
Common Mode, T_A = min to max	±10V min (±12V typ)	*	*
Common Mode Rejection, V_{IN} = ±10V	70dB min (90dB typ)	80dB min (90dB typ)	**
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	±(5 to 18)V	*	±(5 to 22)V
Quiescent Current	7mA max (3mA typ)	*	*
TEMPERATURE			
Operating, Rated Performance	0 to +70°C	*	-55°C to +125°C
Storage	-65°C to +150°C	*	*
PACKAGE OPTIONS:[6] TO-99 Style (H08B)	AD503JH	AD503KH	AD503SH

NOTES:

[1] Open Loop Gain is specified with V_{OS} both nulled and unnulled.

[2] A conservative design would not exceed 500pF of load capacitance.

[3] Input offset voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[4] Bias current specifications are guaranteed after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

[5] See comments in Input Considerations Section.

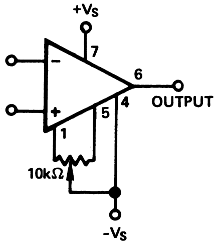
[6] See Section 20 for package outline information.

*Specifications same as for AD503J.

**Specifications same as for AD503K.

Specifications subject to change without notice.

AD506J	AD506K	AD506L	AD506S
*	**	75,000 min (100,000 typ)	**
*	**	50,000 min	25,000 min
*	*	*	*
*	*	*	*
1000pF	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
3.5mV max (1.0mV typ)	1.5mV max (0.5mV typ)	1.0mV max (0.4mV typ)	1.5mV max (0.5mV typ)
*	**	10μV/°C max (5μV/°C typ)	50μV/°C max (20μV/°C typ)
**	100μV/V max (50μV/V typ)	100μV/V max (50μV/V typ)	100μV/V max (50μV/V typ)
*	**	5pA max (2pA typ)	**
*	*	*	*
*	*	*	*
40μV (p-p)	*	*	*
8μV (rms)	*	6μV (rms)	*
80nV/√Hz	*	25nV/√Hz	*
±4V	*	*	*
*	*	*	*
*	**	**	**
*	*	*	*
*	*	*	±(5 to 22)V
7mA max (5mA typ)	*	*	*
*	*	*	-55°C to +125°C
*	*	*	*
AD506JH	AD506KH	AD506LH	AD506SH



Standard Offset Null Circuit

APPLICATIONS CONSIDERATIONS

Bias Current

Most IC FET op amp manufacturers specify maximum bias currents as the value immediately after turn-on. Since FET bias currents double every 10°C and since most FET op amps have case temperature increases of 15°C to 20°C above ambient, initial "maximum" readings may be only ¼ of the true warmed up value. Furthermore, most IC FET op amp manufacturers specify I_b as the average of both input currents, sometimes resulting in twice the "maximum" bias current appearing at the input being used. The total result is that 8X the expected bias current may appear at either input terminal in a warmed up operating unit.

The AD503 and AD506 specify maximum bias currents at either input after warmup, thus giving the user the values he expected.

Improving Bias Current Beyond Guaranteed Values

Bias currents can be substantially reduced in the AD503 and AD506 by decreasing the junction temperature of the device. One technique to accomplish this is to reduce the operating supply voltage. This procedure will decrease the power dissipation of the device, which will in turn result in a lower junction temperature and lower bias currents. The supply voltage effect on bias current is shown in Figure 1.

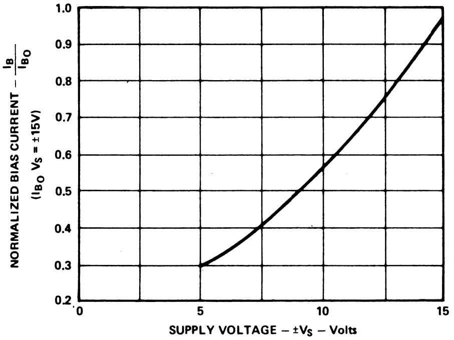


Figure 1. Normalized Bias Current vs. Supply Voltage

Operation of the AD503K and AD506K at ±5V reduces the warmed up bias current by 70% to a typical value of 0.75pA.

A second technique is the use of a suitable heat sink. Wakefield Engineering Series 200 heat sinks were selected to demonstrate this effect. The characteristic bias current vs. case temperature above ambient is shown in Figure 2. Bias current has been normalized with unity representing the 25°C free air reading.

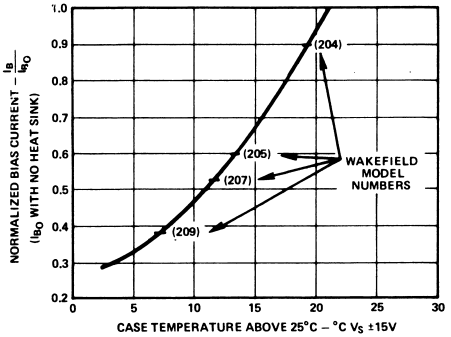


Figure 2. Normalized Bias Current vs. Case Temperature

Note that the use of the model 209 heat sink reduces warmed up bias current by 60% to 1.0pA in the AD503/AD506K.

Both of these techniques may be used together for obtaining lower bias currents. Remember that loading the output can also affect the power dissipation.

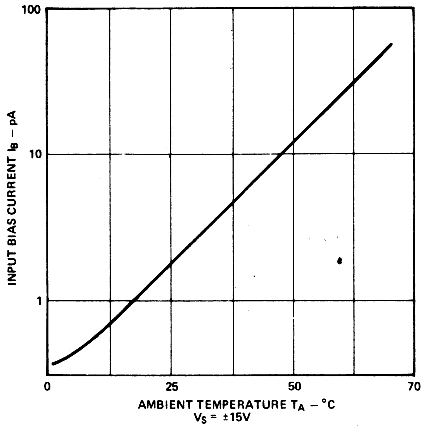


Figure 3. Input Bias Current vs. Temperature

Input Considerations

The common mode input characteristic is shown in Figure 4. Note that positive common mode inputs up to +13.5 volts and negative common mode inputs to $-V_S$ are permissible, without incurring excessive bias currents. To prevent possible damage to the unit, do not exceed $V_{CM} = V_S$.

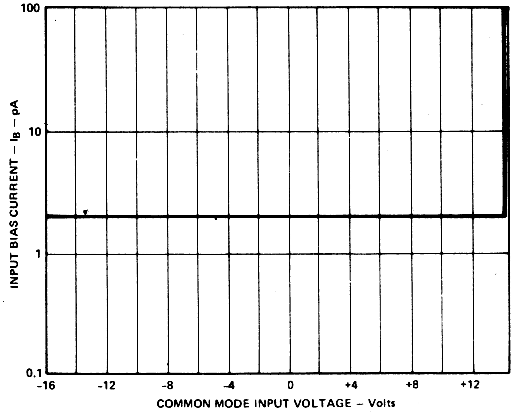


Figure 4. Input Bias Current vs. Common Mode Voltage

Like most other FET input op amps, the AD503 and AD506 display a degraded bias current specification when operated at moderate differential input voltages. The AD503 maintains its specified bias current up to a differential input voltage of ±3V typically, while the AD506's bias current performance is not significantly degraded for $V_{diff} \leqslant 4V$ typically. Above V_{diff} = ±3V in the AD503 and V_{diff} = ±4V in the AD506, the bias current will increase to approximately 400µA. This is not a failure mode. Above ±10V differential input voltage, the bias current will increase 100µA/V_{diff} (in volts), and other parameters may suffer degradation.

ANALOG DEVICES

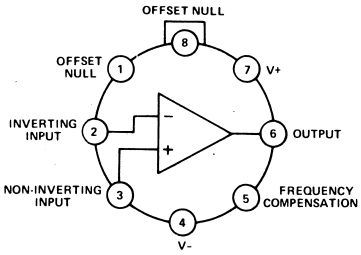
High Accuracy IC Operational Amplifier

AD504

FEATURES

Low V_{OS}: 500μV max (AD504M)
High Gain: 10^6 min (AD504L, M, S)
Low Drift: 0.5μV/°C max (AD504M)
Free of Popcorn Noise

AD504 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW

PRODUCT DESCRIPTION

The Analog Devices AD504J, K, L, M and S IC operational amplifiers provide ultra-low drift and extremely high gain, comparable to that of modular amplifiers, for precision applications. A new double integrator circuit concept combined with a precise thermally balanced layout achieves gain greater than 10^6, offset voltage drift of less than 1μV/°C, small signal unity gain bandwidth of 300kHz, and slew rate of 0.12V/μs. Because of monolithic construction, the cost of the AD504 is significantly below that of modules, and becomes even lower with larger quantity requirements. The amplifier is externally compensated for unity gain with a single 470pF capacitor; no compensation is required for gains above 500. The inputs are fully protected, which permits differential input voltages of up to $\pm V_S$ without voltage gain or bias current degradation due to reverse breakdown. The output is also protected from short circuits to ground and/or either supply voltage, and is capable of driving 1000pF of load capacitance. The AD504J, K, L and M are supplied in the hermetically sealed TO-99 package, and are specified for operation over the 0 to +70°C temperature range. The AD504S is specified over the -55°C to +125°C temperature range and is also supplied in the TO-99 package.

PRODUCT HIGHLIGHTS

1. Fully guaranteed and 100% tested 1μV/°C maximum voltage drift combined with voltage offset of 500μV (AD504L).
2. Fully protected input ($\pm V_S$) and output circuitry. The input protection circuit prevents offset voltage and bias current degradation due to reverse breakdown, and is of critical importance in this type of device whose overall performance is strongly dependent upon front-end stability.
3. Single capacitor compensation eliminates elaborate stabilizing networks while providing flexibility not possible with an internally compensated op amp. This feature allows bandwidth to be optimized by the user for his particular application.
4. High gain is maintained independent of offset nulling, power supply voltage and load resistance.
5. Bootstrapping of the critical input transistor quad produces CMRR and PSRR compatible with the tight 1μV/°C drift. CMRR and PSRR are both in the vicinity of 120dB.

SPECIFICATIONS (typical @ +25°C and ±15V dc unless otherwise noted)

PARAMETER	AD504J	AD504K	AD504L
OPEN LOOP GAIN			
$V_{OS} = \pm 10V$, $R_L \geqslant 2k\Omega$	250,000 min (4×10^6 typ)	500,000 min (4×10^6 typ)	10^6 min (8×10^6 typ)
$T_{min} \leqslant T_A \leqslant T_{max}$	125,000 min (10^6 typ)	250,000 min (10^6 typ)	500,000 min (10^6 typ)
OUTPUT CHARACTERISTICS			
Voltage at $R_L \geqslant 2k\Omega$, $T_{min} \leqslant T_A \leqslant T_{max}$	±10V min (±13V typ)	*	*
Load Capacitance	1000pF	*	*
Output Current	10mA min	*	*
Short Circuit Current	25mA	*	*
FREQUENCY RESPONSE			
Unity Gain, Small Signal, $C_c = 390pF$	300kHz	*	*
Full Power Response, $C_c = 390pF$	1.5kHz	*	*
Slew Rate, Unity Gain, $C_c = 390pF$	0.12V/µs	*	*
INPUT OFFSET VOLTAGE			
Initial Offset, $R_S \leqslant 10k$	2.5mV max (0.5mV typ)	1.5mV max (0.5mV typ)	0.5mV max (0.2mV typ)
vs Temp, $T_{min} \leqslant T_A \leqslant T_{max}$, V_{OS} nulled	5.0µV/°C max (0.5µV/°C typ)	3.0µV/°C max (0.5µV/°C typ)	1.0µV/°C max (0.3µV/°C typ)
$T_{min} \leqslant T_A \leqslant T_{max}$, V_{OS} unnulled†	10µV/°C max (1.5µV/°C typ)	5.0µV/°C max (1.5µV/°C typ)	2.0µV/°C max (1.0µV/°C typ)
vs Supply	25µV/V max	15µV/V max	10µV/V max
@ $T_{min} \leqslant T_A \leqslant T_{max}$	40µV/V	25µV/V max	15µV/V max
vs Time	20µV/mo	15µV/mo	10µV/mo
INPUT OFFSET CURRENT			
@ $T_A = 25°C$	40nA max	15nA max	10nA max
INPUT BIAS CURRENT			
Initial	200nA max	100nA max	80nA max
T_{min} to T_{max}	300nA max	150nA max	100nA max
vs Temp, T_{min} to T_{max}	300pA/°C	250pA/°C	200pA/°C
INPUT IMPEDANCE			
Differential	0.5MΩ	1.0MΩ	1.3MΩ
Common Mode	100MΩ‖4pF	*	*
INPUT NOISE			
Voltage, 0.1 to 10Hz	1.0µV (p-p)	*	*
100Hz	10nV/$\sqrt{Hz}$(rms)	*	*
1kHz	8nV/$\sqrt{Hz}$(rms)	*	*
Current, 0.1 to 10Hz	50pA(p-p)	*	*
100Hz	0.6pA/$\sqrt{Hz}$(rms)	*	*
1kHz	0.5pA/$\sqrt{Hz}$(rms)	*	*
INPUT VOLTAGE RANGE			
Differential or Common Mode, Max Safe	$\pm V_S$	*	*
Common Mode Rejection, $V_{IN} = \pm 10V$	94dB min (120dB typ)	100dB min (120dB typ)	110dB min (120dB typ)
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	±(5 to 18)V	*	*
Current, Quiescent	±4.0mA max (±1.5mA typ)	±3.0mA max (±1.5mA typ)	±3.0mA max (±1.5mA typ)
TEMPERATURE RANGE			
Operating, Rated Performance (T_{min} to T_{max})	0 to +70°C	*	*
Storage	-65°C to +150°C	*	*
PACKAGE OPTION:[1] TO-99 Style (H08B)	AD504JH	AD504KH	AD504LH

*Specifications same as for AD504J.

†This parameter is not 100% tested. Typically, 90% of the units meet this limit.

Specifications subject to change without notice.

[1] See Section 20 for package outline information.

NOTE

Analog Devices 100% tests and guarantees all specified maximum and minimum limits. Certain parameters, because of the relative difficulty and cost of 100% testing, have been specified as "typical" numbers. At ADI, "typical" numbers are subjected to rigid statistical sampling and outgoing quality control procedures, resulting in "typicals" that are indicative of the performance that can be expected by the user.

AD504M	AD504S(AD504S/883)
10^6 min (8 x 10^6 typ)	10^6 min (8 x 10^6 typ)
500,000 min (10^6 typ)	250,000 min
*	*
*	*
*	*
*	*
*	*
*	*
*	*
0.5mV max (0.2mV typ)	0.5mV max
0.5µV/°C max (0.2µV/°C typ)	1.0µV/°C max (0.3µV/°C typ)
1.0µV/°C max (0.5µV/°C typ)	2.0µV/°C max (1.0µV/°C typ)
10µV/V max	10µV/V max
15µV/V max	20µV/V max
10µV/mo	10µV/mo
10nA max	10nA max
80nA max	80nA max
100nA max	200nA max
200pA/°C	200pA/°C
1.3MΩ	1.3MΩ
*	*
0.6µV (p-p) max	*
10nV/√Hz max	*
9nV/√Hz max	*
50pA p-p max	*
0.6pA/√Hz max	*
0.3pA/√Hz max	*
*	*
110dB min (120dB typ)	110dB min (120dB typ)
*	*
*	*
±3.0mA max (±1.5mA typ)	±3mA max (±1.5mA typ)
*	-55°C to +125°C
*	-65°C to +150°C
AD504MH	AD504SH

OFFSET VOLTAGE DRIFT AND NULLING

Most differential operational amplifiers have provisions for adjusting the initial offset voltage to zero with an external trim potentiometer. It is often not realized that there is a resulting increase in voltage drift which accompanies this initial offset adjustment. The increased voltage drift can often be safely ignored in conventional amplifiers, since it may be a small percentage of the specified voltage drift. However, the voltage drift of the AD504 is so small that this effect cannot be ignored.

To achieve low drift over temperature, it is necessary to maintain equal current densities in the input pair. Unless the initial offset nulling circuit is carefully arranged, the nulling circuits will themselves drift with temperature. The resulting change in the input transistor current *ratio* will produce an additional input offset voltage drift. This drift component can actually be larger than the unnulled drift.

Typically, IC op amps are nulled by using an external potentiometer to adjust the ratio of two resistances. These resistances are part of a network from which the input stage emitter currents are derived. Most commercially available op amps use diffused resistors in their internal nulling circuitry, which typically display large positive temperature coefficients of the order of 2000ppm/°C. As a result of the failure of the external potentiometer resistance to track the diffused resistors over temperature, the two resistance branches will drift relative to one another. This will cause a change in the emitter current ratio and induce an offset drift with temperature.

In the AD504, this problem is reduced an order of magnitude by the use of thin film resistors deposited on the monolithic amplifier chip. These resistors, which make up the critical bias network from which the input stage emitter current balance is determined, display typical temperature coefficients of less than 200ppm/°C, an order of magnitude improvement over diffused types. Thus, when the initial offset of the AD504 is trimmed using a low TC pot in combination with the thin film network, the drift induced by nulling even relatively large offsets is extremely small. This means that AD504 units of all three grades (J, K, L) will typically yield significantly better temperature performance in nulled applications than an all-diffused amplifier with comparable initial offset.

Since the intrinsic offset drift of the amplifier is improved by nulling, the direct measurement of any additional drift induced by differing temperature coefficients of resistors would be extremely difficult. However, the *induced* offset drift can be established by calculating the change in the emitter current ratio brought about by the differing TC's of resistances. From the change in this ratio, the offset voltage contribution at any temperature can be easily calculated.

A simple computer program was written to calculate induced offset drift as a function of initial offset voltage nulled. This calculation was made assuming zero TC of the amplifier resistors, and TC's of 200ppm/°C and 2000ppm/°C for the null pot. These results are very nearly equivalent to the case where the pot has zero temperature coefficient and the amplifier resistors drift. The results of these calculations are summarized graphically in Figure 1.

Figure 1 shows the variation of induced voltage drift with nulled offset voltage for:

a. AD504 op amp.
b. 725 typ op amp.

Note that as a result of nulling 1.4mV of offset, ***the AD504 induces 30X less offset drift (only 0.05µV/°C) than the 725 type op amp*** with its actual diffused resistor values and the recommended 100k pot to trim the offset. Actual induced drifts from this source for the AD504 may be even lower in the practical case when metal film resistors or pots are used for nulling, since their TC's tend to closely ***match*** the negative TC's of the thin film resistors on the AD504 chip.

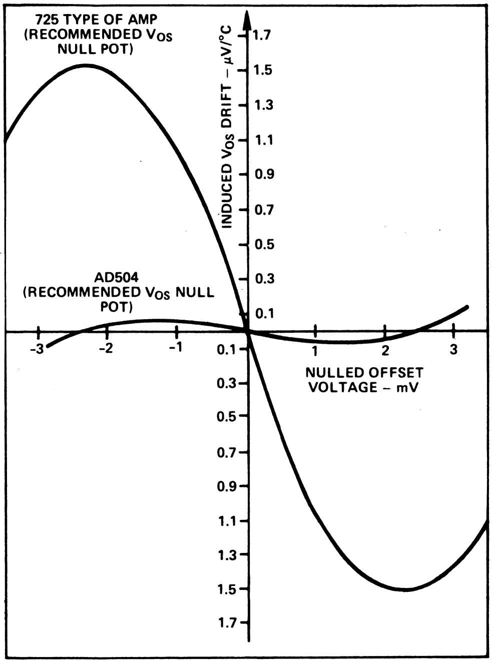


Figure 1. Induced Offset Drift vs. Nulled Offset Using Manufacturer's Recommended Adjustment Potentiometer

NULLING THE AD504

Since calculations show that superior drift performance can be realized with the AD504, special care should be taken to null it in the most advantageous manner. Using the actual values of resistors in the AD504, it is possible to calculate, under worst case conditions, that the total adjustment rage of the AD504 is approximately 8mV. Since the amplifier may often be trimmed to within 1µV, this represents an adjustment of 1 part in 8000. This type of accuracy would require a pot with 0.0125% resolution and stability. Because of the problems of obtaining a pot of this stability, a slightly more sophisticated nulling operation is recommended for applications where offset drift is critical (see Figure 2a).

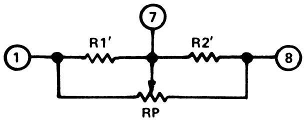


Figure 2a. High Resolution, High Stability Nulling Circuit

NULLING PROCEDURE

1. Null the offset to zero using a commercially available pot (suggest $R_P = 10k\Omega$).
2. Measure pot halves R1 and R2.
3. Calculate:

$$R_1' = \frac{R_1 \times 50k\Omega}{50k\Omega - R_1},\ R_2' = \frac{R_2 \times 50k\Omega}{50k\Omega - R_2}$$

4. Insert R1′ and R2′ (closest 1% fixed metal film resistors).
5. Use an industrial quality 100kΩ pot (R_P) to fine tune the trim.

For applications in which stringent nulling is not required, the user may choose a simplified nulling scheme as shown in Figure 2b. For best results the wiper of the potentiometer should be connected directly to pin 7 of the op amp. This is true for both nulling schemes.

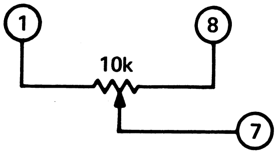


Figure 2b. Simplified Nulling Circuit

INPUT BIAS CURRENT

The input bias current vs. temperature characteristic is displayed in Figure 3.

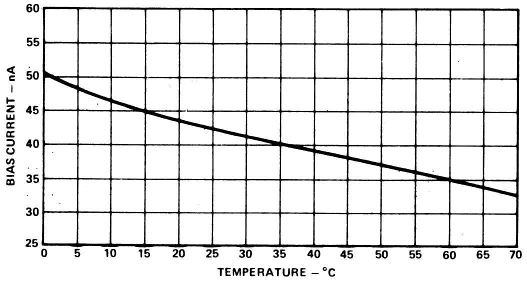


Figure 3. Input Bias Current vs. Temperature

GAIN PERFORMANCE

Most commercially available monolithic op amps have gain characteristics that vary considerably with:

1. Offset Nulling.
2. Load Resistance.
3. Supply Voltage.

Careful design allows the AD504 to maintain gain well in excess of 10^6, independent of nulling, load or supply voltage.

Nulling – The gain of a 741 op amp varies considerably with nulling (see Figure 4).

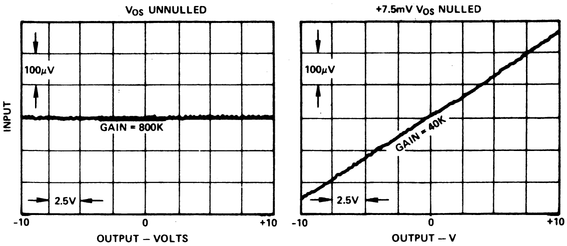


Figure 4. Gain Error Voltage Before and After Nulling a Typical 741 Op Amp

The gain of the AD504 is independent of nulling.

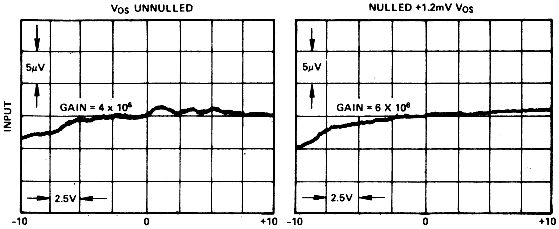


Figure 5. Gain Error Voltage Before and After Nulling the AD504

Load Resistance – The gain of the AD504 is flat with load resistance to 1kΩ loads and below.

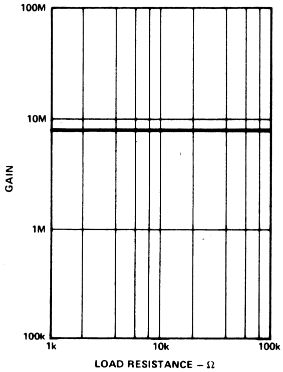


Figure 6. Gain vs. Load Resistance

Supply Voltage – The gain of the AD504 stays well above 1M down to $V_S = \pm5V$.

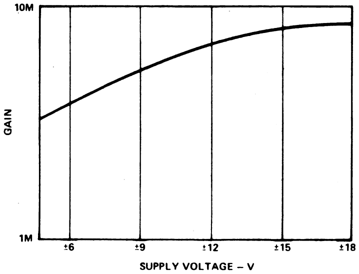


Figure 7. Gain vs. Supply Voltage

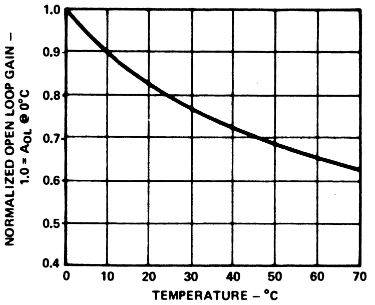


Figure 8. Normalized Open Loop Gain vs. Temperature

NOISE CHARACTERISTICS

An op amp with the precision of the AD504 must have correspondingly low noise levels if the user is to take advantage of its exceptional dc characteristics. Of primary importance in this type of amplifier is the absence of popcorn noise and minimum I/f or "flicker" noise in the 0.01Hz to 10Hz frequency band. Sample noise testing is done on every lot to guarantee that better than 90% of all devices will meet the noise specifications.

Separate voltage and current noise levels referred to the input are specified to enable the designer to calculate or optimize signal-to-noise ratio based on any desired source resistance. The spot noise figures are useful in determining total wideband noise over any desired bandwidth (see Figure 9).

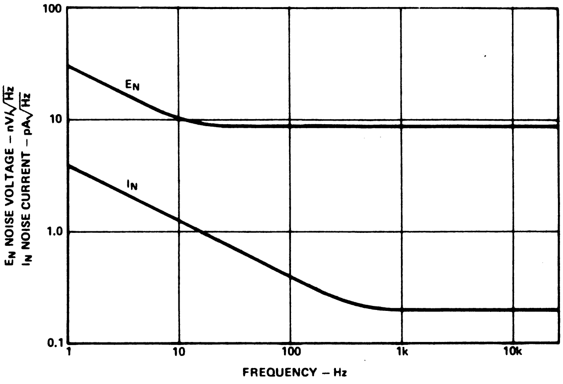


Figure 9. Spot Noise vs. Frequency

The key to success in using the AD504 in precision low noise applications is "attention to detail".

Here are a few reminders to help the user achieve optimum noise performance from the AD504.

1. Use metal film resistors in the source and feedback networks.
2. Use fixed resistors instead of potentiometers for nulling or gain setting.
3. Take advantage of the excellent common-mode noise rejection qualities of the AD504 by connecting the input differentially.
4. Limit the bandwidth of the system to the minimum possible consistent with the desired response time.
5. Use input guarding to reduce capacitive and leakage noise pickup.
6. Avoid ground loops and proximity to strong magnetic or electrostatic fields, etc.

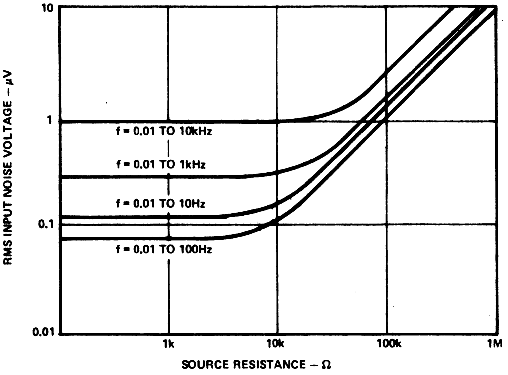


Figure 10. RMS Noise vs. Source Resistance

DYNAMIC PERFORMANCE

The dynamic performance of the AD504, although comparable to most general purpose op amps, is superior to most low drift op amps. Figure 11 shows the small signal frequency response for both open and closed loop gains for a variety of compensating values. Note that the circuit is completely stable for C_C = 390pF with a -3dB bandwidth of 300kHz; with C_C = 0, the -3dB bandwidth is 50kHz at a gain of 2000.

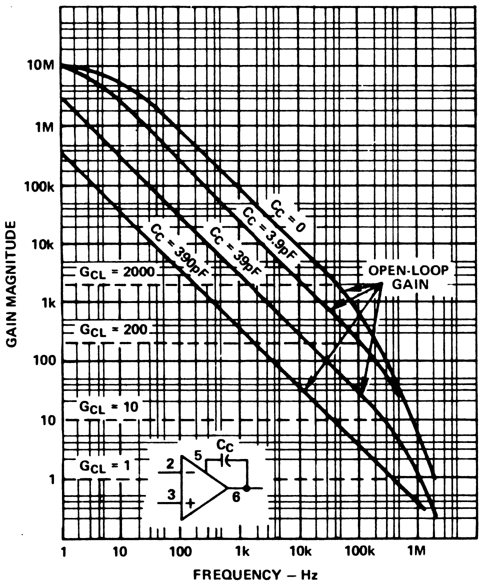


Figure 11. Small Signal Gain vs. Frequency

More important, at unity gain (390pF), full power bandwidth is (Figure 12) 2kHz which corresponds to a 0.12V/µs slew rate. At a gain of 10 (39pF), it increases to 20kHz, corresponding to 1.2V/µs, a considerable improvement over "725 type" amplifiers.

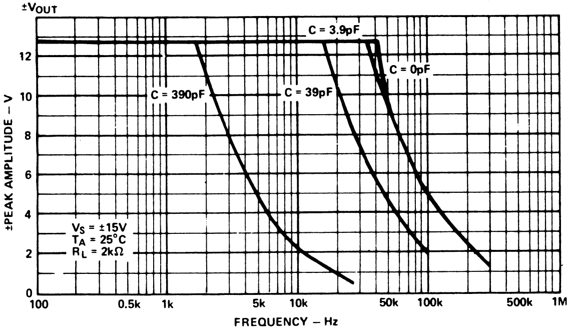


Figure 12. Output Voltage Swing vs. Frequency

Figure 13 shows the voltage follower step response for $V_S = \pm 15V$, $R_L = 2k\Omega$, $C_L = 200pF$ and $C_C = 390pF$.

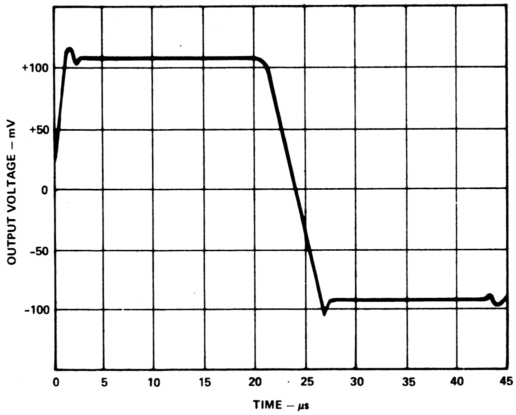


Figure 13. Voltage Follower Step Response

The common mode rejection of the AD504 is typically 120dB, and is shown as a function of frequency in Figure 14.

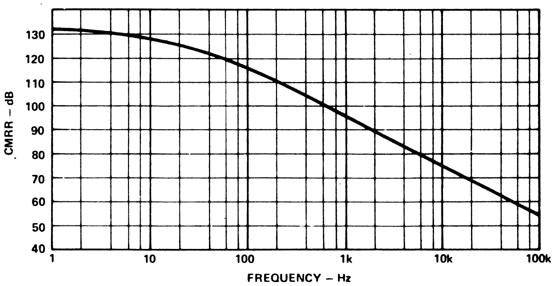


Figure 14. CMRR vs. Frequency

The power supply rejection ratio of the AD504 is shown in Figure 15.

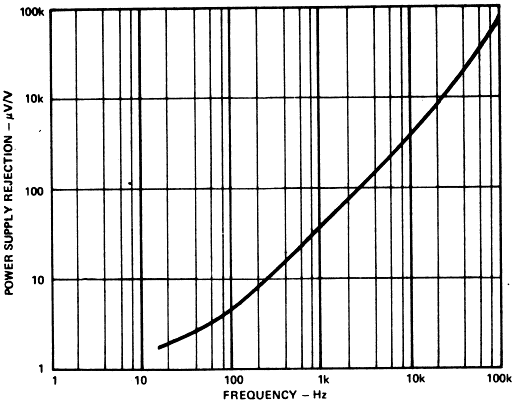


Figure 15. PSRR vs. Frequency

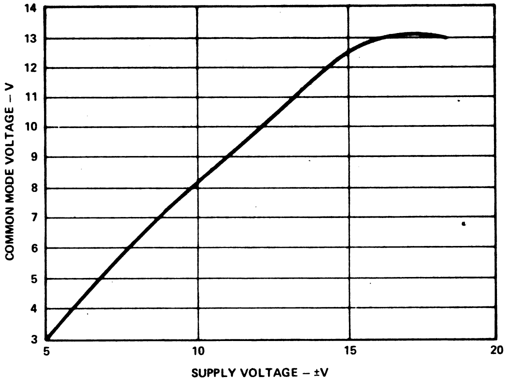


Figure 16. CMV Range vs. Supply Voltage

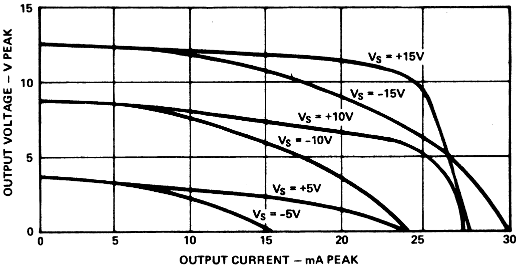


Figure 17. Output Characteristics

THERMAL PERFORMANCE

Temperature Gradients

Most modular and hybrid operational amplifiers are extremely sensitive to thermal gradients. The transient offset voltage response to thermal shock for a high performance modular op amp is shown in Figure 18.

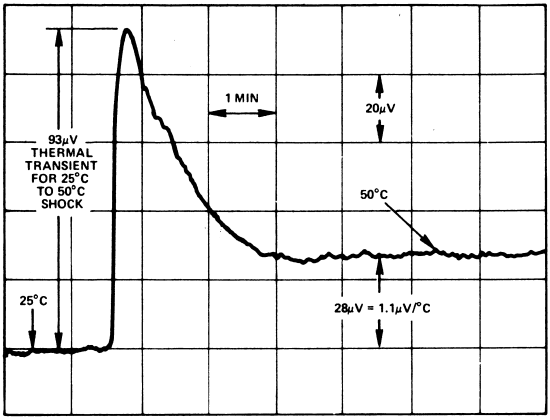


Figure 18. Response to Thermal Shock for High Performance Modular Op Amp

The graph shows the transient offset voltage resulting from a thermal shock when the amplifier's temperature is abruptly changed from 25°C to 50°C by dipping it into a hot silicon oil bath. Note the large overshoot (approximately 60µV) and long settling time (2.5 minutes). Also note the hysteresis of about 30µV.

Monolithic technology affords the AD504 significant improvements in this area. Thermal transients in the AD504 are small and over with quickly (see Figure 19).

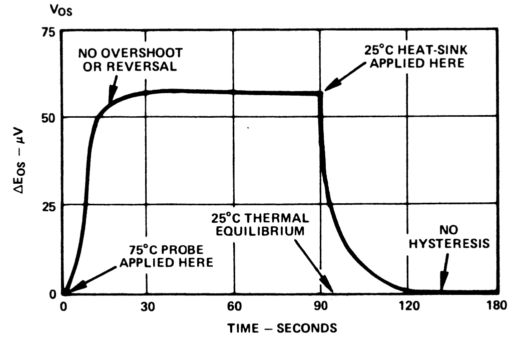


Figure 19. Response to Thermal Shock for AD504

In Figure 19, a 50°C step change in ambient temperature, applied to the can via a room temperature heat sink, then a 75°C thermal probe and back to the heat sink, results in settling to the final value within 30 seconds, for both increases and decreases in temperature. Note that the offset goes directly to its final value, with no spikes or hysteresis.

Warmup Drift

Modular and hybrid op amps have historically been plagued by excessive thermal time constants. Figure 20 shows the typical warmup drift of a high performance modular op amp.

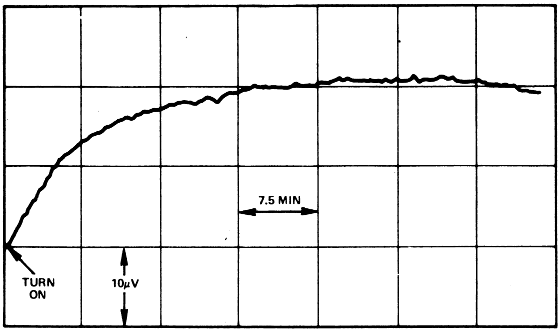


Figure 20. Warmup Voltage Drift for High Performance Modular Op Amp

Note that although warmup drift is low (20µV), it requires a long time to settle (>20 minutes).

Monolithic technology results in significant reduction of thermal time constants (see Figure 21).

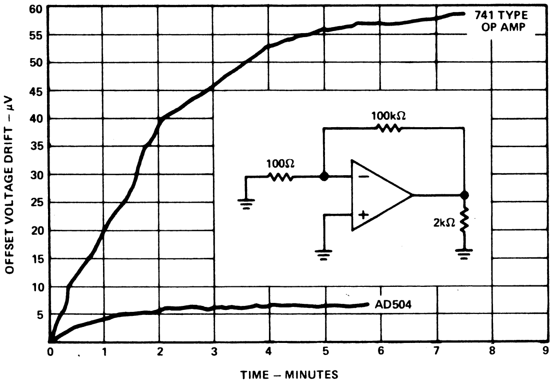


Figure 21. Warmup Voltage Drift for AD504 and 741 Type Op Amp

Note that warmup drift remains low (10µV), but that the thermal time constant decreases significantly to about 2 minutes. If a heat sink were used, total settling time would be completed within 30 seconds. Note that the 741 type op amp has a significantly longer warmup drift and thermal time constant.

ANALOG DEVICES

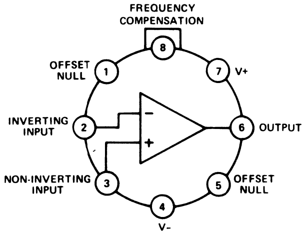
IC, Wideband, Fast Slewing, General Purpose Operational Amplifier

AD507

FEATURES

Gain Bandwidth: 100MHz
Slew Rate: 20V/µs min
I_B: 15nA max (AD507K)
V_{OS}: 3mV max (AD507K)
V_{OS} Drift: 15µV/°C max (AD507K)
High Capacitive Drive

AD507 FUNCTIONAL BLOCK DIAGRAM



**TO-99
TOP VIEW**

PRODUCT DESCRIPTION

The Analog Devices AD507J, K and S are low cost monolithic operational amplifiers that are designed for general purpose applications where high gain bandwidth and high speed are significant requirements. The devices also provide excellent dc performance with low input offset voltage, low offset voltage drift and low bias current. The AD507 is a low cost, high performance alternative to a wide variety of modular and IC op amps; a brief review of the specifications confirms its outstanding price/performance characteristics.

The AD507 is recommended for use where low cost and all around performance, especially at high frequencies, are needed. It is particularly well suited as a fast, high impedance comparator, integrator or wideband amplifier and in sample/hold circuits. It is unconditionally stable for all closed loop gains above 10 without external compensation; the frequency compensation terminal is used for stability at lower closed loop gains. The circuit is short circuit protected and offset voltage nullable. The AD507J and K are specified over the 0 to +70°C temperature range, the AD507S over the full military temperature range, −55°C to +125°C. All devices are packaged in the hermetic TO-99 metal can.

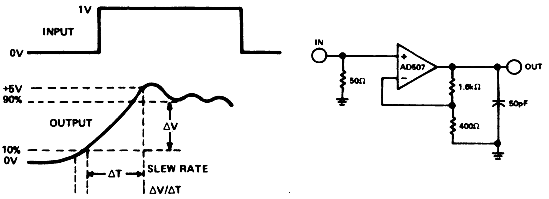
PRODUCT HIGHLIGHTS

1. Excellent dc and ac performance combined with low cost.
2. The AD507 will drive several hundred pF of output capacitance without oscillation.
3. All guaranteed dc parameters, including offset voltage drift, are 100% tested.
4. To insure compliance with gain bandwidth and slew rate specifications, all devices are tested for ac performance characteristics.

SPECIFICATIONS (typical at +25°C and ±15V dc, unless otherwise noted)

PARAMETER	AD507J	AD507K	AD507S(AD507S/883)**
OPEN LOOP GAIN			
$R_L = 2k\Omega, C_L = 50pF$	80,000 min (150,000 typ)	100,000 min (150,000 typ)	100,000 min (150,000 typ)
@ T min to T max	70,000 min	85,000 min	70,000 min
OUTPUT CHARACTERISTICS			
Voltage @ $R_L = 2k\Omega$, $C_L = 50pF$, T_{min} to T_{max}	±10V min (±12V typ)	*	±10V min (±12V typ)
Current @ $V_o = \pm 10V$	±10mA min (±20mA typ)	*	±15mA min (±22mA typ)
Short Circuit Current	25mA	*	25mA
FREQUENCY RESPONSE			
Unity Gain, Small Signal			
@ A = 1 (open loop)	35MHz	*	*
@ A = 100 (closed loop)	1MHz	*	*
Full Power Response	320kHz min (600kHz typ)	400kHz min (600kHz typ)	400kHz min (600kHz typ)
Slew Rate	±20V/μs min (±35V/μs typ)	±25V/μs min (±35V/μs typ)	20V/μs min (±35V/μs typ)
Settling Time (to 0.1%)	900ns	*	*
INPUT OFFSET VOLTAGE			
Initial	5.0mV max (3.0mV typ)	3.0mV max (1.5mV typ)	4mV max (0.5mV typ)
Avg vs Temp, T_{min} to T_{max}	15μV/°C	15μV/°C max (8μV/°C typ)	20μV/°C max (8μV/°C typ)
vs Supply, T_{min} to T_{max}	200μV/V max	100μV/V max	100μV/V max
INPUT BIAS CURRENT			
Initial	25nA max	15nA max	15nA max
T_{min} to T_{max}	40nA max	25nA max	35nA max
INPUT OFFSET CURRENT			
Initial	25nA max	15nA max	15nA max
T_{min} to T_{max}	40nA max	25nA max	35nA max
Avg vs Temp, T_{min} to T_{max}	0.5nA/°C	0.2nA/°C	0.2nA/°C
INPUT IMPEDANCE			
Differential	40MΩ min (300MΩ typ)	*	65MΩ min (500MΩ typ)
Common Mode	1000MΩ	*	*
INPUT VOLTAGE NOISE			
f = 10Hz	100nV/$\sqrt{Hz}$	*	*
f = 100Hz	30nV/$\sqrt{Hz}$	*	*
f = 100kHz	12nV/$\sqrt{Hz}$	*	*
INPUT VOLTAGE RANGE			
Differential, Max Safe	±12.0V	*	*
Common Mode Voltage Range, T_{min} to T_{max}	±11.0V	*	*
Common Mode Rejection @ ±5V, T_{min} to T_{max}	74dB min (100dB typ)	80dB min (100dB typ)	80dB min (100dB typ)
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	±(5 to 20)V	*	*
Current, Quiescent	4.0mA max (3.0mA typ)	*	*
TEMPERATURE RANGE			
Rated Performance	0 to +70°C	*	-55°C to +125°C
Operating	-25°C to +85°C	*	-65°C to +150°C
Storage	-65°C to +150°C	*	*
PACKAGE OPTION:[1] TO-99 Style (H08A)	AD507JH	AD507KH	AD507SH

*Specifications same as AD507J.
**AD507S/883 minimum order 10 pieces.
[1] See Section 20 for package outline information.
Specifications subject to change without notice.



Slew Rate Definition and Test Circuit

APPLICATION CONSIDERATIONS

The AD507 combines excellent dc characteristics and dynamic performance with ease of application. Because it is a wideband, high speed amplifier, care should be exercised in its stabilization. Several practical stabilization techniques are suggested to insure proper operation and minimize user experimentation.

GENERAL PURPOSE WIDEBAND COMPENSATION

The following considerations are intended to provide guidance in critical wideband applications. While not necessary in all cases, the considerations are of prime importance for the user attempting to obtain the highest performance from his circuit design.

High Gain Conditions

The AD507 is fully compensated *internally* for all closed loop gains above 10; however, it is necessary to load the amplifier with 50pF. In many applications this minimum capacitive load will be provided by the load or by a cable at the output of the AD507, making an additional 50pF unnecessary. Figure 1 shows the suggested configuration for general purpose use for closed loop gains above 10.

The 0.1μF ceramic power supply bypass capacitors are considerably more important for the AD507 than for low frequency general purpose amplifiers. Their main purpose is to convert the distributed high frequency ground to a lumped single point (the V+ point). The V+ to V− 0.1μF capacitor equalizes the supply grounds while the 0.1μF capacitor from V+ to signal ground should be returned to signal common. The signal common, which is bypassed to pin 7, is defined as that point at which the input signal source, the feedback network, and the return side of the load are joined to the power common.

Note that the diagrams show each individual capacitor directly connected to the appropriate terminal (pin 7 [V+] and pin 6 [Output]). In addition, it is suggested that all connections be made short and direct, and as physically close to the can as possible, so that the length of any conducting path shared by external components will be minimized.

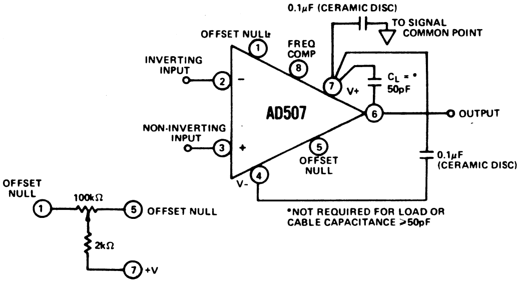


Figure 1. General Purpose Configuration to Closed Loop Gain > 10

Low Gain Conditions

For low closed loop gain applications, the AD507 should be compensated with a 20pF capacitor from pin 8 (frequency compensation) to signal common or pin 7 (V+). This configuration also requires a 30pF feedback capacitor from pin 6 (Output) to pin 8 (see Figure 2). The 50pF minimum load capacitance recommended for uncompensated applications is not required when the AD507 is used in the compensated mode. This compensation results in a unity gain frequency of approximately 10 to 12MHz.

The excellent input characterisitcs of the AD507 make it useful in low frequency applications where both dc and ac performance superior to the 741 type of op amp is desired. Some experimentation may be necessary to optimize the AD507 for the specific requirement. The unity gain bandwidth can be reduced by increasing the value of the compensation capacitor in inverse proportion to the desired bandwidth reduction. It is advisable to increase the feedback capacitor at the same time, maintaining its value about 50% larger than the compensation capacitor. Because the AD507 is fundamentally a wideband amplifier, careful power supply decoupling and compensation component layout are required even in low bandwidth applications.

OFFSET VOLTAGE NULLING

Note that the offset voltage null circuit includes a 2kΩ resistor in series with the wiper arm of the 100kΩ potentiometer. This resistor is not absolutely required, but its use can prevent a condition of false null that can be obtained at the ends of the pot range. The knowledgeable user should have no trouble differentiating between nulling in the pot mid-range and erratic end-range behavior when the wiper is connected directly to V+.

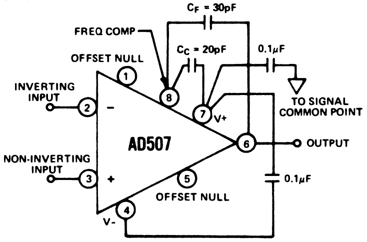


Figure 2. Configuration for Unity Gain Applications

HIGH CAPACITIVE LOADING

Like all wideband amplifiers, the AD507 is sensitive to capacitive loading. Unlike many, however, the AD507 can be used to effectively drive reasonable capacitive loads in virtually all applications, and capacitive loads of several hundred picofarads in a number of specific configurations.

In an inverting gain of ten configuration, the internally compensated amplifier will drive more than 200pF in addition to the recommended 50pF load, or a total of over 250pF. Under such conditions, the slew rate will be only slightly reduced, and the overall settling time somewhat lengthened.

In general, the capacitive drive capability of the AD507 will increase in high gain configurations which reduce closed loop bandwidth.

In any wideband application, it is essential to return the load currents supplied by the amplifier to the power supply without sharing a path with input or feedback signals. This consideration becomes particularly important when driving capacitive loads which may resonate with short lengths of interconnecting wire.

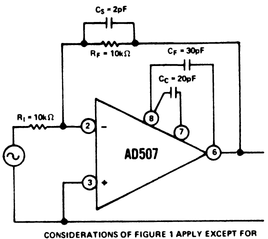
FAST SETTLING TIME

A small capacitor (C_S in Figure 3) will improve the settling time of the AD507, when it is used with large feedback resistors. The AD507 input capacitance (typically 2 or 3pF), together with additional circuit capacitance, will introduce an unwanted pole of open-loop response. The extra phase shift introduced, for example, by 4pF of input capacitance, and

5kΩ input source impedance, will result in an underdamped transient response, and long settling time. A small (1.5 to 3.0pF) feedback capacitor will introduce a zero in the open-loop transfer function, reducing the phase shift and increasing the damping, which will more than compensate for the slight reduction in closed-loop bandwidth.

BIAS COMPENSATION NOT REQUIRED

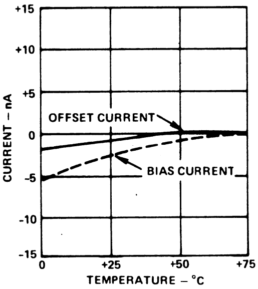
Circuit applications using conventional op amps generally require that the source resistances be matched at the inputs to cancel the effects of the input currents and take advantage of low offset current. In circuits similar to that shown in Figure 3, the compensation resistance would be equal to the parallel combination of R_I and R_F, and for large values would require a bypass capacitor. The AD507 is specially designed to cancel the input currents so as to reduce them to the offset current level. As a result, optimum performance can be obtained even though no bias compensation is used, and the non-inverting input can be connected directly to the signal common.



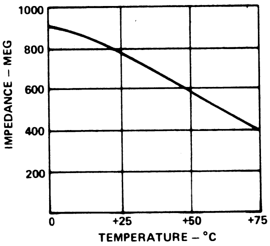
CONSIDERATIONS OF FIGURE 1 APPLY EXCEPT FOR THE LOAD CAPACITOR

Figure 3. Fast Settling Time Configuration

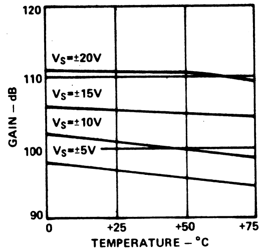
TYPICAL PERFORMANCE CURVES



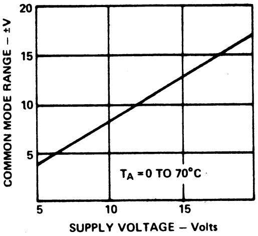
Input Bias Current and Offset Current vs Temperature



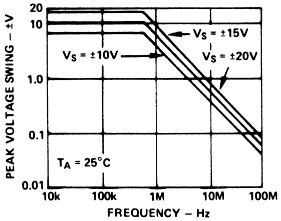
Input Impedance vs Temperature



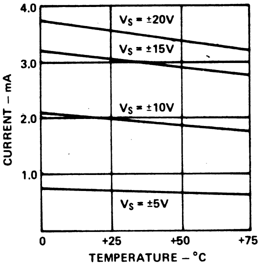
Open Loop Voltage Gain vs Temperature



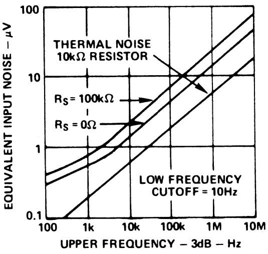
Common Mode Voltage Range vs Supply Voltage



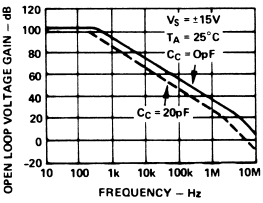
Output Voltage Swing vs Frequency



Power Supply Current vs Temperature



Broadband Input Noise Characteristics



Open Loop Gain vs Frequency

ANALOG DEVICES

High Speed, Fast Settling IC Op Amp

AD509

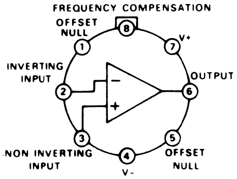
FEATURES

Fast Settling Time (100% Tested)
  0.1% in 500ns max
  0.01% in 2.5μs max
High Slew Rate: 100V/μs min
Low I_{OS}: 25nA max
Guaranteed V_{OS} Drift: 30μV/°C max
High CMRR: 80dB min
Drives 500pF
Low Price

APPLICATIONS

D/A and A/D Conversion
Wideband Amplifiers
Multiplexers
Pulse Amplifiers

AD509 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW

PRODUCT DESCRIPTION

The AD509J, AD509K and AD509S are monolithic operational amplifiers specifically designed for applications requiring fast settling times to high accuracy. The AD509K and AD509S are 100% tested to settle to 0.1% in 500ns max and 0.01% in 2.5μs max, with typical performance that is twice as fast. Other comparable dynamic parameters include a small signal bandwidth of 20MHz, slew rate of 100V/μs min and a full power response of 150kHz min. The devices are internally compensated for all closed loop gains greater than 3, and are compensated with a single capacitor for lower gains.

The input characteristics of the AD509 are consistent with 0.01% accuracy over limited temperature ranges; offset current is 25nA max, offset voltage is 8mV max, nullable to zero, and offset voltage drift is limited to 30μV/°C max. PSRR and CMRR are typically 90dB.

The AD509 is designed for use with high speed D/A or A/D converters where the minimum conversion time is limited by the amplifier settling time. If 0.01% accuracy of conversion is required, a conversion cannot be made in a shorter period than the time required for the amplifier to settle to within 0.01% of its final value.

All devices are supplied in the TO-99 package. The AD509J and AD509K are specified for 0 to +70°C temperature range; the AD509S for operation from −55°C to +125°C.

PRODUCT HIGHLIGHTS

1. The AD509K and AD509S are 100% tested for minimum slew rate and guaranteed to settle to 0.01% of its final value in less than 2.5μs.
2. The AD509 is internally compensated for all closed loop gains above 3, and compensated with a single capacitor for lower gains; thus eliminating the elaborate stabilizing techniques required by other high speed IC op amps.
3. The AD509 will drive capacitive loads of 500pF without any deterioration in settling time. Larger capacitive loads can be driven by tailoring the compensation to minimize settling time.
4. Common Mode Rejection, Gain and Noise are compatible with a 0.01% accuracy device.

SPECIFICATIONS (typical @ +25°C and ±15V dc, unless otherwise specified)

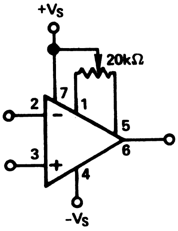
MODEL	AD509J	AD509K	AD509S
OPEN LOOP GAIN			
$R_L = 2k\Omega$	7,500 min (15,000 typ)	10,000 min (15,000 typ)	**
@ T_A = min to max	5,000 min	7,500 min	**
OUTPUT CHARACTERISTICS			
Voltage @ $R_L = 2k\Omega$, T_A = min to max	±10V min (±12V typ)	*	*
FREQUENCY RESPONSE			
Unity Gain, Small Signal	20MHz	*	*
Full Power Response, $V_O = \pm 10V$	1200kHz min (1.6MHz typ)	1500kHz min (2.0MHz typ)	**
Slew Rate, $R_L = 2k\Omega$, $V_O = \pm 10V$, $C_L = 50pF$	80V/μs min (120V/μs typ)	*	100V/μs min (120V/μs typ)
Settling Time			
to 0.1%	200ns	500ns max (200ns typ)	**
to 0.01%	1.0μs	2.5μs max (1.0μs typ)	**
INPUT OFFSET VOLTAGE			
Initial	10mV max (5mV typ)	8mV max (4mV typ)	**
T_A = min to max	14mV max	11mV max	**
Avg vs. Temperature, T_A = min to max	20μV/°C	30μV/°C max (20μV/°C typ)	**
vs. Supply, T_A = min to max	200μV/V max	100μV/V max	**
INPUT BIAS CURRENT			
Initial	250nA max (125nA typ)	200nA max (100nA typ)	**
T_A = min to max	500nA max	400nA max	**
INPUT OFFSET CURRENT			
Initial	50nA max (20nA typ)	25nA max (10nA typ)	**
T_A = min to max	100nA max	50nA max	**
INPUT IMPEDANCE			
Differential	40MΩ min (100MΩ typ)	50MΩ min (100MΩ typ)	**
INPUT VOLTAGE RANGE			
Differential, max safe	±15V	*	*
Common Mode Voltage Range			
T_A = min to max	±10V	*	*
Common Mode Rejection, $V_{cm} = \pm 5V$			
T_A = min to max	74dB min (90dB typ)	80dB min (90dB typ)	**
INPUT VOLTAGE NOISE			
f = 10Hz	$100nV/\sqrt{Hz}$	*	*
f = 100Hz	$30nV/\sqrt{Hz}$	*	*
f = 100kHz	$19nV/\sqrt{Hz}$	*	*
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	±(5 to 20)V	*	*
Current, Quiescent	6mA max (4mA typ)	*	*
TEMPERATURE RANGE			
Rated Performance	0 to +70°C	*	-55°C to +125°C
Storage	-65°C to +150°C	*	*
PACKAGE OPTION:[1] TO-99 Style (H08A)	AD509JH	AD509KH	AD509SH

*Specification same as AD509J.

**Specification same as AD509K.

[1] See Section 20 for package outline information.

Specifications subject to change without notice.



Simplified Nulling Circuit

APPLYING THE AD509

MEASURING SETTLING TIME. Settling time is defined as that period required for an amplifier output to swing from 0 volts to full scale, usually 10 volts, and to settle to within a specified percentage of the final output voltage. For high accuracy systems, the accuracy requirement is normally specified as either 0.1% (10-bit accuracy) or 0.01% (12-bit accuracy) of the 10 volt output level. The settling time period is comprised of an initial propagation delay, an additional time for the amplifier to slew to the vicinity of 10 volts, and a final time period to recover from internal saturation and other effects, and settle within the specified error band. Because settling time depends on both linear and nonlinear factors, there is no simple approach to predicting its final value to different levels of accuracy. In particular, extremely high slew rates do not assure a rapid settling time, since this is only one of many factors affecting settling time. In most high speed amplifiers, after the amplifier has slewed to the vicinity of the final output voltage, it must recover from internal saturation and then allow any overshoot and ringing to damp out. These definitions are illustrated in Figure 1.

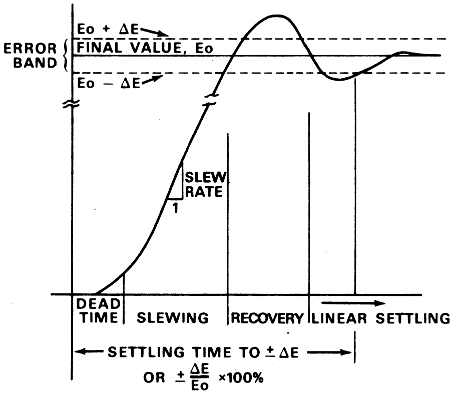


Figure 1. Settling Time

The AD509K and AD509S are 100% tested and guaranteed to settle to 0.1% in 500ns and 0.01% in 2.5μs (see Test Circuit, Figure 2). Note that the devices are tested compensated, at a gain of one, with a 50pF capacitive load. There is no appreciable degradation in settling time when the capacitive load is increased to 500pF, as discussed below. The settling time is computed by summing the output and the input into a differential amplifier, which then drives a scope display. The resultant waveform of ($E_o - E_{in}$) of a typical AD509 is shown in Figure 3. Note that the waveform crosses the 1mV point representing 0.01% accuracy in approximately 1.5μs. The top trace represents the output signal; the bottom trace represents the error signal.

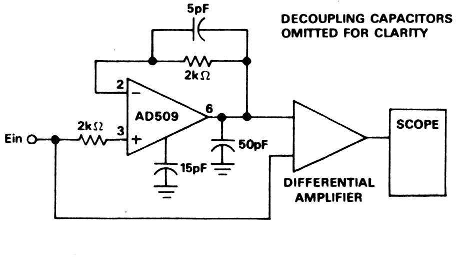


Figure 2. AD509 Settling Time Test Circuit

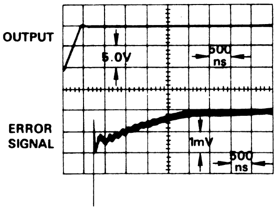


Figure 3. Settling Time of AD509

SETTLING TIME VS. R_f AND R_i. Settling time of an amplifier is a function of the feedback and input resistors, since they interact with the input capacitance of the amplifier. When operating in the non-inverting mode, the source impedance should be kept relatively low; e.g., 5kΩ; in order to insure optimum performance. The small feedback capacitor (5pF) is used in the settling time test circuit in parallel with the feedback resistor to reduce ringing. This capacitor partially cancels the pole formed in the loop gain response as a result of the feedback and input resistors, and the input capacitance.

SETTLING TIME VS. CAPACITIVE LOAD. The AD509 will drive capacitive loads of 500pF without appreciable deterioration in settling time. Larger capacitive loads can be driven by tailoring the compensation to minimize settling time. Figure 4 shows the settling time of a typical AD509, compensated for unity gain with a 15pF capacitor, with a 500pF capacitive load on the output. Note that settling time to 0.01% is still under 2.0μs.

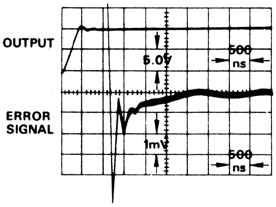


Figure 4. AD509 with 500pF Capacitive Load

SUGGESTIONS FOR MINIMIZING SETTLING TIME. The AD509 has been designed to settle to 0.01% accuracy in 1 to 2.5μs. However, this amplifier is only a building block in a circuit that also has a feedback network, input and output connections, power supply connections, and a number of external components. What has been painstakingly gained in amplifier design can be lost without careful circuit design. Some of the elements of a good high speed design are..........

CONNECTIONS. It is essential that care be taken in the signal and power ground circuits to avoid inducing or generating extraneous voltages in the ground signal paths.

The 0.1μF ceramic power supply bypass capacitors are considerably more important for the AD509 than for low frequency general purpose amplifiers. Their main purpose is to convert the distributed high frequency ground to a lumped single point (the V+ point). The V+ to V− 0.1μF capacitor equalizes the supply grounds while the 0.1μF capacitor from V+ to signal ground should be returned to signal common. The signal common, which is bypassed to pin 7, is defined as that point at which the input signal source, the feedback network, and the return side of the load are joined to the power common.

Note that the diagram shows each individual capacitor directly connected to the appropriate terminal (pin 7 [V+]).

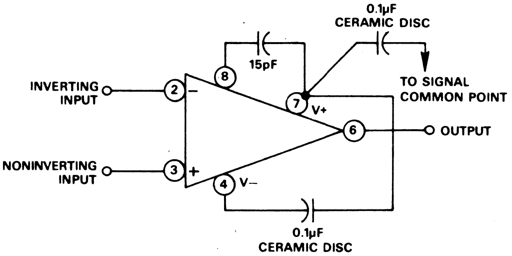


Figure 5. Configuration for Unity Gain Applications

In addition, it is suggested that all connections be short and direct, and as physically close to the case as possible, so that the length of any conducting path shared by external components will be minimized.

COMPONENTS. Resistors are preferably metal film types, because they have less capacitance and stray inductance than wirewound types, and are available with excellent accuracies and temperature coefficients.

Diodes are hot carrier types for the very fastest-settling applications, but 1N914 types are suitable for more routine uses.

Capacitors in critical locations are polystyrene, teflon, or polycarbonate to minimize dielectric absorption.

CIRCUIT. For the fastest settling times, keep leads short, orient components to minimize stray capacitance, keep circuit impedance levels as low as consistent with the output capabilities of the amplifier and the signal source, reduce all external load capacitances to the absolute minimum. Don't overlook sockets or printed circuit board mounting as possible sources of dielectric absorption. Avoid pole-zero mismatches in any feedback networks used with the amplifier. Minimize noise pickup.

DYNAMIC RESPONSE OF AD509

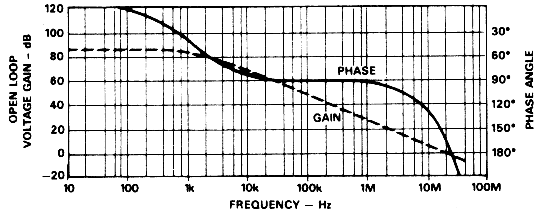


Figure 6. Open Loop Frequency and Phase Response

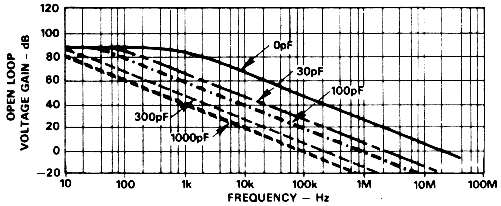


Figure 7. Open Loop Frequency Response for Various C_C's

THE AD509 AS AN OUTPUT AMPLIFIER FOR FAST CURRENT-OUTPUT D-TO-A CONVERTERS

Most fast integrated circuit digital to analog converters have current outputs. That is, the digital input code is translated to an output current proportional to the digital code. In many applications, that output current is converted to a voltage by connecting an operational amplifier in the current-to-voltage conversion mode.

The settling time of the combination depends on the settling time of the DAC and the output amplifier. A good approximation is:

$$t_S \text{ TOTAL} = \sqrt{(t_S \text{ DAC})^2 + (t_S \text{ AMP})^2}$$

Some IC DACs settle to final output value in 100-500 nanoseconds. Since most IC op amps require a longer time to settle to ±0.1% or ±0.01% of final value, amplifier settling time can dominate total settling time. And for a 12-bit DAC, one least significant bit is only 0.024% of full-scale, so low drift and high linearity and precision are also required of the output amplifier.

Figure 8 shows the AD509K connected as an output amplifier with the AD565K, high speed 12-bit IC digital-to-analog converter. The 10 picofarad capacitor, C1, compensates for the 25pF AD565 output capacitance. The voltage output of the AD565K/AD509K combination settles to ±0.01% in one microsecond. The low input voltage drift and high open loop gain of the AD509K assures 12-bit accuracy over the operating temperature range.

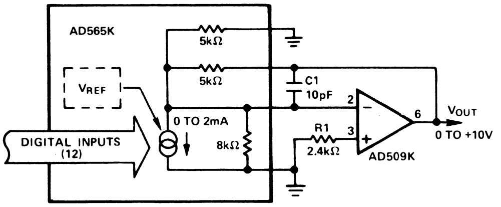


Figure 8. AD507 as an Output Amplifier for a Fast Current-Output D-to-A Converter

ANALOG DEVICES

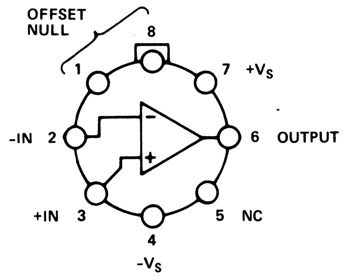
Low Cost, Laser Trimmed, Precision IC Op Amp

AD510

FEATURES

- **Low Cost**
- **Low V_{OS}: 25μV max (AD510L), 100μV max (AD510J)**
- **Low V_{OS} Drift: 0.5μV/°C max (AD510L)**
- **Internally Compensated**
- **High Open Loop Gain: 10^6 min**
- **Low Noise: 1μV p-p 0.01 to 10Hz**

AD510 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW

PRODUCT DESCRIPTION

The AD510 is the first low cost high accuracy IC op amp available. Analog Devices' precise thermally-balanced layout combined with high-yield IC processing provides truly superlative op amp performance at the lowest possible cost. The device is internally compensated, thus eliminating the need for an additional external capacitor.

A truly precision device, the AD510 achieves laser trimmed offset voltages less than 25μV max and offset voltage drifts of 0.5μV/°C max (nulled). Bias currents and offset currents are available at less than 10nA and 2.5nA respectively, while open loop gain is maintained at over 1,000,000, even under loaded conditions. Designed along a thermal axis, the AD510 is unaffected by thermal gradients across the monolithic chip caused by current loading.

The AD510 has fully protected inputs, permitting differential input voltages of up to $\pm V_S$ without voltage gain or bias current degradation due to reverse breakdown. The output is also protected from short circuits and drives 1000pF of load capacitance without oscillation.

The AD510 is specifically designed for applications requiring high precision at the lowest possible cost, such as bridge instruments, stable references, followers and analog computation. Packaged in a hermetically-sealed TO-99 metal can, the AD510 is available in three versions of performance (J, K and L) over the commercial temperature range, 0 to +70°C and one version (S) over the full military temperature range, -55°C to +125°C.

PRODUCT HIGHLIGHTS

1. Offset voltage drift is guaranteed and 100% tested on all models with a controlled temperature drift bath with the offset voltage nulled. Offset voltage on the AD510L is tested following a 3 minute warm-up.
2. The AD510 offers fully protected input (to $\pm V_S$) and output circuitry. The input protection circuit prevents offset voltage and bias current degradation due to reverse breakdown, a critical factor in high accuracy op amps where overall performance is strongly dependent on front-end stability.
3. Internal compensation eliminates the need for elaborate and costly stabilizing networks, often required by many high accuracy IC op amps.
4. A thermally balanced layout maintains high gain (1,000,000 min, K, L and S) independent of offset nulling, power supply voltage and output loading.
5. Bootstrapping of critical input transistors produces CMRR and PSRR of 110dB min and 100dB min, respectively.

SPECIFICATIONS (typical @ +25°C and ±15V dc unless otherwise noted)

MODEL	AD510JH	AD510KH	AD510LH	AD510SH (AD510SH/883B)
OPEN LOOP GAIN				
V_{OS} = ±10V, $R_L > 2k\Omega$	250,000 min	10^6 min	**	**
T_{min} to T_{max}	125,000 min	500,000 min	**	250,000
OUTPUT CHARACTERISTICS				
Voltage @ $R_L \geqslant 2k\Omega$, T_{min} to T_{max}	±10V min	*	*	*
Load Capacitance	1000pF	*	*	*
Output Current	10mA min	*	*	*
Short Circuit Current	25mA	*	*	*
FREQUENCY RESPONSE				
Unity Gain, Small Signal	300kHz	*	*	*
Full Power Response	1.5kHz	*	*	*
Slew Rate, Unity Gain	0.10V/μs	*	*	*
INPUT OFFSET VOLTAGE				
Initial Offset, $R_S \leqslant 10k\Omega$	100μV max	50μV max	25μV max	**
vs. Temp., T_{min} to T_{max}	3.0μV/°C max	1.0μV/°C max	0.5μV/°C max	**
vs. Supply	25μV/V max	10μV/V max	**	**
T_{min} to T_{max}	40μV/V max	15μV/V max	**	20μV/V max
INPUT OFFSET CURRENT				
Initial	5nA max	4nA max	2.5nA max	**
T_{min} to T_{max}	8nA max	6nA max	4nA max	10nA max
INPUT BIAS CURRENT				
Initial	25nA max	13nA max	10nA max	**
T_{min} to T_{max}	40nA max	20nA max	15nA max	30nA max
vs. Temp, T_{min} to T_{max}	±100pA/°C	±50pA/°C	±40pA/°C	**
INPUT IMPEDANCE				
Differential	4MΩ	6MΩ	**	**
Common Mode	$100M\Omega\parallel 4pF$	*	*	*
INPUT NOISE				
Voltage, 0.1Hz to 10Hz	1μV p-p	*	*	*
f = 10Hz	$18nV/\sqrt{Hz}$	*	*	*
f = 100Hz	$13nV/\sqrt{Hz}$	*	*	*
f = 1kHz	$10nV/\sqrt{Hz}$	*	*	*
Current, f = 10Hz	$0.5pA/\sqrt{Hz}$	*	*	*
f = 100Hz	$0.3pA/\sqrt{Hz}$	*	*	*
f = 1kHz	$0.3pA/\sqrt{Hz}$	*	*	*
INPUT VOLTAGE RANGE				
Differential or Common Mode max safe	$\pm V_S$	*	*	*
Common Mode Rejection, V_{in} = ±10V	94dB min	110dB min	**	**
Common Mode Rejection, T_{min} to T_{max}	94dB	100dB min	**	**
POWER SUPPLY				
Rated Performance	±15V	*	*	*
Operating	±(5 to 18)V	*	*	±(5 to 22)V
Current, Quiescent	4mA max	3mA max	**	**
TEMPERATURE RANGE				
Operating Rated Performance	0 to +70°C	*	*	−55°C to +125°C
Storage	−65°C to +150°C	*	*	*
PACKAGE OPTIONS:[1] TO-99 Style (H08B)	AD510JH	AD510KH	AD510LH	AD510SH

NOTES:

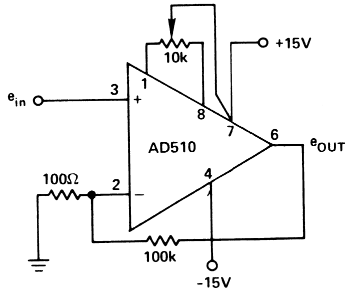
*Specifications same as AD510JH.

**Specifications same as AD510KH.

[1] See Section 20 for package outline information.

Specifications subject to change without notice.

TYPICAL
NON-INVERTING AMPLIFIER CONFIGURATION



NULLING THE AD510

Nulling the AD510 can be achieved using the high resolution circuit of Figure 1.

1. Null the offset to zero using a commercially available pot (approximately 10kΩ).
2. Measure pot halves, R_1 and R_2.
3. Calculate . . . $R_1' = \frac{R_1 \times 50k\Omega}{50k\Omega - R_1}$ $R_2' = \frac{R_2 \times 50k\Omega}{50k\Omega - R_2}$
4. Insert R_1' and R_2' (closest 1% fixed metal film resistors).
5. Use an industrial quality 100kΩ pot (r_p) to fine tune the trim.

Nulling to within 1 microvolt can be achieved using this technique. For best results, the wiper of the potentiometer should be connected directly to pin 7 of the op amp.

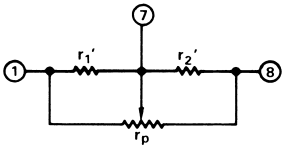


Figure 1. High Resolution, High Stability Nulling Circuit

THE AD510L IN A SIMPLE INSTRUMENTATION AMPLIFIER

The circuit of Figure 2 illustrates a simple instrumentation amplifier suitable for use with strain gauges, thermocouples and other transducers. It provides high input impedance to ground at each of the differential input terminals and excellent common mode rejection.

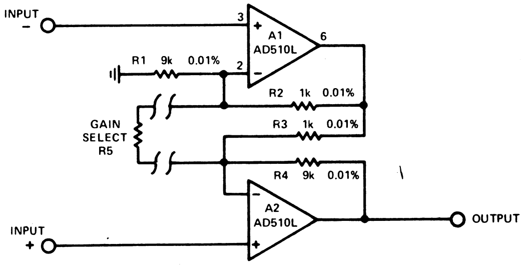


Figure 2. Instrumentation Amplifier

The configuration shown is designed for a gain of 10, however the gain can be varied upwards by adding a gain select resistor R_5. In operation, amplifier A_1 provides a gain of 10/9 for signals at the negative input terminal. This output feeds the inverting amplifier A_2, which has a gain of 9, resulting in an overall gain of 10. For signals at the positive input, the output of A_1 is at ground potential and the amplifier A_2 provides a gain of 10. Thus, the circuit has a gain of 10 for differential signals and 0 for common mode signals; the very high CMRR and open loop gain of the AD510L automatically produces common mode rejection of at least 25,000 at dc at a gain of 10 and over 1,000,000 at a gain of 1000. The common mode rejection, of course, depends upon the resistor ratios and their specified tolerance. Less accurate resistors can be used if the network is trimmed.

For gains of 10 the frequency response is down 3dB at 500kHz, for gains of 1000, 2kHz. Full output of ±10V can be attained up to 1800Hz.

The common mode rejection at 60Hz is limited by the finite gain bandwidth of A_1 causing a phase lag on the negative input signal. At 60Hz the CMRR measures 72dB at a gain of 1000 and 62dB at a gain of 10.

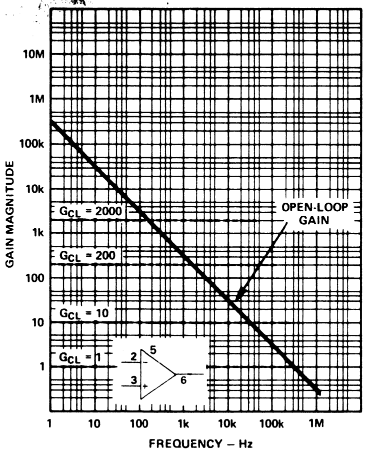


Figure 3. Small Signal Gain vs. Frequency

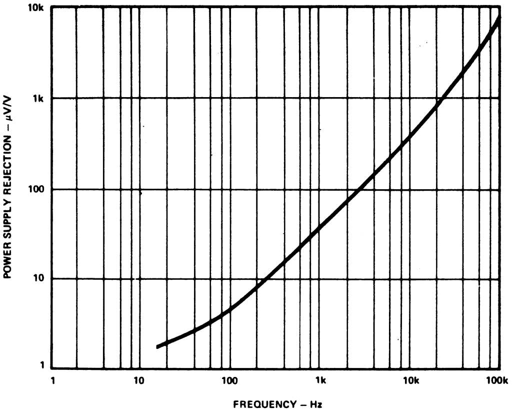


Figure 4. PSRR vs. Frequency

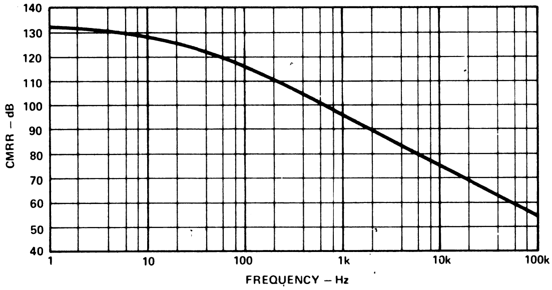


Figure 5. CMRR vs. Frequency

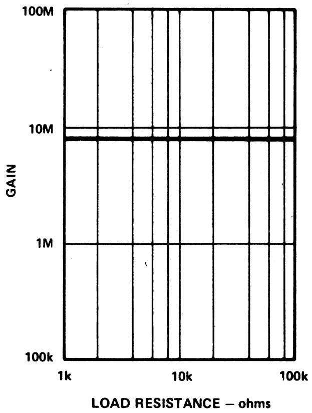


Figure 6. Gain vs. Load Resistance

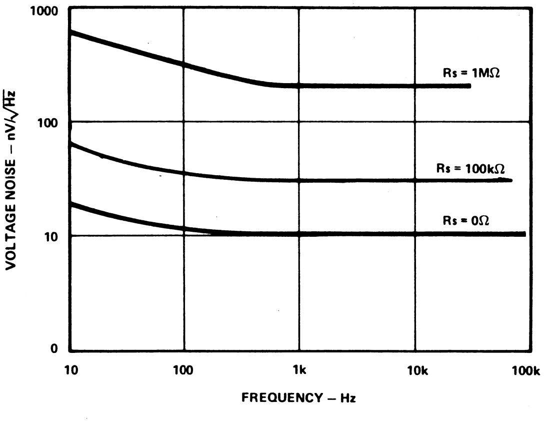


Figure 7. Voltage Noise vs. Frequency

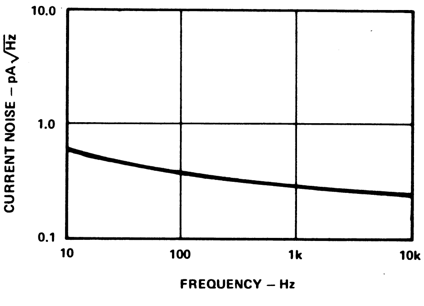


Figure 8. Current Noise vs. Frequency

ANALOG DEVICES

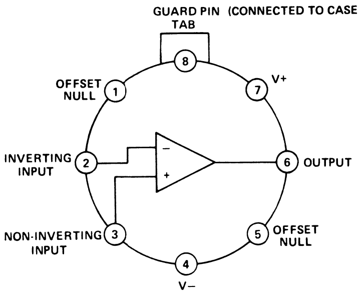
Precision, Low-Power FET-Input Electrometer Op Amp

AD515

FEATURES

Ultra Low Bias Current: 0.075pA max (AD515L)
0.150pA max (AD515K)
0.300pA max (AD515J)
Low Power: 1.5mA max Quiescent Current (0.8mA typ)
Low Offset Voltage: 1.0mV max (AD515 K & L)
Low Drift: 15μV/°C max (AD515K)
Low Noise: 4μV p-p, 0.1 to 10Hz
Low Cost

AD515 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW

PRODUCT DESCRIPTION

The AD515 series of FET-input operational amplifiers are second generation electrometer designs offering the lowest input bias currents available in any standard operational amplifier. The AD515 also delivers laser-trimmed offset voltage, low drift, low noise and low power, a combination of features not previously available in ultra-low bias current circuits. All devices are internally compensated, free of latch-up, and short circuit protected.

The AD515 delivers a new level of versatility and precision to a wide variety of electrometer and very high impedance buffer measurement situations, including photo-current detection, vacuum ion-gauge measurement, long term precision integration, and low drift sample/hold applications. The device is also an excellent choice for all forms of biomedical instrumentation such as pH/pIon sensitive electrodes, very low current oxygen sensors, and high impedance biological microprobes. In addition, the low cost and pin compatibility of the AD515 with standard FET op amps will allow designers to upgrade the performance of present systems at little or no additional cost. The 10^{15} ohm common mode input impedance, resulting from a solid bootstrap input stage, insures that the input bias current is essentially independent of common mode voltage.

As with previous electrometer amplifier designs from Analog Devices, the case is brought out to its own connection (pin 8) so that the case can be independently connected to a point at the same potential as the input, thus minimizing stray leakage to the case. This feature will also shield the input circuitry from external noise and supply transients, as well as reducing common mode input capacitance from 0.8pF to 0.2pF.

The AD515 is available in three versions of bias current and offset voltage, the "J", "K", and "L"; all are specified for rated performance from 0 to +70°C and supplied in a hermetically sealed TO-99 package.

PRODUCT HIGHLIGHTS

1. The AD515 provides the lowest bias currents available in an integrated circuit amplifier.
   - The ultra low input bias currents are specified as the maximum measured at either input with the device fully warmed up on ±15 volt supplies at +25°C ambient with no heat sink. This parameter is 100% tested.
   - By using ±5 volt supplies, input bias current can typically be brought below 50fA.
2. The input offset voltage on all grades is laser trimmed to a level typically less than 500μV.
   - The offset voltage drift is the lowest available in an FET electrometer amplifier.
   - If additional nulling is desired, the amount required will have a minimal effect on offset drift (approximately 3μV/°C per millivolt).
3. The low quiescent current drain of 0.8mA typical and 1.5mA maximum, which is among the lowest available in operational amplifier designs of any type, keeps self-heating effects to a minimum and renders the AD515 suitable for a wide range of remote probe situations.
4. The combination of low input noise voltage and very low input noise current is such that for source impedances from much over one Megohm up to 10^{11} ohm, the Johnson noise of the source will easily dominate the noise characteristic.

SPECIFICATIONS (typical @ +25°C with V_S = ±15V dc, unless otherwise specified)

MODEL	AD515J	AD515K	AD515L
OPEN LOOP GAIN[1]			
V_{OUT} = ±10V, $R_L \geq 2k\Omega$	20,000V/V min	40,000V/V min	25,000V/V min
$R_L \geq 10k\Omega$	40,000V/V min	100,000V/V min	50,000V/V min
T_A = min to max $R_L \geq 2k\Omega$	15,000V/V min	40,000V/V min	25,000V/V min
OUTPUT CHARACTERISTICS			
Voltage @ $R_L = 2k\Omega$, T_A = min to max	±10V min (±12V typ)	*	*
@ $R_L = 10k\Omega$, T_A = min to max	±12V min (±13V typ)	*	*
Load Capacitance[2]	1000pF	*	*
Short Circuit Current	10mA min (25mA typ)	*	*
FREQUENCY RESPONSE			
Unity Gain, Small Signal	350kHz	*	*
Full Power Response	5kHz min (16kHz typ)	*	*
Slew Rate Inverting Unity Gain	0.3V/μs min (1.0V/μs typ)	*	*
Overload Recovery Inverting Unity Gain	100μs max (16μs typ)	*	*
INPUT OFFSET VOLTAGE[3]	3.0mV max (0.4mV typ)	1.0mV max (0.4mV typ)	1.0mV max (0.4mV typ)
vs. Temperature, T_A = min to max	50μV/°C max	15μV/°C max	25μV/°C max
vs. Supply, T_A = min to max	400μV/V max (50μV/V typ)	100μV/V max	200μV/V max
INPUT BIAS CURRENT			
Either Input[4]	300fA max	150fA max	75fA max
INPUT IMPEDANCE			
Differential	$1.6pF \| 10^{13}\Omega$	*	*
Common Mode	$0.8pF \| 10^{15}\Omega$	*	*
INPUT NOISE			
Voltage, 0.1Hz to 10Hz	4.0μV (p-p)	*	*
f = 10Hz	$75nV/\sqrt{Hz}$	*	*
f = 100Hz	$55nV/\sqrt{Hz}$	*	*
f = 1kHz	$50nV/\sqrt{Hz}$	*	*
Current, 0.1 to 10Hz	0.003pA (p-p)	*	*
10Hz to 10kHz	0.01pA rms	*	*
INPUT VOLTAGE RANGE			
Differential	±20V min	*	*
Common Mode, T_A = min to max	±10V min (±12V typ)	*	*
Common Mode Rejection, V_{IN} = ±10V	66dB min (94dB typ)	80dB min	70dB min
Maximum Safe Input Voltage[5]	$\pm V_S$	*	*
POWER SUPPLY			
Rated Performance	±15V typ	*	*
Operating	±5V min (±18V max)	*	*
Quiescent Current	1.5mA max (0.8mA typ)	*	*
TEMPERATURE			
Operating, Rated Performance	0 to +70°C	*	*
Storage	−65°C to +150°C	*	*
PACKAGE OPTIONS[6]: TO-99 Style (H08B)	AD515JH	AD515KH	AD515LH

NOTES

[1] Open Loop Gain is specified with or without nulling of V_{OS}.

[2] A conservative design would not exceed 750pF of load capacitance.

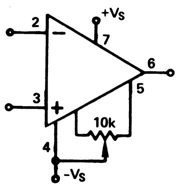
[3] Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[4] Bias Current specifications are guaranteed after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every +10°C.

[5] If it is possible for the input voltage to exceed the supply voltage, a series protection resistor should be added to limit input current to 0.5mA. The input device can handle overload currents of 0.5mA indefinitely without damage. See next page.

[6] See Section 20 for package outline information.

*Specifications same as AD515J.
Specifications subject to change without notice.



Standard Offset Null Circuit

LAYOUT AND CONNECTION CONSIDERATIONS

The design of very high impedance measurement systems introduces a new level of problems associated with the reduction of leakage paths and noise pickup.

1. A primary consideration in high impedance system designs is to attempt to place the measuring device as near to the signal source as possible. This will minimize current leakage paths, noise pickup and capacitive loading. The AD515, with its combination of low offset voltage (normally eliminating the need for trimming), low quiescent current (minimal source heating, possible battery operation), internal compensation and small physical size lends itself very nicely to installation at the signal source or inside a probe. Also, as a result of the high load capacitance rating, the AD515 can comfortably drive a long signal cable.
2. The use of guarding techniques is essential to realizing the capability of the ultra-low input currents of the AD515. Guarding is achieved by applying a low impedance bootstrap potential to the outside of the insulation material surrounding the high impedance signal line. This bootstrap potential is held at the same level as that of the high impedance line; therefore, there is no voltage drop across the insulation, and hence, no leakage. The guard will also act as a shield to reduce noise pickup and serves an additional function of reducing the effective capacitance to the input line. The case of the AD515 is brought out separately to pin 8 so that the case can also be connected to the guard potential. This technique virtually eliminates potential leakage paths across the package insulation, provides a noise shield for the sensitive circuitry, and reduces common-mode input capacitance to about 0.2pF. Figure 1 shows a proper printed circuit board layout for input guarding and connecting the case guard. Figures 2 and 3 show guarding connections for typical inverting and non-inverting applications. If pin 8 is not used for guarding, it should be connected to ground or a power supply to reduce noise.

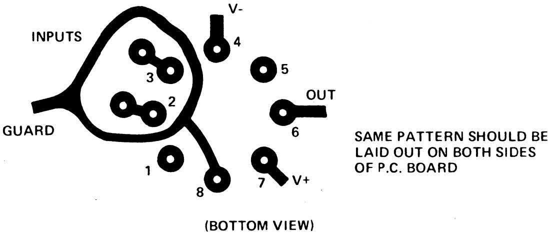


Figure 1. Board Layout for Guarding Inputs with Guarded TO-99 Package

3. Printed circuit board layout and construction is critical for achieving the ultimate in low leakage performance that the AD515 can deliver. The best performance will be realized by using a teflon IC socket for the AD515; but at least a teflon stand-off should be used for the high-impedance lead. If this is not feasible, the input guarding scheme shown in Figure 1 will minimize leakage as much as possible; the guard ring should be applied to both sides of the board. The guard ring is connected to a low impedance potential at the same level as the inputs. High impedance signal lines should not be extended for any unnecessary length on a printed circuit; to minimize noise and leakage, they must be carried in rigid, shielded cables.
4. Another important concern for achieving and maintaining low leakage currents is complete cleanliness of circuit boards and components. Completed assemblies should be washed thoroughly in a low residue solvent such as TMC Freon or high-purity methanol followed by a rinse with deionized water and nitrogen drying. If service is anticipated in a high contaminant or high humidity environment, a high dielectric conformal coating is recommended. All insulation materials except Kel-F or teflon will show rapid degradation of surface leakage at high humidities.

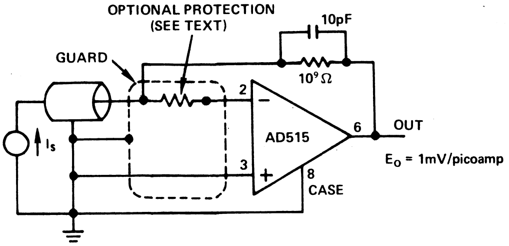


Figure 2. Picoampere Current-to-Voltage Converter Inverting Configuration

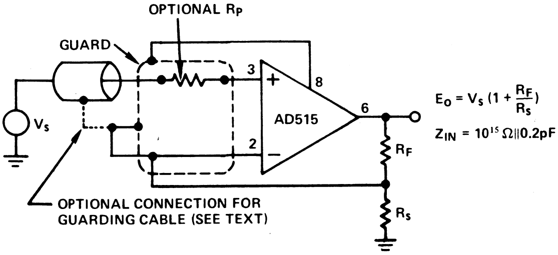

OPTIONAL R_P
GUARD
3
8
AD515
6
$E_O = V_S\left(1 + \frac{R_F}{R_S}\right)$
$Z_{IN} = 10^{15}\Omega \| 0.2pF$
V_S
2
R_F
R_S
OPTIONAL CONNECTION FOR GUARDING CABLE (SEE TEXT)

Figure 3. Very High Impedance Non-Inverting Amplifier

INPUT PROTECTION

The AD515 is guaranteed for a maximum safe input potential equal to the power supply potential. The unique bootstrapped input stage design also allows differential input voltages of up to ±20 volts (or within 10 volts of the sum of the supplies) while maintaining the full differential input resistance of $10^{13}\Omega$, as shown in Figure 10. This makes the AD515 suitable for low speed comparator situations employing a direct connection to a high impedance source.

Many instrumentation situations, such as flame detectors in gas chromatographs, involve measurement of low level currents from high-voltage sources. In such applications, a sensor fault condition may apply a very high potential to the input of the current-to-voltage converting amplifier. This possibility necessitates some form of input protection. Many electrometer type devices, especially CMOS designs, can require elaborate zener protection schemes which often compromise overall performance. The AD515 requires input protection only if the source is not current-limited, and as such is similar to many JFET-input designs. The failure mode would be overheating from excess current rather than voltage breakdown. If the source is not current-limited, all that is required is a resistor in series with the affected input terminal so that the maximum overload current is 0.5mA (for example, 200kΩ for a 100 volt overload). This simple scheme will cause no significant reduction in performance and give complete overload protection. Figures 2 and 3 show proper connections.

COAXIAL CABLE AND CAPACITANCE EFFECTS
If it is not possible to attach the AD515 virtually on top of the signal source, considerable care should be exercised in designing the connecting lines carrying the high impedance signal. Shielded coaxial cable must be used for noise reduction, but use of coaxial cables for high impedance work can add problems from cable leakage, noise, and capacitance. Only the best polyethylene or virgin teflon (not reconstituted) should be used to obtain the highest possible insulation resistance.

Cable systems should be made as rigid and vibration-free as possible since cable movement can cause noise signals of three types, all significant in high impedance systems. Frictional movement of the shield over the insulation material generates a charge which is sensed by the signal line as a noise voltage. Low noise cable with graphite lubricant will reduce the noise, but short rigid lines are better. Cable movements will also make small changes in the internal cable capacitance and capacitance to other objects. Since the total charge on these capacitances cannot be changed instantly, a noise voltage results as predicted from: $\Delta V = Q/\Delta C$. Noise voltage is also generated by the motion of a conductor in a magnetic field.

The conductor-to-shield capacitance of coaxial cable is normally about 30pF/foot. Charging this capacitance can cause considerable stretching of high impedance signal rise-time, thus cancelling the low input capacitance feature of the AD515. There are two ways to circumvent this problem. For inverting signals or low-level current measurements, the signal is carried on the line connected to the inverting input and shielded (guarded) by the ground line as shown in Figure 2. Since the signal is always at virtual ground, no voltage change is required and no capacitances are charged. In many circumstances, this will de-stabilize the circuit; if so, capacitance from output to inverting input will stabilize the circuit.

Non-inverting and buffer situations are more critical since the signal line voltage and therefore charge will change, causing signal delay. This effect can be reduced considerably by connecting the cable shield to guard potential instead of ground, an option shown in Figure 3. Since such a connection results in positive feedback to the input, the circuit may destabilize and oscillate. If so, capacitance from positive input to ground must be added to make the net capacitance at pin 3 positive. This technique can considerably reduce the effective capacitance which must be charged.

Typical Performance Curves

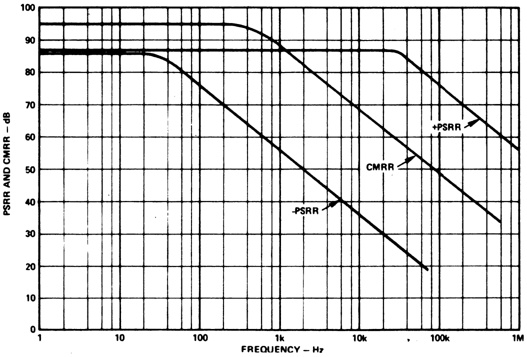


Figure 4. PSRR and CMRR Versus Frequency

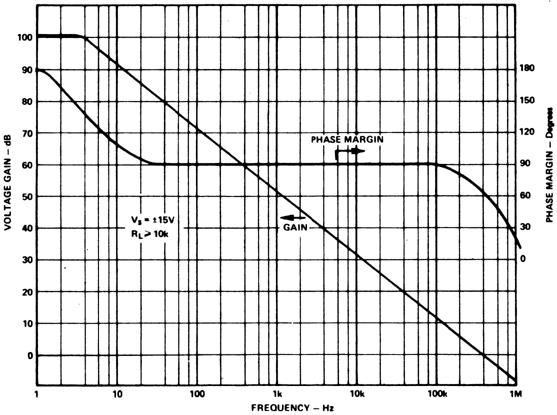


Figure 5. Open Loop Frequency Response

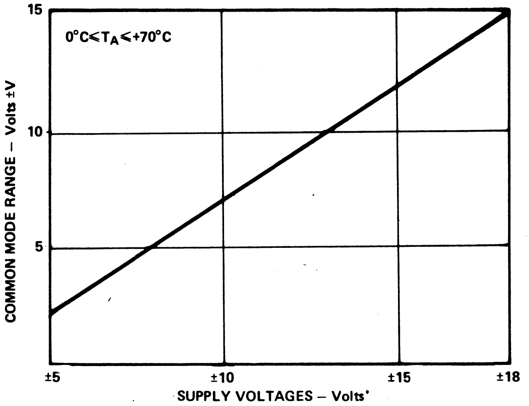


Figure 6. Input Common Mode Range Versus Supply Voltage

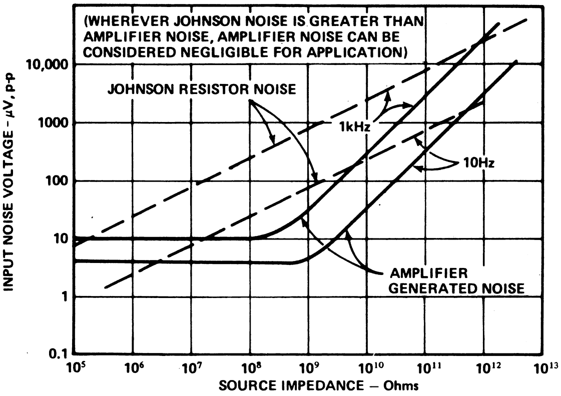


Figure 7. Peak-to-Peak Input Noise Voltage Versus Source Impedance and Bandwidth

ELECTROMETER APPLICATION NOTES

The AD515 offers the lowest input bias currents available in an integrated circuit package. This design will open up many new application opportunities for measurements from very high impedance and very low current sources. Performing accurate measurements of this sort requires careful attention to detail; the notes given here will aid the user in realizing the full measurement potential of the AD515 and perhaps extending its performance limits.

1. As with all junction FET input devices, the temperature of the FET's themselves is all-important in determining the input bias currents. Over the operating temperature range, the input bias currents closely follow a characteristic of doubling every 10°C; therefore, every effort should be made to minimize device operating temperature.
2. The heat dissipation can be reduced initially by careful investigation of the application. First, if it is possible to reduce the required power supplies, this should be done since internal power consumption contributes the largest component of self-heating. To minimize this effect, the quiescent current of the AD515 has been reduced to a level much lower than that of any other electrometer-grade device, but additional performance improvement can be gained by lowering the supply voltages, to ±5 volts if possible. The effects of this are shown in Figure 8, which shows typical input bias current and quiescent current versus supply voltage.
3. Output loading effects, which are normally ignored, can cause a significant increase in chip temperature and therefore bias current. For example, a 2kΩ load driven at 10 volts at the output will cause at least an additional 25 milliwatts dissipation in the output stage (and some in other stages) over the typical 24 milliwatts, thereby at least doubling the effects of self-heating. The results of this form of additional power dissipation are demonstrated in Figure 9, which shows normalized input bias current versus additional power dissipated. Therefore, although many dc performance parameters are specified driving a 2kΩ load, to reduce this additional dissipation, we recommend restricting the load impedance to be at least 10kΩ.

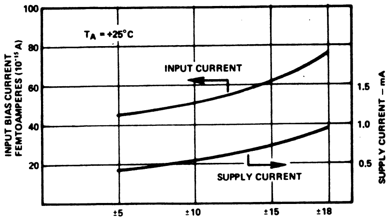


Figure 8. Input Bias Current and Supply Current Versus Supply Voltage

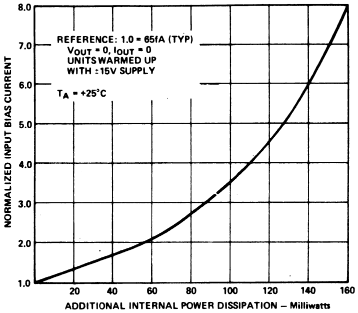


Figure 9. Input Bias Current Versus Additional Power Dissipation

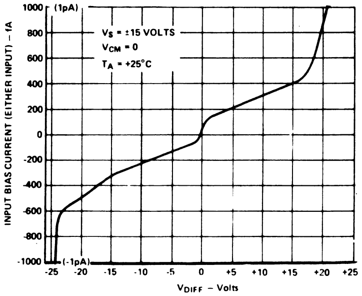


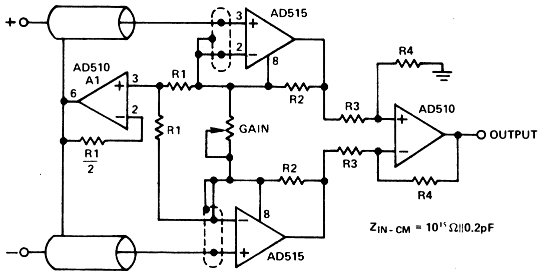
Figure 10. Input Bias Current Versus Differential Input Voltage

AD515 CIRCUIT APPLICATION NOTES

The AD515 is quite simple to apply to a wide variety of applications because of the pre-trimmed offset voltage and internal compensation, which minimize required external components and eliminate the need for adjustments to the device itself. The major considerations in applying this device are the external problems of layout and heat control which have already been discussed. In circuit situations employing the use of very high value resistors, such as low level current to voltage converters, electrometer operational amplifiers can be destabilized by a pole created by the small capacitance at the negative input. If this occurs, a capacitor of 2 to 5pF in parallel with the resistor will stabilize the loop. A much larger capacitor may be used if desired to limit bandwidth and thereby reduce wideband noise.

Selection of passive components employed in high impedance situations is critical. High-megohm resistors should be of the carbon film or deposited ceramic oxide to obtain the best in low noise and high stability performance. The best packaging for high-megohm resistors is a glass body sprayed with silicone varnish to minimize humidity effects. These resistors must be handled very carefully to prevent surface contamination. Capacitors for any high impedance or long term integration situation should be of a polystyrene formulation for optimum performance. Most other types have too low an insulation resistance, or high dielectric absorption.

Unlike situations involving standard operational amplifiers with much higher bias currents, balancing the impedances seen at the input terminals of the AD515 is usually unnecessary and probably undesirable. At the large source impedances where these effects matter, obtaining quality, matched resistors will be difficult. More important, instead of a cancelling effect, as with bias current, the noise voltage of the additional resistor will add by root-sum-of-squares to that of the other resistor thus increasing the total noise by about 40%. Noise currents driving the resistors also add, but in the AD515 are significant only above $10^{11}\Omega$.



(ALL RESISTORS OF SAME NUMBER SHOULD BE MATCHED ±0.1%)
(BUFFER A1 BOOSTS COMMON MODE Z_{IN} BY DRIVING CABLE SHIELDS AT COMMON MODE VOLTAGE AND NEUTRALIZING CM CAPACITANCE)

Figure 11. Very High Impedance Instrumentation Amplifier

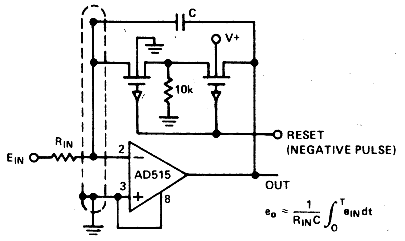


Figure 12. Low Drift Integrator and Low-Leakage Guarded Reset

LOW-LEVEL CURRENT TO VOLTAGE CONVERTERS

Figure 2 shows a standard low-level current-to-voltage converter. To obtain higher sensitivity, it is obvious to simply use a higher value feedback resistor. However, high value resistors above $10^9\Omega$ tend to be expensive, large, noisy and unstable. To avoid this, it may be desirable to use a circuit configuration with output gain, as in Figure 13. The drawback is that input errors of offset voltage drift and noise are multiplied by the same gain, but the precision performance of the AD515 makes the tradeoff easier.

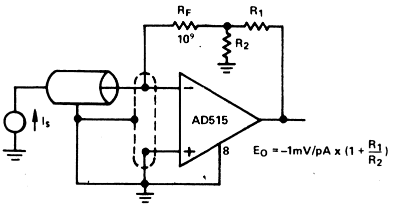


Figure 13. Picoampere to Voltage Converter with Gain

One of the problems with low-level leakage current testing or low-level current transducers (such as Clark oxygen sensors) is finding a way to apply voltage bias to the device while still grounding the device and the bias source. Figure 14 shows a technique in which the desired bias is applied at the non-inverting terminal thus forcing that voltage at the inverting terminal. The current is sensed by R_F, and the AD521 instrumentation amplifier converts the floating differential signal to a single-ended output.

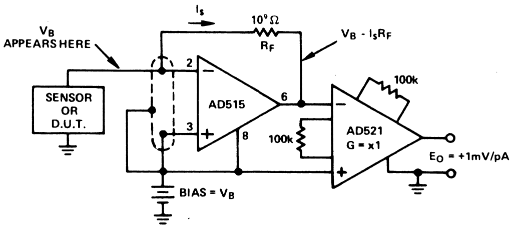


Figure 14. Current-to-Voltage Converters with Grounded Bias and Sensor

ANALOG
DEVICES

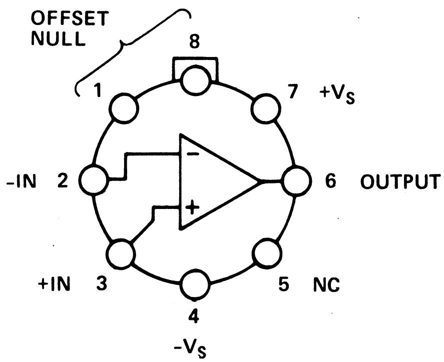
Low Cost, Laser Trimmed, Precision IC Op Amp

AD517

FEATURES

Low Input Bias Current: 1nA max (AD517L)
Low Input Offset Current: 0.25nA max (AD517L)
Low V_{OS}: 50μV max (AD517L), 150μV max (AD517J)
Low V_{OS} Drift: 1.3μV/°C (AD517L)
Internal Compensation
Low Cost

AD517 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW

PRODUCT DESCRIPTION

The AD517 is a high accuracy monolithic op amp featuring extremely low offset voltages and input currents. Analog Devices' thermally-balanced layout and superior IC processing combine to produce a truly precision device at low cost.

The AD517 is laser trimmed at the wafer level (LWT) to produce offset voltages less than 50μV and offset voltage drifts less than 1.3μV/°C unnulled. Superbeta input transistors provide extremely low input bias currents of 1nA max and offset currents as low as 0.25nA max. While these figures are comparable to presently available BIFET amplifiers at room temperature, the AD517 input currents decrease, rather than increase, at elevated temperatures. Open-loop gain in many IC amplifiers is degraded under loaded conditions due to thermal gradients on the chip. However, the AD517 layout is balanced along a thermal axis, maintaining open-loop gain in excess of 1,000,000 for a wide range of load resistances.

The input stage of the AD517 is fully protected, allowing differential input voltages of up to ±V_S without degradation of gain or bias current due to reverse breakdown. The output stage is short-circuit protected and is capable of driving a load capacitance up to 1000pF.

The AD517 is well suited to applications requiring high precision and excellent long-term stability at low cost, such as stable references, followers, bridge instruments and analog computation circuits.

The circuit is packaged in a hermetically sealed TO-99 metal can, and is available in three performance versions (J, K, and L) specified over the commercial 0 to +70°C range; and one version (AD517S) specified over the full military temperature range, −55°C to +125°C. The AD517S is also available with processing to the requirements of MIL-STD-883, Level B.

PRODUCT HIGHLIGHTS

1. Offset voltage is 100% tested and guaranteed on all models. Testing is performed following a 5 minute warm-up period.
2. The AD517 exhibits extremely low input bias currents without sacrificing CMRR (over 100dB) or offset voltage stability.
3. The AD517 inputs are protected (to ±V_S), preventing offset voltage and bias current degradation due to reverse breakdown of the input transistors.
4. Internal compensation is provided, eliminating the need for additional components (often required by high accuracy IC op amps).
5. The AD517 can directly replace 725, 108, and AD510 amplifiers. In addition, it can replace 741-type amplifiers if the offset-nulling potentiometer is removed.
6. Thermally-balanced layout insures high open-loop gain independent of thermal gradients induced by output loading, offset nulling, and power supply variations.

SPECIFICATIONS (typical @ +25°C and ±15V dc unless otherwise noted)

MODEL	AD517J	AD517K	AD517L	AD517S[1]
OPEN LOOP GAIN				
V_O = ±10V, $R_L \geqslant 2k\Omega$	10^6 min	*	*	*
T_{min} to T_{max}	500,000 min	*	*	250,000
OUTPUT CHARACTERISTICS				
Voltage @ $R_L \geqslant 2k\Omega$, T_{min} to T_{max}	±10V min	*	*	*
Load Capacitance	1000pF	*	*	*
Output Current	10mA min	*	*	*
Short Circuit Current	25mA	*	*	*
FREQUENCY RESPONSE				
Unity Gain, Small Signal	250kHz	*	*	*
Full Power Response	1.5kHz	*	*	*
Slew Rate, Unity Gain	0.10V/μs	*	*	*
INPUT OFFSET VOLTAGE				
Initial Offset, $R_S \leqslant 10k\Omega$	150μV max	75μV max	50μV max	**
vs. Temp., T_{min} to T_{max}	3.0μV/°C max	1.8μV/°C max	1.3μV/°C max	**
vs. Supply	25μV/V max	10μV/V max	**	**
(T_{min} to T_{max})	40μV/V max	15μV/V max	**	20μV/V max
INPUT OFFSET CURRENT				
Initial	1nA max	0.75nA max	0.25nA max	**
T_{min} to T_{max}	1.5nA max	1.25nA max	0.4nA max	2nA max
INPUT BIAS CURRENT				
Initial	5nA max	2nA max	1nA max	**
T_{min} to T_{max}	8nA max	3.5nA max	1.5nA max	10nA max
vs. Temp, T_{min} to T_{max}	±20pA/°C	±10pA/°C	±4pA/°C	**
INPUT IMPEDANCE				
Differential	15MΩ‖1.5pF	20MΩ‖1.5pF	**	**
Common Mode	$2.0 \times 10^{11}\ \Omega$	*	*	*
INPUT NOISE				
Voltage, 0.1Hz to 10Hz	2μV p-p	*	*	*
f = 10Hz	35nV/$\sqrt{\text{Hz}}$	*	*	*
f = 100Hz	25nV/$\sqrt{\text{Hz}}$	*	*	*
f = 1kHz	20nV/$\sqrt{\text{Hz}}$	*	*	*
Current, f = 10Hz	0.05pA/$\sqrt{\text{Hz}}$	*	*	*
f = 100Hz	0.03pA/$\sqrt{\text{Hz}}$	*	*	*
f = 1kHz	0.03pA/$\sqrt{\text{Hz}}$	*	*	*
INPUT VOLTAGE RANGE				
Differential or Common Mode max Safe	$\pm V_S$	*	*	*
Common Mode Rejection, V_{in} = ±10V	94dB min	110dB min	**	**
Common Mode Rejection, T_{min} to T_{max}	94dB min	100dB min	**	**
POWER SUPPLY				
Rated Performance	±15V	*	*	*
Operating	±(5 to 18)V	*	*	±(5 to 22)V
Current, Quiescent	4mA max	3mA max	**	**
TEMPERATURE RANGE				
Operating Rated Performance	0 to +70°C	*	*	-55°C to +125°C
Storage	-65°C to +150°C	*	*	*
PACKAGE OPTION:[2] TO-99 Style (H08B)	AD517JH	AD517KH	AD517LH	AD517SH

NOTES

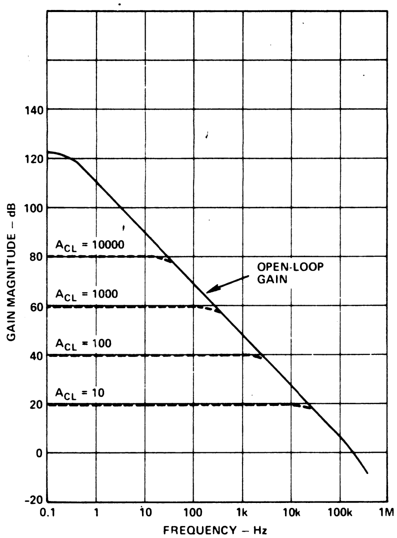
*Specifications same as AD517J

**Specifications same as AD517K

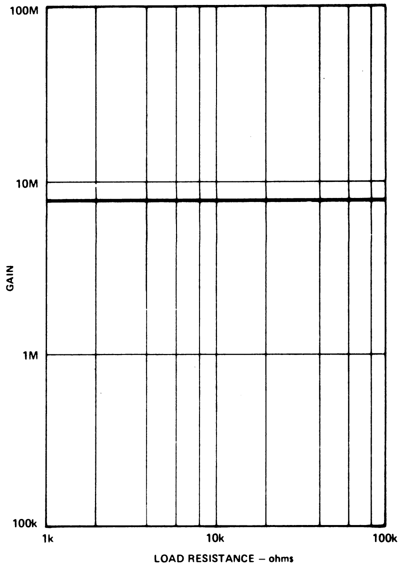
[1] The AD517S is available processed and screened to the requirements of MIL-STD-883, Level B.

[2] See Section 20 for package outline information.

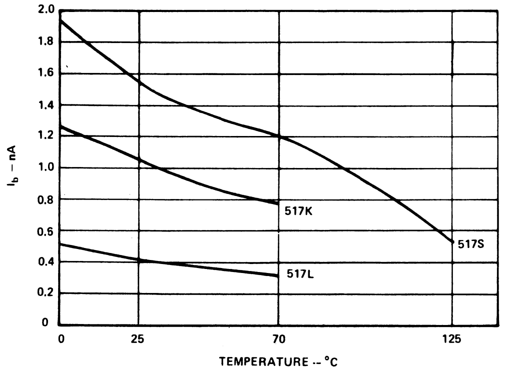
Specifications subject to change without notice.



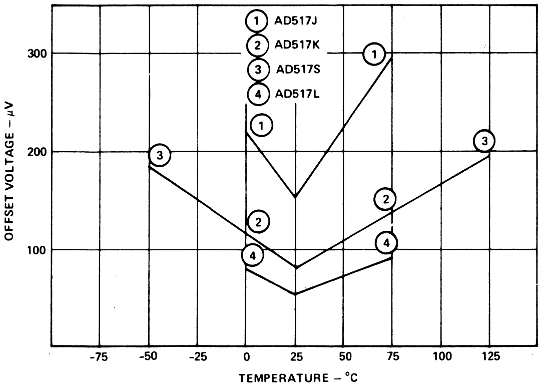
Small-Signal Gain vs. Frequency



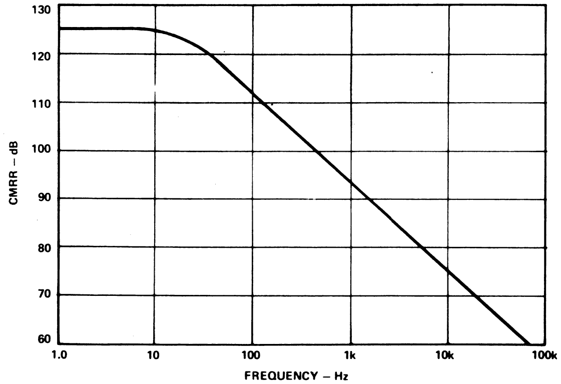
Open-Loop Gain vs. Load Resistance



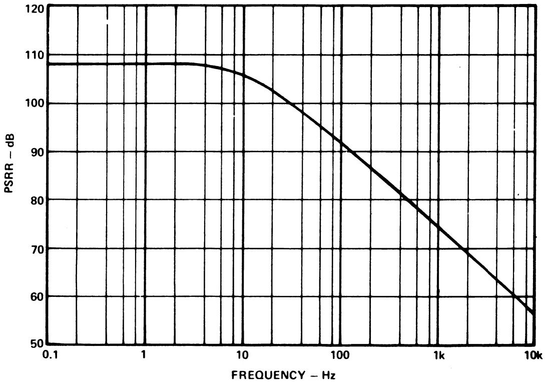
Input Bias Current vs. Temperature



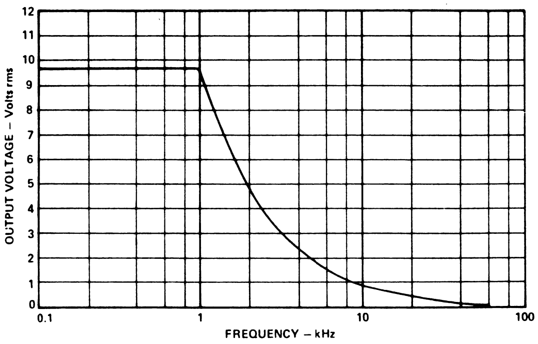
Untrimmed Offset Voltage vs. Temperature



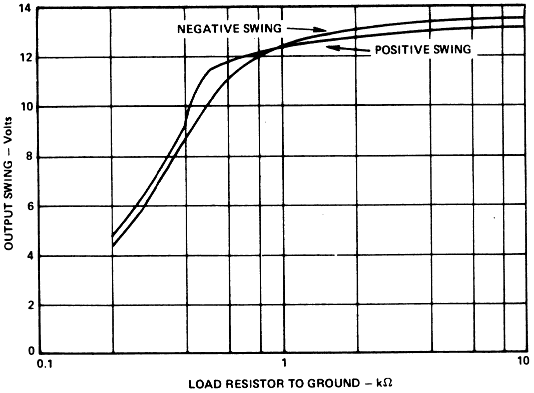
CMRR vs. Frequency



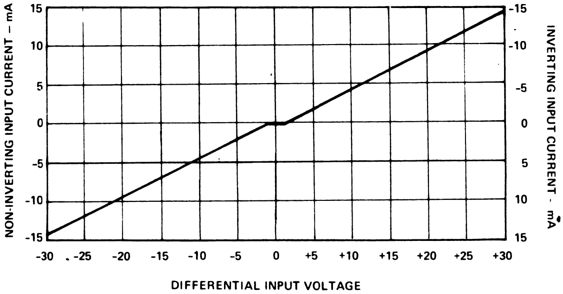
PSRR vs. Frequency



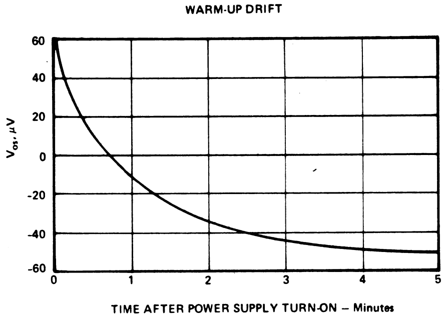
Maximum Undistorted Output vs. Frequency (Distortion ≤ 1%)



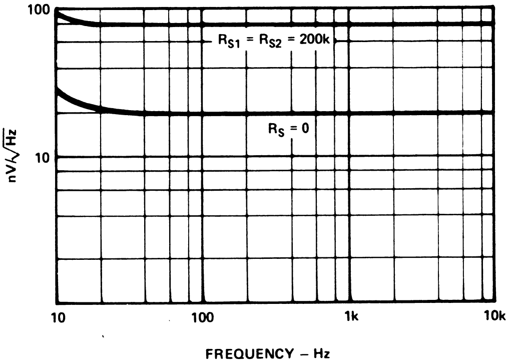
Output Voltage vs. Load Resistance



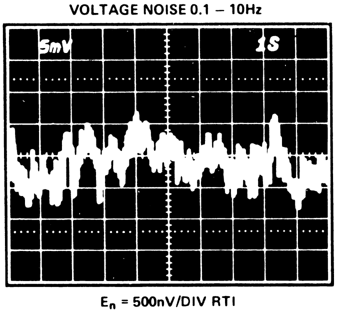
Input Current vs. Differential Input Voltage



Warm-Up Offset Voltage Drift



Total Input Noise Voltage vs. Frequency



Low Frequency Voltage Noise (0.1 to 10Hz)

NULLING THE AD517

The internally-trimmed offset voltage of the AD517 will be low enough for most circuits without further nulling. However, in high precision applications, the AD517 may be nulled using either of the following methods:

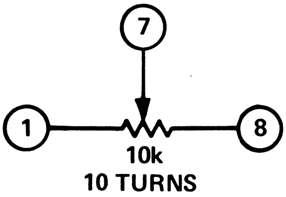
Figure 1A shows a simple circuit using a 10kΩ, ten-turn potentiometer. This circuit allows nulling to within several microvolts.

The circuit of Figure 1B is recommended in applications where nulling to within 1μV is desired. This circuit has the advantage that potentiometer instability effects are reduced by a factor of ten. Values of R_1' and R_2' are calculated as follows:

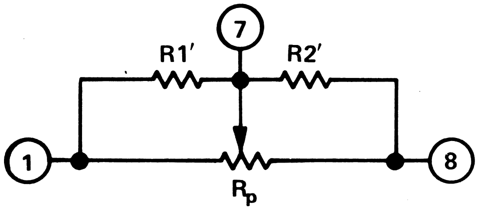
1. Null the offset to zero using a standard 10k pot, as shown in Figure 1A.
2. Measure pot halves R_1 and R_2.
3. Calculate:

$$R_1' = \frac{R_1 \times 50k\Omega,}{50k\Omega - R_1} \qquad R_2' = \frac{R_2 \times 50k\Omega}{50k\Omega - R_2}$$

4. Replace the pot with R_1' and R_2' using the closest value 1% metal film resistors.
5. Use a 100k, ten-turn pot for R_p to complete the nulling.



A. Simple



B. High Precision

Figure 1. Nulling Circuits

AN INSTRUMENT INPUT AMPLIFIER USING THE AD517L

The circuit shown in Figure 2 represents a typical input stage for laboratory instruments and panel meters. The amplifier is non-inverting and offers selectable gains from 1 to 1000 in decade steps.

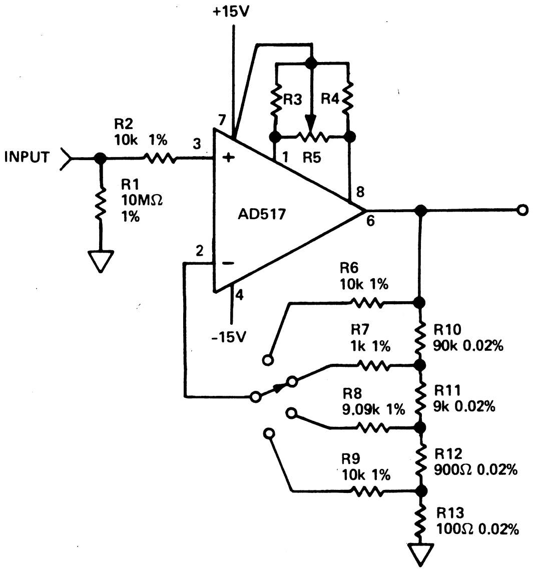


Figure 2. Stable Instrument Input Amplifier

Input impedance of this amplifier is 10 megohms, determined by resistor R_1. The offset nulling network comprised of R_3, R_4 and R_5 is the same one described earlier. If a less precise adjustment can be tolerated, a single 10k potentiometer can be substituted for R_3, R_4 and R_5.

Gain switching is accomplished in the feedback network. The divider consisting of R_{10}, R_{11}, R_{12} and R_{13} determines the gain by dividing the output and returning it to the inverting input of the amplifier. The ratio tolerances of these resistors uniquely determine the gain of the amplifier. The impedance seen by the inverting input is held constant at 10k ohms by R_6, R_7 R_8 or R_9 depending on the gain selected. Since input bias currents flow through equal resistances, the offset voltages produced will cancel each other. The input offset currents will produce an insignificant offset voltage on the order of 1 microvolt. If this offset is nulled out at the highest gain selected, it will be nulled on all ranges.

The AD517 offers excellent temperature stability in this circuit. Once the offset has been zeroed, the error produced by offset current drift will remain quite low due to the extremely low offset current drift of the AD517. A FET-input op amp would not work well in this application, since the input offset currents would double for each 10°C increase in temperature, soon exceeding the input offset currents of the AD517.

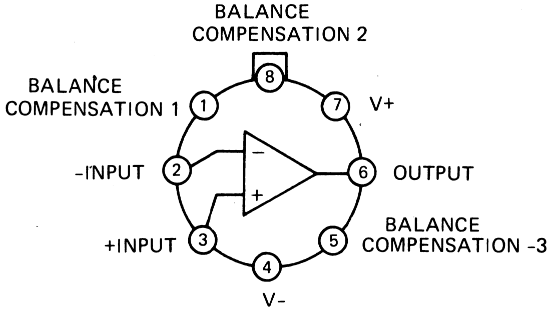
ANALOG DEVICES

Low Cost, High Speed, IC Operational Amplifier

AD518

FEATURES
- Low Cost
- High Slew Rate: 70V/μs
- Wide Bandwidth: 12MHz
- 60° Phase Margin (At Unity Gain Crossover)
- Drives 300pF Load
- Guaranteed Low Offset Drift:
  15μV/°C Max (AD518K)
- Pin Compatible With 118-Type
  Op Amp Series
- MIL-STD-883 Availability

AD518 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW

PRODUCT DESCRIPTION

The AD518J, AD518K, and AD518S are high speed precision monolithic operational amplifiers designed for applications where slew rate and wide bandwidth are required, but low cost and ease of use are essential. The devices are internally compensated for unity gain applications with a 60° phase margin to insure stability, a minimum unity gain slew rate of 50V/μs, and a typical bandwidth of 12MHz. In addition, in inverting applications external feedforward compensation may be added to increase the slew rate to over 100V/μs, and nearly double the bandwidth. If desired, settling time to 0.1% can be reduced to under 1μs with a single external capacitor.

The AD518's dc performance is consistent with its precision dynamic characteristics. The devices feature offset voltages below 2mV, maximum offset drifts of 15μV/°C, and offset currents below 50nA max.

The high slew rate, fast settling time, ease of use, and low cost of the AD518 make it ideal for use with D/A and A/D converters, as well as active filters, sample-and-hold circuits, and as a general purpose, fast, wideband amplifier. The AD518 is supplied in the TO-99 package. The AD518J and AD518K are specified for operation over the 0 to +70°C temperature range; the AD518S for operation from -55°C to +125°C.

PRODUCT HIGHLIGHTS

1. The AD518 offers the user high speed performance and flexibility previously unavailable at low cost . . . .
   - Internal compensation for unity gain applications
   - Capability to increase slew rate to over 100V/μs and double the bandwidth by an external feedforward technique
   - Capability to reduce settling time to under 1μs to 0.1% with a single external capacitor
   - Differential input capability
2. The phase margin of the AD518, uncompensated at the unity gain crossover frequency, is 60°, providing unconditional stability for all conditions. This conservative phase margin represents a clear improvement over that of the 118 series IC op amps currently available.
3. The static performance of the AD518 is consistent with its excellent dynamic performance, providing offset voltage drift under 15μV/°C, CMRR of 80dB, and offset current below 50nA.

SPECIFICATIONS (typical @ +25°C and V_S = ±15V dc unless otherwise specified)

PARAMETER	AD518J	AD518K	AD518S
OPEN LOOP GAIN			
$R_L \geq 2k\Omega$, V_O = ±10V	25,000 min (100,000 typ)	50,000 min (100,000 typ)	50,000 min (100,000 typ)
@ T_A = min to max	20,000 min	25,000 min	25,000 min
OUTPUT CHARACTERISTICS			
Voltage @ $R_L \geq 2k\Omega$, T_A = min to max	±12V min (±13V typ)	*	*
Current @ V_O = ±10V	±10mA	*	*
Short Circuit Current	25mA	*	*
FREQUENCY RESPONSE			
Unity Gain, Small Signal	12MHz	*	*
Slew Rate, Unity Gain	50V/μs min (70V/μs typ)	*	*
Settling Time to 0.1% (Single Capacitor Compensation)	800ns	*	*
Phase Margin, Uncompensated at Unity Gain Crossover Frequency	60°	*	*
INPUT OFFSET VOLTAGE			
Initial, $R_S \leq 10k\Omega$	10mV max (4mV typ)	4mV max (2mV typ)	4mV max (2mV typ)
@ T_A = min to max	15mV max	6mV max	6mV max
Avg vs. Temp, T_A = min to max	10μV/°C	15μV/°C max (5μV/°C typ)	20μV/°C max (10μV/°C typ)
Avg vs. Supply, T_A = min to max	65dB min (80dB typ)	80dB min (90dB typ)	80dB min (90dB typ)
INPUT BIAS CURRENT			
Initial	500nA max (120nA typ)	250nA max (120nA typ)	250nA max (120nA typ)
@ T_A = min to max	750nA max	400nA max	400nA max
INPUT OFFSET CURRENT			
Initial	200nA max (30nA typ)	50nA max (6nA typ)	50nA max (6nA typ)
@ T_A = min to max	300nA max	100nA max	100nA max
INPUT IMPEDANCE			
Differential	0.5MΩ min (3.0MΩ typ)	*	*
INPUT VOLTAGE RANGE[1]			
Common Mode, max safe	±V_S	*	*
Operating, V_S = ±15V	±11.5V	*	*
Common Mode Rejection Ratio	70dB min (100dB typ)	80dB min (100dB typ)	80dB min (100dB typ)
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	±(5 to 20)V	*	*
Current, Quiescent	10mA max (5mA typ)	7mA max (5mA typ)	7mA max (5mA typ)
TEMPERATURE RANGE			
Rated Performance	0 to +70°C	*	-55°C to +125°C
Storage	-65°C to +150°C	*	*
PACKAGE OPTION:[2] TO-99 Style (H08A)	AD518JH	AD518KH	AD518SH

NOTES

[1] The inputs are shunt with back-to-back diodes; if the differential input exceeds ±1 volt, a resistor should be used to limit the input current to 10mA.

[2] See Section 20 for package outline information.

*Specifications same as AD518J.

Specifications subject to change without notice.

STABILITY & PHASE MARGIN

Perhaps one of the most meaningful ways to express the relative stability of a closed loop amplifier is in terms of phase margin. Phase margin is measured at that frequency where the open loop gain of the amplifier becomes unity or 0dB. It is the additional amount of phase shift that, if introduced in the loop, would make the loop unstable.

At very low frequencies the gain of most operational amplifiers is generally large. Moreover, the amplifier output signal is very nearly in phase with the differential input signal. This output is, therefore, nearly 180° out of phase with the feedback signal applied to the inverting input. At sufficiently high frequencies the gain of the amplifier begins to decrease as a function of frequency, with the resulting consequence of a lagging phase characteristic. That is, as the gain falls with increasing frequency, the phase of the output signal at a given frequency will lag the phase of the input signal. The phase shift depends most critically on the slope of the gain curve with respect to the logarithm of the frequency at the frequency where the phase is measured. If the gain changes more rapidly than 12dB/octave over a substantial frequency range, the minimum resulting phase shift may exceed 180°.

To insure amplifier stability, it is necessary that the phase shift near the unity gain frequency (12MHz in the AD518) is less than 180°. Moreover, it is generally required that the phase shift be substantially below the critical stability point to insure proper system performance. If the unity gain phase shift approaches 180°, the system will be on the verge of oscillation. As a result, there will be a large peak in the closed loop response near the unity loop gain frequency. This sharply peaked frequency response generally causes an undesirable small signal transient response with a poorly damped overshoot.

The term *phase margin* refers to the difference between 180° and the actual frequency-dependent phase shift at the system unity gain frequency. It is the margin between the actual system phase shift and the critical phase shift at which oscillation will occur. Not only does it indicate the relative immunity to oscillation, but it also gives some indication about the peaking and overshoot that can be expected.

The simple pole or frequency response of a single R-C network has a gain slope of 6dB/octave. This response has an associated phase shift which is asymptotic to −90°. Linear systems which are dominated by this characteristic in their open loop response are stable. They show no overshoot or ringing in their small signal transient response. Additional poles, either above or below the unity loop gain frequency, will add phase shift. As phase shift increases up to a lagging phase of about 120°, representing a 60° phase margin, little or no peaking will result. As the unity gain phase shift increases, peaking becomes more and more evident. For example, as the phase shift reaches 160° (20° of phase margin), between 9 and 10dB of peaking will occur.

The AD518 has been designed for a 60° phase margin at the unity gain crossover frequency, for absolute stability and absence of ringing and overshoot. (Note the transient response of the AD518 in Figure 1.) Note also in Figure 2 that the phase shift at 12MHz, the unity gain crossover frequency, is 120°, representing 60° of phase margin.

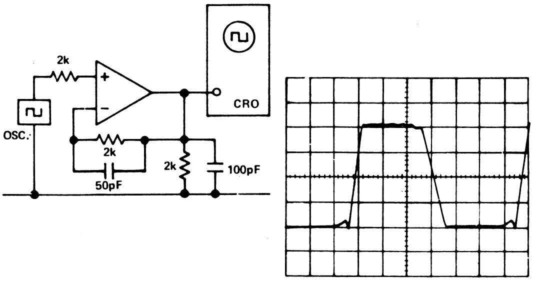


Figure 1. Transient Response of the AD518

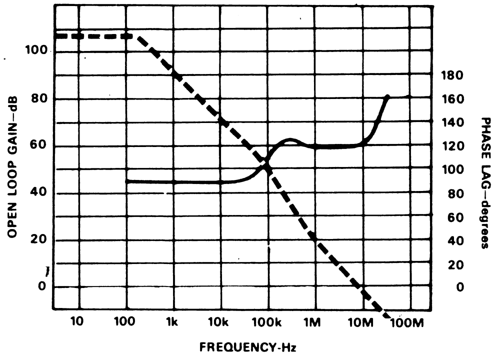


Figure 2. Amplitude and Phase Response of the AD518

THE FLEXIBILITY OF THE AD518

MINIMUM SETTLING TIME APPLICATIONS

For applications where a minimum settling time is desired, the settling time of the AD518 may be reduced significantly by employing the compensation scheme suggested in Figure 3.

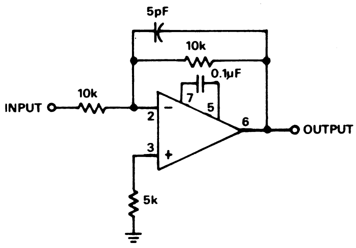


Figure 3. Minimum Settling Time Compensation

Using the 0.1μF capacitor from Pin 5 to V+ (Pin 7), the settling time to 0.1% is reduced from 2μs to 800ns.

HIGHER BANDWIDTH OR HIGHER SLEW RATE APPLICATIONS

For applications where higher bandwidth is desired, the bandwidth of the AD518 may be increased to nearly 25MHz by using the feedforward technique shown in Figure 4.

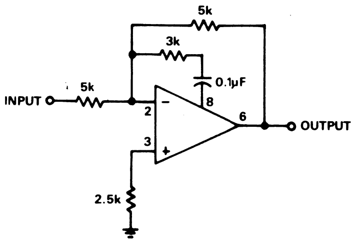


Figure 4. High Bandwidth Configuration

For applications where higher slew rate is desired, the slew rate of the AD518 may be nearly doubled using the technique shown in Figure 5.

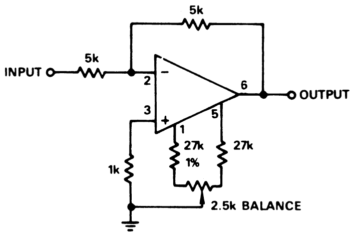


Figure 5. High Slew Rate Configuration

Note that the techniques of Figures 4 and 5 may be used in conjunction with each other to both double the bandwidth to 25MHz and increase the slew rate to 100–140V/μs.

USING THE AD518

The connection scheme employed when using the AD518 is considerably more important than for low frequency, general purpose amplifiers. The primary purpose of the 0.1μF bypass capacitors shown in Figure 6 is to convert the distributed high frequency ground to a lumped single point (the V+ point). The V+ to V– 0.1μF capacitor equalizes the supply grounds, while the 0.1μF capacitor from V+ to signal ground should be returned to signal common. This signal common, which is bypassed to pin 7, is defined as that point at which the input signal source, the feedback network, and the return side of the load are joined to the power common.

When using the AD518, this decoupling configuration should be used in conjunction with the configuration of Figures 3, 4 and 5, depending on the specific application.

Note that the diagram shows each individual capacitor directly connected to the appropriate terminal. In addition, it is suggested that all connections be made short and direct, and as physically close to the can as possible, so that the length of any conducting path shared by external components will be minimized.

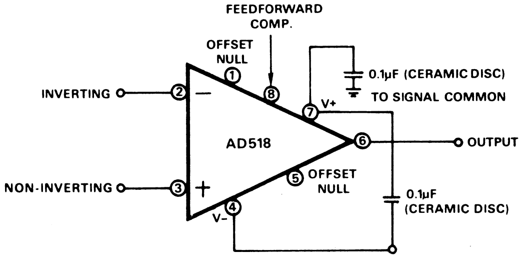
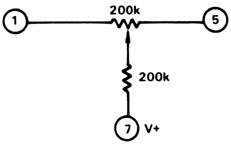


Figure 6. General Purpose Connection Diagram

NULLING THE AD518



OTHER IC HIGH SPEED AMPLIFIERS AVAILABLE

AD507	35MHz Gain Bandwidth Slew Rate of 25V/μs min Bias Current of 15nA max Offset Voltage Drift of 15μV/°C max
AD509	Settles to 0.01% in 1μs Settles to 0.1% in 200ns Slew Rate of 100V/μs min

ANALOG DEVICES

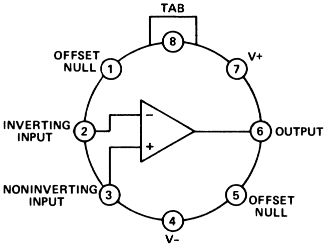
High Accuracy, Low Cost, FET-Input Operational Amplifier

AD540

FEATURES

Low Cost
Low I_b: 25pA max (K)
Low V_{OS}: 20mV max (K)
Low V_{OS} Drift: 25μV/°C max (K)
High Differential Input Voltage Capability: ±20V

AD540 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW

PRODUCT DESCRIPTION

The AD540 is the lowest cost, high accuracy FET-input op amp available which provides the user with low bias currents, high overall performance, and accurately specified predictable operation. The device offers maximum bias currents as low as 25pA, offset voltages below 20mV, maximum offset voltage drift below 25μV/°C and a minimum gain of 50,000.

All devices are free from latchup and are short-circuit protected. No external compensation is required as the internal 6dB/octave roll-off provides stability in closed loop applications.

The AD540 is suggested for all FET-input amplifier requirements where low cost is of prime importance. Its performance is comparable to modular FET op amps, but its IC construction reduces the price significantly below that of modules.

All versions of the AD540 are supplied in the hermetically-sealed, 8-pin, TO-99 package. The AD540J and AD540K are specified for 0 to +70°C applications, while the AD540S is offered for operation over the full military temperature range of -55°C to +125°C.

PRODUCT HIGHLIGHTS

1. The AD540 op amp meets specified input bias current and offset voltage values after full warm-up. Conventional high speed IC testing does not allow for self-heating of the chip due to internal power dissipation under operating conditions.
2. The bias currents of the AD540 are specified as a maximum for either input. Conventional IC FET op amps generally specify bias currents as the average of the two input currents.
3. Unlike many FET-input op amps, the AD540 allows a maximum differential input voltage of ±20V dc. Standard "bootstrapped" FET-input op amps permit maximum differential input voltages of only about ±3V.
4. Offset nulling of the AD540 is accomplished without affecting the operating current of the FET's and results in relatively small changes in temperature drift characteristics. The additional drift induced by nulling is only ±2.0μV/°C per millivolt of nulled offset, compared to several times this for other IC FET op amps.
5. The gain of the AD540 is measured with the offset voltage nulled. Nulling a FET-input op amp can cause the gain to decrease below its specified limit. The gain of the AD540 is fully guaranteed with the offset voltage both nulled and unnulled.

SPECIFICATIONS (typical @ +25°C and V_S = ±15V dc unless otherwise specified)

MODEL	AD540J	AD540K	AD540S
OPEN LOOP GAIN[1]			
V_{out} = ±10V, $R_L \geqslant 2k\Omega$	20,000 min	50,000 min	**
T_A = min to max	15,000 min	25,000 min	**
OUTPUT CHARACTERISTICS			
Voltage @ $R_L = 2k\Omega$, T_A = min to max	±10V min (±13V typ)	*	*
Voltage @ $R_L = 10k\Omega$, T_A = min to max	±12V min (±14V typ)	*	*
Short Circuit Current	25mA	*	*
FREQUENCY RESPONSE			
Unity Gain, Small Signal	1.0MHz	*	*
Full Power Response	100kHz	*	*
Slew Rate, Unity Gain	6.0V/μs	*	*
INPUT OFFSET VOLTAGE[2]	50mV max	20mV max	**
vs. Temperature	75μV/°C max	25μV/°C max	50μV/°C max
vs. Supply, T_A = min to max	400μV/V max	300μV/V max	**
INPUT BIAS CURRENT			
Either Input[3]	50pA max	25pA max	**
INPUT IMPEDANCE			
Differential	$10^{10}\Omega \| 2pF$	*	*
Common Mode	$10^{11}\Omega \| 2pF$	*	*
INPUT VOLTAGE RANGE			
Differential[4]	±20V	*	*
Common Mode	±10V min (±12V typ)	*	*
Common Mode Rejection, V_{in} = ±10V	70dB min	*	*
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	±(5 to 18)V	*	*
Quiescent Current	7mA max (3mA typ)	*	*
TEMPERATURE RANGE			
Operating, Rated Performance	0 to +70°C	*	-55°C to +125°C
Storage	-65°C to +150°C	*	*
PACKAGE OPTIONS:[5] TO-99 Style (H08B)	AD540JH	AD540KH	AD540SH

NOTES:

[1] Open Loop Gain is specified with V_{OS} both nulled and unnulled.

[2] Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

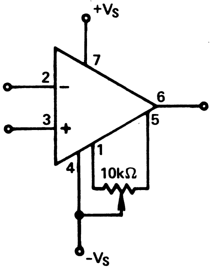
[3] Bias Current specifications are guaranteed after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

[4] Defined as voltage between inputs, such that neither exceeds ±10V from ground.

[5] See Section 20 for package outline information.

* Specifications same as AD540J.
** Specifications same as AD540K.

Specifications subject to change without notice.



Standard Offset Nulling Circuit

APPLYING THE AD540

The AD540 is especially designed for low cost applications involving the measurement of low level currents or small voltages from high impedance sources in which bias current can be a primary source of error. Input bias current contributes to error in two ways: (1) in current measuring configurations the bias current limits the resolution of a current signal; (2) the bias current produces a voltage offset which is proportional to the value of input resistance (in the case of an inverting configuration) or source impedance (when the non-inverting "buffer" connection is used). The AD540 FET-input operational amplifier is, therefore, of use where small currents are to be measured or where relatively low voltage drift is necessary despite large values of source resistance.

APPLICATIONS CONSIDERATIONS

BIAS CURRENTS. Most IC FET op amp manufacturers specify maximum bias currents as the value immediately after turn-on. Since FET bias currents double every 10°C and since most FET op amps have case temperature increases of 15°C to 20°C above ambient, initial "maximum" readings may be only ¼ of the true warmed-up value. Furthermore, most IC FET op amp manufacturers specify I_b as the average of both input currents, sometimes resulting in twice the maximum bias current appearing at the input being used. The total result is that 8X the expected bias current may appear at either input terminal in a warmed-up operating unit.

The AD540 specifies maximum bias current at either input after warm-up, thus giving the user the values he expected.

IMPROVING BIAS CURRENT BEYOND GUARANTEED VALUES. Bias currents can be substantially reduced in the AD540 by decreasing the junction temperature of the devices. One technique to accomplish this is to reduce the operating supply voltage. This procedure will decrease the power dissipation of the device, which will in turn result in a lower junction temperature and lower bias currents. The supply voltage effect on bias current is shown in Figure 1.

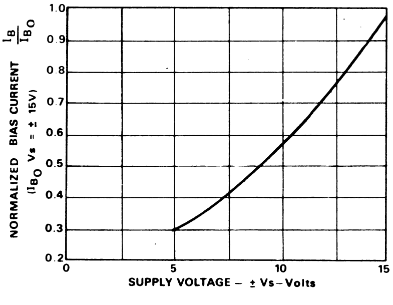


Figure 1. Normalized Bias Current vs. Supply Voltage

Operation of the AD540K at ±5V reduces the warmed-up bias current by 70% to a typical value of 8pA.

A second technique is the use of a suitable heat sink. Wakefield Engineering Series 200 heat sinks were selected to demonstrate this effect. The characteristic bias current vs. case temperature above ambient is shown in Figure 2. Bias current has been normalized with unity representing the 25°C free air reading. Note that the use of the Model 209 heat sink reduces warmed-up bias current by 60% to 10pA in the AD540K.

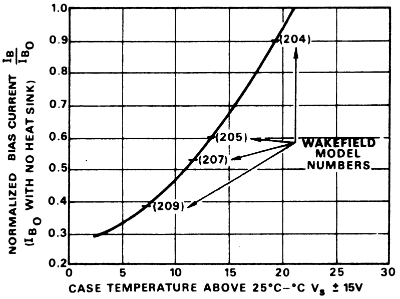


Figure 2. Normalized Bias Current vs. Case Temperature

Both of these techniques may be used together for obtaining lower bias currents. Remember that loading the output can also affect the power dissipation.

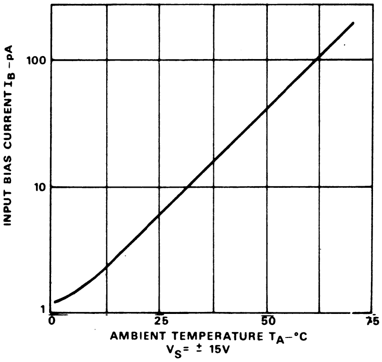


Figure 3. Input Bias Current vs. Temperature

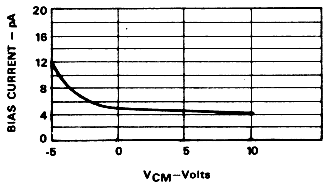


Figure 4. Bias Current vs. Common Mode Voltage

INPUT CONSIDERATIONS. Unlike some FET-input operational amplifiers, the AD540 accommodates differential input voltages of up to ±20V....without any degradation in bias current. In certain time-dependent applications, such as charge amplifiers and integrators, large differential input voltages temporarily occur which may exceed the rated value of a typical FET op amp (approximately ±3V differential).

By utilizing un-bootstrapped FET's at the inputs, the AD540 assures the user of expected performance at large differential input voltages....without the use of protective diodes or resistors.

OFFSET VOLTAGE DRIFT. Most commercially available IC FET op amps are nulled by adjusting the FET operating currents, causing the offset voltage temperature coefficients to vary 3 to 6μV/°C per millivolt of offset nulled. Thus a conventional FET op amp with 20mV initial offset, when nulled may display an additional offset drift of 60 to 120μV/°C, in addition to its nulled value.

The AD540 achieves nulling without disturbing the operating currents of the FET's, thus allowing a substantial reduction in drift. Figure 5 graphically displays the offset drift performance of the AD540, nulled and unnulled. As can be seen, nulling the device can result in either positive or negative offset drifts given by the slope $\Delta V_{OS}/\Delta T$. The nulled curves represent the maximum changes in drift, indicating performance considerably better than many other IC FET op amps which null V_{OS} by varying the operating currents of the FET's.

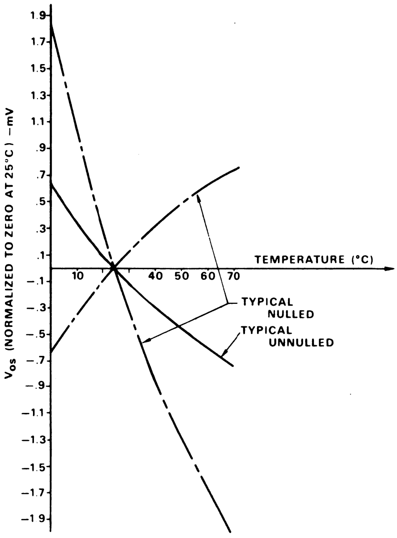


Figure 5. V_{OS} vs. Temperature

NOISE PERFORMANCE. The noise spectral density vs. frequency for the AD540 is given in Figure 6. The curve shows approximately $300nV/\sqrt{Hz}$ at 10Hz, declining in a 1/f fashion (1/f for power, $1/\sqrt{f}$ for voltage) to approximately $12nV/\sqrt{Hz}$ at higher frequencies.

Current noise in the AD540 is approximately $0.001pA/\sqrt{Hz}$ at low frequencies. Above 300Hz, the current noise generated by the op amp increases at a 3dB/octave rate, determined by $\omega e_n C_{in}$, where e_n = spectral noise density and C_{in} = input capacitance. In most practical applications, the current noise from source or feedback resistors will be larger than the low frequency current noise from the amplifier.

At high frequencies, the total circuit current noise is equal to $\omega e_n C$, where C is the sum of all input and feedback capacitors. In well-shielded circuits, C is usually 10 to 100pF, so that the $\omega e_n C$ can be a significant factor. Thus the user should attempt to minimize C.

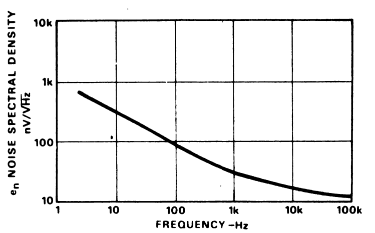


Figure 6. Noise Spectral Density vs. Frequency

DYNAMIC PERFORMANCE. The AD540 is internally compensated to achieve a –3dB bandwidth of 1MHz (see Figure 7). At unity gain the full power bandwidth is 50kHz minimum, and typically 100kHz. Slew rates are 3V/μs minimum and 6V/μs typical (see Figure 8 and Figure 9).

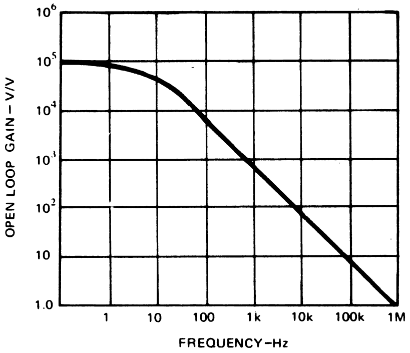


Figure 7. Small Signal Gain vs. Frequency

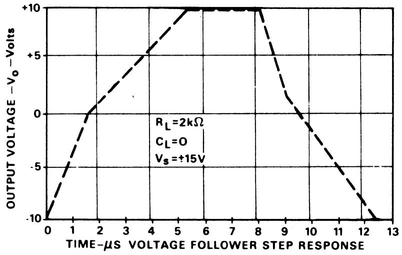


Figure 8. Voltage Follower Step Response

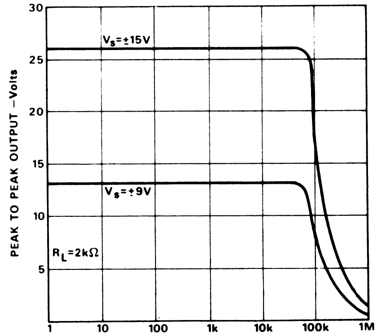


Figure 9. P-P Output vs. Frequency

ANALOG DEVICES

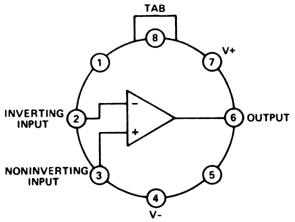
Precision Low Cost BIFET Op Amp

AD542

FEATURES

Low Bias Current: 25pA max, warmed-up (AD542K,L), 50pA max (AD542J)
Low Offset Voltage: 0.5mV max (AD542L), 1.0mV max (AD542K)
Low Offset Voltage Drift: 5µV/°C max (AD542L), 10µV/°C max (AD542K) 20µV/°C max (AD542J)
Low Quiescent Current: 1.5mA max
Low Price

AD542 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW

PRODUCT DESCRIPTION

The AD542 is a precision, monolithic FET-input operational amplifier fabricated with the most advanced BIFET and laser trimming technologies. The AD542 offers bias currents significantly lower than currently available BIFET devices: 25pA max, warmed-up for the AD542K and L, 50pA max for the AD542J. In addition, the offset voltage is laser trimmed to less than 0.5mV on the AD542L and 1.0mV on the AD542K utilizing Analog's exclusive laser-wafer-trimming (LWT) process. When combined with the AD542's low offset voltage drift (5µV/°C max for "L", 10µV/°C max for "K"), these features offer the user IC performance truly superior to existing BIFET op amps – and at low, BIFET pricing.

The key to BI-FET technology is the ion-implanted JFET. Ion-implantation (as opposed to diffusion) permits the fabrication of precision, matched JFETs on a monolithic bipolar chip. Analog Devices optimizes the BIFET process to produce bias currents lower than other popular BIFET op amps and specifies each device for the maximum value at either input in the fully warmed-up condition. Additional benefits of this optimization include low voltage noise (2µV p-p, 0.1 – 10Hz), and low quiescent current.

The AD542 is recommended for any operational amplifier application requiring excellent dc performance at low and moderate costs. Precision instrument front ends requiring accurate amplification of millivolt level signals from megohm source impedances will benefit from the device's excellent combination of low offset voltage and drift, low bias current and low 1/f noise. High common mode rejection (80dB, min on the "K" and "L" versions) and high open-loop gain–even under heavy loading–ensures better than "12-bit" linearity in high impedance buffer applications. Additionally, bandwidth and slew rate are much increased over presently available precision, bipolar op amps.

The AD542 is available in three versions: the "J", "K" and "L", all specified over the 0 to +70°C temperature range and one version, "S", over the -55°C to +125°C military operating temperature range. All devices are packaged in the hermetically-sealed, TO-99 metal can.

PRODUCT HIGHLIGHTS

1. Improved BIFET processing on the AD542 results in the lowest bias current available in a BIFET op amp.
2. Analog Devices, unlike some manufacturers, specifies each device for the maximum bias current at either input in the warmed-up condition, thus assuring the user that the AD542 will meet its published specifications in actual use.
3. Laser-wafer-trimming reduces offset voltage to as low as 0.5mV max (AD542L), thus eliminating the need for external nulling in many situations.
4. If offset nulling is required, the additional offset voltage drift induced will be minimal. (Offset voltage drift can increase an additional 3µV/°C per mV of offset nulled.)
5. Low voltage noise (2µV, p-p), and low offset voltage drift enhance the AD542's performance as a precision op amp.
6. The 1.5mA max quiescent current enables the device to be used in numerous portable applications where low battery drain is essential. This is achieved without sacrificing open loop gain or the ability to drive up to a 10mA load.

SPECIFICATIONS (typical @ +25°C and $V_S = \pm 15V$ dc unless otherwise specified)

MODEL	AD542J	AD542K	AD542L	AD542SH (AD542SH/883B)[1]
OPEN LOOP GAIN[2]				
$V_{out} = \pm 10V$, $R_L \geqslant 2k\Omega$	100,000 min	250,000 min	**	**
T_A = min to max	100,000 min	250,000 min	**	**
OUTPUT CHARACTERISTICS				
Voltage @ $R_L = 2k\Omega$, T_A = min to max	±10V min (±12V typ)	*	*	*
Voltage @ $R_L = 10k\Omega$, T_A = min to max	±12V min (±13V typ)	*	*	*
Short Circuit Current	25mA	*	*	*
FREQUENCY RESPONSE				
Unity Gain, Small Signal	1.0MHz	*	*	*
Full Power Response	50kHz	*	*	*
Slew Rate, Unity Gain	3.0V/µs	*	*	*
INPUT OFFSET VOLTAGE[3]	2.0mV max	1.0mV max	0.5mV max	**
vs. Temperature	20µV/°C max	10µV/°C max	5µV/°C max	15µV/°C max
vs. Supply, T_A = min to max	200µV/V max	100µV/V max	**	**
INPUT BIAS CURRENT				
Either Input[4]	50pA max	25pA max	**	**
Input Offset Current	5pA	2pA	**	**
INPUT IMPEDANCE				
Differential	$10^{12}\Omega\|6pF$	*	*	*
Common Mode	$10^{12}\Omega\|6pF$	*	*	*
INPUT VOLTAGE RANGE				
Differential[5]	±20V	*	*	*
Common Mode	±10V min (±12V typ)	*	*	*
Common Mode Rejection, $V_{in} = \pm 10V$	76dB min	80dB min	**	**
POWER SUPPLY				
Rated Performance	±15V	*	*	*
Operating	±(5 to 18)V	*	*	*
Quiescent Current	1.5mA max	*	*	*
VOLTAGE NOISE				
0.1-10Hz	2µV p-p	*	*	*
10Hz	$70nV/\sqrt{Hz}$	*	*	*
100Hz	$45nV/\sqrt{Hz}$	*	*	*
1kHz	$30nV/\sqrt{Hz}$	*	*	*
10kHz	$25nV/\sqrt{Hz}$	*	*	*
TEMPERATURE RANGE				
Operating, Rated Performance	0 to +70°C	*	*	-55 to +125°C
Storage	-65 to +150°C	*	*	*
PACKAGE OPTION:[6] TO-99 Style (H08B)	AD542JH	AD542KH	AD542LH	AD542SH

NOTES:

[1] The AD542SH/883B is an AD542SH which is inspected and processed to the requirements of MIL-STD-883, Level B.

[2] Open Loop Gain is specified with V_{OS} both nulled and unnulled.

[3] Input Offset Voltage specifications are guaranteed after 5 minutes of operation at $T_A = +25°C$.

[4] Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at $T_A = +25°C$. For higher temperatures, the current doubles every 10°C.

[5] Defined as voltage between inputs, such that neither exceeds ±10V from ground.

[6] See Section 20 for package outline information.

*Specifications same as AD542J.
**Specifications same as AD542K.

Specifications subject to change without notice.

Typical Characteristics

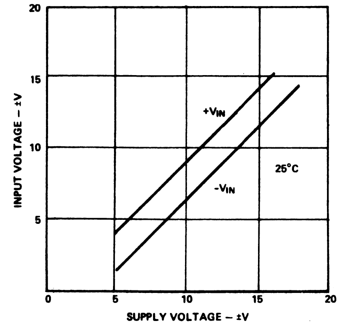


Figure 1. Input Voltage Range vs. Supply Voltage

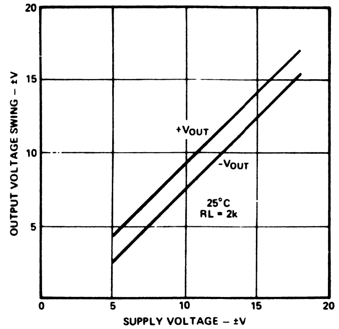


Figure 2. Output Voltage Swing vs. Supply Voltage

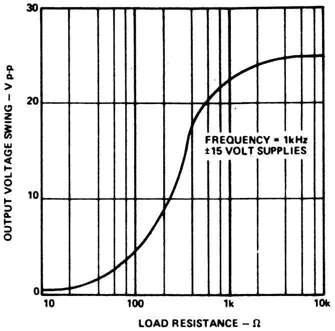


Figure 3. Output Voltage Swing vs. Resistive Load

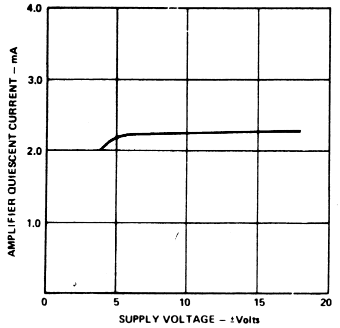


Figure 4. Quiescent Current vs. Supply Voltage

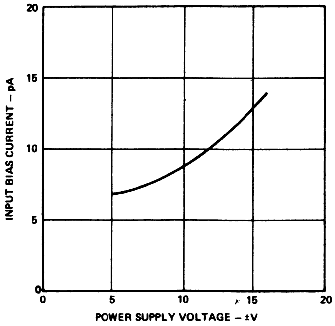


Figure 5. Input Bias Current vs. Supply Voltage

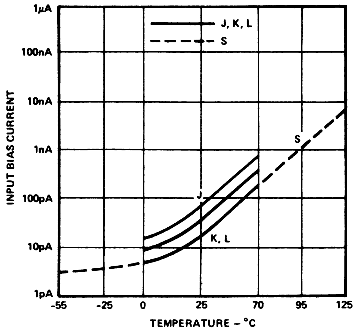


Figure 6. Input Bias Current vs. Temperature

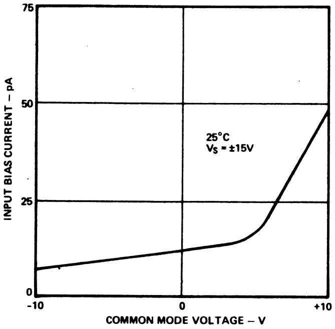


Figure 7. Input Bias Current vs. CMV

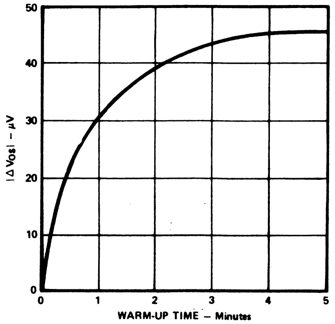


Figure 8. Input Offset Voltage Turn On Drift vs. Time

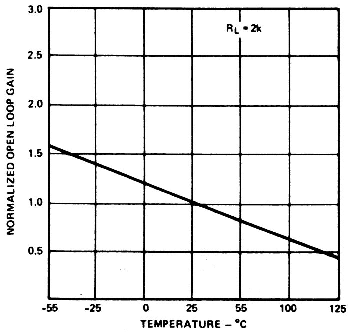


Figure 9. Open Loop Gain vs. Temperature

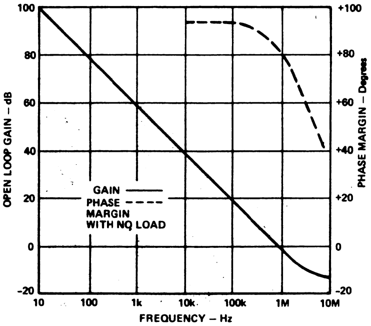


Figure 10. Open Loop Frequency Response

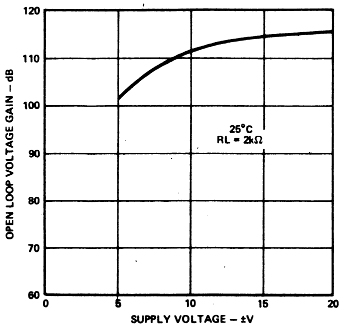


Figure 11. Open Loop Voltage Gain vs. Supply Voltage

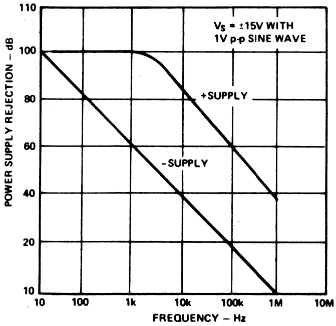


Figure 12. Power Supply Rejection vs. Frequency

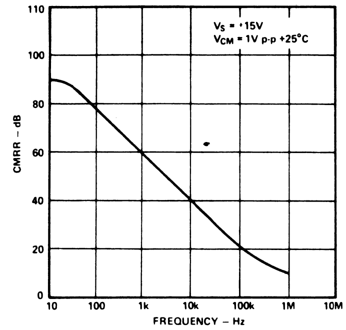


Figure 13. Common Mode Rejection vs. Frequency

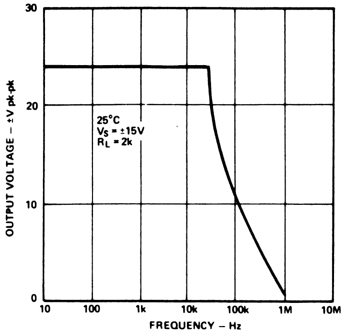


Figure 14. Large Signal Frequency Response

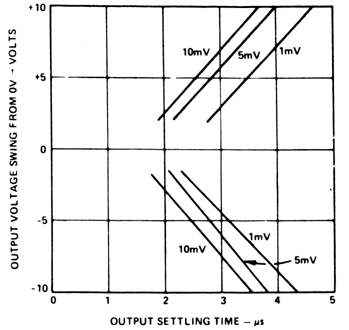


Figure 15. Output Settling Time vs. Output Swing and Error (Circuit of Figure 23)

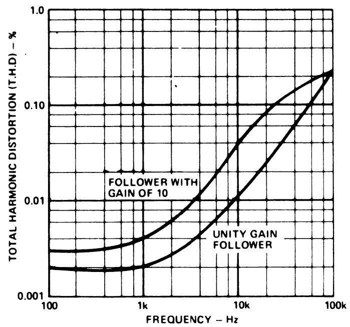


Figure 16. Total Harmonic Distortion vs. Frequency

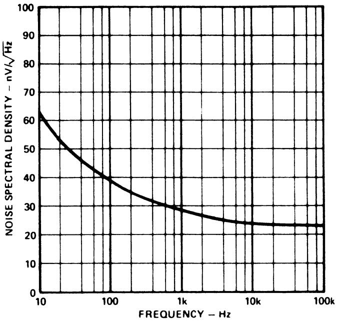


Figure 17. Input Noise Voltage Spectral Density

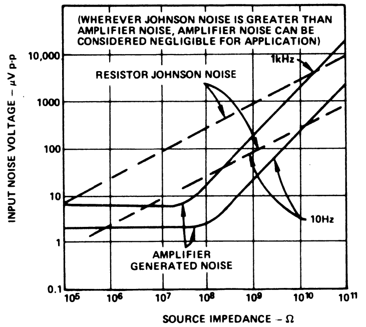
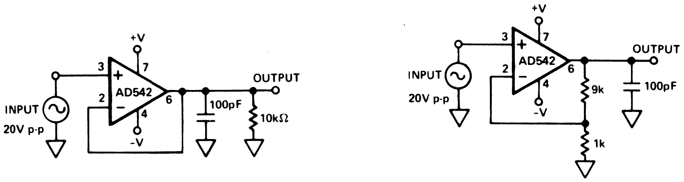


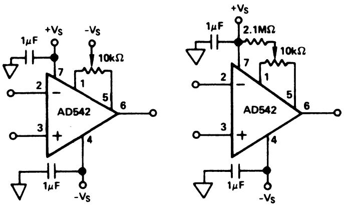
Figure 18. Total Noise vs. Source Resistance



a. Unity Gain Follower

b. Follower with Gain = 10

Figure 19. T.H.D. Test Circuits



a. Standard Null Circuit b. Null to +VS

Figure 20. Offset Voltage Null Circuits

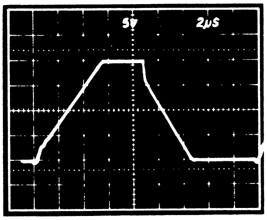


Figure 21a. Unity Gain Follower Pulse Response (Large Signal)

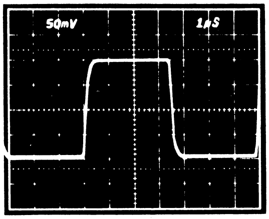


Figure 21b. Unity Gain Follower Pulse Response (Small Signal)

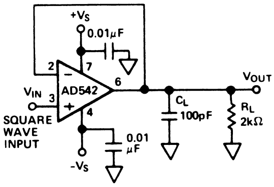


Figure 21c. Unity Gain Follower

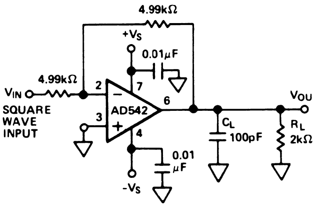


Figure 22a. Unity Gain Inverter

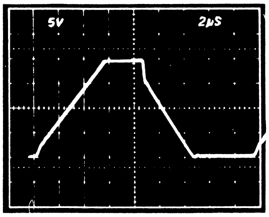


Figure 22b. Unity Gain Inverter Pulse Response (Large Signal)

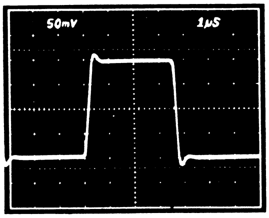


Figure 22c. Unity Gain Inverter Pulse Response (Small Signal)

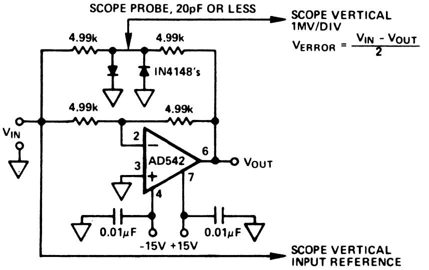

SCOPE PROBE, 20pF OR LESS
SCOPE VERTICAL 1MV/DIV
$V_{ERROR} = \frac{V_{IN} - V_{OUT}}{2}$
4.99k
4.99k
IN4148's
4.99k
4.99k
VIN
AD542
VOUT
0.01μF
0.01μF
-15V
+15V
SCOPE VERTICAL INPUT REFERENCE

Figure 23. Settling Time Test Circuit

Fast settling time (8μs to 0.01% for 20V p-p step), low power and low offset voltage make the AD542 an excellent choice for use as an output amplifier for current output D/A converters such as the AD7541.

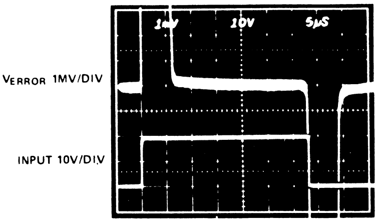


Figure 24. Settling Characteristic Detail

The upper trace of the oscilloscope photograph of Figure 23 shows the settling characteristic of the AD542. The lower trace represents the input to Figure 22. The AD542 has been designed for fast settling to 0.01%, however, feedback components, circuit layout and circuit design must be carefully considered to obtain optimum settling time.

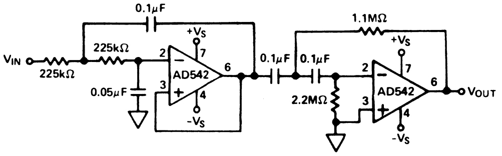
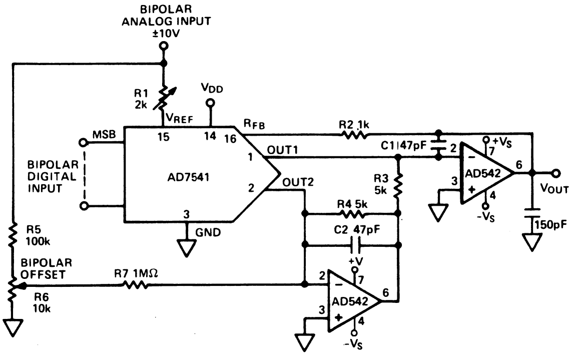


Figure 25. 0.1Hz to 10Hz Band Pass Filter

The low frequency (1/f) noise has a power spectrum that is inversely proportional to frequency. Typically this noise is not important above 10Hz, but it can be important for low frequency-high gain applications.

The low noise characteristics of the AD542 make it ideal for 1/f noise testing circuits. The circuit of Figure 24 is 0.1Hz to 10Hz band pass filter with second order filter characteristics.

The output impedance of a CMOS DAC varies with the digital word thus changing the noise of the amplifier circuit. This effect will cause a nonlinearity whose magnitude is dependent on the offset voltage of the amplifier. The AD542K with trimmed offset will minimize the effect. The Schottky protection diodes recommended for use with many older CMOS DACs are not required when using the AD542.



NOTES:
1. R3/R4 MATCH 0.05% OR BETTER.
2. R1, R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED

Figure 26a. AD542 Used as DAC Output Amplifier

Figure 26a illustrates the AD7541 12-bit digital-to-analog converter, connected for bipolar operation. Since the digital input can accept bipolar numbers and V_{REF} can accept a bipolar analog input, the circuit can perform a 4-quadrant multiplication.

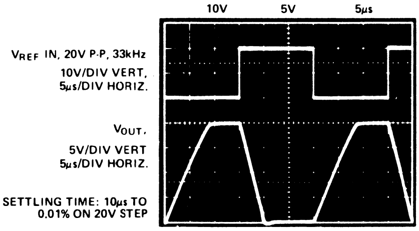


Figure 26b. Voltage Output DAC Settling Characteristic

The photo above shows the output of the circuit of Figure 26a. The upper trace represents the reference input, and the bottom trace shows the output voltage for a digital input of all ones on the DAC. The 47pF capacitor across the feedback resistor compensates for the DAC output capacitance, and the 150pF load capacitor serves to minimize output glitches.

Low amplifiers or log ratio amplifiers are useful in applications requiring compression of wide-range analog input data, linearization of transducers having exponential outputs, and analog computing, ranging from simple translation of natural relationships in log form (e.g., computing absorbance as the log-ratio of input currents), to the use of logarithms in facilitating analog computation of terms involving arbitrary exponents and multi-term products and ratios.

The picoamp level input current and low offset voltage of the AD542 make it suitable for wide dynamic range log amplifiers. Figure 22 is a schematic of a log ratio circuit employing the AD542 that can achieve less than 1% conformance error over 5 decades of current input, 1nA to 100μA. For voltage inputs, the dynamic range is typically 50mV to 10V for 1% error, limited on the low end by the amplifiers' input offset voltage.

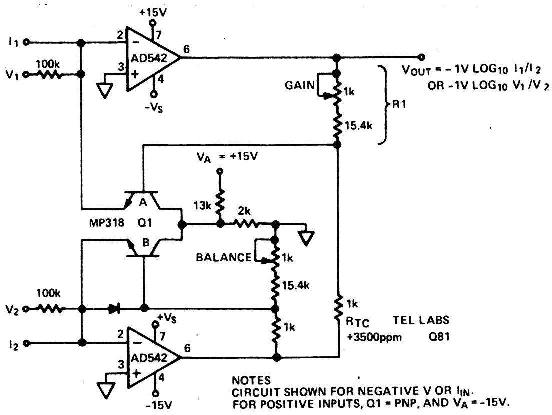


Figure 27. Log-Ratio Amplifier

The conversion between current (or voltage) input and log output is accomplished by the base emitter junctions of the dual transistor Q1. Assuming Q1 has $\beta > 100$, which is the case for the specified transistor, the base-emitter voltage on side 1 is to a close approximation:

$$V_{BE\,A} = kT/q \ln I_1/I_{S1}$$

This circuit is arranged to take the difference of the V_{BE}'s of Q1A and Q1B, thus producing an output voltage proportional to the log of the *ratio* of the inputs:

$$V_{OUT} = -K\,(V_{BE\,A} - V_{BE\,B}) = -\frac{KkT}{q}(\ln I_1/I_{S1} - \ln I_2/I_{S2})$$
$$V_{OUT} = -K\,kT/q \ln I_1/I_2$$

The scaling constant, K is set by R1 and R_{TC} to about 16, to produce 1V change in output voltage per decade difference in input signals. R_{TC} is a special resistor with a +3500ppm/°C temperature coefficient, which makes K inversely proportional to temperature, compensating for the "T" in kT/q. The log-ratio transfer characteristic is therefore independent of temperature.

This particular log ratio circuit is free from the dynamic problems that plague many other log circuits. The -3dB bandwidth is 50kHz over the top 3 decades, 100nA to 100µA, and decreases smoothly at lower input levels. This circuit needs no additional frequency compensation for stable operation from input current sources, such as photodiodes, that may have 100pF of shunt capacitance. For larger input capacitances a 20pF integration capacitor around each amplifier will provide a smoother frequency response.

This log ratio amplifier can be readily adjusted for optimum accuracy by following this simple procedure. First, apply V1 = V2 = -10.00V and adjust "Balance" for V_{OUT} = 0.00V. Next apply V1 = -10.00V, V2 = -1.00V and adjust gain for V_{OUT} = +1.00V. Repeat this procedure until gain and balance readings are within 2mV of ideal values.

The low input bias current (35pA) and low noise characteristics of the AD542 make it suitable for electrometer applications such as photo diode preamplifiers and picoampere current-to-voltage converters. The use of guarding techniques in printed circuit board layout and construction is critical for achieving the ultimate in low leakage performance that the AD542 can deliver. The input guarding scheme shown in Figure 28 will minimize leakage as much as possible; the guard ring should be applied to both sides of the board. The guard ring is connected to a low impedance potential at the same level as the inputs. High impedance signal lines should not be extended for any unnecessary length on a printed circuit; to minimize noise and leakage, they must be carried in rigid shielded cables.

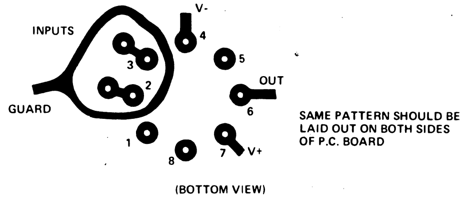


Figure 28. Board Layout for Guarding Inputs with TO-99 Package

INPUT PROTECTION

The AD542 is guaranteed for a maximum safe input potential equal to the power supply potential. The input stage design also allows differential input voltages of up to ±0.5 volts while maintaining the full differential input resistance of $10^{12}\Omega$. This makes the AD542 suitable for low speed voltage comparators directly connected to a high impedance source.

Many instrumentation situations, such as flame detectors in gas chromatographs, involve measurement of low level currents from high-voltage sources. In such applications, a sensor fault condition may apply a very high potential to the input of the current-to-voltage converting amplifier. This possibility necessitates some form of input protection. Many electrometer type devices, especially CMOS designs, can require elaborate zener protection schemes which often compromise overall performance. The AD542 requires input protection only if the source is not current-limited, and as such is similar to many JFET-input designs. The failure mode would be overheating from excess current rather than voltage breakdown. If the source is not current-limited, all that is required is a resistor in series with the affected input terminal so that the maximum overload current is 1.0mA (for example, 100kΩ for a 100 volt overload). This simple scheme will cause no significant reduction in performance and give complete overload protection. Figure 29 shows proper connections.

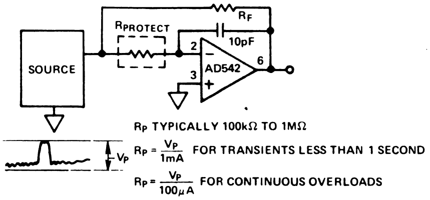

RF
RPROTECT
10pF
2
3
6
AD542
SOURCE
VP
RP TYPICALLY 100kΩ TO 1MΩ
RP = VP/1mA FOR TRANSIENTS LESS THAN 1 SECOND
RP = VP/100µA FOR CONTINUOUS OVERLOADS

Figure 29. AD542 Input Protection

ANALOG DEVICES

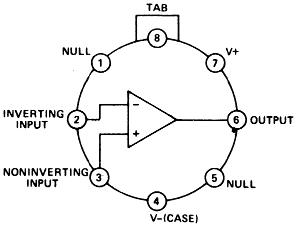
High Speed Implanted FET-Input Op Amp

AD544

FEATURES

Low Bias Current: 25pA max, warmed-up
Low Offset Voltage: 500μV max
Low Offset Voltage Drift: 5μV/°C max
Low Input Voltage Noise: 2μV p-p
Low Quiescent Current: 2.5mA max
High Slew Rate: 13V/μs
Fast Settling to ±0.01%: 3μs
Low Total Harmonic Distortion: 0.0015% at 1kHz

AD544 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW

PRODUCT DESCRIPTION

The AD544 is a high speed monolithic FET-input operational amplifier fabricated with the most advanced bipolar, JFET and laser trimming technologies. The AD544 offers bias currents significantly lower than currently available monolithic FET-input devices: 25pA max, warmed-up for the AD544K and L, 50pA max for the AD544J. In addition, the offset voltage is laser trimmed to less than 0.5mV on the AD544L and 1.0mV on the AD544K utilizing Analog's laser-wafer-trimming (LWT) process. When combined with the AD544's low offset voltage drift (5μV/°C max for "L", 10μV/°C max for "K"), these features offer the user IC performance truly superior to existing FET-input op amps—and at low, monolithic pricing.

The key technology required for monolithic JFET-input op amps is the ion-implanted JFET. Ion-implantation (as opposed to diffusion) permits the fabrication of precision, matched JFET's on a monolithic bipolar chip. Analog Devices optimizes the process to produce bias currents lower than other popular FET-input op amps and specifies each device for the maximum value at either input in the fully warmed-up condition. Additional benefits of this optimization include low voltage noise (2μV p-p, 0.1–10Hz), and low quiescent current.

The AD544 is recommended for any operational amplifier application requiring excellent ac and dc performance at low cost. The 2MHz bandwidth and low offset of the AD544 make it an excellent choice as an output amplifier for current output D/A Converters such as the AD7541, 12-Bit CMOS DAC. High common mode rejection (80dB, min on the "K" and "L" versions) and open-loop gain ensures better than "12-bit" linearity in high impedance buffer applications.

The AD544 is available in four versions: the "J", "K" and "L" are specified over the 0 to +70°C temperature range and the "S" over the -55°C to +125°C operating temperature range. All devices are packaged in the hermetically-sealed, TO-99 metal can.

PRODUCT HIGHLIGHTS

1. Improved bipolar and JFET processing on the AD544 results in the lowest bias current available in a high speed monolithic FET op amp.
2. Analog Devices, unlike some manufacturers, specifies each device for the maximum bias current at either input in the warmed-up condition, thus assuring the user that the AD544 will meet its published specifications in actual use.
3. Laser-wafer-trimming reduces offset voltage to as low as 0.5mV max (AD544L), thus eliminating the need for external nulling in many situations.
4. If offset nulling is required, the additional offset voltage drift induced will be minimal. (In some devices, offset voltage drift can increase an additional 3μV/°C per mV of offset nulled.)
5. Low voltage noise (2μV, p-p), and low offset voltage drift (5μV/°C) enhance the AD544's performance as a precision op amp.
6. The high slew rate (13.0V/μs) and fast settling time to 0.01% (3.0μs) make the AD544 ideal for D/A, A/D, sample-hold circuits and high speed integrators.
7. Low harmonic distortion (0.0015%) makes the AD544 an ideal choice for audio applications.

SPECIFICATIONS (typical @ +25°C and V_S = ±15V dc unless otherwise specified)

MODEL	AD544J	AD544K	AD544L	AD544S (AD544SH/883B)[1]
OPEN LOOP GAIN[2]				
V_{OUT} = ±10V, $R_L \geqslant 2k\Omega$	30,000 min	50,000 min	**	**
T_A = min to max $R_L = 2k\Omega$	20,000 min	40,000 min	**	*
OUTPUT CHARACTERISTICS				
Voltage @ $R_L = 2k\Omega$, T_A = min to max	±10V min (±12V typ)	*	*	*
Voltage @ $R_L = 10k\Omega$, T_A = min to max	±12V min (±13V typ)	*	*	*
Short Circuit Current	25mA	*	*	*
FREQUENCY RESPONSE				
Unity Gain, Small Signal	2.0MHz	*	*	*
Full Power Response	200kHz	*	*	*
Slew Rate, Unity Gain	13.0V/μs (8.0V/μs min)	*	*	*
Total Harmonic Distortion, f = 1kHz	0.0025%	*	*	*
INPUT OFFSET VOLTAGE[3]	2.0mV max	1.0mV max	0.5mV max	**
vs. Temperature	20μV/°C max	10μV/°C max	5μV/°C max	15μV/°C max
vs. Supply, T_A = min to max	200μV/V max	100μV/V max	**	**
INPUT BIAS CURRENT				
Either Input[4]	50pA max (10 typ)	25pA max (10 typ)	**	**
Input Offset Current	5pA	2pA	**	**
INPUT IMPEDANCE				
Differential	$10^{12}\Omega \| 6pF$	*	*	*
Common Mode	$10^{12}\Omega \| 3pF$	*	*	*
INPUT VOLTAGE RANGE				
Differential[5]	±20V	*	*	*
Common Mode	±10V min (±12V typ)	*	*	*
Common Mode Rejection, V_{IN} = ±10V	74dB min	80dB min	**	**
POWER SUPPLY				
Rated Performance	±15V	*	*	*
Operating	±(5 to 18)V	*	*	*
Quiescent Current	2.5mA max (1.8mA typ)	*	*	*
VOLTAGE NOISE				
0.1-10Hz	2μV p-p	*	*	*
10Hz	$35nV/\sqrt{Hz}$	*	*	*
100Hz	$22nV/\sqrt{Hz}$	*	*	*
1kHz	$18nV/\sqrt{Hz}$	*	*	*
10kHz	$16nV/\sqrt{Hz}$	*	*	*
TEMPERATURE RANGE				
Operating, Rated Performance	0 to +70°C	*	*	-55°C to +125°C
Storage	-65°C to +150°C	*	*	*
PACKAGING OPTIONS[6]:				
TO-99 Style (HO8B)	AD544JH	AD544KH	AD544LH	AD544SH

NOTES

[1] The AD544S/883 is an AD544S which is inspected and processed to the full requirements of MIL-STD-883, Level B. A complete listing of the tests is available on request.

[2] Open Loop Gain is specified with V_{OS} both nulled and unnulled.

[3] Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[4] Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

[5] Defined as voltage between inputs, such that neither exceeds ±10V from ground.

[6] See Section 20 for package outline information.

*Specifications same as AD544J.
**Specifications same as AD544K.

Specifications subject to change without notice.

Typical Characteristics

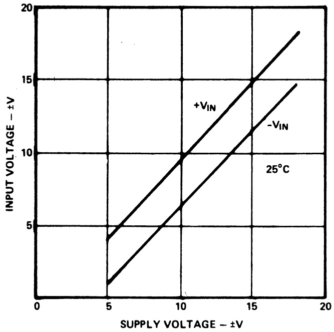


Figure 1. Input Voltage Range vs. Supply Voltage

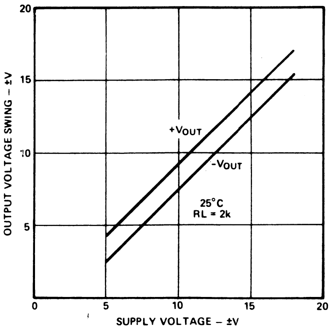


Figure 2. Output Voltage Swing vs. Supply Voltage

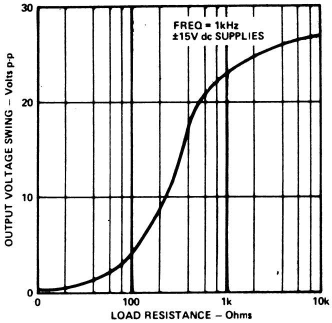


Figure 3. Output Voltage Swing vs. Resistive Load

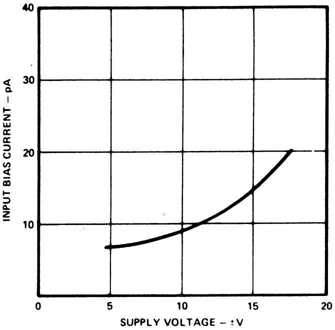


Figure 4. Input Bias Current vs. Supply Voltage

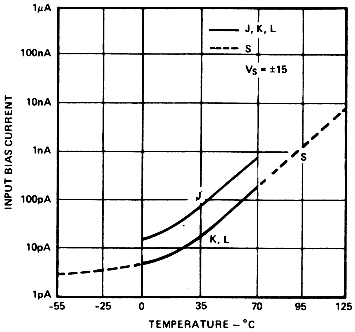


Figure 5. Input Bias Current vs. Temperature

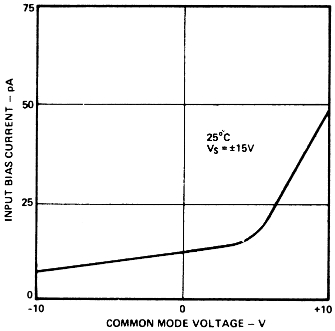


Figure 6. Input Bias Current vs. CMV

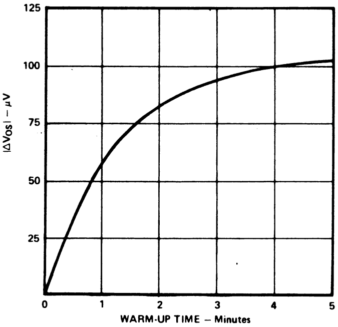


Figure 7. Change in Offset Voltage vs. Warm-Up Time

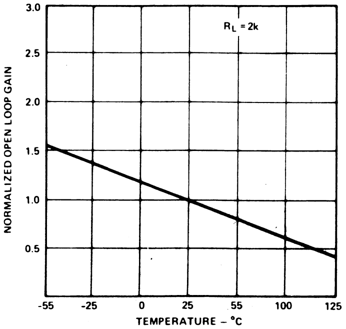


Figure 8. Open Loop Gain vs. Temperature

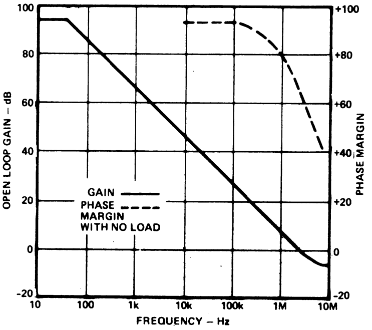


Figure 9. Open Loop Frequency Response

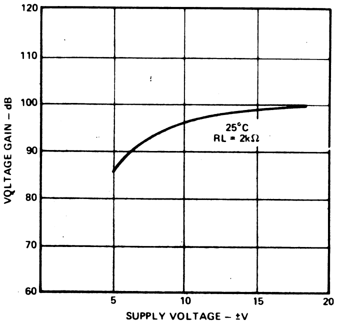


Figure 10. Open Loop Voltage Gain vs. Supply Voltage

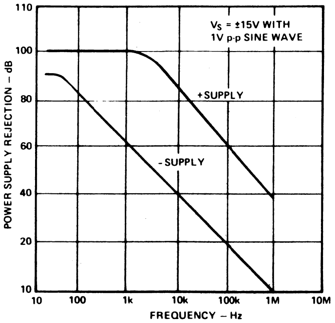


Figure 11. Power Supply Rejection vs. Frequency

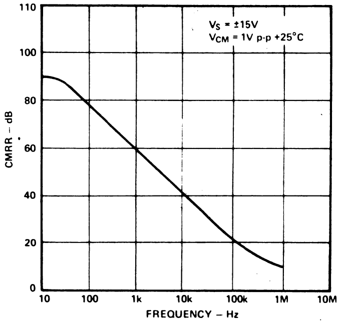


Figure 12. Common Mode Rejection Ratio vs. Frequency

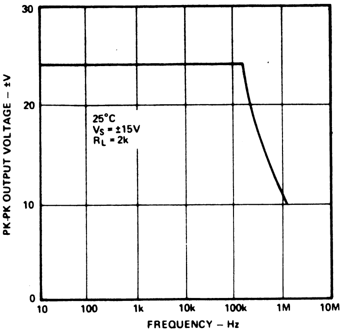


Figure 13. Large Signal Frequency Response

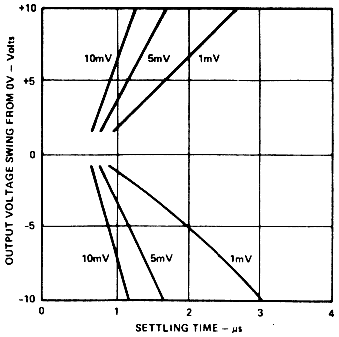


Figure 14. Output Settling Time vs. Output Swing and Error (Circuit of Figure 23a)

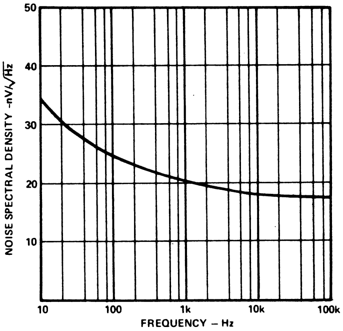


Figure 15. Noise Spectral Density

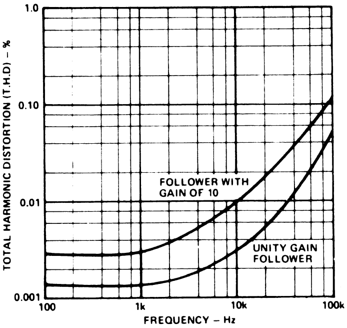


Figure 16. Total Harmonic Distortion vs. Frequency

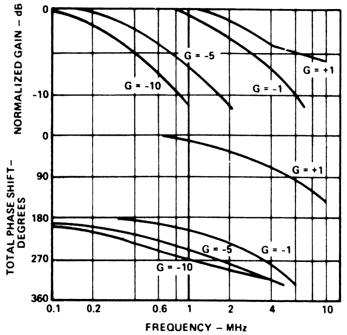


Figure 17. Closed Loop Gain & Phase vs. Frequency

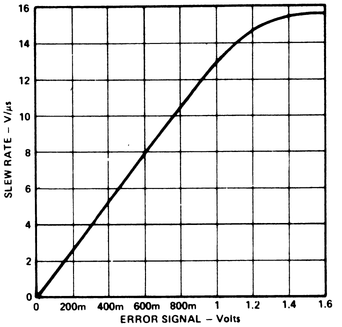
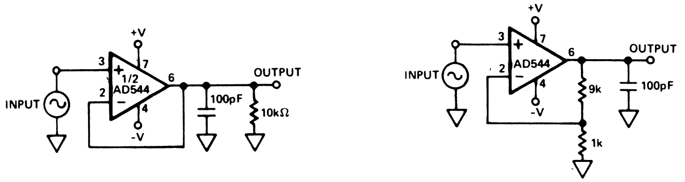


Figure 18. Slew Rate vs. Error Signal



a. Unity Gain Follower

b. Follower with Gain = 10

Figure 19. T.H.D. Test Circuits

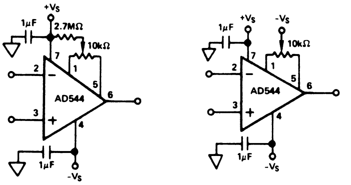


Figure 20. Offset Null Configuration

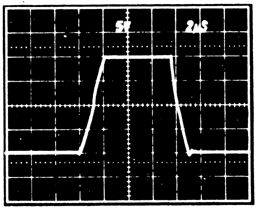


Figure 21a. Unity Gain Follower Pulse Response (Large Signal)

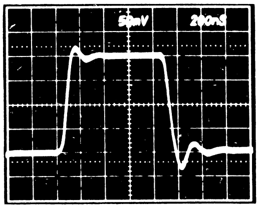


Figure 21b. Unity Gain Follower Pulse Response (Small Signal)

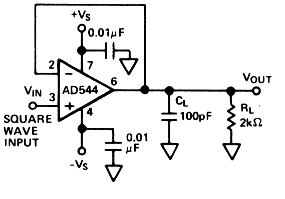


Figure 21c. Unity Gain Follower

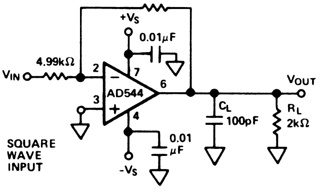


Figure 22a. Unity Gain Inverter

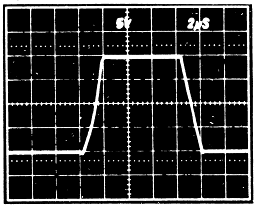


Figure 22b. Unity Gain Inverter Pulse Response (Large Signal)

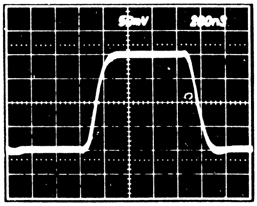


Figure 22c. Unity Gain Inverter Pulse Response (Small Signal)

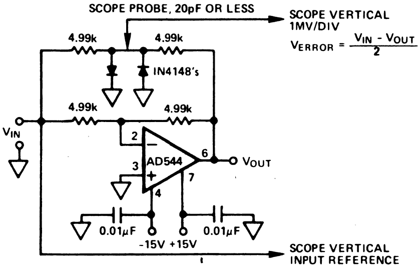


Figure 23a. Settling Time Test Circuit

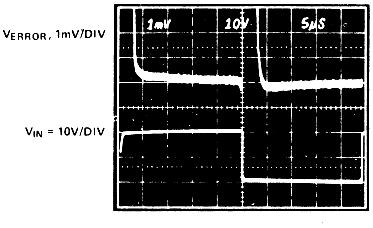


Figure 23b. Settling Characteristic Detail

The fast settling time (3.0μs to 0.01% for 20V p-p step) and low offset voltage make the AD544 an excellent choice as an output amplifier for current output D/A converters such as the AD7541. The upper trace of the oscilloscope photograph of Figure 23b shows the settling characteristics of the AD544. The lower trace represents the input to Figure 23a. The AD544 has been designed for fast settling to 0.01%, however, feedback components, circuit layout and circuit design must be carefully considered to obtain the optimum settling time.

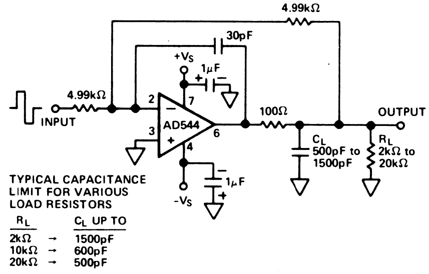
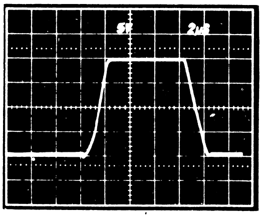


Figure 24. Circuit for Driving a Large Capacitive Load



Transient Response $R_L = 2k\Omega$ $C_L = 500pF$

The circuit in Figure 24 employs a 100Ω isolation resistor which enables the amplifier to drive capacitive loads exceeding 500pF; the resistor effectively isolates the high frequency feedback from the load and stabilizes the circuit. Low frequency feedback is returned to the amplifier summing junction via the low pass filter formed by the 100Ω series resistor and the load capacitance, C_L.

The low input bias current (35pA), low noise, high slew rate and high bandwidth characteristics of the AD544 make it suitable for electrometer applications such as photodiode preamplifiers and picoampere current-to-voltage converters. The use of guarding techniques in printed circuit board layout and construction is critical for achieving the ultimate in low leakage performance that the AD544 can deliver. The input guarding scheme shown in Figure 25 will minimize leakage as much as possible. The same layout should be used on both sides of a double side board. The guard ring is connected to a low impedance potential at the same level as the inputs. High impedance signal lines should not be extended for any unnecessary length on a printed circuit; to minimize noise and leakage, such conductors should be replaced by rigid shielded cables.

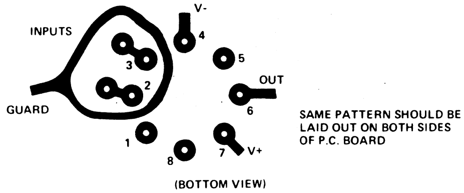


Figure 25. Board Layout for Guarding Inputs with TO-99 Package

INPUT PROTECTION

The AD544 is guaranteed for a maximum safe input potential equal to the power supply potential. The input stage design also allows differential input voltages of up to ±1 volt while maintaining the full differential input resistance of $10^{12}\,\Omega$. This makes the AD544 suitable for comparator situations employing a direct connection to high impedance source.

Many instrumentation situations, such as flame detectors in gas chromatographs, involve measurement of low level currents from high-voltage sources. In such applications, a sensor fault condition may apply a very high potential to the input of the current-to-voltage converting amplifier. This possibility necessitates some form of input protection. Many electrometer type devices, especially CMOS designs, can require elaborate zener protection schemes which often compromise overall performance. The AD544 requires input protection only if the source is not current-limited, and as such is similar to many JFET-input designs. The failure mode would be overheating from excess current rather than voltage breakdown. If the source is not current-limited, all that is required is a resistor in series with the affected input terminal so that the maximum overload current is 1.0mA (for example, 100kΩ for a 100 volt overload). This simple scheme will cause no significant reduction in performance and give complete overload protection. Figure 26 shows proper connections.

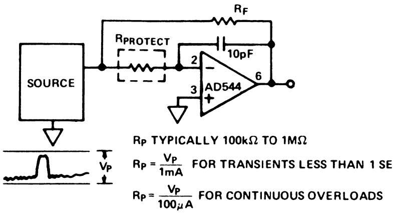
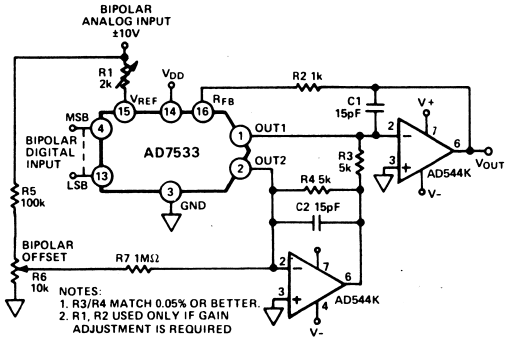

RF
RPROTECT
10pF
2
6
3
AD544
SOURCE
VP
RP TYPICALLY 100kΩ TO 1MΩ
RP = VP/1mA FOR TRANSIENTS LESS THAN 1 SECOND
RP = VP/100μA FOR CONTINUOUS OVERLOADS

Figure 26. AD544 Input Protection



NOTES:
1. R3/R4 MATCH 0.05% OR BETTER.
2. R1, R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED

Figure 27a. AD544 Used as DAC Output Amplifiers

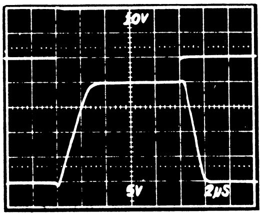


Figure 27b. Large Signal Response

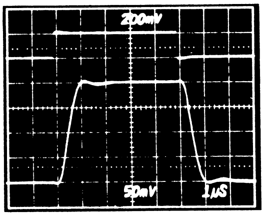


Figure 27c. Small Signal Response

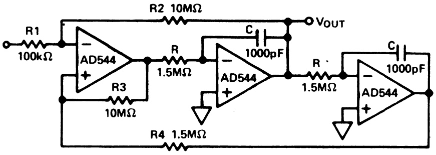
Figure 27a illustrates the 10-bit digital-to-analog converter, AD7533, connected for bipolar operation. Since the digital input can accept bipolar numbers and V_{REF} can accept a bipolar analog input, the circuit can perform a 4-quadrant multiplying function. The photos exhibit the response to a step input at V_{REF}. Figure 27b is the large signal response and Figure 27c is the small signal response.

The output impedance of a CMOS DAC varies with the digital word thus changing the noise gain of the amplifier circuit. The effect will cause a nonlinearity the magnitude of which is dependent on the offset voltage of the amplifier. The AD544K with trimmed offset will minimize the effect. The Schottky protection diodes recommended for use with many older CMOS DACs are not required when using the AD544.

ACTIVE FILTERS

Literature on active filter techniques and characteristics based on operational amplifiers is readily available. The successful application of an active filter however, depends on the component selection to achieve the desired performance. The AD544 is recommended for filters in medical, instrumentation, data acquisition and audio applications, because of its high gain bandwidth figure, symmetrical slewing, low noise, and low offset voltage.

The state variable filter (Figure 28) is stable, easily tuned and is independent of circuit Q and gain. The use of the AD544 with its low input bias current simplifies the resistor (R3, R4) selection for the passband center frequency, circuit Q and voltage gain.



f_o = CENTER FREQUENCY = $1/2\pi$ RC

Q_o = QUALITY FACTOR = $\frac{R_1 + R_2}{2R_1}$

H_o = GAIN AT RESONANCE = R_2/R_1

$R_3 = R_4 \approx 10^8/f_o$

Qo, IS ADJUSTABLE BY VARYING R2

fo, IS ADJUSTABLE BY VARYING R OR C

Figure 28. Band Pass State Variable Filter

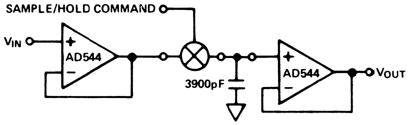


Figure 29. Sample and Hold Circuit

The sample and hold circuit, shown in Figure 29 is suitable for use with 8-bit A/D converters. The acquisition time using a 3900pF capacitor and fast CMOS SPST (ADG200) switch is 15µs.

The droop rate is very low 25 X 10^{-9} V/µs due to the low input bias currents of the AD544. Care should be taken to minimize leakage paths. Leakages around the hold capacitor will increase the droop rate and degrade performance.

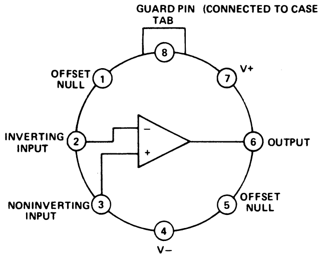
ANALOG DEVICES

Precision, Low Drift FET-Input Op Amp

AD545

FEATURES
Low Offset Voltage: 0.5mV max (AD545L), 0.25mV max (AD545M)
Low Offset Voltage Drift: 5μV/°C max (AD545L), 3μV/°C max (AD545M)
Low Power: 1.5mA max
Low Bias Current: 1pA max (AD545K, L, M)
Low Noise: 3μV p-p, 0.1 to 10Hz
Low Cost

AD545 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW

PRODUCT DESCRIPTION

The AD545 is a precision FET-input operational amplifier with overall performance far superior to the general purpose IC FET-input op amp. The device is fabricated using a low leakage FET paired with a low power op amp. Bias current is specified as 2pA max for the AD545J and 1pA max for the AD545K, L and M. Offset voltage is laser trimmed to 0.5mV max for the AD545L, 0.25mV max for the AD545M. All devices also feature low voltage noise and power consumption. The AD545 is internally compensated, short circuit protected and free of latch-up.

The AD545 series offers a broad combination of performance features previously unavailable from a single device. For precision applications the AD545M specifies a 0.25mV max offset voltage, 3μV/°C max drift and 1pA max bias current. The AD545J, with a 1mV max offset voltage, 25μV/°C max drift and 2pA max bias current, is the best price performance choice.

These devices are recommended for a variety of general purpose and precision applications requiring low bias currents and high input impedance such as pH/plon sensitive electrodes, photo-current detectors, biological microprobes, long term precision integrators and vacuum iongauge measurements. The versatility of the AD545 is further enhanced by its excellent low frequency noise (3μV p-p, 0.1 to 10Hz) and low power consumption (1.5mA max) for portable applications.

As with previous electrometer amplifier designs from Analog Devices, the case is guarded thus minimizing stray leakage. This feature will also shield the input circuitry from external noise and supply transients, as well as reducing common mode input capacitance from 0.8pF to 0.2pF.

The AD545 is available in four versions of bias current and offset voltage, the "J", "K", "L", and "M". All are specified from 0 to +70°C and supplied in a hermetically sealed TO-99 package.

PRODUCT HIGHLIGHTS

1. The offset voltage on the AD545 is laser trimmed to a level typically less than 250μV. Offset voltage drift is significantly lower than previously available FET-input devices (3μV/°C max for the AD545M). If additional external nulling is desired, the effect on drift is minimal (approximately 3μV/°C per millivolt, nulled).
2. Bias current is specified as the maximum measured at either input with the device fully warmed up on ±15V supplies at +25°C ambient.
3. The low quiescent current drain of 0.8mA typical, and 1.5mA max, is among the lowest of any IC op amp and keeps self heating to a minimum.
4. The combination of low input noise voltage and very low input noise current is such that for source impedances from much over one megohm up to 10^{11} ohm, the Johnson noise of the source will easily dominate the noise characteristics.

SPECIFICATIONS (typical @ +25°C with V_S = ±15V dc, unless otherwise specified)

MODEL	AD545J	AD545K	AD545L	AD545M
OPEN LOOP GAIN[1]				
V_{OUT} = ±10V, $R_L \geqslant 2k\Omega$	20,000V/V min	40,000V/V min	40,000V/V min	40,000V/V min
$R_L \geqslant 10k\Omega$	40,000V/V min	50,000V/V min	50,000V/V min	50,000V/V min
T_A = min to max $R_L \geqslant 2k\Omega$	15,000V/V min	25,000V/V min	40,000V/V min	40,000V/V min
OUTPUT CHARACTERISTICS				
Voltage @ $R_L = 2k\Omega$, T_A = min to max	±10V min (±12V typ)	*	*	*
@ $R_L = 10k\Omega$, T_A = min to max	±12V min (±13V typ)	*	*	*
Load Capacitance[2]	500pF	*	*	*
Short Circuit Current	10mA min (25mA typ)	*	*	*
FREQUENCY RESPONSE				
Unity Gain, Small Signal	700kHz	*	*	*
Full Power Response	5kHz min (16kHz typ)	*	*	*
Slew Rate Inverting Unity Gain	0.3V/μs min (1.0V/μs typ)	*	*	*
Overload Recovery Inverting Unity Gain	100μs max (16μs typ)	*	*	*
INPUT OFFSET VOLTAGE[3]	1.0mV max	1.0mV max	0.5mV max	0.25mV max
vs. Temperature, T_A = min to max	25μV/°C max	15μV/°C max	5μV/°C max	3μV/°C max
vs. Supply, T_A = min to max	400μV/V max (50μV/V typ)	200μV/V max	200μV/V max	200μV/V max
INPUT BIAS CURRENT				
Either Input[4]	2pA max	1pA max	1pA max	1pA max
INPUT IMPEDANCE				
Differential	$1.6pF \| 10^{13}\Omega$	*	*	*
Common Mode	$0.8pF \| 10^{15}\Omega$	*	*	*
INPUT NOISE				
Voltage, 0.1Hz to 10Hz	3.0μV (p-p)	*	*	5μV (p-p) max
f = 10Hz	$55nV/\sqrt{Hz}$	*	*	*
f = 100Hz	$45nV/\sqrt{Hz}$	*	*	*
f = 1kHz	$35nV/\sqrt{Hz}$	*	*	*
Current, 0.1 to 10Hz	0.01pA (p-p)	*	*	*
10Hz to 10kHz	0.03pA rms	*	*	*
INPUT VOLTAGE RANGE				
Differential	±20V min	*	*	*
Common Mode, T_A = min to max	±10V min (±12V typ)	*	*	*
Common Mode Rejection, V_{IN} = ±10V	66dB min (80dB typ)	70dB min	76dB min	76dB min
Maximum Safe Input Voltages[5]	$\pm V_S$	*	*	*
POWER SUPPLY				
Rated Performance	±15V typ	*	*	*
Operating	±5V min (±18V max)	*	*	*
Quiescent Current	1.5mA max (0.8mA typ)	*	*	*
TEMPERATURE				
Operating, Rated Performance	0 to +70°C	*	*	*
Storage	−65°C to +150°C	*	*	*
PACKAGE OPTION[6]				
TO-99 Style (H08B)	AD545JH	AD545KH	AD545LH	AD545MH

*Specifications same as AD545J.

NOTES

[1] Open Loop Gain is specified with or without nulling of V_{OS}.

[2] A conservative design would not exceed 500pF of load capacitance.

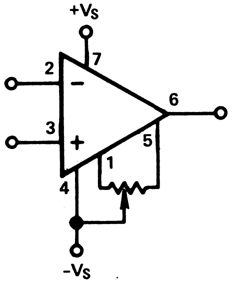
[3] Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[4] Bias Current specifications are guaranteed after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every +10°C.

[5] If it is possible for the input voltage to exceed the supply voltage, a series protection resistor should be added to limit input current to 0.5mA. The input devices can handle overload currents of 0.5mA indefinitely without damage.

[6] See Section 20 for package outline information.

Specifications subject to change without notice.



Standard Offset Null Circuit

LAYOUT AND CONNECTION CONSIDERATIONS

The design of very high impedance measurement systems introduces a new level of problems associated with the reduction of leakage paths and noise pickup.

1. A primary consideration in high impedance system designs is to attempt to place the measuring device as near to the signal source as possible. This will minimize current leakage paths, noise pickup and capacitive loading.
2. The use of guarding techniques is essential to realizing the capability of the low input currents of the AD545. Guarding is achieved by applying a low impedance bootstrap potential to the outside of the insulation material surrounding the high impedance signal line. This bootstrap potential is held at the same level as that of the high impedance line; therefore, there is no voltage drop across the insulation, and hence, no leakage. The guard will also act as a shield to reduce noise pickup and serves the additional function of reducing the effective capacitance to the input line. The case of the AD545 is brought out separately to pin 8 so that it can also be connected to the guard potential. This technique virtually eliminates potential leakage paths across the package insulation, provides a noise shield for the sensitive circuitry, and reduces common-mode input capacitance to about 0.2pF. Figure 10 shows a proper printed circuit board layout for input guarding and connecting the case guard. Figures 2 and 3 show guarding connections for typical inverting and non-inverting applications. If pin 8 is not used for guarding, it should be connected to ground or one of the amplifier's power supplies to reduce noise.
3. Printed circuit board layout and construction is critical in achieving low leakage performance. The best performance will be realized by using a teflon IC socket for the AD545 but at least a teflon stand-off should be used for the high-impedance lead. If this is not feasible, the input guarding scheme shown in Figure 10 will minimize leakage as much as possible and should be applied to both sides of the board. The guard ring is connected to a low impedance potential at the same level as the inputs. High impedance signal lines should not be extended for any unnecessary length on a printed circuit; to minimize noise and leakage, they must be carried in rigid, shielded cables.

APPLICATION NOTES

The AD545 offers one of the lowest input bias currents available in an integrated circuit package. Performing accurate measurements with this device requires careful attention to detail; the notes given here will aid the user in realizing the full measurement potential of the AD545 and extending its performance limits.

1. As with all junction FET input devices, the temperature of the FET's themselves is all-important in determining the input bias currents. Over the operating temperature range, the input bias currents closely follow a characteristic of doubling every 10°C; therefore, every effort should be made to minimize device operating temperature
2. The heat dissipation can be reduced initially by careful investigation of the application. First, if possible, reduce the required power supplies, since internal power consumption contributes the largest component of self-heating. The effects of this are shown in Figure 7, which shows typical input bias current and quiescent current versus supply voltage.
3. Output loading effects, which are normally ignored, can cause a significant increase in chip temperature and therefore bias current. For example, a 2kΩ load driven at 10 volts at the output will cause at least an additional 25 milliwatts dissipation in the output stage (and some in other stages) over the typical 24 milliwatts, thereby at least doubling the effects of self-heating. The results of this form of additional power dissipation are demonstrated in Figure 9, which shows normalized input bias current versus additional power dissipated (it doubles every 10°C); we recommend restricting the load impedance to be at least 10kΩ.

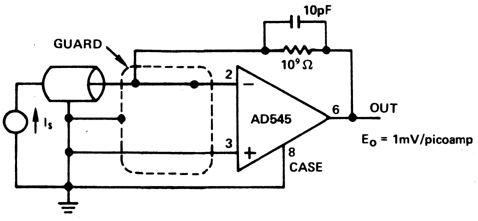


Figure 1. Picoampere Current-to-Voltage Converter Inverting Configuration

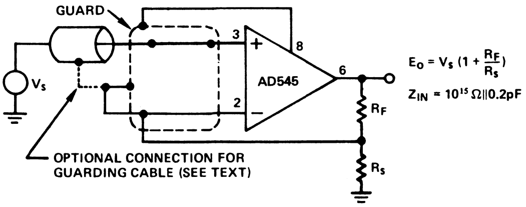

GUARD
3
+
8
6
AD545
V_s
2
−
R_F
R_s
OPTIONAL CONNECTION FOR GUARDING CABLE (SEE TEXT)
$E_O = V_s\,(1 + \frac{R_F}{R_s})$
$Z_{IN} = 10^{15}\,\Omega \| 0.2\text{pF}$

Figure 2. Very High Impedance Non-Inverting Amplifier

Typical Performance Curves

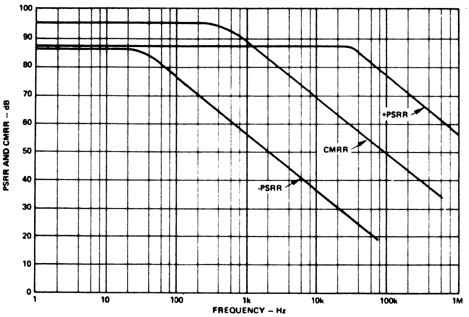


Figure 3. PSRR and CMRR Versus Frequency

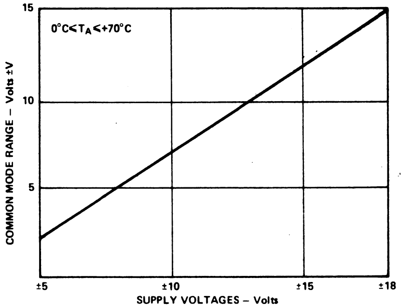


Figure 4. Input Common Mode Range Versus Supply Voltage

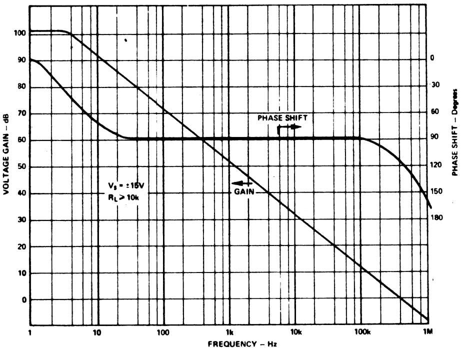


Figure 5. Open Loop Frequency Response

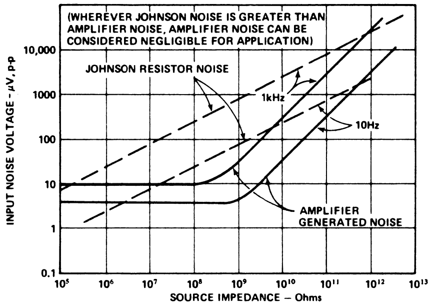


Figure 6. Total Input Noise Voltage Versus Source Impedance and Bandwidth

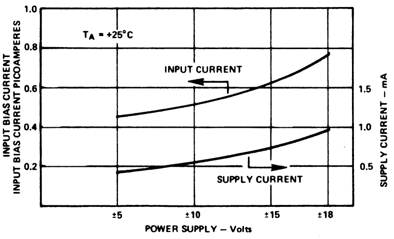


Figure 7. Input Bias Current and Supply Current Versus Supply Voltage

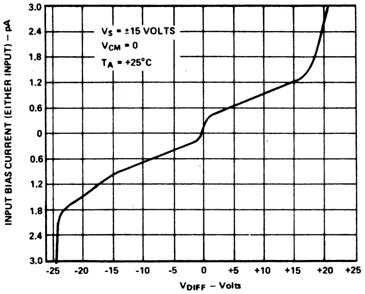


Figure 8. Input Bias Current Versus Differential Input Voltage

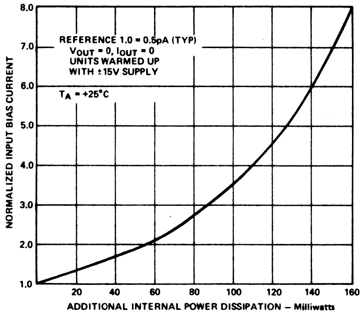
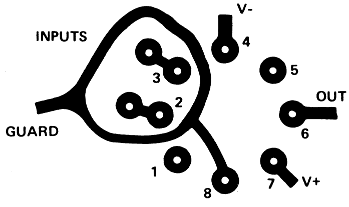


Figure 9. Input Bias Current Versus Addition Power Dissipation



SAME PATTERN SHOULD BE
LAID OUT ON BOTH SIDES
OF P.C. BOARD

(BOTTOM VIEW)

Figure 10. Board Layout for Guarding Inputs with Guarded TO-99 Package

ANALOG DEVICES

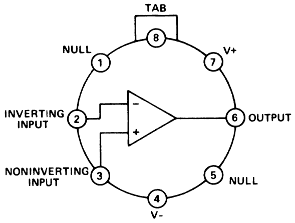
Ultra Low Drift BIFET Operational Amplifier

AD547

FEATURES

Ultra Low Drift (1μV/°C–AD547L)
Low Offset Voltage (0.25mV–AD547L)
Low Input Bias Currents (25pA–AD547L, K)
Low Quiescent Current (1.5mA)
Low Noise (2μV p-p)
High Open Loop Gain (110dB–AD547K, L, S)

AD547 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW

PRODUCT DESCRIPTION

The AD547 is a monolithic, FET input operational amplifier combining the very low input bias current advantages of a BIFET op amp with offset and drift performance previously available only from high quality bipolar amplifiers.

The exclusive Analog Devices laser wafer trim process trims both the input offset voltage and offset voltage drift to levels far lower than any competing BIFET amplifier (1mV, 5μV/°C–AD547JH, 0.25mV, 1μV/°C–AD547LH).

In addition to superior low drift performance, the AD547 offers the lowest guaranteed input bias currents of any BIFET amplifier with 50pA max for the J grade and 25pA max for the L grade. Since Analog Devices, unlike most other manufacturers, specifies input bias current with the amplifiers warmed-up, our BIFET amplifiers are specified under actual operating conditions.

The AD547 is especially designed for use in applications, such as instrumentation signal conditioning and analog computation, that require a high degree of precision at low cost.

The AD547 is offered in three commercial versions, J, K and L specified from 0 to +70°C and one military version, the S, specified from -55°C to +125°C. All grades are packaged in hermetically sealed TO-99 cans. The S grade is available fully screened to MIL-STD-883, Level B.

PRODUCT HIGHLIGHTS

1. Advanced laser wafer trimming techniques reduce offset voltage drift to 1μV/°C max and reduce offset voltage to only 0.25mV max on the AD547L.
2. Analog Devices BIFET processing provides 25pA max (10pA typical) bias currents specified after 5 minutes of warm-up.
3. Low voltage noise, high open loop gain and outstanding offset performance make the AD547 a true precision BIFET amplifier.
4. The low quiescent supply current, typically 1.1mA, enables the AD547 to bring a new level of precision to applications where low power consumption is essential.
5. A further benefit on the AD547's low power consumption and low offset voltage drift is a minimal warm-up drift after power is applied (typically 7μV shift for the AD547L).

SPECIFICATIONS (typical @ +25°C and V_S = ±15V dc unless otherwise specified)

MODEL	AD547J	AD547K	AD547L	AD547SH (AD547SH/883B)[1]
OPEN LOOP GAIN[2]				
V_{out} = ±10V, $R_L \geqslant 2k\Omega$	100,000 min	250,000 min	**	**
T_A = min to max	100,000 min	250,000 min	**	**
OUTPUT CHARACTERISTICS				
Voltage @ $R_L = 2k\Omega$, T_A = min to max	±10V min (±12V typ)	*	*	*
Voltage @ $R_L = 10k\Omega$, T_A = min to max	±12V min (±13V typ)	*	*	*
Short Circuit Current	25mA	*	*	*
FREQUENCY RESPONSE				
Unity Gain, Small Signal	1.0MHz	*	*	*
Full Power Response	50kHz	*	*	*
Slew Rate, Unity Gain	3.0V/μs	*	*	*
INPUT OFFSET VOLTAGE[3]	1.0mV max	0.5mV max	0.25mV max	**
vs. Temperature[4]	5μV/°C max	2μV/°C max	1μV/°C max	5μV/°C max
vs. Supply, T_A = min to max	200μV/V max	100μV/V max	**	**
INPUT BIAS CURRENT				
Either Input[5]	10pA (50pA max)	10pA (25pA max)	**	**
Input Offset Current	5pA	2pA	**	**
INPUT IMPEDANCE				
Differential	$10^{12}\Omega\|\|6pF$	*	*	*
Common Mode	$10^{12}\Omega\|\|6pF$	*	*	*
INPUT VOLTAGE RANGE				
Differential[6]	±20V	*	*	*
Common Mode	±10V min (±12V typ)	*	*	*
Common Mode Rejection, V_{IN} = ±10V	76dB min	80dB min	**	**
POWER SUPPLY				
Rated Performance	±15V	*	*	*
Operating	±(5 to 18)V	*	*	*
Quiescent Current	1.5mA max (1.1mA typ)	*	*	*
VOLTAGE NOISE				
0.1-10Hz	2μV p-p typ	4μV p-p max	**	**
10Hz	$70nV/\sqrt{Hz}$	*	*	*
100Hz	$45nV/\sqrt{Hz}$	*	*	*
1kHz	$30nV/\sqrt{Hz}$	*	*	*
10kHz	$25nV/\sqrt{Hz}$	*	*	*
TEMPERATURE RANGE				
Operating, Rated Performance	0 to +70°C	*	*	-55°C to +125°C
Storage	-65°C to +150°C	*	*	*
PACKAGE OPTION[7]				
TO-99 STYLE (H08B)	AD547JH	AD547KH	AD547LH	AD547SH

NOTES

[1] The AD547SH is offered screened to MIL-STD-883, Level B.

[2] Open Loop Gain is specified with V_{OS} both nulled and unnulled.

[3] Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[4] Input Offset Voltage Drift is specified with the offset voltage unnulled. Nulling will induce an additional 3μV/°C/mV of nulled offset.

[5] Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

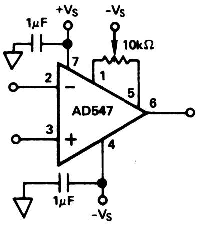
[6] Defined as the maximum safe voltage between inputs, such that neither exceeds ±10V from ground.

[7] See Section 20 for package outline information.

*Specifications same as AD547J.

**Specifications same as AD547K.

Specifications subject to change without notice.



Standard Null Circuit

Typical Characteristics

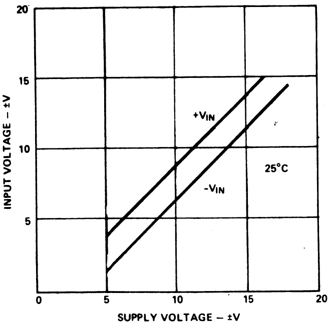


Figure 1. Input Voltage Range vs. Supply Voltage

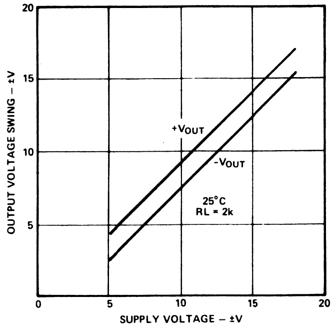


Figure 2. Output Voltage Swing vs. Supply Voltage

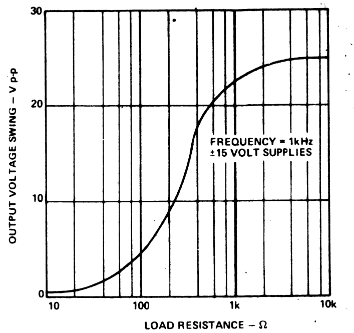


Figure 3. Output Voltage Swing vs. Resistive Load

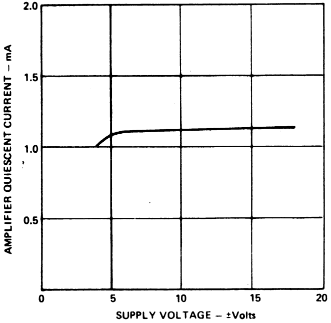


Figure 4. Quiescent Current vs. Supply Voltage

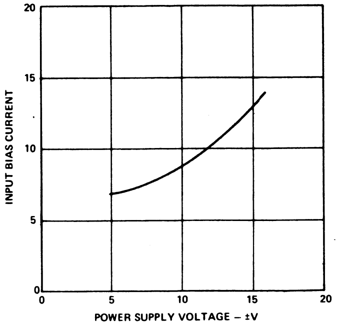


Figure 5. Input Bias Current vs. Supply Voltage

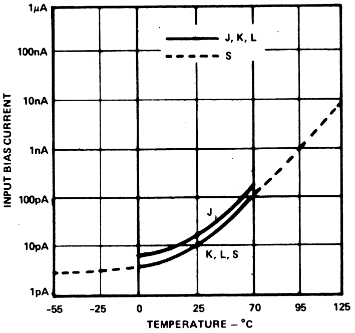


Figure 6. Input Bias Current vs. Temperature

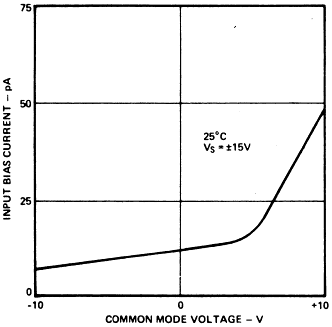


Figure 7. Input Bias Current vs. CMV

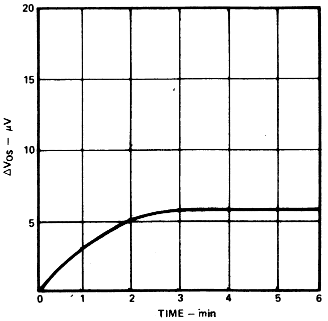


Figure 8. Input Offset Voltage Turn On Drift vs. Time

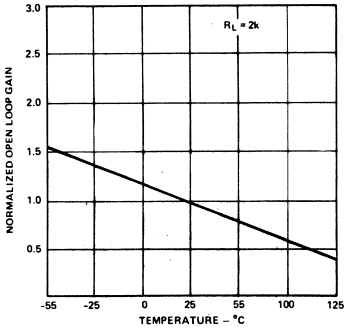


Figure 9. Open Loop Gain vs. Temperature

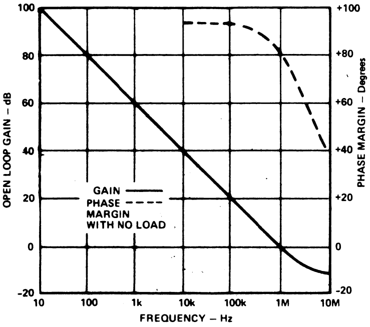


Figure. 10 Open Loop Frequency Response

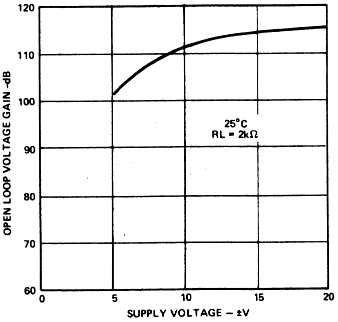


Figure 11. Open Loop Voltage Gain vs. Supply Voltage

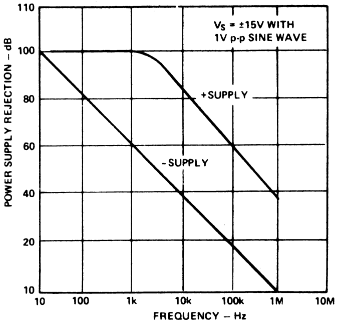


Figure 12. Power Supply Rejection vs. Frequency

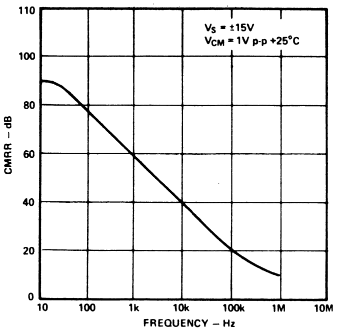


Figure 13. Common Mode Rejection vs. Frequency

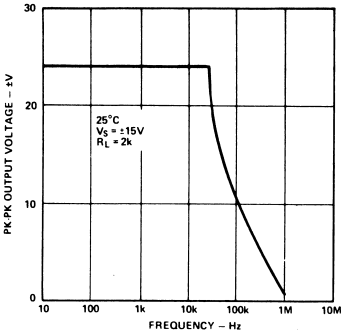


Figure 14. Large Signal Frequency Response

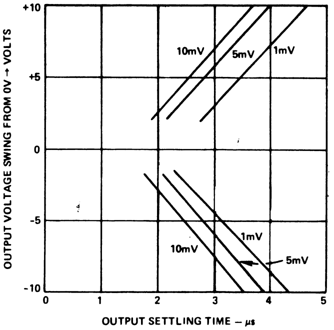


Figure 15. Output Settling Time vs. Output Swing and Error (Circuit of Figure 20)

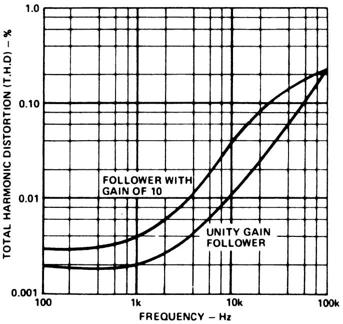


Figure 16. Total Harmonic Distortion vs. Frequency

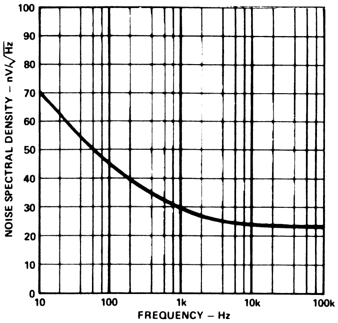


Figure 17. Input Noise Voltage Spectral Density

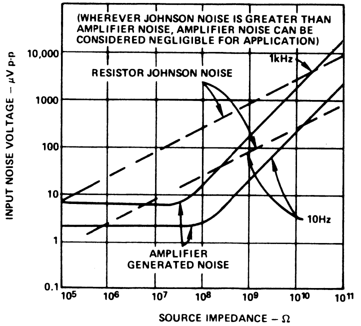
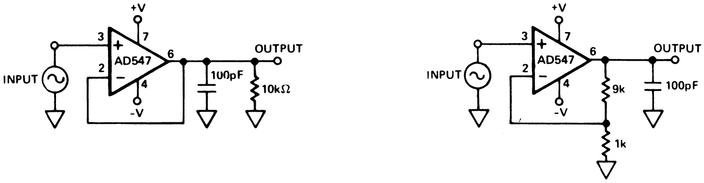


Figure 18. Total Noise vs. Source Resistance



a. Unity Gain Follower

b. Follower with Gain = 10

Figure 19. T.H.D. Test Circuits

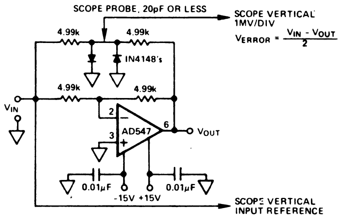


Figure 20. Settling Time Test Circuit

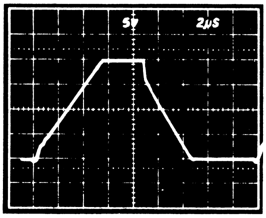


Figure 21a. Unity Gain Follower Pulse Response (Large Signal)

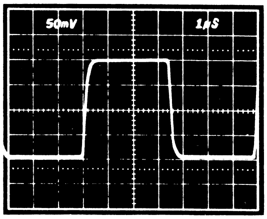


Figure 21b. Unity Gain Follower Pulse Response (Small Signal)

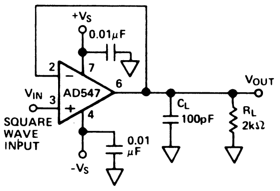


Figure 21c. Unity Gain Follower

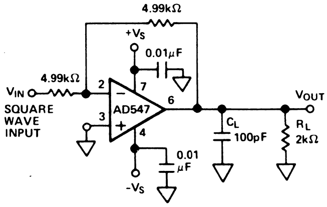


Figure 22a. Unity Gain Inverter

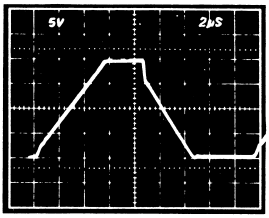


Figure 22b. Unity Gain Inverter Pulse Response (Large Signal)

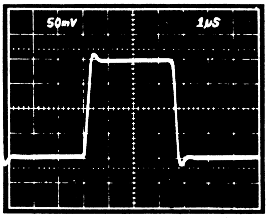


Figure 22c. Unity Gain Inverter Pulse Response (Small Signal)

APPLICATION NOTES

The AD547 was designed for high performance op-amp applications that require true dc precision. To capitalize on all of the performances available from the AD547 there are some practical error sources that should be considered in using this precision BIFET.

The bias currents of JFET input amplifiers double with every 10°C increase in chip temperature. Therefore, minimizing the junction temperature of the chip will result in extending the performance limits of the device.

1. Heat dissipation due to power consumption is the main contributor to self-heating and can be minimized by reducing the power supplies to the lowest level allowed by the application.
2. The effects of output loading should be carefully considered. Greater power dissipation increases bias currents and decreases open loop gain.

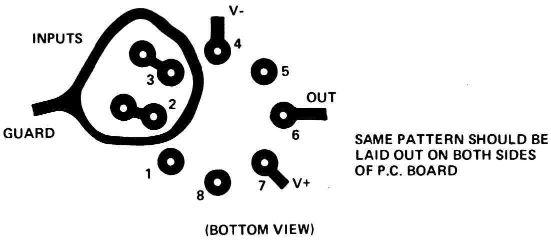


Figure 23. Board Layout for Guarding Inputs with TO-99 Package

GUARDING

The low input bias current (25pA) and low noise characteristics of the AD547 make it suitable for electrometer applications such as photo diode preamplifiers and picoampere current-to-voltage converters. The use of guarding techniques in printed circuit board layout and construction is critical for achieving the ultimate in low leakage performance available from AD547. The input guarding scheme shown in Figure 23 will minimize leakage as much as possible; the guard ring is connected to a low impedance potential at the same level as the inputs. High impedance signal lines should not be extended for any unnecessary length on a printed circuit; to minimize noise and leakage, they must be carried in rigid shielded cables.

OFFSET NULLING

The AD547 has low initial offset voltage to compliment its excellent drift performance. Even so, in some applications it is necessary to null out even this low offset voltage. Precision bipolar amplifiers such as the AD510 or AD OP-07 ideally have zero drift when their offset is nulled to zero, this is not the case for FET input amplifiers. A BIFET amplifier will typically exhibit a change of 3μV/°C in drift for each mV of offset voltage nulled.

In view of this fact the circuit of Figure 24 is recommended for the most critical applications. The current in the AD590 is proportional to absolute temperature. This current through the 15Ω resistor generates a small drift proportional to the setting of the null potentiometer. This drift just cancels the drift induced by nulling. This circuit will typically remove all but ±0.5μV/°C per mV of nulled offset. For best results the 15Ω resistor should be connected directly to the V− pin of the AD547. This prevents any signal from coupling into the null terminals via changing currents in the supply rails.

INPUT PROTECTION

The AD547 is guaranteed for a maximum safe input potential equal to the power supply potential. The input stage design also allows for differential input voltages of up to ±0.5 volts while maintaining the full differential input resistance of $10^{12}\,\Omega$. This makes the AD547 suitable for voltage comparators directly connected to a high impedance source.

Many instrumentation situations, such as flame detectors in gas chromatographs, involve measurement of low level currents from high-voltage sources. In such applications, a sensor fault condition may apply a very high potential to the input of the current-to-voltage converting amplifier. This possibility necessitates some form of input protection. Many electrometer type devices, especially CMOS designs, can require elaborate zener protection schemes which often compromise overall performance. The AD547 requires input protection only if the source is not current-limited and, as such, is similar to many JFET-input designs. (The failure would be due to overheating from excess current rather than voltage breakdown.) If this is the case, a resistor in series with the affected input terminal is required so that the maximum overload current is 1.0mA (for example, 100kΩ for a 100 volt overload). This simple scheme will cause no significant reduction in performance and give complete overload protection. Figure 25 shows proper connections.

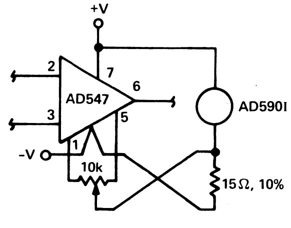


Figure 24. Offset Nulling Circuit

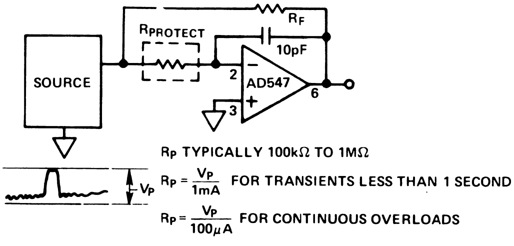
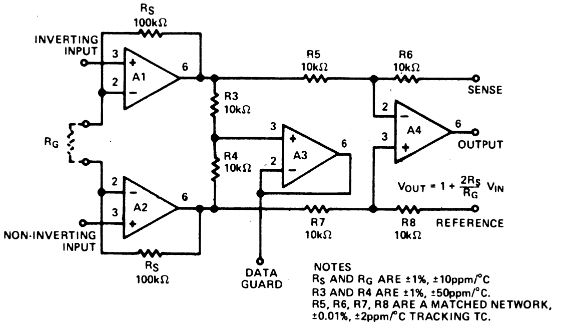

RF
RPROTECT
10pF
SOURCE
2
AD547
6
3
Rp TYPICALLY 100kΩ TO 1MΩ
Vp
Rp = Vp/1mA FOR TRANSIENTS LESS THAN 1 SECOND
Rp = Vp/100μA FOR CONTINUOUS OVERLOADS

Figure 25. Input Protection

A PRECISION INSTRUMENTATION AMPLIFIER

The instrumentation amplifier of Figure 26 utilizes the outstanding characteristics of the AD547 to provide high performance at a reasonable cost.

The low drift, low bias currents and high open loop gain provide both high accuracy and linearity. The input amplifiers A1 and A2 are AD547Ls selected for their low offset characteristics (0.25mV of offset voltage and 1µV/°C drift) and low bias currents (25pA max). The use of the AD547Ls as the input guarantees a maximum input offset voltage drift of 2µV/°C with an input offset voltage of 0.5mV max untrimmed. A3 is an AD741JH and A4 is an AD547J. These serve two unrelated but critical purposes, A4 is the output amplifier and A3 is an active data guard.



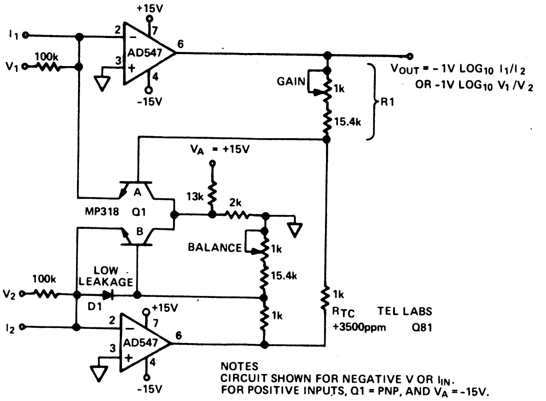
NOTES
R_S AND R_G ARE ±1%, ±10ppm/°C
R3 AND R4 ARE ±1%, ±50ppm/°C.
R5, R6, R7, R8 ARE A MATCHED NETWORK, ±0.01%, ±2ppm/°C TRACKING TC.

Figure 26. Precision FET Input Instrumentation Amplifier

USING THE AD547 IN LOG AMPLIFIER APPLICATIONS

Log amplifiers or log ratio amplifiers are useful in applications requiring compression of wide-range analog input data, linearization of transducers having exponential outputs, and analog computing, ranging from simple translation of natural relationships in log form (e.g., computing absorbance as the log-ratio of input currents), to the use of logarithms in facilitating analog computation of terms involving arbitrary exponents and multi-term products and ratios.

The picoamp level input current and low offset voltage of the AD547 make it suitable for wide dynamic range log amplifiers. Figure 27 is a schematic of a log ratio circuit employing the AD547 that can achieve less than 1% conformance error over 5 decades of current input, 1nA to 100µA. For voltage inputs, the dynamic range is typically 50mV to 10V for 1% error, limited on the low end by the amplifier's input offset voltage.



NOTES
CIRCUIT SHOWN FOR NEGATIVE V OR I_{IN}.
FOR POSITIVE INPUTS, Q1 = PNP, AND V_A = -15V.

Figure 27. Log-Ratio Amplifier

The conversion between current (or voltage) input and log output is accomplished by the base emitter junctions of the dual transistor Q1. Assuming Q1 has $\beta > 100$, which is the case for the specified transistor, the base-emitter voltage on side 1 is to a close approximation:

$$V_{BE\ A} = kT/q \ln I_1/I_{S1}$$

This circuit is arranged to take the difference of the V_{BE}'s of Q1A and Q1B, thus producing an output voltage proportional to the log of the *ratio* of the inputs:

$$V_{OUT} = -K\,(V_{BE\ A} - V_{BE\ B}) = -\frac{KkT}{q}(\ln I_1/I_{S1} - \ln I_2/I_{S2})$$

$$V_{OUT} = -K\,kT/q \ln I_1/I_2$$

The scaling constant, K is set by R1 and R_{TC} to about 16, to produce 1V change in output voltage per decade difference in input signals. R_{TC} is a special resistor with a +3500ppm/°C temperature coefficient, which makes K inversely proportional to temperature, compensating for the "T" in kT/q. The log-ratio transfer characteristic is therefore independent of temperature.

This particular log ratio circuit is free from the dynamic problems that plague many other log circuits. The -3dB bandwidth is 50kHz over the top 3 decades, 100nA to 100µA, and decreases smoothly at lower input levels. This circuit needs no additional frequency compensation for stable operation from input current sources, such as photodiodes, that may have 100pF of shunt capacitance. For larger input capacitances a 20pF integration capacitor around each amplifier will provide a smoother frequency response.

This log ratio amplifier can be readily adjusted for optimum accuracy by following this simple procedure. First, apply V1 = V2 = -10.00V and adjust "Balance" for V_{OUT} = 0.00V. Next apply V1 = -10.00V, V2 = -1.00V and adjust gain for V_{OUT} = +1.00V. Repeat this procedure until gain and balance readings are within 2mV of ideal values.

ANALOG DEVICES

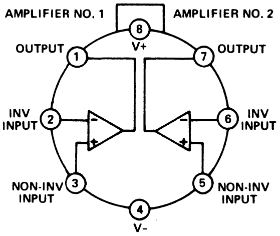
Precision Low Cost Dual BIFET Op Amp

AD642

FEATURES

Matched Offset Voltage
Matched Offset Voltage Over Temperature
Matched Bias Current
Crosstalk -124dB at 1kHz
Low Bias Current: 35pA max Warmed Up
Low Offset Voltage: 500μV max
Low Input Voltage Noise: 2μV p-p
High Open Loop Gain
Low Quiescent Current: 2.8mA max
Low Total Harmonic Distortion
Standard Dual Amplifier Pin Out

AD642 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW

PRODUCT DESCRIPTION

The AD642 is a pair of matched high speed monolithic FET-input operational amplifiers fabricated with the most advanced bipolar, JFET and laser trimming technologies. The AD642 offers matched bias currents that are significantly lower than currently available monolithic dual FET input operational amplifiers: 35pA max matched to 25pA for the AD642K and L; 75pA max, matched to 35pA for the AD642J and S. In addition, the offset voltage is laser trimmed to less than 0.5mV and matched to 0.25mV for the AD642L, 1.0mV and matched to 0.5mV for the AD642K, utilizing Analog's laser-wafer trimming (LWT) process.

The tight matching and temperature tracking between the operational amplifiers is achieved by ion-implanted JFETs and laser-wafer trimming. Ion-implantation permits the fabrication of precision, matched JFETs on a monolithic bipolar chip. This optimizes the process to produce matched bias currents which have lower initial bias currents than other popular FET input op amps. Laser-wafer trimming each amplifier's input offset voltage assures a tight initial match, this combined with superior IC processing guarantees offset voltage tracking over the temperature range.

The AD642 is recommended for applications in which excellent ac and dc performance is required. The matched amplifiers provide a low cost solution for true instrumentation amplifiers, log ratio amplifiers, and output amplifiers for four quadrant multiplying D/A converters such as the AD7541.

The AD642 is available in three versions: the "J", "K" and "L", all specified over the 0 to +70°C temperature range and one version, "S", over the -55°C to +125°C military operating temperature range. All devices are packaged in the hermetically-sealed, TO-99 metal can.

PRODUCT HIGHLIGHTS

1. The AD642 has tight matching specifications to ensure high performance, eliminating the need to match individual devices.
2. Analog Devices, unlike some manufacturers, specifies each device for the maximum bias current at either input in the warmed-up condition, thus assuring the user that the AD642 will meet its published specifications in actual use.
3. Laser-wafer-trimming reduces offset voltage to as low as 0.5mV max and matched side to side to 0.25mV (AD642L), thus eliminating the need for external nulling.
4. Low voltage noise (2μV, p-p), and high open loop gain enhance the AD642's performance as a precision op amp.
5. The standard dual amplifier pin out allows the AD642 to replace lower performance duals without redesign.

SPECIFICATIONS (typical @ +25°C and $V_S = \pm 15V$ dc unless otherwise specified)

MODEL	AD642JH	AD642KH	AD642LH	AD642SH(AD642SH/883B)[1]
OPEN LOOP GAIN				
$V_{OUT} = \pm 10V$, $R_L \geqslant 2k\Omega$	100,000 min	250,000 min	**	**
T_A = min to max	100,000 min	250,000 min	**	**
OUTPUT CHARACTERISTICS				
Voltage @ $R_L = 2k\Omega$, T_A = min to max	±10V min (±12V typ)	*	*	*
Voltage @ $R_L = 10k\Omega$, T_A = min to max	±12V min (±13V typ)	*	*	*
Short Circuit Current	25mA	*	*	*
FREQUENCY RESPONSE				
Unity Gain, Small Signal	1.0MHz	*	*	*
Full Power Response	50kHz	*	*	*
Slew Rate, Unity Gain	3.0V/µs	*	*	*
INPUT OFFSET VOLTAGE[2]	2.0mV max	1.0mV max	0.5mV max	**
$T_{min} - T_{max}$	3.5mV max	2.0mV max	1.0mV max	*
vs. Supply, T_A = min to max	200µV/V max	100µV/V max	**	**
INPUT BIAS CURRENT				
Either Input[3]	10pA, 75pA max	10pA, 35pA max	**	**
Input Offset Current	5pA	2pA	**	**
MATCHING CHARACTERISTICS[4]				
Offset Voltage	1.0mV max	0.5mV max	0.25mVmax	**
Offset Voltage $T_{min}-T_{max}$	3.5mV max	2.0mV max	1.0mV max	*
Input Bias Current	35pA max	25pA max	**	*
Crosstalk–1kHz 20V p-p	-124dB	*	*	*
INPUT IMPEDANCE				
Differential	$10^{12}\Omega \| 6pF$	*	*	*
Common Mode	$10^{12}\Omega \| 6pF$	*	*	*
INPUT VOLTAGE RANGE				
Differential[5]	±20V	*	*	*
Common Mode	±10V min (±12V typ)	*	*	*
Common Mode Rejection, $V_{IN} = \pm 10V$	76dB min	80dB min	**	**
POWER SUPPLY				
Rated Performance	±15V	*	*	*
Operating	±(5 to 18)V	*	*	*
Quiescent Current	2.8mA max	*	*	*
VOLTAGE NOISE				
0.1-10Hz	2µV p-p	*	*	*
10Hz	$70nV/\sqrt{Hz}$	*	*	*
100Hz	$45nV/\sqrt{Hz}$	*	*	*
1kHz	$30nV/\sqrt{Hz}$	*	*	*
10kHz	$25nV/\sqrt{Hz}$	*	*	*
TEMPERATURE RANGE				
Operating, Rated Performance	0 to +70°C	*	*	-55°C to +125°C
Storage	-65°C to +150°C	*	*	*
PACKAGING OPTIONS[6]				
TO-99 Style (H08B)	AD642JH	AD642KH	AD642LH	AD642SH

NOTES

[1] The AD642SH/883B is an AD642SH which is inspected and processed to the full requirements of MIL-STD-883, Level B. A complete listing of the tests is available on request.

[2] Input Offset Voltage specifications are guaranteed after 5 minutes of operation at $T_A = +25°C$.

[3] Bias current specifications are guaranteed maximum at either input after 5 minutes of operation at $T_A = +25°C$. For higher temperatures, the current doubles every 10°C.

[4] Matching is defined as the difference between parameters of the two amplifiers.

[5] Defined as the maximum safe voltage between inputs, such that neither exceeds ±10V from ground.

[6] See Section 20 for package outline information.

*Specifications same as AD642JH.

**Specifications same as AD642KH.

Specifications subject to change without notice.

Typical Characteristics

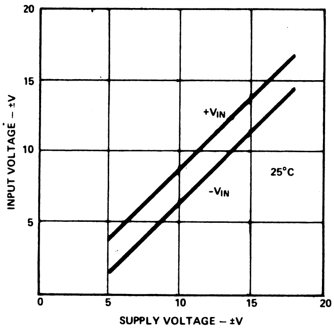


Figure 1. Input Voltage Range vs. Supply Voltage

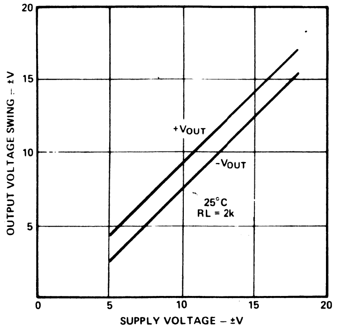


Figure 2. Output Voltage Swing vs. Supply Voltage

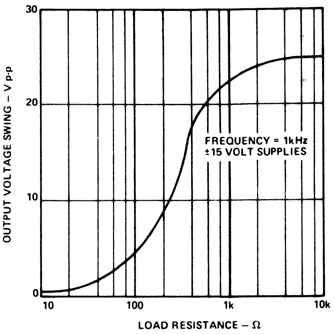


Figure 3. Output Voltage Swing vs. Resistive Load

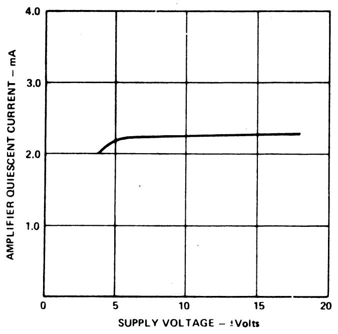


Figure 4. Quiescent Current vs. Supply Voltage

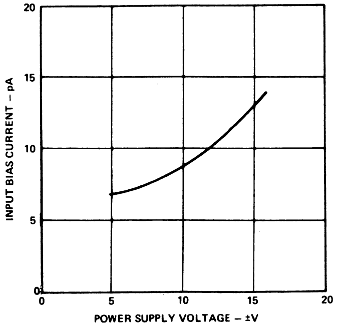


Figure 5. Input Bias Current vs. Supply Voltage

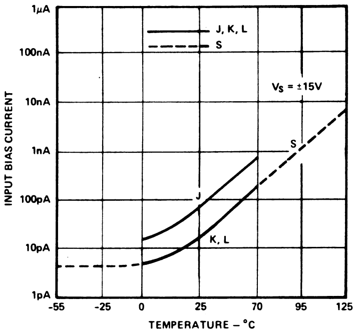


Figure 6. Input Bias Current vs. Temperature

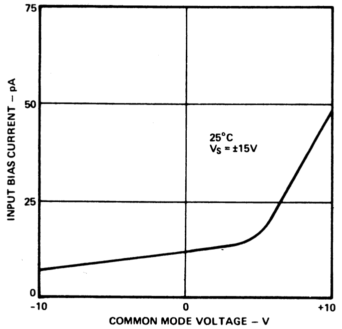


Figure 7. Input Bias Current vs. CMV

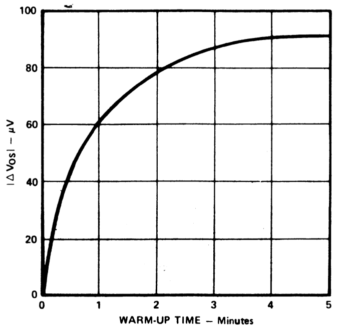


Figure 8. Input Offset Voltage Turn On Drift vs. Time

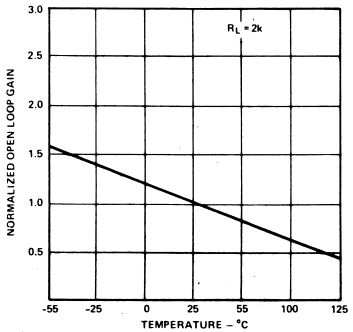


Figure 9. Open Loop Gain vs. Temperature

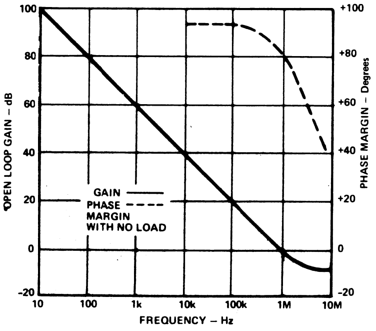


Figure 10. Open Loop Frequency Response

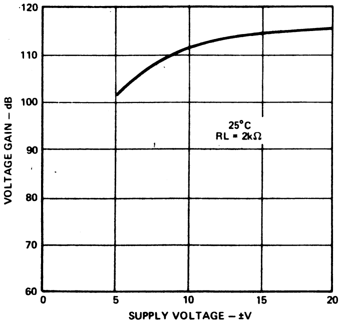


Figure 11. Open Loop Voltage Gain vs. Supply Voltage

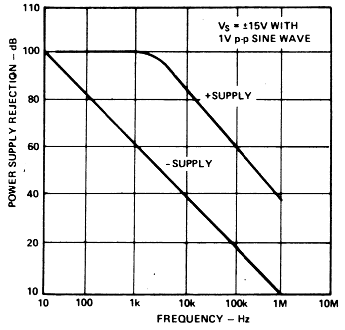


Figure 12. Power Supply Rejection vs. Frequency

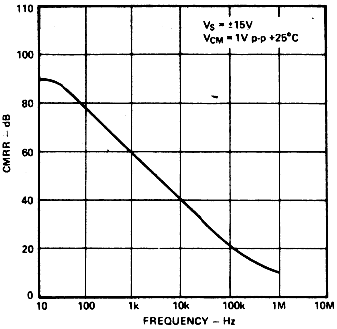


Figure 13. Common Mode Rejection vs. Frequency

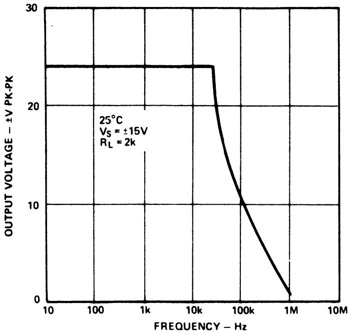


Figure 14. Large Signal Frequency Response

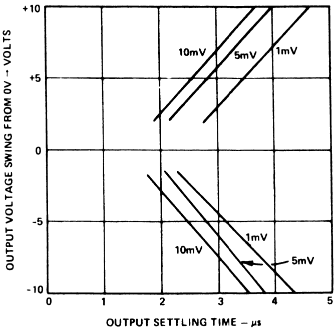


Figure 15. Output Settling Time vs. Output Swing and Error (Circuit of Figure 23)

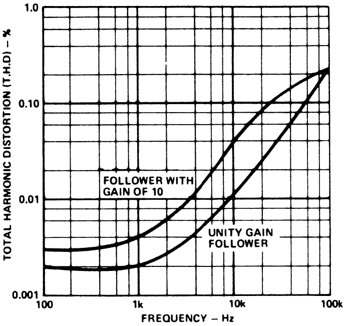


Figure 16. Total Harmonic Distortion vs. Frequency

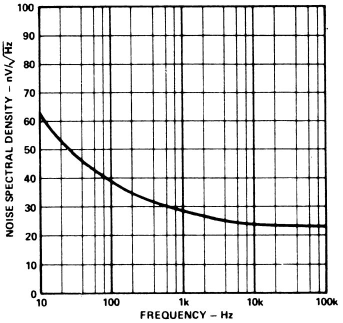


Figure 17. Input Noise Voltage Spectral Density

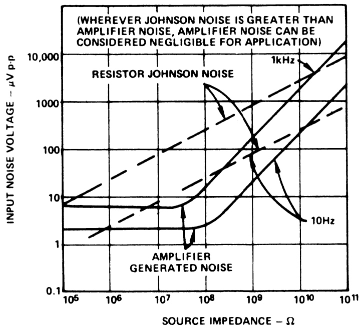
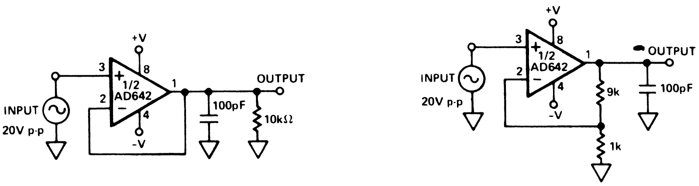


Figure 18. Total Noise vs. Source Resistance



a. Unity Gain Follower *b. Follower with Gain = 10*

Figure 19. T.H.D. Test Circuits

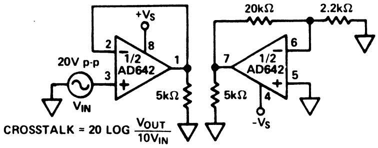


Figure 20. Crosstalk Test Circuit

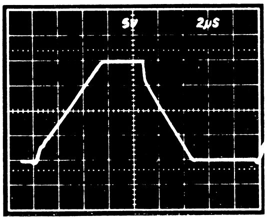


Figure 21a. Unity Gain Follower Pulse Response (Large Signal)

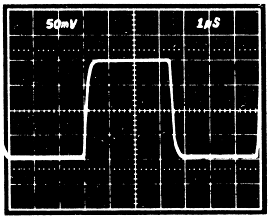


Figure 21b. Unity Gain Follower Pulse Response (Small Signal)

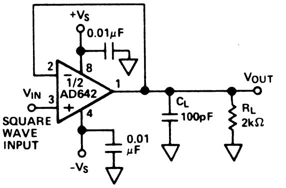


Figure 21c. Unity Gain Follower

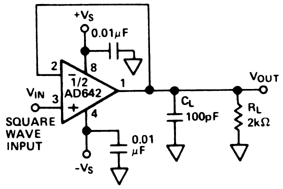


Figure 22a. Unity Gain Inverter

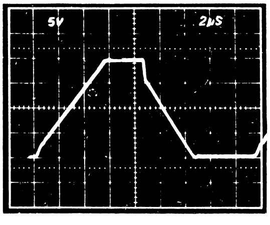


Figure 22b. Unity Gain Inverter Pulse Response (Large Signal)

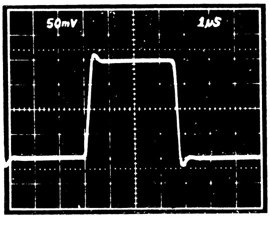


Figure 22c. Unity Gain Inverter Pulse Response (Small Signal)

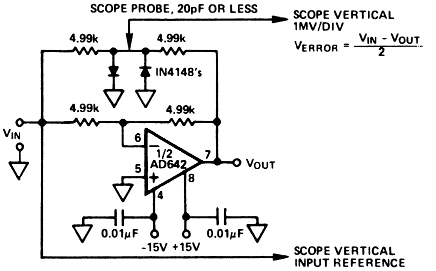

SCOPE PROBE, 20pF OR LESS
SCOPE VERTICAL 1MV/DIV
$V_{ERROR} = \frac{V_{IN} - V_{OUT}}{2}$
4.99k
4.99k
IN4148's
4.99k
4.99k
VIN
1/2 AD642
VOUT
0.01μF
0.01μF
-15V +15V
SCOPE VERTICAL INPUT REFERENCE

Figure 23. Settling Time Test Circuit

Fast settling time (8μs to 0.01% for 20V p-p step), low power and low offset voltage make the AD642 an excellent choice for use as an output amplifier for current output D/A converters such as the AD7541.

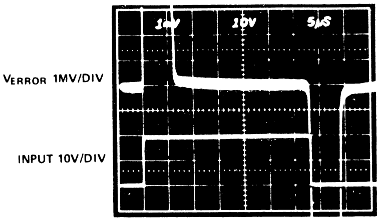


Figure 24. Settling Characteristic Detail

The upper trace of the oscilloscope photograph of Figure 24 shows the settling characteristic of the AD642. The lower trace represents the input to Figure 23. The AD642 has been designed for fast settling to 0.01%, however, feedback components, circuit layout and circuit design must be carefully considered to obtain optimum settling time.

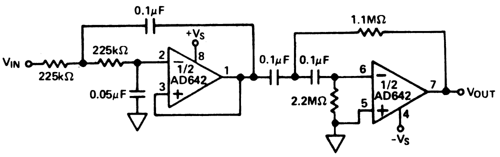
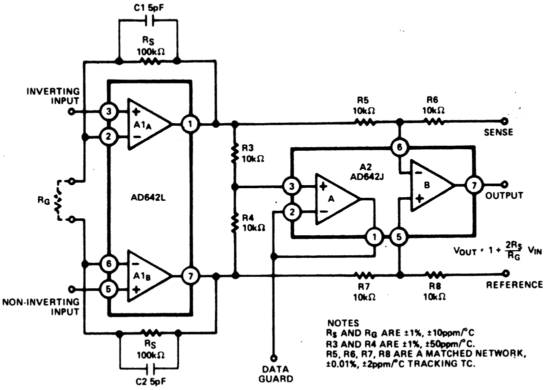


Figure 25. 0.1Hz to 10Hz Band Pass Filter

The low frequency (1/f) noise has a power spectrum that is inversely proportional to frequency. Typically this noise is not important above 10Hz, but it can be important for low frequency-high gain applications.

The low noise characteristics of the AD642 make it ideal for 1/f noise testing circuits. The circuit of Figure 25 is a 0.1Hz to 10Hz bandpass filter with second order filter characteristics.

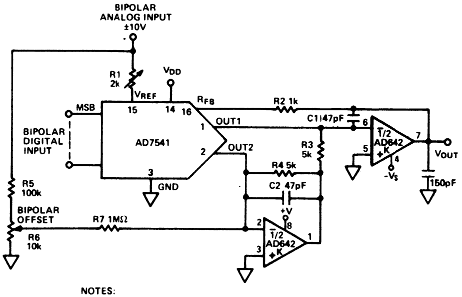
The circuit illustrated in Figure 26 uses two AD642s to construct an instrumentation amplifier with low input current (35pA max), high linearity and low offset voltage and offset voltage drift. The AD644 may be substituted for increased speed, but the higher open-loop gain of the AD642 maintains better linearity over the gain range of 1 to 1000. Amplifier A1 is an AD642L for low input offset voltage (250μV max) and low input offset voltage drift at high gains because matching and tracking are very important for the balanced input stage. Amplifier A2 serves two nonrelated functions, output amplifier and active data-guard drive, and does not require close matching between sections; thus it may be an AD642J.



NOTES
R_S AND R_G ARE ±1%, ±10ppm/°C
R3 AND R4 ARE ±1%, ±50ppm/°C.
R5, R6, R7, R8 ARE A MATCHED NETWORK, ±0.01%, ±2ppm/°C TRACKING TC.

Figure 26. Precision FET Input Instrumentation Amplifier

The output impedance of a CMOS DAC varies with the digital word thus changing the noise of the amplifier circuit. This effect will cause a nonlinearity whose magnitude is dependent on the offset voltage of the amplifier. The AD642K with trimmed offset will minimize the effect. The Schottky protection diodes recommended for use with many older CMOS DACs are not required when using the AD642.



NOTES:
1. R3/R4 MATCH 0.05% OR BETTER.
2. R1, R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED

Figure 27a. AD642 Used as DAC Output Amplifier

Figure 27a illustrates the AD7541 12-bit digital-to-analog converter, connected for bipolar operation. Since the digital input can accept bipolar numbers and V_{REF} can accept a bipolar analog input, the circuit can perform a 4-quadrant multiplication.

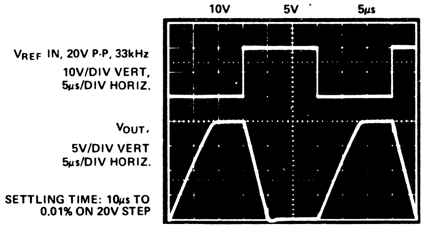
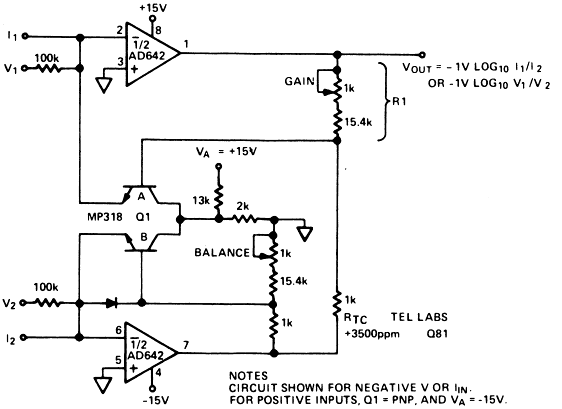


Figure 27b. Voltage Output DAC Settling Characteristic

The photo above shows the output of the circuit of Figure 27a. The upper trace represents the reference input, and the bottom trace shows the output voltage for a digital input of all ones on the DAC. The 47pF capacitor across the feedback resistor compensates for the DAC output capacitance, and the 150pF load capacitor serves to minimize output glitches.

Low amplifiers or log ratio amplifiers are useful in applications requiring compression of wide-range analog input data, linearization of transducers having exponential outputs, and analog computing, ranging from simple translation of natural relationships in log form (e.g., computing absorbance as the log-ratio of input currents), to the use of logarithms in facilitating analog computation of terms involving arbitrary exponents and multi-term products and ratios.

The picoamp level input current and low offset voltage of the AD642 make it suitable for wide dynamic range log amplifiers. Figure 28 is a schematic of a log ratio circuit employing the AD642 that can achieve less than 1% conformance error over 5 decades of current input, 1nA to 100µA. For voltage inputs, the dynamic range is typically 50mV to 10V for 1% error, limited on the low end by the amplifiers' input offset voltage.



NOTES
CIRCUIT SHOWN FOR NEGATIVE V OR I_{IN}.
FOR POSITIVE INPUTS, Q1 = PNP, AND V_A = -15V.

Figure 28. Log-Ratio Amplifier

The conversion between current (or voltage) input and log output is accomplished by the base emitter junctions of the dual transistor Q1. Assuming Q1 has $\beta > 100$, which is the case for the specified transistor, the base-emitter voltage on side 1 is to a close approximation:

$$V_{BE\ A} = kT/q \ln I_1/I_{S1}$$

This circuit is arranged to take the difference of the V_{BE}'s of Q1A and Q1B, thus producing an output voltage proportional to the log of the *ratio* of the inputs:

$$V_{OUT} = -K(V_{BE\ A} - V_{BE\ B}) = -\frac{KkT}{q}(\ln I_1/I_{S1} - \ln I_2/I_{S2})$$

$$V_{OUT} = -K\,kT/q \ln I_1/I_2$$

The scaling constant, K is set by R1 and R_{TC} to about 16, to produce 1V change in output voltage per decade difference in input signals. R_{TC} is a special resistor with a +3500ppm/°C temperature coefficient, which makes K inversely proportional to temperature, compensating for the "T" in kT/q. The log-ratio transfer characteristic is therefore independent of temperature.

This particular log ratio circuit is free from the dynamic problems that plague many other log circuits. The -3dB bandwidth is 50kHz over the top 3 decades, 100nA to 100µA, and decreases smoothly at lower input levels. This circuit needs no additional frequency compensation for stable operation from input current sources, such as photodiodes, that may have 100pF of shunt capacitance. For larger input capacitances a 20pF integration capacitor around each amplifier will provide a smoother frequency response.

This log ratio amplifier can be readily adjusted for optimum accuracy by following this simple procedure. First, apply V1 = V2 = -10.00V and adjust "Balance" for V_{OUT} = 0.00V. Next apply V1 = -10.00V, V2 = -1.00V and adjust gain for V_{OUT} = +1.00V. Repeat this procedure until gain and balance readings are within 2mV of ideal values.

The low input bias current (35pA) and low noise characteristics of the AD642 make it suitable for electrometer applications such as photo diode preamplifiers and picoampere current-to-voltage converters. The use of guarding techniques in printed circuit board layout and construction is critical for achieving the ultimate in low leakage performance that the AD642 can deliver. The input guarding scheme shown in Figure 29 will minimize leakage as much as possible; the guard ring should be applied to both sides of the board. The guard ring is connected to a low impedance potential at the same level as the inputs. High impedance signal lines should not be extended for any unnecessary length on a printed circuit; to minimize noise and leakage, they must be carried in rigid shielded cables.

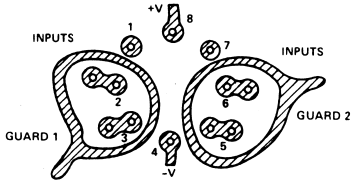
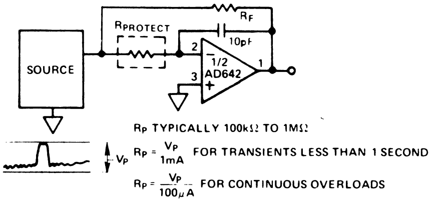


Figure 29. Board Layout for Guarding Inputs

INPUT PROTECTION

The AD642 is guaranteed for a maximum safe input potential equal to the power supply potential. The input stage design also allows differential input voltages of up to ±0.5 volts while maintaining the full differential input resistance of $10^{12}\Omega$. This makes the AD642 suitable for low speed voltage comparators directly connected to a high impedance source.

Many instrumentation situations, such as flame detectors in gas chromatographs, involve measurement of low level currents from high-voltage sources. In such applications, a sensor fault condition may apply a very high potential to the input of the current-to-voltage converting amplifier. This possibility necessitates some form of input protection. Many electrometer type devices, especially CMOS designs, can require elaborate zener protection schemes which often compromise overall performance. The AD642 requires input protection only if the source is not current-limited, and as such is similar to many JFET-input designs. The failure mode would be overheating from excess current rather than voltage breakdown. If the source is not current-limited, all that is required is a resistor in series with the affected input terminal so that the maximum overload current is 1.0mA (for example, 100kΩ for a 100 volt overload). This simple scheme will cause no significant reduction in performance and give complete overload protection. Figure 30 shows proper connections.



R_P TYPICALLY 100kΩ TO 1MΩ

$R_P = \frac{V_P}{1mA}$ FOR TRANSIENTS LESS THAN 1 SECOND

$R_P = \frac{V_P}{100\mu A}$ FOR CONTINUOUS OVERLOADS

Figure 30. AD642 Input Protection

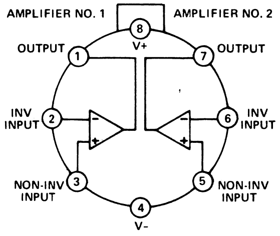
ANALOG DEVICES

Dual High Speed Implanted FET-Input Op Amp

AD644

FEATURES
- Matched Offset Voltage
- Matched Offset Voltage Over Temperature
- Matched Bias Currents
- Crosstalk -124dB at 1kHz
- Low Bias Current: 35pA max Warmed Up
- Low Offset Voltage: 500μV max
- Low Input Voltage Noise: 2μV p-p
- High Slew Rate: 13V/μs
- Low Quiescent Current: 4.5mA max
- Fast Settling to ±0.01%: 3μs
- Low Total Harmonic Distortion: 0.0015% at 1kHz
- Standard Dual Amplifier Pin Out

AD644 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW

PRODUCT DESCRIPTION

The AD644 is a pair of matched high speed monolithic FET-input operational amplifiers fabricated with the most advanced bipolar, JFET and laser trimming technologies. The AD644 offers matched bias currents that are significantly lower than currently available monolithic dual FET input operational amplifiers: 35pA max, matched to 25pA for the AD644K and L, 75pA max matched to 35pA for the AD644J and S. In addition, the offset voltage is laser trimmed to less than 0.5mV, and matched to 0.25mV for the AD644L, 1.0mV and matched to 0.5mV for the AD644K, utilizing Analog Devices' laser-wafer trimming (LWT) process.

The tight matching and temperature tracking between the operational amplifiers is achieved by ion-implanted JFETs and laser-wafer trimming. Ion-implantation permits the fabrication of precision, matched JFETs on a monolithic bipolar chip. This process optimizes the ability to produce matched amplifiers which have lower initial bias currents than other popular FET input op amps. Laser-wafer trimming each amplifier's input offset voltage assures tight initial match and superior IC processing guarantees offset voltage tracking over the temperature range.

The AD644 is recommended for applications in which both excellent ac and dc performance is required. The matched amplifiers provide a low cost solution to true wideband instrumentation amplifiers, low dc drift active filters and output amplifiers for four quadrant multiplying D/A converters such as the AD7541, 12-bit CMOS DAC.

The AD644 is available in four versions: the "J", "K" and "L" are specified over the 0 to +70°C temperature range and the "S" over the -55°C to +125°C operating temperature range. All devices are packaged in the hermetically-sealed, TO-99 metal can.

PRODUCT HIGHLIGHTS

1. The AD644 has tight side to side matching specifications to ensure high performance without matching individual devices.
2. Analog Devices, unlike some manufacturers, specifies each device for the maximum bias current at either input in the warmed-up condition, thus assuring the user that the AD644 will meet its published specifications in actual use.
3. Laser-wafer-trimming reduces offset voltage to as low as 0.5mV max matched side to side to 0.25mV (AD644L), thus eliminating the need for external nulling.
4. Improved bipolar and JFET processing on the AD644 result in the lowest matched bias current available in a high speed monolithic FET op amp.
5. Low voltage noise (2μV p-p) and high open loop gain enhance the AD644's performance as a precision op amp.
6. The high slew rate (13.0V/μs) and fast settling time to 0.01% (3.0μs) make the AD644 ideal for D/A, A/D, sample-hold circuits and dual high speed integrators.
7. Low harmonic distortion (0.0015%) and low crosstalk (-124dB) make the AD644 an ideal choice for stereo audio applications.
8. The standard dual amplifier pin out allows the AD644 to replace lower performance duals without redesign.

SPECIFICATIONS (typical @ +25°C and $V_S = \pm 15V$ dc unless otherwise specified)

MODEL	AD644J	AD644K	AD644L	AD644S (AD644S/883B)[1]
OPEN LOOP GAIN				
$V_{OUT} = \pm 10V$, $R_L \geqslant 2k\Omega$	30,000 min	50,000 min	**	**
T_A = min to max, $R_L = 2k\Omega$	20,000 min	40,000 min	**	*
OUTPUT CHARACTERISTICS				
Voltage @ $R_L = 2k\Omega$, T_A = min to max	±10V min (±12V typ)	*	*	*
Voltage @ $R_L = 10k\Omega$, T_A = min to max	±12V min (±13V typ)	*	*	*
Short Circuit Current	25mA	*	*	*
FREQUENCY RESPONSE				
Unity Gain, Small Signal	2.0MHz	*	*	*
Full Power Response	200kHz	*	*	*
Slew Rate, Unity Gain	13.0V/μs (8.0V/μs min)	*	*	*
Total Harmonic Distortion, f = 1kHz	0.0015%	*	*	*
INPUT OFFSET VOLTAGE[2]	2.0mV max	1.0mV max	0.5mV max	**
Input Offset Voltage $T_{min}-T_{max}$	3.5mV max	2.0mV max	1.0mV max	*
vs. Supply, T_A = min to max	200μV/V max	100μV/V max	**	**
INPUT BIAS CURRENT				
Either Input[3]	10pA (75pA max)	10pA (35pA max)	**	**
Input Offset Current	10pA	5pA	**	**
MATCHING CHARACTERISTICS[4]				
Input Offset Voltage	1.0mV max	0.5mV max	0.25mV max	**
Input Offset Voltage $T_{min}-T_{max}$	3.5mV max	2.0mV max	1.0mV max	*
Input Bias Current	35pA max	25pA max	**	*
Crosstalk	-124dB	*	*	*
INPUT IMPEDANCE				
Differential	$10^{12}\Omega \| 6pF$	*	*	*
Common Mode	$10^{12}\Omega \| 3pF$	*	*	*
INPUT VOLTAGE RANGE				
Differential[5]	±20V	*	*	*
Common Mode	±12V (±10V min)	*	*	*
Common Mode Rejection, $V_{IN} = \pm 10V$	76dB min	80dB min	**	**
POWER SUPPLY				
Rated Performance	±15V	*	*	*
Operating	±(5 to 18)V	*	*	*
Quiescent Current	3.5mA (4.5mA max)	*	*	*
VOLTAGE NOISE				
0.1-10Hz	2μV p-p	*	*	*
10Hz	$35nV/\sqrt{Hz}$	*	*	*
100Hz	$22nV/\sqrt{Hz}$	*	*	*
1kHz	$18nV/\sqrt{Hz}$	*	*	*
10kHz	$16nV/\sqrt{Hz}$	*	*	*
TEMPERATURE RANGE				
Operating, Rated Performance	0 to +70°C	*	*	-55°C to +125°C
Storage	-65°C to +150°C	*	*	*
PACKAGING OPTIONS[6]:				
TO-99 Style (HO8B)	AD644JH	AD644KH	AD644LH	AD644SH

NOTES

[1] The AD644S/883B is an AD644S which is inspected and processed to the requirements of MIL-STD-883, Level B. A complete listing of the tests is available on request.

[2] Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[3] Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

[4] Matching is defined as the difference between parameters of the two amplifiers.

[5] Defined as voltage between inputs, such that neither exceeds ±10V from ground.

[6] See Section 20 for package outline information.

*Specifications same as AD644J.

**Specifications same as AD644K.

Specifications subject to change without notice.

Typical Characteristics

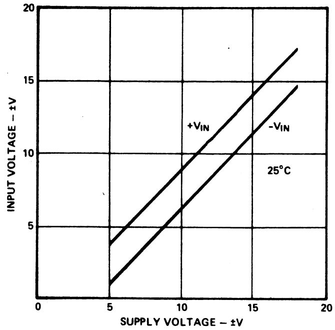


Figure 1. Input Voltage Range vs. Supply Voltage

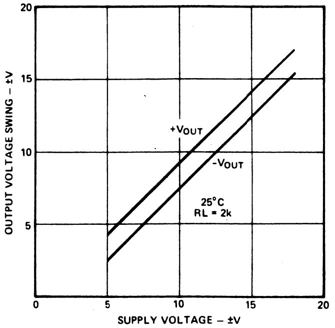


Figure 2. Output Voltage Swing vs. Supply Voltage

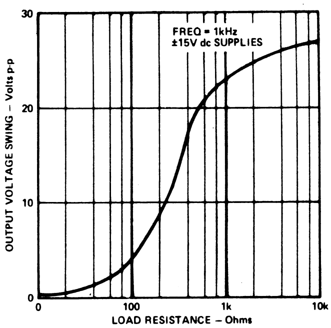


Figure 3. Output Voltage Swing vs. Resistive Load

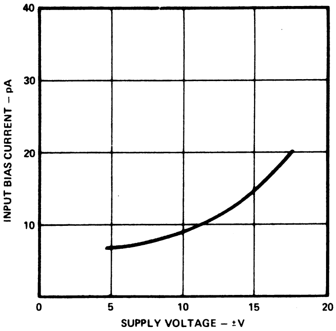


Figure 4. Input Bias Current vs. Supply Voltage

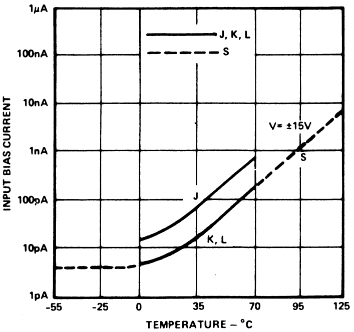


Figure 5. Input Bias Current vs. Temperature

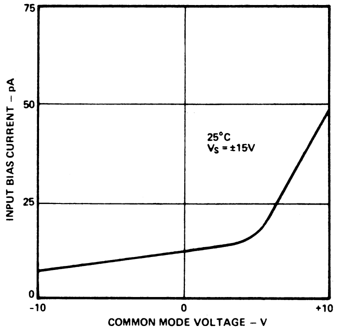


Figure 6. Input Bias Current vs. CMV

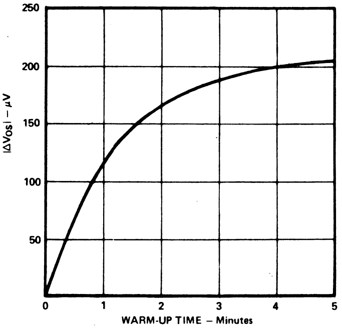


Figure 7. Change in Offset Voltage vs. Warm-Up Time

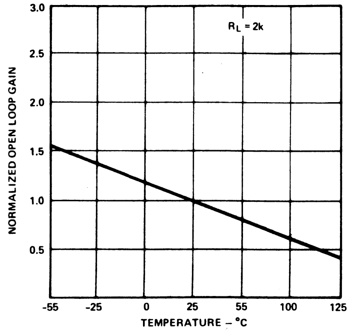


Figure 8. Open Loop Gain vs. Temperature

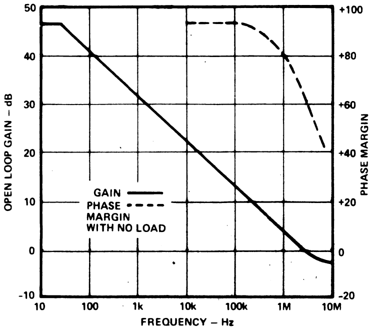


Figure 9. Open Loop Frequency Response

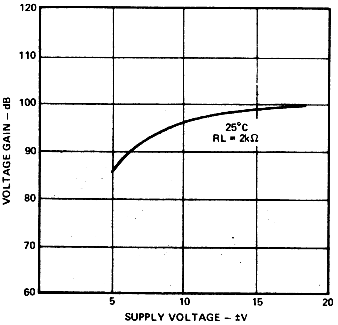


Figure 10. Open Loop Voltage Gain vs. Supply Voltage

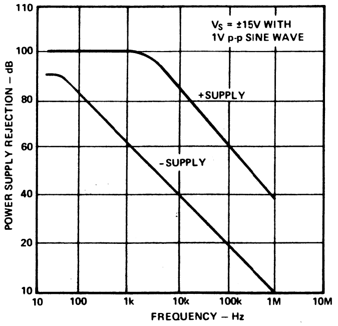


Figure 11. Power Supply Rejection vs. Frequency

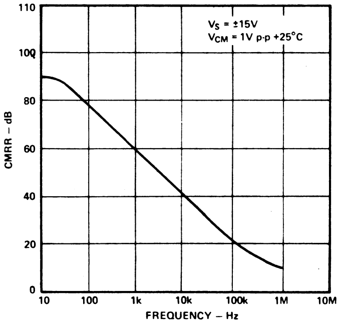


Figure 12. Common Mode Rejection Ratio vs. Frequency

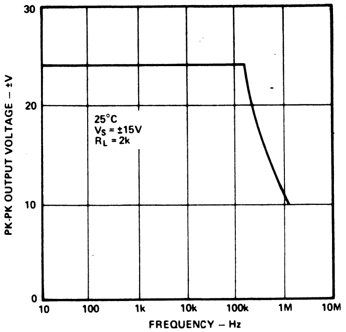


Figure 13. Large Signal Frequency Response

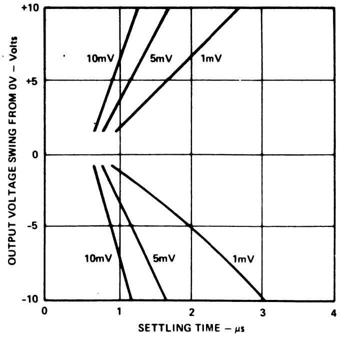


Figure 14. Output Settling Time vs. Output Swing and Error (Circuit of Figure 23a)

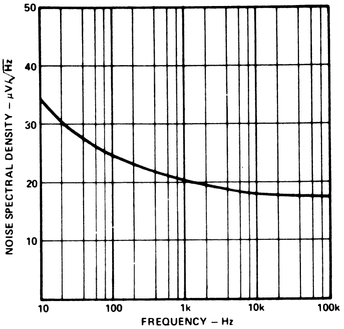


Figure 15. Noise Spectral Density

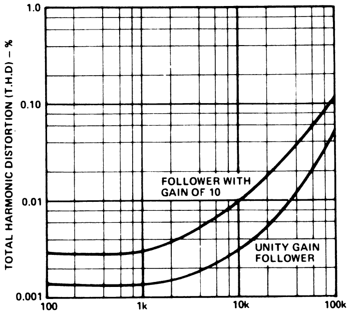


Figure 16. Total Harmonic Distortion vs. Frequency

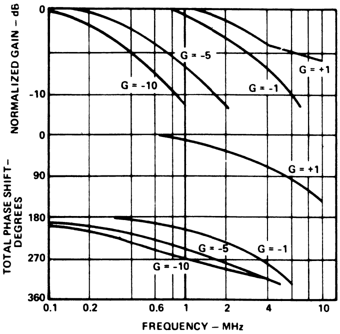


Figure 17. Closed Loop Gain & Phase vs. Frequency

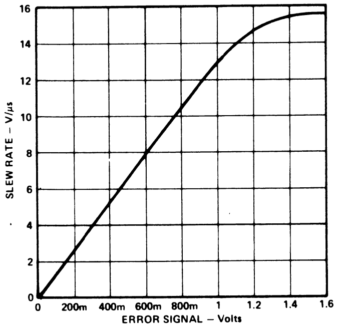
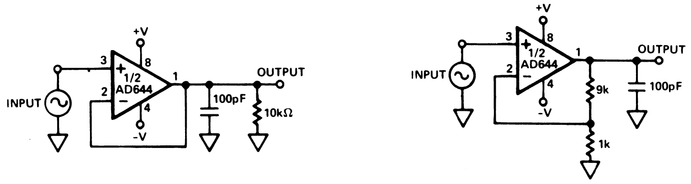


Figure 18. Slew Rate vs. Error Signal



a. Unity Gain Follower

b. Follower with Gain = 10

Figure 19. T.H.D. Test Circuits

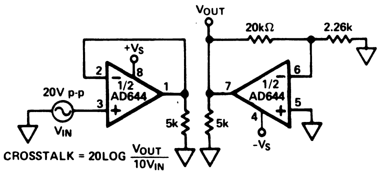


Figure 20. Crosstalk Test Circuit

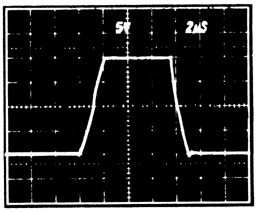


Figure 21a. Unity Gain Follower Pulse Response (Large Signal)

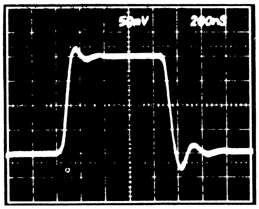


Figure 21b. Unity Gain Follower Pulse Response (Small Signal)

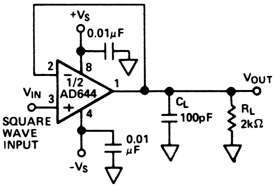


Figure 21c. Unity Gain Follower

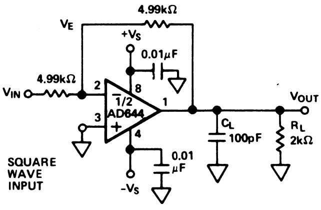


Figure 22a. Unity Gain Inverter

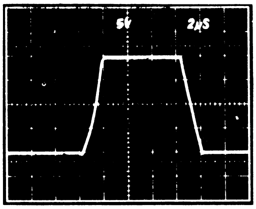


Figure 22b. Unity Gain Inverter Pulse Response (Large Signal)

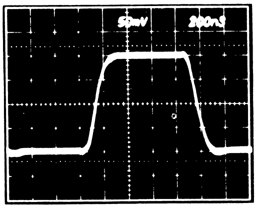


Figure 22c. Unity Gain Inverter Pulse Response (Small Signal)

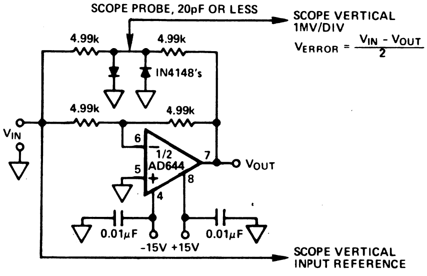


Figure 23a. Settling Time Test Circuit

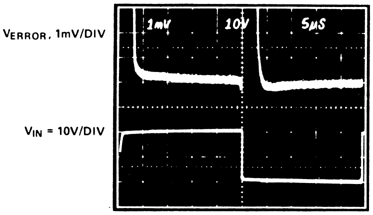
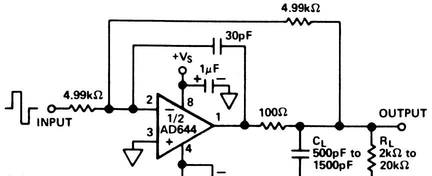


Figure 23b. Settling Characteristic Detail

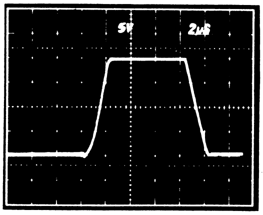
The fast settling time (3.0µs to 0.01% for 20V p-p step) and low offset voltage make the AD644 an excellent choice as an output amplifier for current output D/A converters such as the AD7541. The upper trace of the oscilloscope photograph of Figure 23b shows the settling characteristics of the AD644. The lower trace represents the input to Figure 23a. The AD644 has been designed for fast settling to 0.01%, however, feedback components, circuit layout and circuit design must be carefully considered to obtain the optimum settling time.



TYPICAL CAPACITANCE LIMIT FOR VARIOUS LOAD RESISTORS

R_L		C_L UP TO
2kΩ	→	1500pF
10kΩ	→	600pF
20kΩ	→	500pF

Figure 24. Circuit for Driving a Large Capacitive Load



Transient Response $R_L = 2k\Omega$ $C_L = 500pF$

The circuit in Figure 24 employs a 100Ω isolation resistor which enables the amplifier to drive capacitive loads exceeding 500pF; the resistor effectively isolates the high frequency feedback from the load and stabilizes the circuit. Low frequency feedback is returned to the amplifier summing junction via the low pass filter formed by the 100Ω series resistor and the load capacitance, C_L.

The low input bias current (35pA), low noise, high slew rate and high bandwidth characteristics of the AD644 make it suitable for electrometer applications such as photodiode preamplifiers and picoampere current-to-voltage converters. The use of guarding techniques in printed circuit board layout and construction is critical for achieving the ultimate in low leakage performance that the AD644 can deliver. The input guarding scheme shown in Figure 25 will minimize leakage as much as possible. The same layout should be used on both sides of a double side board. The guard ring is connected to a low impedance potential at the same level as the inputs. High impedance signal lines should not be extended for any unnecessary length on a printed circuit; to minimize noise and leakage, such conductors should be replaced by rigid shielded cables.

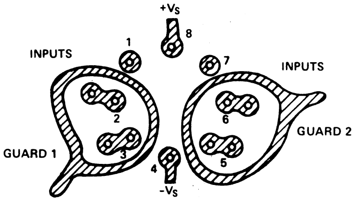
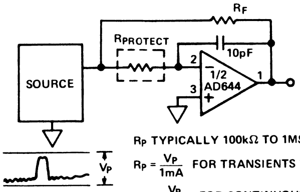


Figure 25. Board Layout for Guarding Inputs

INPUT PROTECTION

The AD644 is guaranteed for a maximum safe input potential equal to the power supply potential. The input stage design also allows differential input voltages of up to ±1 volt while maintaining the full differential input resistance of $10^{12}\,\Omega$. This makes the AD644 suitable for comparator situations employing a direct connection to high impedance source.

Many instrumentation situations, such as flame detectors in gas chromatographs, involve measurement of low level currents from high-voltage sources. In such applications, a sensor fault condition may apply a very high potential to the input of the current-to-voltage converting amplifier. This possibility necessitates some form of input protection. Many electrometer type devices, especially CMOS designs, can require elaborate zener protection schemes which often compromise overall performance. The AD644 requires input protection only if the source is not current-limited, and as such is similar to many JFET-input designs. The failure mode would be overheating from excess current rather than voltage breakdown. If the source is not current-limited, all that is required is a resistor in series with the affected input terminal so that the maximum overload current is 1.0mA (for example, 100kΩ for a 100 volt overload). This simple scheme will cause no significant reduction in performance and give complete overload protection. Figure 26 shows proper connections.

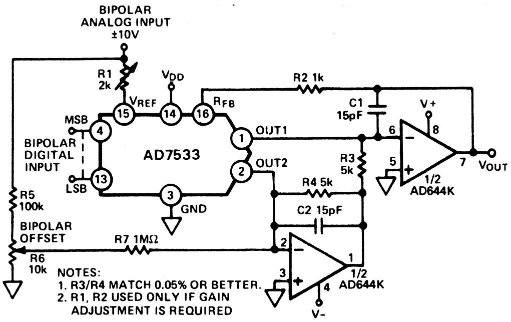


R_P TYPICALLY 100kΩ TO 1MΩ

$R_P = \frac{V_P}{1mA}$ FOR TRANSIENTS LESS THAN 1 SECOND

$R_P = \frac{V_P}{100\mu A}$ FOR CONTINUOUS OVER LOADS

Figure 26. AD644 Input Protection



NOTES:
1. R3/R4 MATCH 0.05% OR BETTER.
2. R1, R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED

Figure 27a. AD644 Used as DAC Output Amplifiers

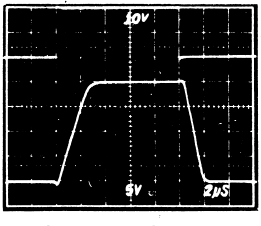


Figure 27b. Large Signal Response

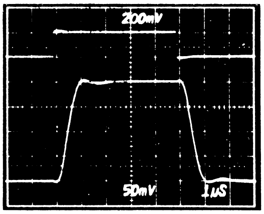


Figure 27c. Small Signal Response

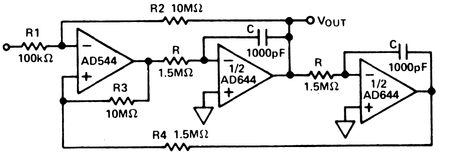
Figure 27a illustrates the 10-bit digital-to-analog converter, AD7533, connected for bipolar operation. Since the digital input can accept bipolar numbers and V_{REF} can accept a bipolar analog input, the circuit can perform a 4-quadrant multiplying function. The photos exhibit the response to a step input at V_{REF}. Figure 27b is the large signal response and Figure 27c is the small signal response.

The output impedance of a CMOS DAC varies with the digital word thus changing the noise gain of the amplifier circuit. The effect will cause a nonlinearity the magnitude of which is dependent on the offset voltage of the amplifier. The AD644K with trimmed offset will minimize the effect. The Schottky protection diodes recommended for use with many older CMOS DACs are not required when using the AD644.

ACTIVE FILTERS

Literature on active filter techniques and characteristics based on operational amplifiers is readily available. The successful application of an active filter however, depends on the component selection to achieve the desired performance. The AD644 is recommended for filters in medical, instrumentation, data acquisition and audio applications, because of its high gain bandwidth figure, symmetrical slewing, low noise, and low offset voltage.

The state variable filter (Figure 28) is stable, easily tuned and is independent of circuit Q and gain. The use of the AD644 with its low input bias current simplifies the resistor (R3, R4) selection for the passband center frequency, circuit Q and voltage gain.



f_o = CENTER FREQUENCY = $1/2\pi R_C$

Q_o = QUALITY FACTOR = $\frac{R_1 + R_2}{2R_1}$

H_o = GAIN AT RESONANCE = R_2/R_1

$R_3 = R_4 \approx 10^8/f_o$

Qo, IS ADJUSTABLE BY VARYING R2

fo, IS ADJUSTABLE BY VARYING R OR C

Figure 28. Band Pass State Variable Filter

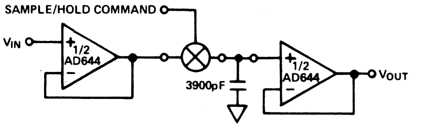
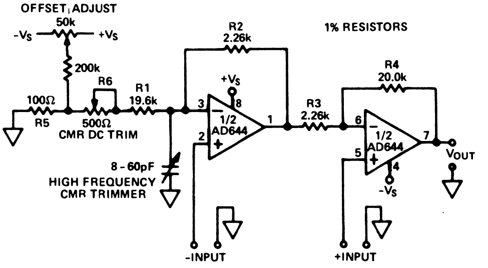


Figure 29. Sample and Hold Circuit

The sample and hold circuit, shown in Figure 29 is suitable for use with 8-bit A/D converters. The acquisition time using a 3900pF capacitor and fast CMOS SPST (ADG200) switch is 15μs.

The droop rate is very low 25×10^{-9} V/μs due to the low input bias currents of the AD644. Care should be taken to minimize leakage paths. Leakages around the hold capacitor will increase the droop rate and degrade performance.



$\text{GAIN} = 1 + \frac{R_4}{R_3}$ $\quad R_2 = R_3$, $R_4 = R_1 + R_5 + R_6$ $\quad \text{GAIN} = \frac{V_O}{(+V_{IN} - (-V_{IN})}$

INSTRUMENTATION AMPLIFIER WITH GAIN OF TEN

Figure 30. Wide Bandwidth Instrumentation Amplifier

The AD644 in the circuit of Figure 30 provides highly accurate signal conditioning with high frequency input signals. It provides an offset voltage drift of 10μV/°C, CMRR of 80dB over the range of dc to 10kHz and a bandwidth of 200kHz (-3dB) at 20V p-p output. The circuit of Figure 30 can be configured for a gain range of 1 to 1000 with a typical nonlinearity of 0.01% at a gain of 10.

ANALOG DEVICES

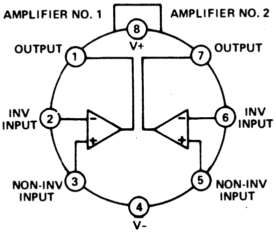
Ultra-Low Drift Dual BIFET Op Amp

AD647

FEATURES

- Low Offset Voltage Drift
- Matched Offset Voltage
- Matched Offset Voltage Over Temperature
- Matched Bias Current
- Crosstalk -124dB at 1kHz
- Low Bias Current: 35pA max Warmed Up
- Low Offset Voltage: 250μV max
- Low Input Voltage Noise: 2μV p-p
- High Open Loop Gain: 108dB
- Low Quiescent Current: 2.8mA max
- Low Total Harmonic Distortion
- Standard Dual Amplifier Pin Out

AD647 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW

PRODUCT DESCRIPTION

The AD647 is an ultra low drift dual JFET amplifier that combines high performance and convenience in a single package.

The AD647 uses the most advanced ion-implantation and laser wafer drift trimming technologies to achieve the highest performance currently available in a dual JFET. Ion-implantation permits the fabrication of matched JFETs on a monolithic bipolar chip. Laser wafer drift trimming trims both the initial offset voltage and its drift with temperature to provide offsets as low as 100μV (250μV max) and drifts of 2.5μV/°C max.

In addition to outstanding individual amplifier performance, the AD647 offers guaranteed and tested matching performance on critical parameters such as offset voltage, offset voltage drift and bias currents.

This high level of performance makes the AD647 especially well suited for high precision instrumentation amplifier applications that previously would have required the costly selection and matching of space wasting single amplifiers.

The AD647 also offers high levels of performance for Digital to Analog Converter output amplifiers, and filtering applications.

The AD647 is offered in four performance grades, three commercial (the J, K, and L) and one military (the S). All are supplied in hermetically sealed 8-pin TO-99 packages.

PRODUCT HIGHLIGHTS

1. The AD647 is guaranteed and tested to tight matching specifications to ensure high performance and to eliminate the selection and matching of single devices.
2. Laser wafer drift trimming reduces offset voltage and offset voltage drifts to 250μV and 2.5μV/°C max.
3. Voltage noise is guaranteed at 4μV p-p max (0.1 to 10Hz) on K, L and S grades.
4. Bias current (35pA K, L, S; 75pA J) is specified after five minutes of operation.
5. Total supply current is a low 2.8mA max.
6. High open loop gain ensures high linearity in precision instrumentation amplifier applications.
7. The standard dual amplifier pin out permits the direct substitution of the AD647 for lower performance devices.

SPECIFICATIONS (typical @ +25°C and V_S = ±15V dc unless otherwise specified)

MODEL	AD647JH	AD647KH	AD647LH	AD647SH(AD647SH/883B)[1]
OPEN LOOP GAIN				
$V_{OUT} = \pm 10V$, $R_L \geqslant 2k\Omega$	100,000 min	250,000 min	**	**
T_A = min to max	100,000 min	250,000 min	**	**
OUTPUT CHARACTERISTICS				
Voltage @ $R_L = 2k\Omega$, T_A = min to max	±10V min (±12V typ)	*	*	*
Voltage @ $R_L = 10k\Omega$, T_A = min to max	±12V min (±13V typ)	*	*	*
Short Circuit Current	25mA	*	*	*
FREQUENCY RESPONSE				
Unity Gain, Small Signal	1.0MHz	*	*	*
Full Power Response	50kHz	*	*	*
Slew Rate, Unity Gain	3.0V/μs	*	*	*
INPUT OFFSET VOLTAGE[2]	1.0mV max	0.5mV max	0.25mV max	**
vs. Temperature	10.0μV/°C max	5μV/°C max	2.5μV/°C max	*
vs. Supply, T_A = min to max	200μV/V max	100μV/V max	**	**
INPUT BIAS CURRENT				
Either Input[3]	10pA (75pA max)	10pA (35pA max)	**	**
Input Offset Current	5pA	2pA	**	**
MATCHING CHARACTERISTICS[4]				
Offset Voltage	1.0mV max	0.5mV max	0.25mV max	**
vs. Temperature, $T_{min} - T_{max}$	10μV/°C max	5.0μV/°C max	2.5μV/°C max	*
Input Bias Current	35pA max	25pA max	**	**
Crosstalk–1kHz 20V p-p	-124dB	*	*	*
INPUT IMPEDANCE				
Differential	$10^{12}\Omega \| 6pF$	*	*	*
Common Mode	$10^{12}\Omega \| 6pF$	*	*	*
INPUT VOLTAGE RANGE				
Differential[5]	±20V	*	*	*
Common Mode	±10V min (±12V typ)	*	*	*
Common Mode Rejection, $V_{IN} = \pm 10V$	76dB min	80dB min	**	**
POWER SUPPLY				
Rated Performance	±15V	*	*	*
Operating	±(5 to 18)V	*	*	*
Quiescent Current	2.8mA max	*	*	*
VOLTAGE NOISE				
0.1-10Hz	2μV p-p	4μV p-p max	**	**
10Hz	$70nV/\sqrt{Hz}$	*	*	*
100Hz	$45nV/\sqrt{Hz}$	*	*	*
1kHz	$30nV/\sqrt{Hz}$	*	*	*
10kHz	$25nV/\sqrt{Hz}$	*	*	*
TEMPERATURE RANGE				
Operating, Rated Performance	0 to +70°C	*	*	-55°C to +125°C
Storage	-65°C to +150°C	*	*	*
PACKAGING OPTION[6]				
TO-99 Style (H08B)	AD647JH	AD647KH	AD647LH	AD647SH

NOTES

[1] The AD647SH/883B is an AD647SH which is inspected and processed to the full requirements of MIL-STD-883, Level B. A complete listing of the tests is available on request.

[2] Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[3] Bias current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

[4] Matching is defined as the difference between parameters of the two amplifiers.

[5] Defined as the maximum safe voltage between inputs, such that neither exceeds ±10V from ground.

[6] See Section 20 for package outline information.

*Specifications same as AD647JH.

**Specifications same as AD647KH.

Specifications subject to change without notice.

Typical Characteristics

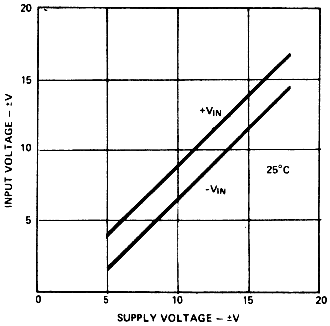


Figure 1. Input Voltage Range vs. Supply Voltage

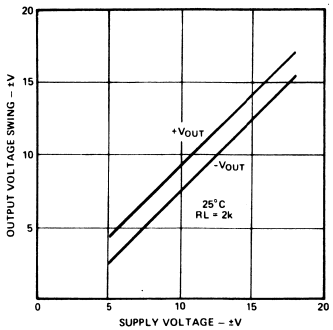


Figure 2. Output Voltage Swing vs. Supply Voltage

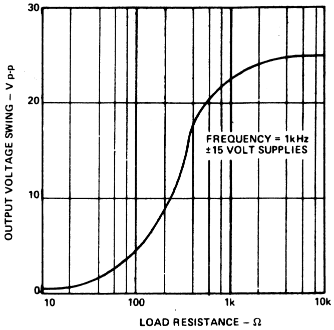


Figure 3. Output Voltage Swing vs. Resistive Load

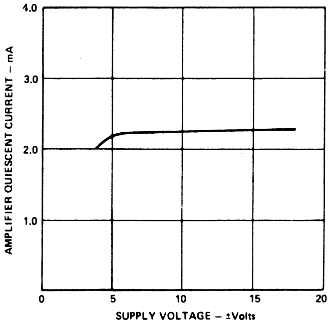


Figure 4. Quiescent Current vs. Supply Voltage

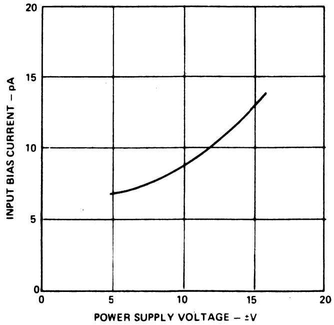


Figure 5. Input Bias Current vs. Supply Voltage

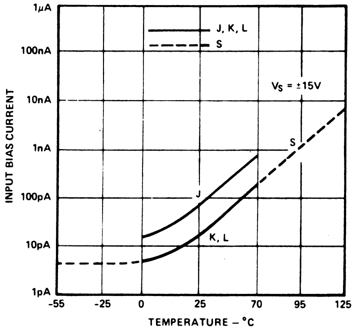


Figure 6. Input Bias Current vs. Temperature

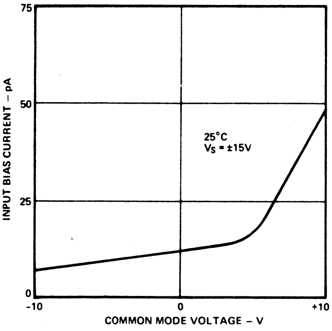


Figure 7. Input Bias Current vs. CMV

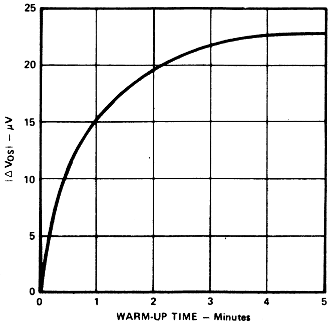


Figure 8. Input Offset Voltage Turn On Drift vs. Time

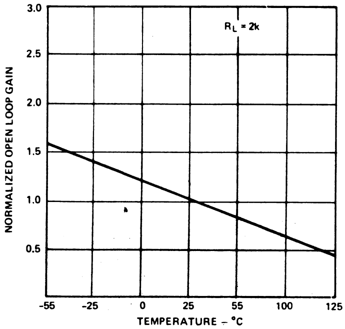


Figure 9. Open Loop Gain vs. Temperature

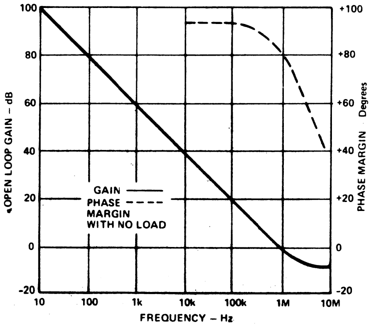


Figure 10. Open Loop Frequency Response

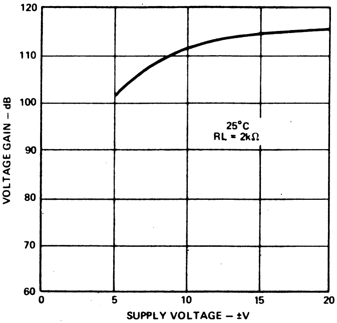


Figure 11. Open Loop Voltage Gain vs. Supply Voltage

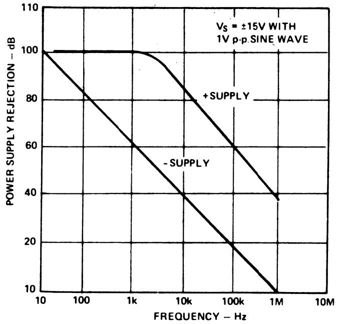


Figure 12. Power Supply Rejection vs. Frequency

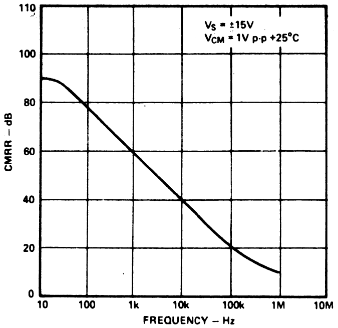


Figure 13. Common Mode Rejection vs. Frequency

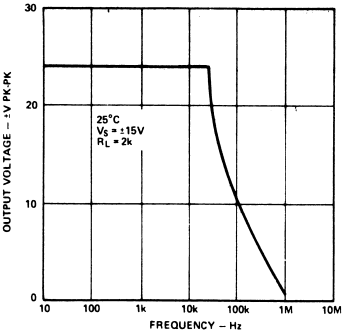


Figure 14. Large Signal Frequency Response

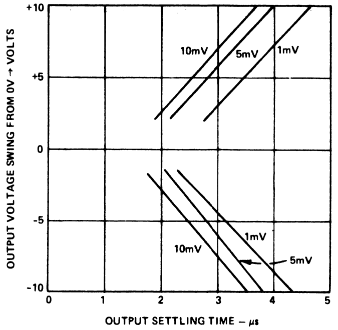


Figure 15. Output Settling Time vs. Output Swing and Error (Circuit of Figure 23)

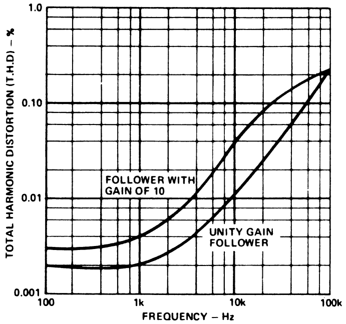


Figure 16. Total Harmonic Distortion vs. Frequency

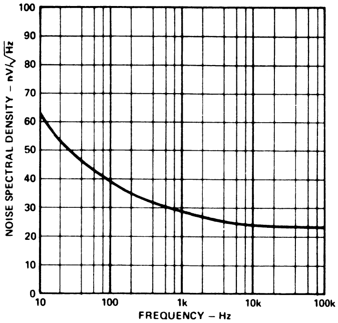


Figure 17. Input Noise Voltage Spectral Density

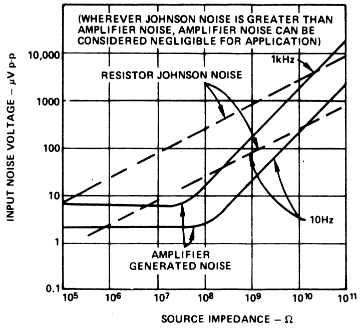
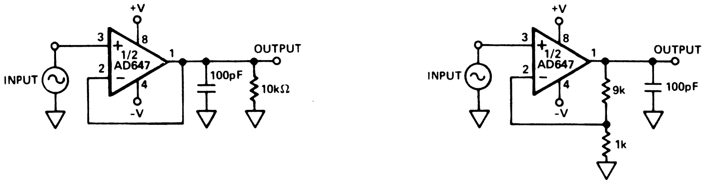


Figure 18. Total rms Noise vs. Source Resistance



a. *Unity Gain Follower*

b. *Follower with Gain = 10*

Figure 19. T.H.D. Test Circuits

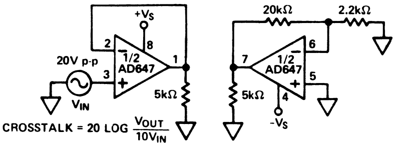


Figure 20. Crosstalk Test Circuit

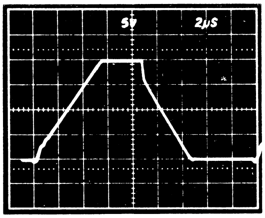


Figure 21a. Unity Gain Follower Pulse Response (Large Signal)

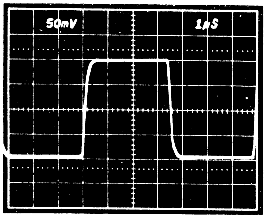


Figure 21b. Unity Gain Follower Pulse Response (Small Signal)

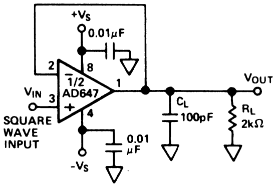


Figure 21c. Unity Gain Follower

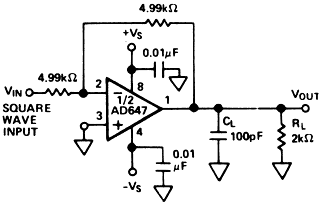


Figure 22a. Unity Gain Inverter

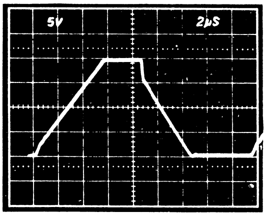


Figure 22b. Unity Gain Inverter Pulse Response (Large Signal)

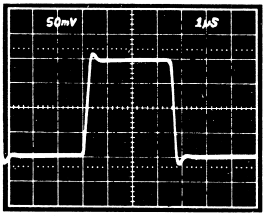


Figure 22c. Unity Gain Inverter Pulse Response (Small Signal)

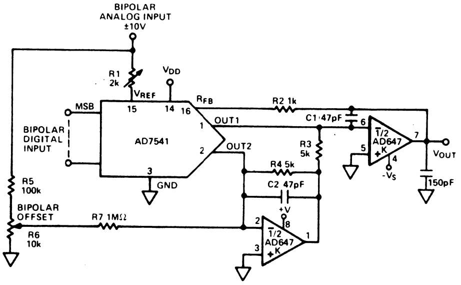
APPLICATION NOTES

The AD647 is fully specified under actual operating conditions to insure high performance in any application, but there are some steps that will improve on even this high level of performance.

The bias current of a JFET amplifier doubles with every 10°C increase in junction temperature. Any heat source that can be eliminated or minimized will significantly improve bias current performance. To account for normal power dissipation, the largest contributor to chip self-heating, the bias currents of the AD647 are guaranteed fully warmed up with ±15V supplies. A decrease in supply voltage will decrease power consumption, resulting in a corresponding drop in bias currents.

Open loop gain and bias currents, to some extent, are affected by output loading. In applications where high linearity is essential, load impedance should be kept as high as possible to minimize degradation of open loop gain.

The outstanding ac and dc performance of the AD647 make it an ideal choice for critical instrumentation applications. In such applications, leakage paths, line losses and external noise sources should be considered in the layout of printed circuit boards. A guard ring surrounding the inputs and connected to a low impedance potential (at the same level as the inputs) should be placed on both sides of the circuit board. This will eliminate leakage paths that could degrade bias current performance. All signal paths should be shielded to minimize noise pick-up.



NOTES:
1. R3/R4 MATCH 0.05% OR BETTER.
2. R1, R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED

Figure 23. AD647 Used as DAC Output Amplifier

A CMOS DAC AMPLIFIER

The output impedance of a CMOS DAC, such as the AD7541, varies with digital input code. This causes a corresponding variation in the noise gain of the DAC-amplifier combination. This noise gain modulation introduces a nonlinearity whose magnitude is dependent on the amount of offset voltage present.

Laser wafer drift trimming lowers the initial offset voltage and the offset voltage drift of the AD647, therefore minimizing the effect of this nonlinearity and its drift with temperature. This, in conjunction with the low bias current and high open loop gain, makes the AD647 ideal for DAC output amplifier applications.

THE AD647 USED WITH THE AD7546

Figure 24 shows the AD647 used with the AD7546 16-bit segment DAC. In this application, amplifier performance is critical to the overall performance of the AD7546. A1 is used as a dual precision buffer. Here the offset voltage match, low offset voltage and high open loop gain of the AD647 ensure monotonicity and high linearity over the entire operating temperature range. A2 serves a dual function: amplifier A is a Track and Hold circuit that deglitches the DAC output and amplifier B acts as an output amplifier. The performance of the amplifiers of A2 is crucial to the accuracy of the system. The errors of these amplifiers are added to the errors due strictly to DAC imperfections. For this reason great care should be used in the selection of these amplifiers. The matching characteristics, low bias current and low temperature coefficients of the AD647 make it ideal for this application.

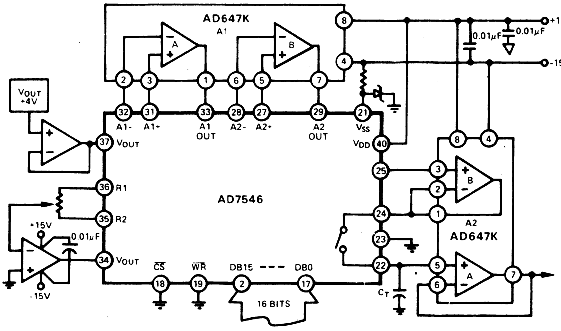


Figure 24. AD647 Used with AD7546 16-Bit DAC

USING THE AD647 IN LOG AMPLIFIER APPLICATIONS

Log amplifiers or log ratio amplifiers are useful in a wide range of analog computational applications, ranging from the simple linearization of exponential transducer outputs to the use of logarithms in computations involving multi-term products or arbitrary exponents. Log amps also facilitate the compression of wide ranging analog input signals into a range that can be easily handled using standard circuit techniques.

The picoamp level input current and low offset voltage of the AD647 make it suitable for wide dynamic range log amplifiers. Figure 27 is a schematic of a log ratio circuit employing the AD647 that can achieve less than 1% conformance error over 5 decades of current input, 1nA to 100µA. For voltage inputs, the dynamic range is typically 50mV to 10V for 1% error, limited on the low end by the amplifiers' input offset voltage.

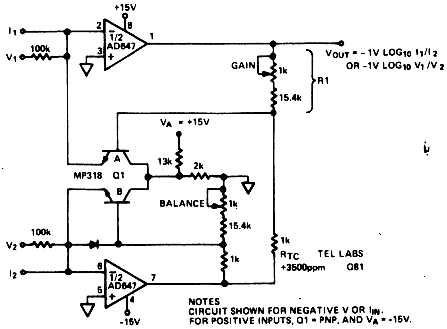

+15V
I_1
V_1
100k
2
8
3
1
1/2
AD647
V_{OUT} = -1V LOG_{10} I_1/I_2
OR -1V LOG_{10} V_1/V_2
GAIN
1k
15.4k
R1
V_A = +15V
A
13k
2k
MP318 Q1
B
BALANCE
1k
15.4k
100k
V_2
1k
R_{TC} TEL LABS
+3500ppm Q81
I_2
6
5
7
4
1/2
AD647
1k
-15V
NOTES
CIRCUIT SHOWN FOR NEGATIVE V OR I_{IN}.
FOR POSITIVE INPUTS, Q1 = PNP, AND V_A = -15V.

Figure 25. Log-Ratio Amplifier

The conversion between current (or voltage) input and log output is accomplished by the base-emitter junctions of the dual transistor Q1. Assuming Q1 has $\beta > 100$, which is the case for the specified transistor, the base-emitter voltage on side 1 is to a close approximation:

$$V_{BE\ A} = kT/q \ln I_1/I_{S1}$$

This circuit is arranged to take the difference of the V_{BE}'s of Q1A and Q1B, thus producing an output voltage proportional to the log of the *ratio* of the inputs:

$$V_{OUT} = -K(V_{BE\ A} - V_{BE\ B}) = -\frac{KkT}{q}(\ln I_1/I_{S1} - \ln I_2/I_{S2})$$

$$V_{OUT} = -K\, kT/q \ln I_1/I_2$$

The scaling constant, K is set by R1 and R_{TC} to about 16, to produce a 1V change in output voltage per decade difference in input signals. R_{TC} is a special resistor with a +3500ppm/°C temperature coefficient, which makes K inversely proportional to temperature, compensating for the "T" in kT/q. The log-ratio transfer characteristic is therefore independent of temperature.

This particular log ratio circuit is free from the dynamic problems that plague many other log circuits. The -3dB bandwidth is 50kHz over the top 3 decades, 100nA to 100µA, and decreases smoothly at lower input levels. This circuit needs no additional frequency compensation for stable operation from input current sources, such as photodiodes, which may have 100pF of shunt capacitance. For larger input capacitances a 20pF integration capacitor around each amplifier will provide a smoother frequency response.

This log ratio amplifier can be readily adjusted for optimum accuracy by following this simple procedure. First, apply V1 = V2 = -10.00V and adjust "Balance" for V_{OUT} = 0.00V. Next apply V1 = -10.00V, V2 = -1.00V and adjust gain for V_{OUT} = +1.00V. Repeat this procedure until gain and balance readings are within 2mV of ideal values.

ACTIVE FILTERS

In active low pass filtering applications the dc accuracy of the amplifiers used is critical to the performance of the filter circuits. DC error sources such as offset voltage and bias currents represent the largest individual contributors to output error. Offset voltages will be passed by the filtering network and may, depending on the design of the filter circuit, be amplified and generate unacceptable output offset voltages. In filter circuits for low frequency ranges large value resistors are used to generate the low pass filter function. Input bias currents passing through these resistors will generate an additional offset voltage that will also be passed to the output of the filter.

The use of the AD647 will minimize these error sources and, therefore, maximize filter accuracy. The wide variety of performance levels of the AD647 allows for just the amount of accuracy required for any given application.

AD647 AS AN INSTRUMENTATION AMPLIFIER

The circuit shown in Figure 26 uses the AD647 to construct an ultra high precision instrumentation amplifier. In this type of application the matching characteristics of a monolithic dual amplifier are crucial to ensure high performance.

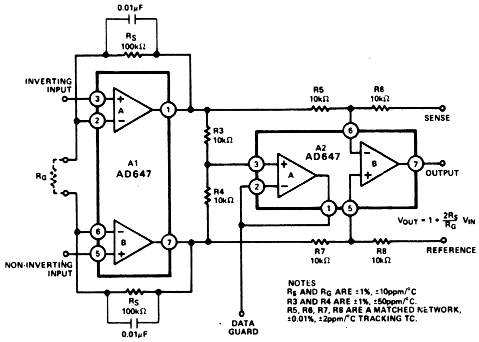


Figure 26. Precision FET Input Instrumentation Amplifier

The use of an AD647L as the input amplifier A1, guarantees maximum offset voltage of 250µV, drift of 2.5µV/°C and bias currents of 35pA. A2 serves two less critical functions in the amplifier and, therefore can be an AD647J. Amplifier A is an active data guard which increases ac CMRR and minimizes extraneous signal pickup and leakage. Amplifier B is the output amplifier of the instrumentation amplifier. To attain the precision available from this configuration, a great deal of care should be taken when selecting the external components. CMRR will depend on the matching of resistors R1, R2, R3, and R4. The gain drift performance of this circuit will be affected by the matching TC of the resistors used.

ANALOG DEVICES

Low Cost High Accuracy IC Op Amps

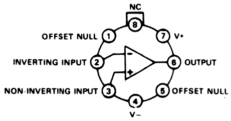
AD741 SERIES

FEATURES

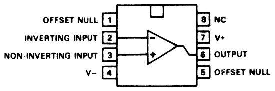
Precision Input Characteristics
- Low V_{OS}: 0.5mV max (L)
- Low V_{OS} Drift: 5μV/°C max (L)
- Low I_b: 50nA max (L)
- Low I_{OS}: 5nA max (L)
- High CMRR: 90dB min (K, L)

High Output Capability
- A_{ol} = 25,000 min, 1kΩ load (J, S) T_{min} to T_{max}
- V_O = ±10V min, 1kΩ load (J, S)

AD741 SERIES FUNCTIONAL DIAGRAMS



TO-99
TOP VIEW



8-PIN MINI DIP
TOP VIEW

GENERAL DESCRIPTION

The Analog Devices AD741 series are high performance monolithic operational amplifiers. All the devices feature full short circuit protection and internal compensation.

The Analog Devices AD741J, AD741K, AD741L and AD741S are specially tested and selected versions of the standard AD741 operational amplifier. Improved processing and additional electrical testing guarantee the user precision performance at a very low cost. The AD741J, K and L substantially increase overall accuracy over the standard AD741C by providing maximum limits on offset voltage drift and significantly reducing the errors due to offset voltage, bias current, offset current, voltage gain, power supply rejection, and common mode rejection. For example, the AD741L features maximum offset voltage drift of 5μV/°C, offset voltage of 0.5mV max, offset current of 5nA max, bias current of 50nA max, and a CMRR of 90dB min. The AD741S offers guaranteed performance over the extended temperature range of −55°C to +125°C, with max offset voltage drift of 15μV/°C, max offset voltage of 4mV, max offset current of 25nA, and a minimum CMRR of 80dB.

HIGH OUTPUT CAPABILITY

Both the AD741J and AD741S offer the user the additional advantages of high guaranteed output current and gain at low values of load impedance. The AD741J guarantees a minimum gain of 25,000 swinging ±10V into a 1kΩ load from 0 to +70°C. The AD741S guarantees a minimum gain of 25,000 swinging ±10V into a 1kΩ load from −55°C to +125°C.

All devices feature full short circuit protection, high gain, high common mode range, and internal compensation. The AD741J, K and L are specified for operation from 0 to +70°C, and are available in both the TO-99 and mini-DIP packages. The AD741S is specified for operation from −55°C to +125°C, and is available in the TO-99 package.

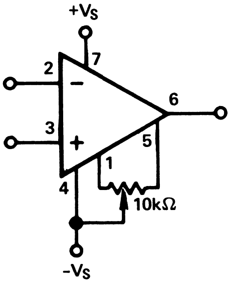
SPECIFICATIONS (typical @ +25°C and ±15V dc, unless otherwise specified)

	AD741C			AD741			AD741J			
Model	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
OPEN LOOP GAIN										
$R_L = 1k\Omega, V_O = \pm10V$							50,000	200,000		V/V
$R_L = 2k\Omega, V_O = \pm10V$	20,000	200,000		50,000	200,000					V/V
T_A = min to max $R_L = 2k\Omega$	15,000			25,000			25,000			V/V
OUTPUT CHARACTERISTICS										
Voltage @ $R_L = 1k\Omega$, T_A = min to max							±10	±13		V
Voltage @ $R_L = 2k\Omega$, T_A = min to max	±10	±13		±10	±13					V
Short Circuit Current		25			25			25		mA
FREQUENCY RESPONSE										
Unity Gain, Small Signal		1			1			1		MHz
Full Power Response•		10			10			10		kHz
Slew Rate		0.5			0.5			0.5		V/μs
Transient Response (Unity Gain)										
Rise Time $C_L \leq 10V$ p-p		0.3			0.3			0.3		μs
Overshoot		5.0			5.0			5.0		%
INPUT OFFSET VOLTAGE										
Initial, $R_S \leq 10k\Omega$, Adj. to Zero		1.0	6.0		1.0	5.0		1.0	3.0	mV
T_A = min to max		1.0	7.5		1.0	6.0			4.0	mV
Average vs. Temperature (Untrimmed)									20	μV/°C
vs. Supply, T_A = min to max								30	100	μV/V
INPUT OFFSET CURRENT										
Initial		20	200		20	200		5	50	nA
T_A = min to max		40	300		85	500			100	nA
Average vs. Temperature								0.1		nA/°C
INPUT BIAS CURRENT										
Initial		80	500		80	500		40	200	nA
T_A = min to max		120	800		300	1,500			400	nA
Average vs. Temperature								0.6		nA/°C
INPUT IMPEDANCE DIFFERENTIAL	0.3	2.0		0.3	2.0			1.0		MΩ
INPUT VOLTAGE RANGE[1]										
Differential, max Safe									±30	V
Common Mode, max Safe	±12	±13		±12	±13			±15		V
Common Mode Rejection, $R_S = \leq 10k\Omega$, T_A = min to max, $V_{IN} = \pm12V$	70	90		70	90		80	90		dB
POWER SUPPLY										
Rated Performance		±15			±15			±15		V
Operating							±5		±18	V
Power Supply Rejection Ratio		30	150		30	150				μV/V
Quiescent Current		1.7	2.8		1.7	2.8		2.2	3.3	mA
Power Consumption		50	85		50	85		50	85	mW
T_A = min					60	100				mW
T_A = max					45	75				mW
TEMPERATURE RANGE										
Operating Rated Performance	0		+70	-55		+125	0		+70	°C
Storage	-65		+150	-65		+150	-65		+150	°C

NOTE

[1] For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Specifications subject to change without notice.



Standard Nulling Offset Circuit

SPECIFICATIONS (typical @ +25°C and ±15V dc, unless otherwise specified)

Model	AD741K			AD741L			AD741S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OPEN LOOP GAIN										
$R_L = 1k\Omega, V_O = \pm10V$							50,000	200,000		V/V
$R_L = 2k\Omega, V_O = \pm10V$	50,000	200,000		50,000	200,000					V/V
T_A = min to max $R_L = 2k\Omega$	25,000			25,000			25,000			V/V
OUTPUT CHARACTERISTICS										
Voltage @ $R_L = 1k\Omega$, T_A = min to max										V
Voltage @ $R_L = 2k\Omega$, T_A = min to max	±10	±13		±10	±13		±10	±13		V
Short Circuit Current		25			25			25		mA
FREQUENCY RESPONSE										
Unity Gain, Small Signal		1			1			1		MHz
Full Power Response		10			10			10		kHz
Slew Rate		0.5			0.5			0.5		V/μs
Transient Respone (Unity Gain)										
Rise Time		0.3			0.3			0.3		μs
Overshoot		5.0			5.0			5.0		%
INPUT OFFSET VOLTAGE										
Initial, $R_S \leq 10k\Omega$, Adj. to Zero		0.5	2.0		0.2	0.5		1.0	2	mV
T_A = min to max			3.0			1.0			4	mV
Average vs. Temperature (Untrimmed)		6.0	15.0		2.0	5.0		6.0	15.0	μV/°C
vs. Supply, T_A = min to max		5	15.0		5	15.0		30	100	μV/V
INPUT OFFSET CURRENT										
Initial		2	10		2	5		2	10	nA
T_A = min to max			15			10			25	nA
Average vs. Temperature		0.02	0.2		0.02	0.1		0.1	0.25	nA/°C
INPUT BIAS CURRENT										
Initial		30	75		30	50		30	75	nA
T_A = min to max			120			100			250	nA
Average vs. Temperature		0.6	1.5		0.6	1.0		0.6	2.0	nA/°C
INPUT IMPEDANCE DIFFERENTIAL		2			2			2		MΩ
INPUT VOLTAGE RANGE[1]										
Differential, max Safe		±30			±30			±30		V
Common Mode max Safe		±15			±15			±15		V
Common Mode Rejection, $R_S \leq 10k\Omega$, T_A = min to max $V_{IN} = \pm12V$	90	100		90	100		90	100		dB
POWER SUPPLY										
Rated Performance		±15			±15			±15		V
Operating	±5		±22	±5		±22	±5		±22	V
Power Supply Rejection Ratio										μV/V
Quiescent Current		1.7	2.8		1.7	2.8		2.0	2.8	mA
Power Consumption		50	85		50	85		50	85	mW
T_A = min								60	100	mW
T_A = max								115	75	mW
TEMPERATURE RANGE										
Operating Rated Performance	0		+70	0		+70	-55		+125	°C
Storage	-65		+150	-65		+150	-65		+150	°C

NOTE

[1] For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Specifications subject to change without notice.

ORDERING GUIDE

Model	Temperature Range	Package[1]	Initial Off-Set Voltage
AD741CN	0 to +70°C	MINI-DIP (N8A)	6.0mV
AD741CH	0 to +70°C	TO-99	6.0mV
AD741JN	0 to +70°C	MINI-DIP (N8A)	3.0mV
AD741JH	0 to +70°C	TO-99	3.0mV
AD741KN	0 to +70°C	MINI-DIP (N8A)	2.0mV
AD741KH	0 to +70°C	TO-99	2.0mV
AD741LN	0 to +70°C	MINI-DIP (N8A)	0.5mV
AD741LH	0 to +70°C	TO-99	0.5mV
AD741H	-55°C to +125°C	TO-99	5.0mV
AD741SH	-55°C to +125°C	TO-99	2.0mV
AD741SH/883B	-55°C to +125°C	TO-99	2.0mV

[1] See Section 20 for package outline information.

MIL-STANDARD-883

The AD741S and AD741 are available with screening to MIL-STD-883, Method 5004, Class B.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings	AD741, J, K, L, S	AD741C
Supply Voltage	±22V	±18V
Internal Power Dissipation	500mW[1]	500mW
Differential Input Voltage	±30V	±30V
Input Voltage	±15V	±15V
Storage Temperature Range	-65°C to +150°C	-65°C to +150°C
Lead Temperature (soldering, 60 seconds)	300°C	300°C
Output Short Circuit Duration	Indefinite[2]	Indefinite

NOTES

[1] Rating applies for case temperature to +125°C. Derate TO-99 linearity at 6.5mW/°C for ambient temperatures above +70°C.

[2] Rating applies for shorts to ground or either supply at case temperatures to +125°C or ambient temperatures to +75°C.

Typical Performance Curves

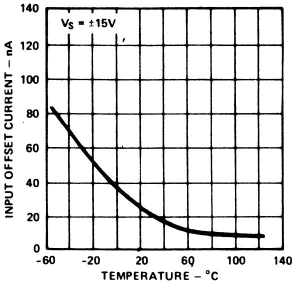


Figure 1. Offset Current vs. Temperature

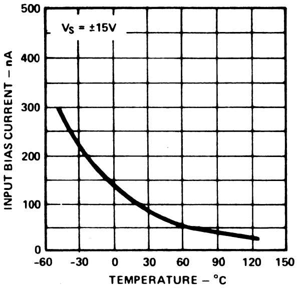


Figure 2. Bias Current vs. Temperature

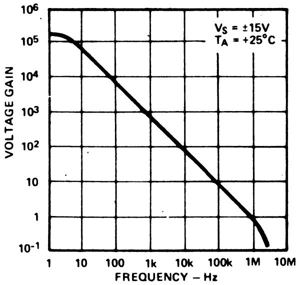


Figure 3. Open Loop Gain vs. Frequency

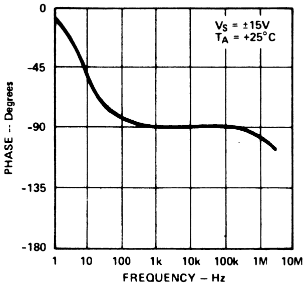


Figure 4. Open Loop Phase Response vs. Frequency

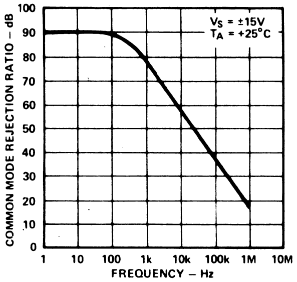


Figure 5. Common Mode Rejection vs. Frequency

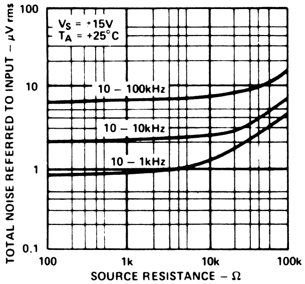


Figure 6. Broad Band Noise vs. Source Resistance

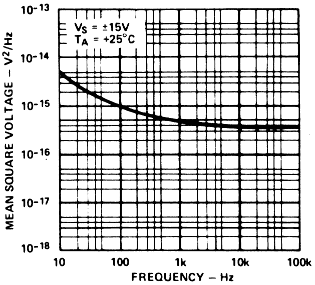


Figure 7. Input Noise Voltage vs. Frequency

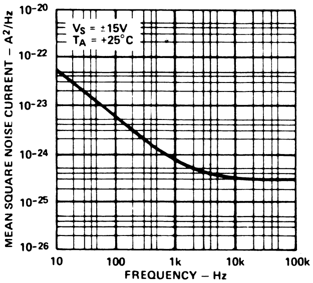


Figure 8. Input Noise Current vs. Frequency

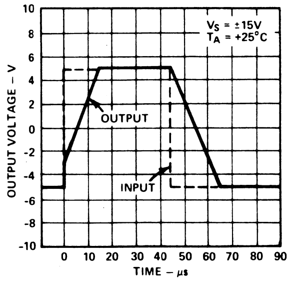


Figure 9. Voltage Follower Large Signal Pulse Response

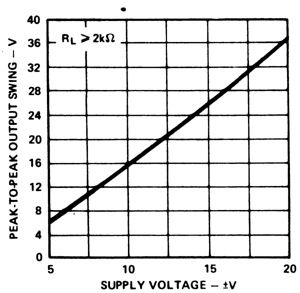


Figure 10. Output Voltage Swing vs. Supply Voltage

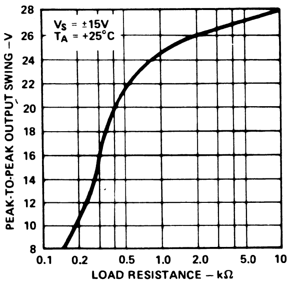


Figure 11. Output Voltage Swing vs. Load Resistance

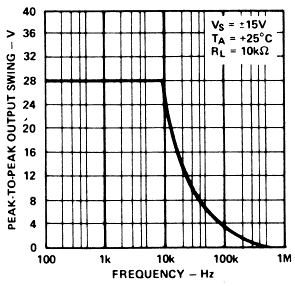


Figure 12. Output Voltage Swing vs. Frequency

ANALOG DEVICES

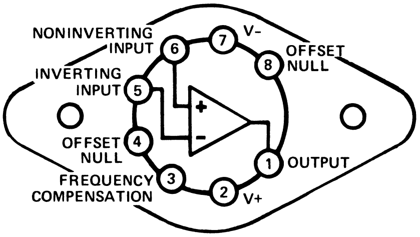
Wideband, Fast-Settling FET-Input Op Amp

AD3554

FEATURES

Very High Slew Rate: 1000V/µs
Fast Settling: 150ns max to ±0.05%
Gain Bandwidth Product: 1.7GHz typical
High Output Current: 100mA min @ V_{OUT} = 10V
Full Differential Input

AD3554 FUNCTIONAL BLOCK DIAGRAM



TO-3 STYLE
BOTTOM VIEW

PRODUCT DESCRIPTION

The AD3554 is a FET-input, hybrid operational amplifier that features an excellent combination of high slew rate, fast settling time and large gain-bandwidth product. The AD3554 has a full differential input with matched input FETs for low offset voltage.

The AD3554 can supply ±100mA at 10 volts. The slew rate is 1000V/µs minimum; 1200V/µs is typical. Settling time to ±0.05% of final value is only 150ns when configured as a unity gain amplifier. The user can optimize the combination of bandwidth, slew rate, and settling time for a particular application by selecting the external compensation capacitor.

The AD3554 is recommended for any operational amplifier application where speed and bandwidth are important considerations. The high slew rate and fast settling time make the AD3554 an excellent choice for use in fast D/A converters, fast current amplifiers, integrators, waveform generators and multiplexer buffers.

The AD3554 is available in three versions: the "A" and "B" are specified over the -25°C to +85°C temperature range and "S" over the -55°C to +125°C operating temperature range. All devices are packaged in the hermetically-sealed TO-3 style metal can.

PRODUCT HIGHLIGHTS

1. The high slew rate (1000V/µs min) and fast settling time to 0.01% (250ns max) make the AD3554 ideal for D/A, A/D, sample-hold circuits and high speed integrators.
2. Laser trimming techniques reduce offset voltage to as low as 1mV max (AD3554B), thus eliminating the need for external nullling in many applications.
3. Very high gain-bandwidth product (1.7GHz typically at A = 1000) makes the AD3554 an ideal choice for high frequency amplifier applications.
4. FET inputs result in a low bias current (50pA max, 10pA typ) in a high gain-bandwidth product operational amplifier.
5. Full differential input makes the AD3554 ideal for all standard operational amplifier applications such as high speed integrators, differentiators, high gain amplifiers, etc.
6. The 100mA at 10V output makes the AD3554 suitable for many applications that require high output power, such as cable drivers.

SPECIFICATIONS (typical @ +25°C and $V_S = \pm15V$ dc unless otherwise specified)

MODEL	AD3554A	AD3554B	AD3554S
OPEN LOOP GAIN			
No Load	106dB (100dB min)	*	*
$R_L = 100\Omega$	96dB (90dB min)	*	*
OUTPUT CHARACTERISTICS			
Voltage @ $I_O = \pm100mA$	±11V (±10V min)	*	*
Output Resistance, Open Loop @ f = 10MHz	20Ω		
Current @ $V_O = \pm10V$	±125mA (±100mA min)	*	*
FREQUENCY RESPONSE			
Bandwidth (0dB, Small Signal, $C_F = 0$)[1]	90MHz (70MHz min)	*	*
Gain-Bandwidth Product, $C_F = 0$,[1]			
G = 10V/V	225MHz (150MHz min)	*	*
G = 100V/V	725MHz (425MHz min)	*	*
G = 1000V/V	1700MHz (1000MHz min)	*	*
Full Power Bandwidth, $C_F = 0$, $V_O = 20V$ p-p, $R_L = 100\Omega$[1]	19MHz (16MHz min)	*	*
Slew Rate, $C_F = 0$, $V_O = 20V$ p-p, $R_L = 100\Omega$	1200V/μs (1000V/μs min)	*	*
Settling Time[1], A = -1, to ±1%	60ns	*	*
to ±0.1%	120ns	*	*
to ±0.05%	140ns (150ns max)	*	*
to ±0.01%	200ns (250ns max)	*	*
INPUT OFFSET VOLTAGE	0.5mV (2.0mV max)	0.2mV (1.0mV max)	**
vs. Temperature	20μV/°C (50μV/°C max)	8μV/°C (15μV/°C max)	12μV/°C (25μV/°C max)
vs. Supply, T_A = min to max	80μV/V (300μV/V max)	*	*
INPUT BIAS CURRENT			
Either Input[2]	10pA (50pA max)	*	*
vs. Supply Voltage	1pA/V	*	*
INPUT IMPEDANCE			
Differential	$10^{11}\Omega\|\|2pF$	*	*
Common Mode	$10^{11}\Omega\|\|2pF$	*	*
INPUT VOLTAGE RANGE			
Max Safe Input Voltage	$\pm V_{CC}$	*	*
Common Mode	$\pm(\|V_{CC}\|-4)$	*	*
Common Mode Rejection, V_{CM} = +7V, -10V	78dB (44dB min)	*	*
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	±(5 to 18)V	*	*
Quiescent Current	28mA (45mA max)	*	*
INPUT NOISE			
Voltage, f_o = 1Hz	$125nV/\sqrt{Hz}$ ($450nV/\sqrt{Hz}$ max)[1]	*	*
f_o = 10Hz	$50nV/\sqrt{Hz}$ ($160nV/\sqrt{Hz}$ max)[1]	*	*
f_o = 100Hz	$25nV/\sqrt{Hz}$ ($90nV/\sqrt{Hz}$ max)[1]	*	*
f_o = 1kHz	$15nV/\sqrt{Hz}$ ($50nV/\sqrt{Hz}$ max)[1]	*	*
f_o = 10kHz	$10nV/\sqrt{Hz}$ ($35nV/\sqrt{Hz}$ max)[1]	*	*
f_o = 100kHz	$8nV/\sqrt{Hz}$ ($25nV/\sqrt{Hz}$ max)[1]	*	*
f_o = 1MHz	$7nV/\sqrt{Hz}$ ($25nV/\sqrt{Hz}$ max)[1]	*	*
f_B = 0.3Hz to 10Hz	2μV, p-p (7μV, p-p max)	*	*
f_B = 10Hz to 1MHz	8μV, rms (25μV, rms max)	*	*
Current, f_B = 3Hz to 10Hz	45fA, p-p	*	*
f_B = 10Hz to 1MHz	2pA, rms	*	*
TEMPERATURE RANGE			
Operating, Rated Performance	-25°C to +85°C	*	-55°C to +125°C
Storage	-65°C to +150°C	*	*
PACKAGE OPTION[3] TO-3 Style (H08-C)	AD3554AH	AD3554BH	AD3554SH

NOTES

[1] This parameter is guaranteed but not tested. This specification is established to a 90% confidence level.

[2] Bias Current specifications are guaranteed maximum at either input at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

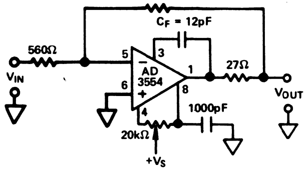
[3] See Section 20 for package outline information.

*Specifications same as AD3554A.

**Specifications same as AD3554B.

Specifications subject to change without notice.

TYPICAL APPLICATION



X10 Inverting Amplifier

ANALOG DEVICES

Ultra Fast FET Operational Amplifier

ADLH0032G/ADLH0032CG

FEATURES

- 2nd Source; Replaces All LH0032G
- High Slew Rate; 500V/µs
- Wide 70MHz Bandwidth
- Operation Guaranteed -55°C to +125°C (ADLH0032G)
- High Input Impedance of $10^{12}\,\Omega$
- 2mV Input Offset Voltage

APPLICATIONS

- High Speed DAC Comparators
- ADC and SHA Input Buffers
- High Speed Integrators
- Video Amplifiers

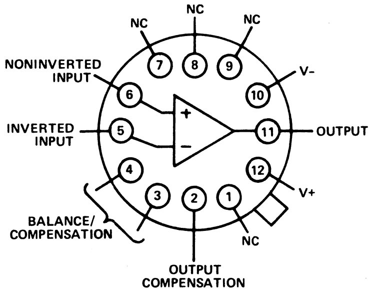
GENERAL DESCRIPTION

The ADLH0032G and ADLH0032CG are high slew rate, high input impedance, differential operational amplifiers, suitable for numerous applications in high-speed signal processing. These second source devices are the same in every characteristic as other LH0032G/LH0032CG amplifiers, and thus are particularly suited for comparator applications due to their high allowable differential input capabilities (±15V), ease of output clamping, and high output drive capabilities.

Featuring a wide 70MHz bandwidth, high input impedance ($10^{12}\,\Omega$), and high output drive capacity, the ADLH0032G and ADLH0032CG have already been designed into such applications as summing amplifiers in high-speed DACs, Buffer Amps in ADCs and high-speed SHAs, as well as other applications normally reserved for special purpose video amplifiers.

The ADLH0032G is guaranteed over the entire MIL temperature range from -55°C to +125°C, while the commercial grade ADLH0032CG is guaranteed from -25°C to +85°C. Both devices are packaged in a TO-8 metal can package. The ADLH0032G is available screened to MIL-883B requirements (see ordering guide).

ADLH0032G/ADLH0032CG
FUNCTIONAL BLOCK DIAGRAM



TO-8 PACKAGE
BOTTOM VIEW

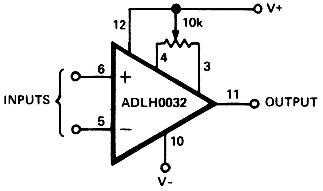


Figure 1. Offset Null

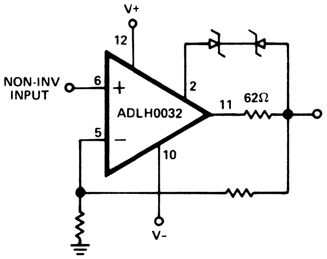


Figure 2. Output Short Circuit Protection

SPECIFICATIONS

Model		**ADLH0032G, ADLH0032CG**
ABSOLUTE MAXIMUM RATINGS		
Supply Voltage		±18V
Power Dissipation		See Characteristic Curves
Differential Input Voltage		±30V
Input Voltage		$\pm V_S$
Operating Temperature Range	ADLH0032G	-55°C to +125°C
	ADLH0032CG	-25°C to +85°C
Storage Temperature Range		-65°C to +150°C
Lead Temperature (soldering, 10sec)		300°C

		ADLH0032G			ADLH0032CG			
Parameter	**Conditions**	**min**	**typ**	**max**	**min**	**typ**	**max**	**Units**
DC ELECTRICAL CHARACTERISTICS[1]								
Input Offset Voltage[2]	$T_J = +25°C$		2	5		5	15	mV
				10			20	
Input Offset Current[2]	$T_J = +25°C$		5	25		10	50	pA
				25			5	nA
Input Bias Current[2]	$T_J = +25°C$		10	100		25	200	pA
				50			15	nA
Average Offset Voltage Drift			25	50		25	50	μV/°C
Large Signal Voltage Gain	$V_{OUT} = \pm 10V$, F = 1kHz, $R_L = 1k\Omega$, $T_C = +25°C$	60	70		60	70		dB
	$V_{OUT} = \pm 10V$, $R_L = 1k\Omega$, F = 1kHz	57			57			dB
Input Voltage Range		±10	±12		±10	±12		V
Output Voltage Swing	$R_L = 1k\Omega$	±10	±13.5		±10	±13		V
Power Supply Rejection Ratio	$\Delta V_S = \pm 10V$	50	60		50	60		dB
Common Mode Rejection Ratio	$\Delta V_{IN} = 10V$	50	60		50	60		dB
Supply Current	$T_C = +25°C$		18	20		20	22	mA
AC ELECTRICAL CHARACTERISTICS[3]								
Slew Rate	$A_V = +1$, $\Delta V_{IN} = 20V$	350	500		350	500		V/μs
Settling Time to 1% of Final Value	$A_V = -1$, $\Delta V_{IN} = 20V$		100			100		ns
Settling Time to 0.1% of Final Value	$A_V = -1$, $\Delta V_{IN} = 20V$		300			300		ns
Small Signal Rise Time	$A_V = +1$, $\Delta V_{IN} = 1V$		8	20		8	20	ns
Small Signal Delay Time	$A_V = +1$, $\Delta V_{IN} = 1V$		10	25		10	25	ns
MTBF[4]								
Meantime Between Failures	2.03×10^6 Hours							
PACKAGE OPTION[5]			H12A			H12A		

---

[1] These specifications apply for $V_S = \pm 15V$ and -55°C to +125°C for the ADLH0032G and -25°C to +85°C for the ADLH0032CG.

[2] Due to high speed automatic test techniques employed these parameters are correlated to junction temperature.

[3] These specifications apply for $V_S = \pm 15V$, $R_L = 1k\Omega$, $T_C = +25°C$.

[4] ADLH0032G/883 calculated per MIL-HNBK 217, Ground; Fixed; Temperature (Case) = 70°C.

[5] See Section 20 for package outline information.

[6] Refer to Package Type G = TO-8 Hermetically Sealed Can.

[7] Specifies processing to MIL-883B.

Specifications subject to change without notice.

ORDERING INFORMATION[6]

Model	**Temperature Range**
ADLH0032CG	-25°C to +85°C
ADLH0032G	-55°C to +125°C
ADLH0032G/883[7]	-55°C to +125°C

Applying the ADLH0032G/ADLH0032CG

POWER SUPPLY DECOUPLING

The ADLH0032G/ADLH0032CG, like most high-speed circuits, are sensitive to stray capacitances and layout. Power supplies should be bypassed as near to ±V (Pins 10 and 12) as possible, using low inductance capacitors such as 0.01μF disc ceramics. Components for compensation should also be located close to the appropriate pins to reduce stray capacitances. A large ground plane area for low-impedance ground paths is highly recommended.

HEAT SINKING

The ADLH0032G/ADLH0032CG are specified for operation without any heat sink. Since internal power dissipation does create a significant temperature rise, improved bias current performance can be achieved by using a small heat sink such as the Thermalloy 2241 or equivalent. Since the case of the ADLH0032G/ADLH0032CG has no internal connection, it may be electrically connected to the heat sink. This, however, will affect the stray capacitances to all pins, therefore requiring adjustment of all circuit compensation values.

INPUT CAPACITANCE

Inverting Input:

For optimum performance, the inverting input should be compensated by a small capacitance, around 10pF, across the feedback resistor. This is because the 5pF input capacitance may cause significant time constants with high-value resistors. The capacitor value may be changed somewhat depending on the effects of layout and closed loop gain.

Noninverting Input:

To divert leakage currents away from the noninverting input and to reduce the effective input capacitance, it is desirable to bootstrap the case and/or a guard conductor to the inverting input. The resulting input capacitance of a unity gain follower configured this way will be less than 1 picofarad.

TYPICAL APPLICATIONS

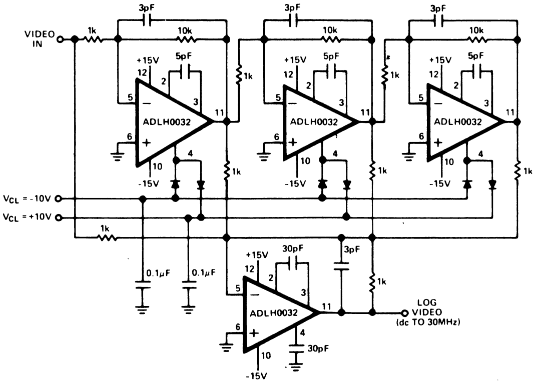


Figure 3. DC to Video Log Amplifier

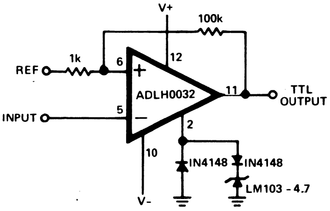


Figure 4. High Impedance, High Speed Comparator

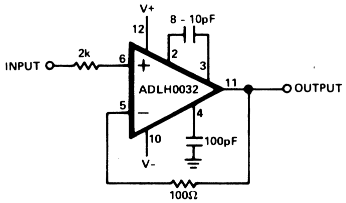


Figure 6. Unity Gain Follower

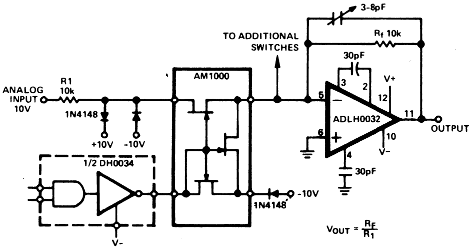


Figure 5. Current Mode Multiplexer

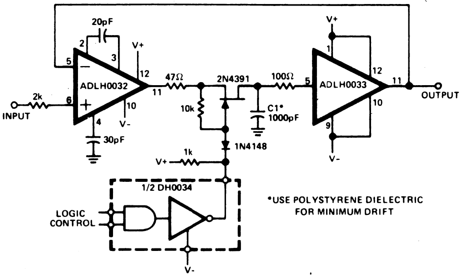
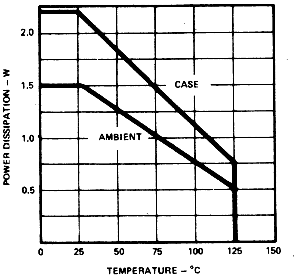
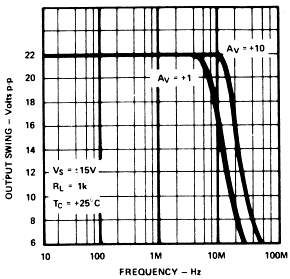


Figure 7. High Speed Sample and Hold

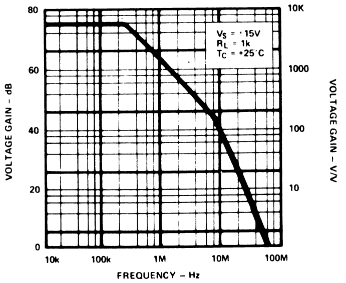
Typical Performance Curves



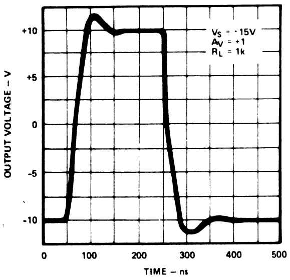
Maximum Power Dissipation



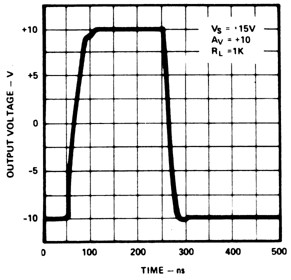
Large Signal Frequency Response



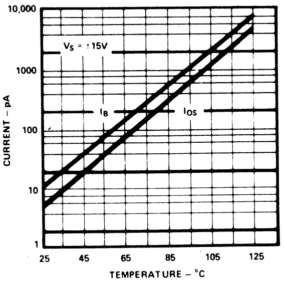
Open Loop Frequency Response



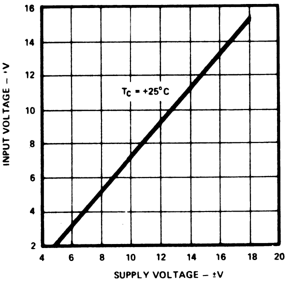
Large Signal Pulse Response



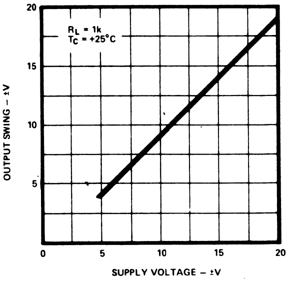
Large Signal Pulse Response



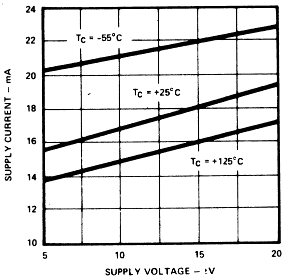
Input Bias and Offset Current vs. Temperature



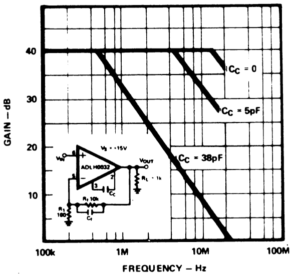
Input Voltage Range



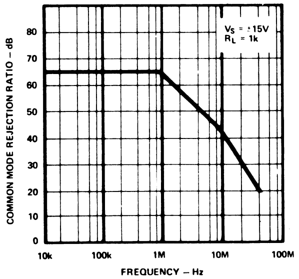
Output Swing



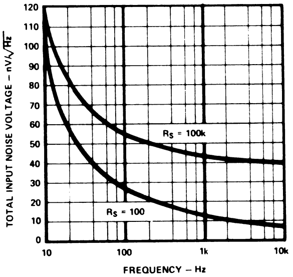
Supply Current vs. Supply Voltage



Closed Loop Frequency Response



Common Mode Rejection Ratio vs. Frequency



*Total Input Noise Voltage vs. Frequency**

**Includes Contribution From Source Resistance*

ANALOG DEVICES

High Speed Buffer Amplifiers

ADLH0033G/ADLH0033CG

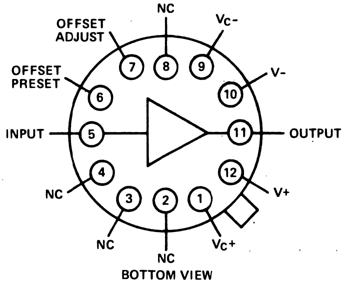
FEATURES

2nd Source– Replaces All LH0033G Series
Wide Bandwidth–dc to 100MHz
High Slew Rate–1500V/μs
Operates on Single or Dual Power Supplies
Operation Guaranteed -55°C to +125°C (ADLH0033G)
High $10^{11}\,\Omega$ Input Impedance

APPLICATIONS

High-Speed Line Drivers
Video Impedance Transformation
High-Speed A/D Input Buffers
Nuclear Instrumentation Amplifiers
Coaxial Cable Drive

ADLH0033G/ADLH0033CG
FUNCTIONAL BLOCK DIAGRAM



TO-8 PACKAGE

GENERAL DESCRIPTION

The ADLH0033G and ADLH0033CG are superhigh speed (1500V/μs slew rate) and high input impedance ($10^{11}\,\Omega$) buffer amplifiers, designed to replace all LH0033 series amplifiers in applications such as high-speed line drivers or as high impedance buffers for fast A/D converters and comparators.

The ADLH0033G and ADLH0033CG are rated for operation over the voltage range of ±5V to ±20V. The ADLH0033G is guaranteed over the temperature range of -55°C to +125°C, while the commercial grade ADLH0033CG is guaranteed over the range of -25°C to +85°C.

Guaranteed operation over temperature of the ADLH0033G is achieved by using specially selected junction FET's and the latest state-of-the-art laser trimming techniques. They are available in the industry standard 12 pin TO-8 metal can. Screening to the requirements of MIL-883B is available.

OPERATION WITHIN AN OP AMP LOOP

When using the ADLH0033G/ADLH0033CG as a current booster or isolation buffer with op amps such as LH0032, 118, 741, etc., an isolation resistor of at least 47Ω must be used between the op amp's output and the input of the ADLH0033G.

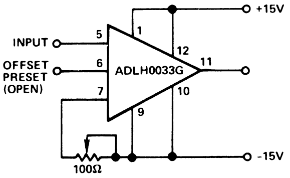


Figure 1. Offset Adjustment

HEAT SINKING

To assure maximum output drive capability of the ADLH0033G/ADLH0033CG over temperature, heat sinks should be used. The cases are electrically isolated from the circuit and thus may be connected to system grounds.

POWER SUPPLY BYPASSING

To prevent oscillation, power supply bypassing is recommended. Use low-inductance ceramic disc caps, keeping lead lengths as short as possible (1/4″ to 1/2″ max from device package), connected between ground plane and each supply lead. Use one or two 0.1μF caps in parallel with a 4.7μF tantalum for best results.

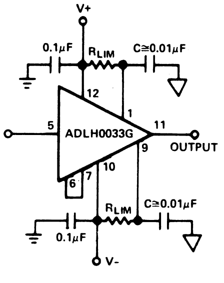


Figure 2. Short Circuit Protection Using Current Limiting Resistors (R_{LIM})

SPECIFICATIONS

	ADLH0033G	ADLH0033CG
ABSOLUTE MAXIMUM RATINGS		
Supply Voltage (V+ - V-)	40V	
Maximum Power Dissipation (see curves)	1.5W	
Maximum Junction Temperature	175°C	
Input Voltage	Equal to Supplies	
Continuous Output Current	±100mA	
Peak Output Current	±250mA	
Operating Temperature ADLH0033G	-55°C to +125°C	
ADLH0033CG	-25°C to +85°C	
Storage Temperature Range	-65°C to +150°C	
Lead Temperature (Soldering, 10 sec.)	300°C	

		ADLH0033G			ADLH0033CG			
Parameter	**Conditions**	**min**	**typ**	**max**	**min**	**typ**	**max**	**Units**
DC ELECTRICAL CHARACTERISTICS[1]								
Input Bias Current	$T_C = 25°C$[2]		0.1			0.15		nA
				10			5	nA
Input Impedance	$R_L = 1k\Omega$	10^{10}	10^{11}		10^{10}	10^{11}		Ω
Voltage Gain	$V_{IN} = 1V$ rms, f = 1kHz, $R_L = 1k\Omega$, $R_S = 100k\Omega$	0.97	0.98	1.0	0.96	0.98	1.0	V/V
Output Offset Voltage	$R_S = 100k\Omega$, $T_C = 25°C$		5	10		12	20	mV
	$R_S = 100k\Omega$			15			25	mV
Output Offset Voltage TC	$R_S = 100k\Omega$, $-55°C \leq T_C \leq 125°C$		50	100		50	100	μV/°C
Output Impedance	$V_{IN} = 1V$ rms, f = 1kHz $R_S = 100k\Omega$, $R_L = 1k\Omega$		6	10		6	10	Ω
Output Voltage Swing	$R_L = 1k\Omega$	±12	±13		±12	±13		V
	$R_L = 100\Omega$, $T_C = 25°C$	±9			±9			V
	$V_S = \pm5V$, $R_L = 1k\Omega$		6			6		V p-p
Supply Current	$V_{IN} = 0V$, $V_S = \pm15V$		20	22		21	24	mA
	$V_S = \pm5V$		18			18		mA
Power Consumption	$V_{IN} = 0V$, $V_S = \pm15V$		600	660		630	720	mW
	$V_S = \pm5V$		180			180		mW
AC ELECTRICAL CHARACTERISTICS ($T_C = 25°C$, $V_S = \pm15V$, $R_S = 50\Omega$, $R_L = 1k\Omega$)								
Slew Rate	$V_{IN} = \pm10V$	1000	1500		1000	1400		V/μs
Bandwidth	$V_{IN} = 1V$ rms		100			100		MHz
Phase Nonlinearity	BW = 1 to 20MHz		2			2		Degrees
Rise Time	$\Delta V_{IN} = 0.5V$		2.9			3.2		ns
Propagation Delay	$\Delta V_{IN} = 0.5V$		1.2			1.5		ns
Harmonic Distortion	f>1kHz		<0.1			<0.1		%
MTBF[3] Meantime Between Failure	5.5×10^6 hours							
PACKAGE OPTION[4]	H12A							

---

[1] Unless otherwise specified, these specifications apply for +15V applied to pins 1 and 12, -15V applied to pins 9 and 10, and pin 6 connected to pin 7.

[2] Unless otherwise noted, specifications apply over a temperature range, $-55°C < T_C < +125°C$ for the ADLH0033G, and $-25°C < T_C < +85°C$ for the ADLH0033CG. Typical values shown are for $T_C = 25°C$.

[3] ADLH0033G/883 calculated per Mil Handbook 217. Ground: Fixed; Temperature (case) = 70°C.

[4] See Section 20 for package outline information.

[5] Specifies processing to MIL-883B.

Specifications subject to change without notice.

ORDERING INFORMATION

Model	Temperature Range
ADLH0033CG	-25°C to +85°C
ADLH0033G	-55°C to +125°C
ADLH0033G/883[5]	-55°C to +125°C

Applying the ADLH0033G/ADLH0033CG

LAYOUT CONSIDERATIONS

As is the case with any high-speed design, proper layout is critical to avoid the introduction of unnecessary errors due to high-frequency coupling, stray capacitance, and the like.

Large ground planes should be used whenever possible to provide a low resistance, low inductance circuit path, as well as shielding the effects of high-frequency coupling. Sockets should be avoided, as the increased inter-lead capacitance can degrade bandwidth. Input and output connections should be kept as short as practical.

OFFSET ADJUSTMENT

The ADLH0033G/ADLH0033CG are factory trimmed for output voltage offsets well within the guaranteed limits, thereby eliminating the need to calibrate each device individually. To use this feature, simply connect Pin 6 (OFFSET PRESET) to Pin 7 (OFFSET ADJUST).

When it is desirable to eliminate any errors due to output offsets, the circuit of Figure 1 may be used to adjust these errors to zero.

SHORT CIRCUIT PROTECTION

The circuit of Figure 2 is used to protect the ADLH0033G/ ADLH0033CG from short circuits on the output. The value of R_{LIM} is determined by the following:

$$R_{LIM} \cong \frac{V+}{I_{sc}} = \frac{V-}{I_{sc}}$$

Where I_{sc} = Output Current under short circuit conditions $\leqslant$100mA.

Note that output voltage swing will also be somewhat limited in this configuration; however, decoupling of Pins 1 and 9 through disc type capacitors to ground as shown in Figure 2 will restore full output swing and slew rate.

OPERATION WITH ASYMMETRICAL SUPPLIES

Since Symmetrical Power Supplies may not always be desirable or available, the ADLH0033G/ADLH0033CG is designed to operate on Asymmetrical Supplies. This causes an apparent output offset; however, this is because of the amplifier's gain of less than unity. To accurately predict the output voltage shift due to Asymmetrical Supplies, use the following formula:

$$A_{VO} \cong (1 - A_V)\,\frac{(V+ - V-)}{2} = 0.005\,(V+ - V-)$$

Where A_V = No Load Voltage Gain, typically 0.99
V+ = Positive Supply Voltage
V− = Negative Supply Voltage

Of course, these apparent offsets may be adjusted to zero by using the circuit shown in Figure 1, OFFSET ADJUSTMENT.

CAPACITIVE LOADING

The ADLH0033G/ADLH0033CG have been designed to drive capacitive loads of several thousand picofarads (such as coaxial cable) without oscillation. In these applications, peak current resulting from (C X dv/dt) should be limited below the absolute maximum peak current rating of ±250mA.

Also, power dissipation due to driving capacitive loads plus standby power should be kept below the total power rating of 1.5W.

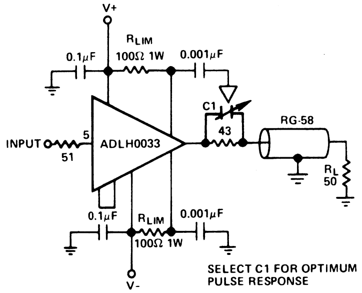


Figure 3. Coaxial Cable Drive

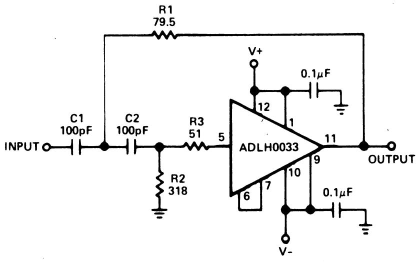


Figure 4. Wideband Two Pole High Pass Filter

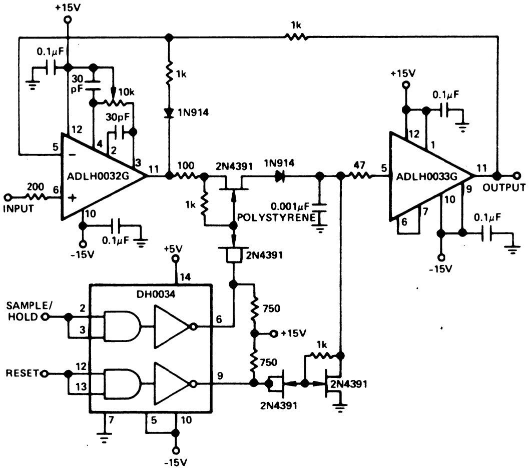


Figure 5. High Speed Peak Detector

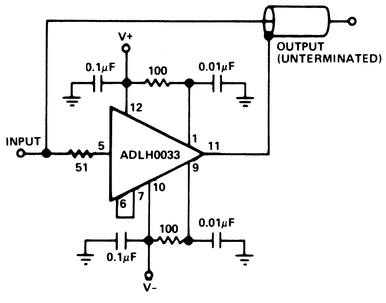
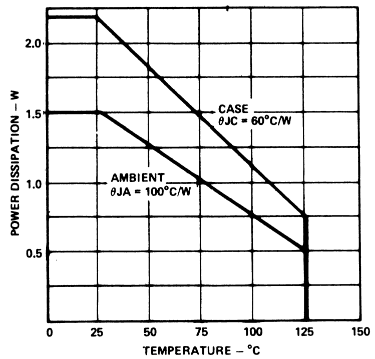
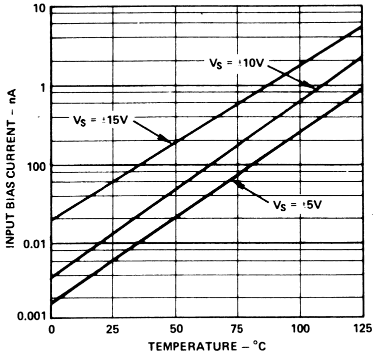


Figure 6. High Speed Shield/Line Driver

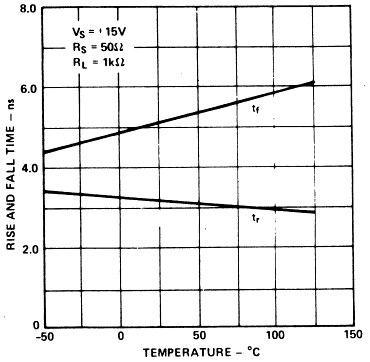
Typical Performance Curves



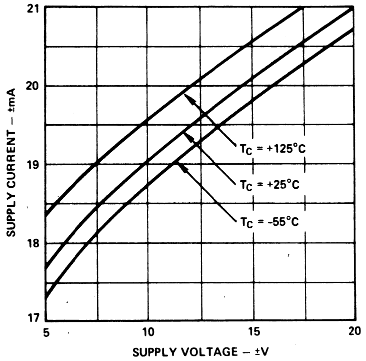
Power Dissipation vs Temperature



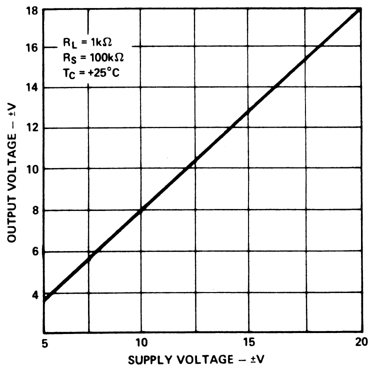
Input Bias Current vs Temperature



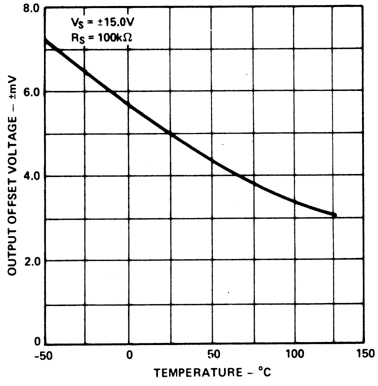
Rise and Fall Time vs Temperature



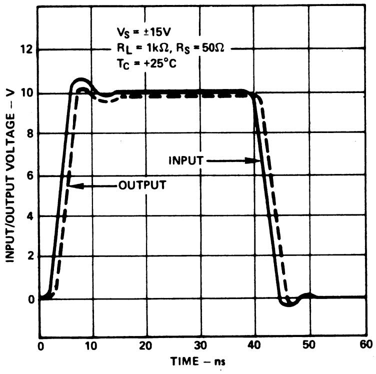
Supply Current vs Supply Voltage



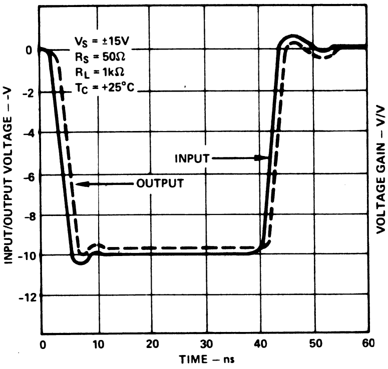
Output Voltage vs Supply Voltage



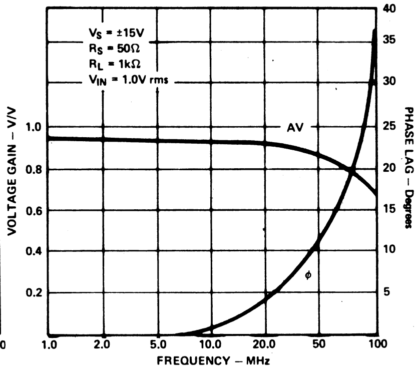
Output Offset Voltage vs Temperature



Positive Pulse Response



Negative Pulse Response



Frequency Response

ANALOG DEVICES

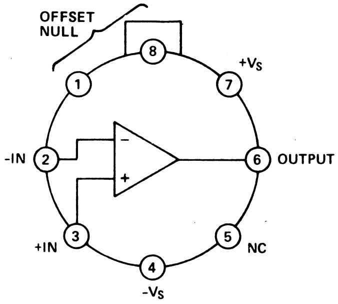
Ultra-Low Offset Voltage Op Amp

AD OP-07

FEATURES

Ten Times More Gain Than Other OP-07 Devices (3.0M min)
Ultra-Low Offset Voltage: 10μV
Ultra-Low Offset Voltage Drift: 0.2μV/°C
Ultra-Stable vs. Time: 0.2μV/month
Ultra-Low Noise: 0.35μV p-p
No External Components Required
Monolithic Construction
High Common Mode Input Range: ±14.0V
Wide Power Supply Voltage Range: ±3V to ±18V
Fits 725, 108A/308A, 741 Sockets

AD OP-07 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW

PRODUCT DESCRIPTION

The AD OP-07 is an improved version of the industry-standard OP-07 precision operational amplifier. A guaranteed minimum open-loop voltage gain of 3,000,000 (AD OP-07A) represents an order of magnitude improvement over older designs; this affords increased accuracy in high closed loop gain applications. Input offset voltages as low as 10μV, bias currents of 0.7nA, internal compensation and device protection eliminate the need for external components and adjustments. An input offset voltage temperature coefficient of 0.2μV/°C and long-term stability of 0.2μV/month eliminate recalibration or loss of initial accuracy.

A true differential operational amplifier, the AD OP-07 has a high common mode input voltage range (±14V) high common mode rejection ratio (up to 126dB) and high differential input impedance (50MΩ); these features combine to assure high accuracy in noninverting configurations. Such applications include instrumentation amplifiers, where the increased open-loop gain maintains high linearity at high closed-loop gains.

The AD OP-07 is available in five performance grades. The AD OP-07E, AD OP-07C and AD OP-07D are specified for operation over the 0 to +70°C temperature range, while the AD OP-07A and AD OP-07 are specified for -55°C to +125°C operation. Processing to the requirements of MIL-STD-883, Class B, is available on the AD OP-07 and AD OP-07A. All devices are packaged in TO-99 hermetically-sealed metal cans.

PRODUCT HIGHLIGHTS

1. Increased open-loop voltage gain (3.0 million, min) results in better accuracy and linearity in high closed-loop gain applications.
2. Ultra-low offset voltage and offset voltage drift, combined with low input bias currents, allow the AD OP-07 to maintain high accuracy over the entire operating temperature range.
3. Internal frequency compensation, ultra-low input offset voltage and full device protection eliminate the need for additional components. This reduces circuit size and complexity and increases reliability.
4. High input impedances, large common mode input voltage range and high common mode rejection ratio make the AD OP-07 ideal for noninverting and differential instrumentation applications.
5. Monolithic construction along with advanced circuit design and processing techniques result in low cost.
6. The input offset voltage is trimmed at the wafer stage. Unmounted chips are available for hybrid circuit applications.

SPECIFICATIONS (T_A = +25°C, V_S = ±15V, unless otherwise specified)

MODEL		AD OP-07E			AD OP-07C			AD OP-07D		
PARAMETER	SYMBOL	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
OPEN LOOP GAIN	A_{VO}	2,000	5,000		1,200	4,000		1,200	4,000	
		1,800	4,500		1,000	4,000		1,000	4,000	
		300	1,000		300	1,000		300	1,000	
OUTPUT CHARACTERISTICS										
Maximum Output Swing	V_{OM}	±12.5	±13.0		±12.0	±13.0		±12.0	±13.0	
		±12.0	±12.8		±11.5	±12.8		±11.5	±12.8	
		±10.5	±12.0			±12.0				
		±12.0	±12.6		±11.0	±12.6		±11.0	±12.6	
Open-Loop Output Resistance	R_O		60			60			60	
FREQUENCY RESPONSE										
Closed Loop Bandwidth	BW		0.6			0.6			0.6	
Slew Rate	SR		0.17			0.17			0.17	
INPUT OFFSET VOLTAGE										
Initial	V_{OS}		30	75		60	150		60	150
			45	130		85	250		85	250
Adjustment Range			±4			±4			±4	
Average Drift										
No External Trim	TCV_{OS}		0.3	1.3		0.5	(Note 3) 1.8		0.7	(Note 3) 2.5
With External Trim	TCV_{OSN}		0.3	1.3		0.4	1.6 (Note 3)		0.7	2.5 (Note 3)
Long Term Stability	V_{OS}/Time		0.3	1.5		0.4	2.0		0.5	3.0
INPUT OFFSET CURRENT										
Initial	I_{OS}		0.5	3.8		0.8	6.0		0.8	6.0
			0.9	5.3		1.6	8.0		1.6	8.0
Average Drift	TCI_{OS}		8	35 (Note 3)		12	50 (Note 3)		12	50 (Note 3)
INPUT BIAS CURRENT										
Initial	I_B		±1.2	±4.0		±1.8	±7.0		±2.0	±12
			±1.5	±5.5		±2.2	±9.0		±3.0	±14
Average Drift	TCI_B		13	35 (Note 3)		18	50 (Note 3)		18	50 (Note 3)
INPUT RESISTANCE										
Differential	R_{IN}	15	50		8	33		7	31	
Common Mode	R_{IN} CM		160			120			120	
INPUT NOISE										
Voltage	e_n p-p		0.35	0.6		0.38	0.65		0.38	0.65
Voltage Density	e_n		10.3	18.0		10.5	20.0		10.5	20.0
			10.0	13.0		10.2	13.5		10.2	13.5
			9.6	11.0		9.8	11.5		9.8	11.5
Current	i_n p-p		14	30		15	35		15	35
Current Density	i_n		0.32	0.80		0.35	0.90		0.35	0.90
			0.14	0.23		0.15	0.27		0.15	0.27
			0.12	0.17		0.13	0.18		0.13	0.18
INPUT VOLTAGE RANGE										
Common Mode	CMVR	±13.0	±14.0		±13.0	±14.0		±13.0	±14.0	
		±13.0	±13.5		±13.0	±13.5		±13.0	±13.5	
Common Mode Rejection Ratio	CMRR	106	123		100	120		94	110	
		103	123		97	120		94	106	
POWER SUPPLY										
Current, Quiescent	I_Q		3.0	4.0		3.5	5.0		3.5	5.0
Power Consumption	P_D		90	120		105	150		105	150
			6.0	8.4		6.0	8.4		6.0	8.4
Rejection Ratio	PSRR	94	107		90	104		90	104	
		90	104		86	100		86	100	
OPERATING TEMPERATURE RANGE	T_{min}, T_{max}	0		+70	0		+70	0		+70
PACKAGE OPTION[5]										
TO-99 Style – (H08B)			AD OP-07EH			AD OP-07CH			AD OP-07DH	
Mini-Dip – (N8A)			AD OP-07EN			AD OP-07CN			AD OP-07DN	

NOTES:

[1] The AD OP-07A and AD OP-07 are available processed to MIL-STD-883, Class B. Order AD OP-07AH-883B or AD OP-07H-883B.

[2] Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. Additionally, AD OP-07A offset voltage is measured five minutes after power supply application at 25°C, -55°C and +125°C.

[3] Parameter is not 100% tested; 90% of units meet this specification.

[4] Long Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods of time and is extrapolated from high temperature test data. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV – Parameter is not 100% tested: 90% of units meet this specification.

[5] See Section 20 for package outline information.

Specifications subject to change without notice.

AD OP-07A[1]			AD OP-07[1]				
MIN	TYP	MAX	MIN	TYP	MAX	TEST CONDITIONS	UNITS
3,000	5,000		2,000	5,000		$R_L \geq 2k\Omega$, $V_O = \pm10V$	V/mV
2,000	4,000		1,500	4,000		$R_L \geq 2k\Omega$, $V_O = \pm10V$, T_{min} to T_{max}	V/mV
300	1,000		300	1,000		$R_L \geq 500\Omega$, $V_O = \pm0.5V$, $V_S = \pm3V$	V/mV
±12.5	±13.0		±12.5	±13.0		$R_L \geq 10k\Omega$	V
±12.0	±12.8		±12.0	±12.8		$R_L \geq 2k\Omega$	V
±10.5	±12.0		±10.5	±12.0		$R_L \geq 1k\Omega$	V
±12.0	±12.6		±12.0	±12.6		$R_L \geq 2k\Omega$, T_{min} to T_{max}	V
	60			60		$V_O = 0$, $I_O = 0$	Ω
	0.6			0.6		$A_{VCL} = +1.0$	MHz
	0.17			0.17		$R_L \geq 2k$	V/µs
	10	25		30	75	Note 2	µV
	25	60		60	200	Note 2, T_{min} to T_{max}	µV
	±4			±4		$R_P = 20k\Omega$	mV
	0.2	0.6		0.3	1.3	T_{min} to T_{max}	µV/°C
	0.2	0.6		0.3	1.3	$R_P = 20k\Omega$, T_{min} to T_{max}	µV/°C
	0.2	1.0		0.2	1.0	Note 4	µV/Month
	0.3	2.0		0.4	2.8		nA
	0.8	4.0		1.2	5.6	T_{min} to T_{max}	nA
	5	25		8	50	T_{min} to T_{max}	pA/°C
	±0.7	±2.0		±1.0	±3.0		nA
	±1.0	±4.0		±2.0	±6.0	T_{min} to T_{max}	nA
	8	25		13	50	T_{min} to T_{max}	pA/°C
30	80		20	60			MΩ
	200			200			GΩ
	0.35	0.6		0.35	0.6	0.1Hz to 10Hz, Note 3	µV p-p
	10.3	18.0		10.3	18.0	$f_O = 10Hz$, Note 3	nV/√Hz
	10.0	13.0		10.0	13.0	$f_O = 100Hz$, Note 3	nV/√Hz
	9.6	11.0		9.6	11.0	$f_O = 1kHz$, Note 3	nV/√Hz
	14	30		14	30	0.1Hz to 10Hz, Note 3	pA p-p
	0.32	0.80		0.32	0.80	$f_O = 10Hz$, Note 3	pA/√Hz
	0.14	0.23		0.14	0.23	$f_O = 100Hz$, Note 3	pA/√Hz
	0.12	0.17		0.12	0.17	$f_O = 1kHz$, Note 3	pA/√Hz
±13.0	±14.0		±13.0	±14.0			V
±13.0	±13.5		±13.0	±13.5		T_{min} to T_{max}	V
110	126		110	126		$V_{CM} = \pm CMVR$	dB
106	123		106	123		$V_{CM} = \pm CMVR$, T_{min} to T_{max}	dB
	3.0	4.0		3.0	4.0	$V_S = \pm15V$	mA
	90	120		90	120	$V_S = \pm15V$	mW
	6.0	8.4		6.0	8.4	$V_S = \pm3V$	mW
100	110		100	110		$V_S = \pm3V$ to $\pm18V$	dB
94	106		94	106		$V_S = \pm3V$ to $\pm18V$, T_{min} to T_{max}	dB
-55		+125	-55		+125		°C
	AD OP-07AH –			AD OP-07H –			

ABSOLUTE MAXIMUM RATINGS

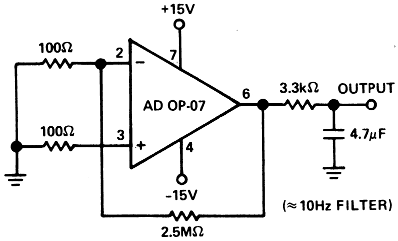
Supply Voltage	±22V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±22V
Output Short Circuit Duration	Indefinite
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
OP-07A, OP-07	-55°C to +125°C
OP-07E, OP-07C, OP-07D	0 to +70°C
Lead Temperature Range (Soldering, 60sec)	300°C

NOTES:

Note 1: Maximum package power dissipation vs. ambient temperature.

Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (H)	80°C	7.1mW/°C

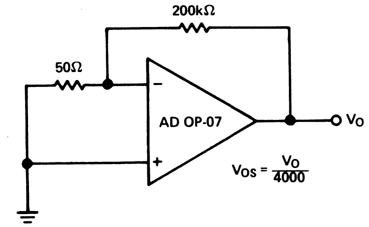
Note 2: For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.



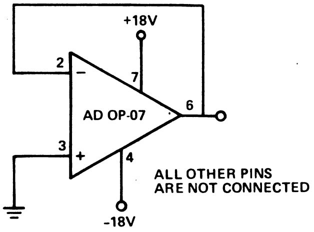
INPUT REFERRED NOISE = $\frac{V_O}{25{,}000} = \frac{5mV/cm}{25{,}000}$ = 200nV/cm

SEE NOISE PHOTO, NEXT PAGE

Low Frequency Noise Test Circuit



Offset Voltage Test Circuit



Burn-In Circuit

Applying the AD OP-07

The AD OP-07 may be directly substituted for other OP-07's as well as 725, 108/208/308, 108A/208A/308A, 714, OP-05 or LM11 devices, with or without removal of external frequency compensation or offset nulling components. If used to replace 741 devices, offset nulling components must be removed (or referenced to $+V_S$). Input offset voltage of the AD OP-07 is very low, but if additional nulling is required, the circuit shown in Figure 1 is recommended.

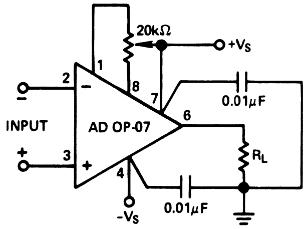


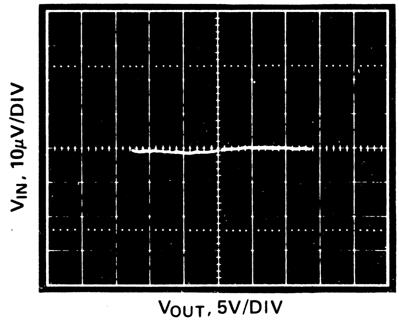
Figure 1. Optional Offset Nulling Circuit and Power Supply Bypassing

The AD OP-07 provides stable operation with load capacitances up to 500pF and ±10V swings; larger capacitances should be decoupled with 50Ω resistor.

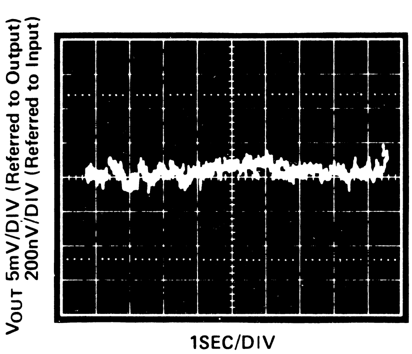
Stray thermoelectric voltages generated by dissimilar metals (thermocouples) at the contacts to the input terminals can prevent realization of the drift performance indicated. Best operation will be obtained when both input contacts are maintained at the same temperature, preferably close to the temperature of the device's package.

Although the AD OP-07 features high power supply rejection, the effects of noise on the power supplies may be minimized by bypassing the power supplies as close to pins 4 and 7 of the AD OP-07 as possible, to load ground with a good-quality 0.01µF ceramic capacitor as shown in Figure 1.

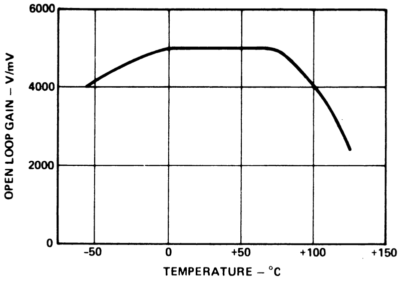
Performance Curves (typical @ T_A = +25°C, V_S = ±15V, AD OP-07 Grade Device unless otherwise noted)



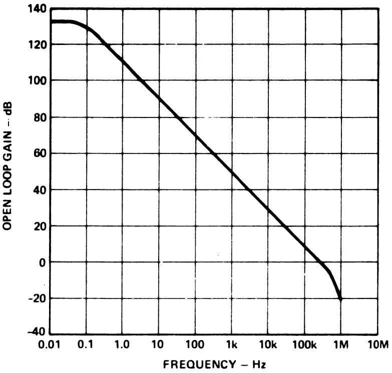
AD OP-07 Open Loop Gain Curve



AD OP-07 Low Frequency Noise (See Test Circuit, on the Previous Page)

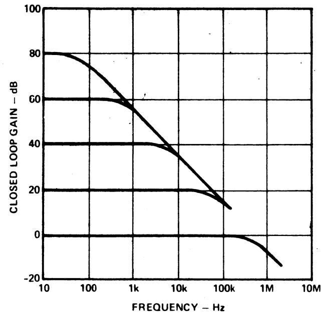


Open Loop Gain vs. Temperature

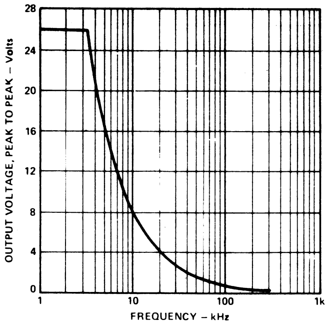


Open Loop Frequency Response

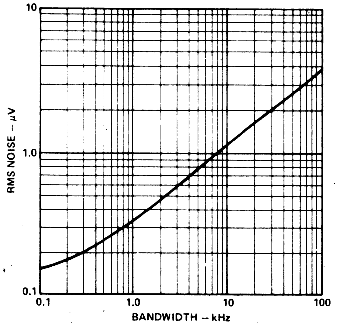
Typical Performance Curves



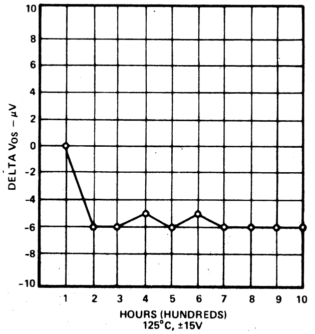
Closed Loop Response for Various Gain Configurations



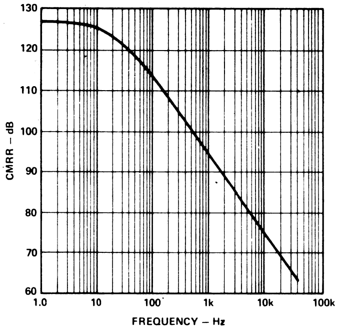
Maximum Undistorted Output vs. Frequency



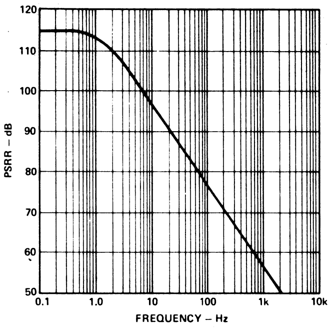
Input Wideband Noise vs. Bandwidth (0.1Hz to Frequency Indicated)



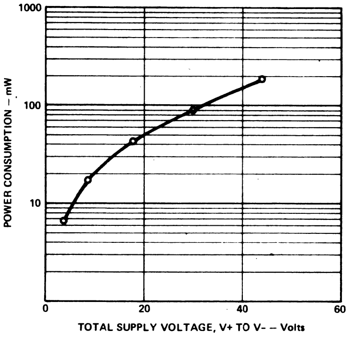
Offset Voltage vs. Time



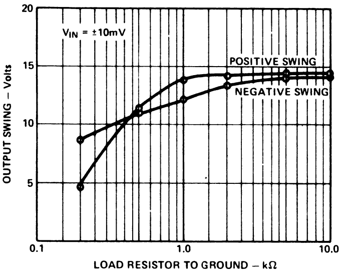
CMRR vs. Frequency



PSRR vs. Frequency



Power Consumption vs. Power Supply



Output Voltage vs. Load Resistance

ANALOG DEVICES

Fast Settling Video Operational Amplifier

HOS-050, 050A, 050C

FEATURES

80ns Settling to 0.1%; 200ns to 0.01%
100MHz Gain Bandwidth Product
55MHz 3dB Bandwidth
100mA Output @ ±10V

APPLICATIONS

D/A Current Converter
Video Pulse Amplifier
CRT Deflection Amplifier
Wideband Current Booster

GENERAL DESCRIPTION

The HOS-050, HOS-050A, and HOS-050C op amps are very high speed wideband operational amplifiers designed to complement the Analog Devices' lines of high speed data acquisition products. They feature a 100MHz gain bandwidth product; slew rate of 300V/µs; and settling time of 80ns to ±0.1%.

The HOS-050A, HOS-050, and HOS-050C have typical input offset voltages of 10mV, 25mV, and 45mV, respectively.

All models have a rated output of ±100mA minimum, and an exceptional noise spec of only 7µV rms, dc to 2MHz; they are ideally suited for a broad range of video applications.

FAST-SETTLING OP AMPS

At one time, operational amplifiers could be specified according to slew rates, bandwidth, and drive capability; and these parameters would be sufficient. Settling time was not considered until the use of high speed video D/A converters became widespread.

The conversion speed of the D/A can be limited by the settling time of the output amplifier, so it has become essential to select an op amp whose settling time is compatible with the D/A converter.

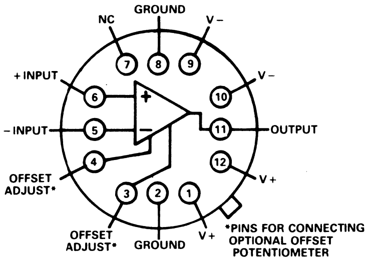
The increased emphasis on settling time has, in some cases, created a preoccupation with slew rates in the minds of some designers. But slew rate is only one component in establishing settling time.

The amount of overshoot, and the ringing which are present at the end of a step function change also have an effect. These parameters, in turn, are influenced by the bandwidth (or lack of it) when operating the op amp with closed loop gains greater than one.

The HOS-050 Series stands up under close scrutiny of these characteristics because of its 100MHz gain bandwidth product. The use of these amplifiers in a wide variety of applications has confirmed their suitability for video circuits.

The HOS-050 is also available with MIL-883 processing. Model numbers change from HOS-050 to HOS-050B; and HOS-050A to HOS-050AB.

HOS-050/A/C FUNCTIONAL BLOCK DIAGRAM



TO-8
BOTTOM VIEW

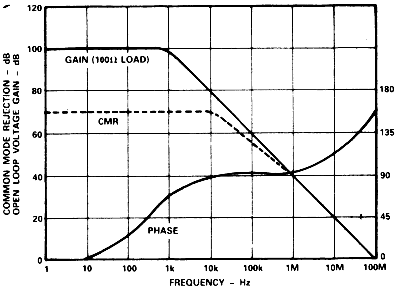


Figure 1. HOS-050 Frequency Response

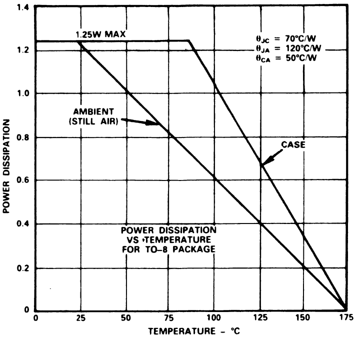


Figure 2. Power Dissipation vs. Temperature

SPECIFICATIONS (typical @ +25°C and ± 15V unless otherwise specified)

Model	HOS-050	HOS-050A	HOS-050C
ABSOLUTE MAXIMUM RATINGS			
Supply Voltages (V_S)	± 18V	*	*
Power Dissipation	See Figure 2	*	*
Input Voltage	± V_S	*	*
Differential Input Voltage	± V_S	*	*
Operating Temperature Range (case)	− 55°C to + 125°C	*	− 25°C to + 85°C
Junction Temperature	175°C	*	*
Storage Temperature Range	− 65°C to + 150°C	*	*
Lead Temperature (soldering, 10 sec.)	300°C	*	*

DC ELECTRICAL CHARACTERISTICS

Parameter	Conditions	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
Open Loop Gain	R_L = 100Ω		100			*			*		dB
Rated Output	R_L = >100Ω										
Voltage		± 10/8			*			*			V
Current											
(not short circuit protected)		± 100			*			*			mA
Voltage	R_L = >200Ω	± 10			*			*			V
Input Offset Voltage	Adjustable to Zero										
Initial	@ + 25°C		25	35		10	15		45	65	mV
vs. Temperature			50	150		20	35		75	200	µV/°C
vs. Power Supply Voltage			0.5			*			*		mV/V
Input Bias Current											
Initial	@ + 25°C		1	2		*	*		*	*	nA
vs. Temperature			Doubles			*			*		/10°C
Input Offset Current											
Initial	@ + 25°C		± 100			*			*		nA
Input Impedance											
Differential	}In parallel with 5pF		10^{10}			*			*		Ω
Common Mode			10^{10}			*			*		Ω
Input Voltage Range											
Common Mode		± 10		± 18	*		*	*		*	V
Differential				± 18			*			*	V
Common Mode Rejection			70			*			*		dB
Input Noise	R_{FF} = 100Ω; R_{FB} = 1kΩ										
dc to 100kHz			5			*			*		µV rms
dc to 2MHz			7			*			*		µV rms

AC ELECTRICAL CHARACTERISTICS[1]

Parameter	Conditions	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
Slew Rate	A = − 1; R_{FF} = R_{FB} = 500Ω; Load = 100Ω		300			*			*		V/µs
Noninverting Slew Rate	A = 2; R_{FF} = R_{FB} = 1000Ω; Load = 100Ω		320			*			*		V/µs
Overload Recovery	50% Overdrive		400			*			*		ns
Gain Bandwidth Product	R_{FF} = R_{FB} = 500Ω		100			*			*		MHz
Small Signal Bandwidth, − 3dB	A = − 1; R_{FF} = R_{FB} = 500Ω		45			*			*		MHz
	A = − 1; R_{FF} = R_{FB} = 1000Ω		35			*			*		MHz
	A = − 2; R_{FF} = R_{FB} = 500Ω; R_{FB} = 1000Ω		35			*			*		MHz
	A = − 4; R_{FF} = R_{FB} = 250Ω; R_{FB} = 1000Ω		30			*			*		MHz
Output Impedance				<1			*			*	Ω
Noninverting Bandwidth, − 3dB	A = 2; R_{FF} = R_{FB} = 1000Ω; 100Ω load; 10pF capacitance										
	5-volt p-p output		25			*			*		MHz
	4-volt p-p output		30			*			*		MHz
	2-volt p-p output		55			*			*		MHz
	A = 3; R_{FF} = 500Ω; R_{FB} = 1000Ω; 100Ω, 1000 Ω; or 2000Ω load; 10pF capacitance										
	10-volt p-p output		17			*			*		MHz
	5-volt p-p output		25			*			*		MHz

AC ELECTRICAL CHARACTERISTICS[1] (Continued)

Parameter	Conditions	HOS-050			HOS050A			HOS-050C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Noninverting Bandwidth, −3dB (continued)	A = 5; R_{FF} = 500Ω; R_{FB} = 2000Ω; 100Ω, 1000Ω, or 2000Ω load/10pF capacitance										
	5-volt p-p output		15			*			*		MHz
	4-volt p-p output		30			*			*		MHz
	2-volt p-p output		40			*			*		MHz
	1-volt p-p output		40			*			*		MHz
Full Power Bandwidth	Output = + 10V/ − 8V @ ± 100mA; 5% distortion		5			*			*		MHz
Settling Time to 0.1%	A = − 1; R_{FF} = R_{FB} = 500Ω										
Inverting	V_{OUT} = ±5V										
(See Figure 5)	V_{OUT} = ±2.5V										
Noninverting	A = 2; R_{FF} = R_{FB} = 500Ω										
	Max Load capacitance = 75pF										
	V_{OUT} = ±5V		200			*			*		ns
	V_{OUT} = ±2.5V		135			*			*		ns
Harmonic Distortion (See Figure 9)	A = − 1; Load = 1000Ω Signal = 4MHz; 2V output		−63			*			*		dB
Noninverting Harmonic Distortion (See Figure 10)	A = 2; R_{FF} = R_{FB} = 1000Ω; Load = 1000Ω; Signal = 4MHz; 2V output		−59			*			*		dB
Power Supply											
Voltage	Rated performance		± 15			*			*		V dc
Voltage	Operating range	± 12		± 18	*		*	*		*	V dc
Current	Quiescent		± 20	± 25		*	*		*	*	mA
Power Consumption	Quiescent		0.6			*			*		W
Power Dissipation				1.25			*			*	W
Temperature Range											
Operating (Case)	(See Figure 2 for	− 55		+ 125	*		*	− 25		+ 85	°C
Storage	Derating Information)	− 65		+ 150	*		*	*		*	°C
Meantime Between Failures (MTBF)	MIL-HNBK 217; Ground; Fixed; Case = 70°C 883B Processing	2.78 × 10^6			*			*			Hours

Notes:

[1] Specification for Inverting Mode unless otherwise noted.

*Specification same as HOS-050

Individual socket assemblies (one per pin) are available from AMP as part number 6-330808-0.

Specifications subject to change without notice.

PIN DESIGNATIONS[1]

PINS	FUNCTION
1	+V
2	GROUND
3	OFFSET ADJ*
4	OFFSET ADJ*
5	− INPUT
6	+ INPUT
7	NC
8	GROUND
9	−V
10	−V
11	OUTPUT
12	+V

[1] SEE SECTION 20 (H12A) FOR PACKAGE OUTLINE INFORMATION.

*PINS FOR CONNECTING OPTIONAL OFFSET POTENTIOMETER.

VOLTAGE AMPLIFIERS/CURRENT BOOSTERS

Video op amps such as the HOS-050 are generally characterized by high gain bandwidth products, fast settling times, and high output drive.

One of the most common uses of video op amps is for D/A converter output voltage amplification or current boosting. Figure 3 is one example of this type of application. In this circuit, the internal resistance of the D/A is the feed forward resistor for the op amp.

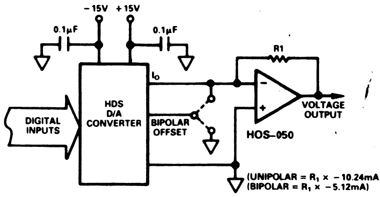


Figure 3. Inverting Unipolar or Bipolar Voltage Output

The HDS Series D/A converters are fast-settling, current output D/As available in 8-, 10-, and 12-bit resolutions. Both TTL and ECL versions are available, and settling times range from 10ns for 8-bit units through 40ns for 12-bit units.

The circuit which is shown will provide a negative unipolar output with binary coding on the input, and bipolar offset grounded. It will provide a bipolar output with complementary offset binary coding on the input, and bipolar offset connected to I_O.

An approximation of the total settling time for the D/A op amp combination is calculated by:

$$T_S = \sqrt{T_D{}^2 + T_O{}^2}$$

where T_D is D/A settling time and T_O is HOS-050 settling time.

This approximation is valid because both the D/A and the HOS-050 exhibit 6dB/octave roll-off charateristics (single pole response); and the combination of low D/A output capacitance and op amp input capacitance does not materially affect the formula.

The user of the HOS-050 should remember the current flowing in the feedback resistor (R1) must be subtracted from the output available from the HOS-050.

There is a tendency, because of this fact, to use a high value of feedback resistor to assure maximum current drive being available for driving low impedances; but this approach may create undesirable side effects.

Calculating the minimum load that can be driven under two conditions of feedback resistor values will serve to illustrate the difference.

Assume the feedback resistor value is 500Ω. If output voltage of the HOS-050 is 10 volts, and output current is 100mA, minimum load would be:

$$\frac{E_O \max}{I_O \max - I_{RFB}} = \frac{10V}{100mA - 20mA} = \frac{10V}{80mA} = 125\Omega \text{ minimum load}$$

where: E_O max = peak voltage needed
I_O max = maximum continuous current HOS-050 can produce
I_{RFB} = current in feedback resistor at peak voltage

Assume the feedback resistor value is 5,000Ω. Minimum load would be:

$$\frac{E_O \max}{I_O \max - I_{RFB}} = \frac{10V}{100mA - 2mA} = \frac{10V}{98mA} = 102\Omega \text{ minimum load}$$

Designs which strive for driving a minimum load (by increasing the feedback resistor) can create settling problems because of a fundamental characteristic of op amp circuits . . . the higher the feedback resistance, the slower the system response.

This phenomenon is the result of increased impedance for driving stray capacitances in the circuit employing the op amp, and fixed capacitances in the summing node.

Impedances need to be kept as low as possible consistent with low distortion; and stray capacitances need to be eliminated to the maximum possible extent. A large ground plane structure is recommended to help assure low ground impedances. In addition, 0.1µF ceramic capacitors and 3-10µF tantalum capacitors connected as close as possible to power supply inputs will decrease the potential for parasitic oscillations and other noise signals.

Another argument for limiting the size of the feedback resistor is because of its effect on bandwidth. Bandwidth of the HOS-050 op amp and the value of the feedback resistor are inversely related.

At any given gain of the op amp, the gain setting with the widest bandwidth will be the one which employs the lower value of feedback. As an example, a gain of 1 can be achieved with $R_{FF} = R_{FB} = 500\Omega$; or $R_{FF} = R_{FB} = 1{,}000\Omega$. Small-signal bandwidth for the first combination is typically 45MHz; bandwidth for the second is typically 35MHz.

OFFSET AND GAIN ADJUSTMENT

Figure 4 shows a method of using the HOS-050 op amp which allows adjusting the offset and gain of the output voltage.

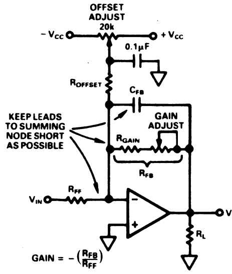


Figure 4. HOS–050 Offset and Gain Adjust

As shown, the gain of the circuit is established by the equation:

$$G = -\left(\frac{R_{FB}}{R_{FF}}\right)$$

where R_{FB} is the total of R_{GAIN} and Gain Adjust.

Once the user has established the desired gain for the illustrated circuit, the value of R_{FB} can be used to determine the correct value of R_{OFFSET} with the equation:

$$R_{OFFSET} = -\left(\frac{V_{CC} \times R_{FB}}{\Delta E_O}\right)$$

where ΔE_O is the desired amount of offset on the output.

Assume $\pm V_{CC} = \pm 15V$; $R_{GAIN} = 900\Omega$; Gain Adjust = 100Ω; the desired change on the output = ±1 volt.

Under these conditions, R_{OFFSET} will be $15k\Omega$:

$$R_{OFFSET} = -\left(\frac{15V \times [900 + 100]}{1V}\right)$$

$$R_{OFFSET} = -\left(\frac{15kV}{1V}\right)$$

$$R_{OFFSET} = 15{,}000\Omega$$

Figure 4 shows bipolar output operation. If unipolar output is desired, the appropriate V_{CC} should be removed from the Offset Adjust potentiometer.

The $0.1\mu F$ capacitor attached to the wiper arm of the Offset Adjust control isolates the control and helps prevent adjustment noise from appearing on the output of the HOS-050.

C_{FB} can be any value between 0 and 20pF, depending on the value of R_{GAIN}; and should be selected to optimize settling time for the particular circuit layout in which the HOS-050 is being used.

The Gain Adjust control should be a low value, low inductance cermet trimming potentiometer.

Note: R_{FF}, R_{GAIN}, C_{FB} and R_{OFFSET} must be located as close to the summing node of the HOS-050 as physically possible. This helps prevent additional capacitance in the summing node and corresponding bad effects on frequency response and settling times.

Variable controls (such as Offset Adjust and Gain Adjust) should never be tied to the summing node of the op amp. Their correct electrical locations are those shown in Figure 4.

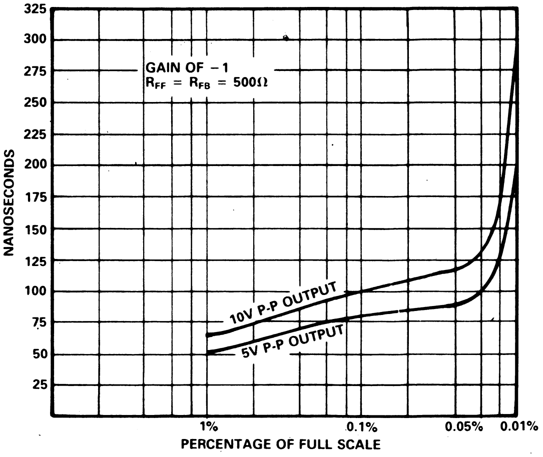


Figure 5. Settling Time – Inverting Mode

SETTLING TIME MEASUREMENT

Although there are some exceptions, most members of industry are in agreement on the description which says settling time is:

> The interval of time from the application of an ideal step function input until the closed-loop amplifier output has entered and remains within a specified error band.

The well-informed user needs to be alert to the consequences of settling time specs which do not meet that description.

This definition encompasses the major components which comprise settling time. They include (1) propogation delay through the amplifier; (2) slewing time to approach the final output value; (3) the time of recovery from the overload associated with slewing; and (4) linear settling to within the specified error band.

Expressed in these terms, the measurement of settling time is obviously a challenge and needs to be done accurately to assure the user that the amplifier is worth consideration for his application.

Figure 6 is the test circuit for measuring settling time to 0.1%. This method creates a "false" summing junction and the error band is observed at that point.

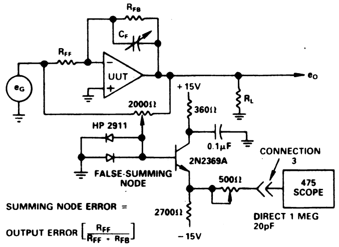


Figure 6. Settling Time Test Circuit for 0.1% Settling

If one were to attempt the measurement at the "true" summing junction of the op amp, the results would be misleading. All scope probes will add capacitance to the input and will change the response of the system. Making the measurement at the output of the amplifier is also impractical, since scope nonlinearities and reading inaccuracies caused by overdriving the scope preclude accurate measurements to the tolerances which are required.

The false summing junction method causes the amplifier to subtract the output from the input; only one-half the actual error appears at the false junction, and it can be measured to the required accuracies.

The false junction is clamped with diodes to limit the voltage excursion appearing at that point. This is necessary because the amplifier will be overdriven and one-half its input voltage will appear at the junction. Without the clamps, the scope used for making the measurement would be overdriven and its recovery time would mask the settling time of the amplifier.

The test circuit for measuring settling time to 0.01%, Figure 7, is simply an extension of the same basic technique. Measuring to the closer tolerance requires additional gain in the circuit driving the oscilloscope.

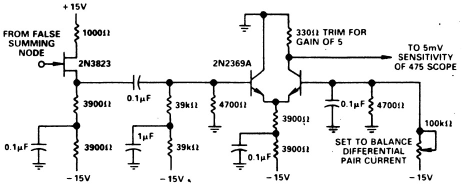


Figure 7. Settling Time Test Circuit for 0.01% Settling

IMPEDANCE MATCHING

The characteristics of the HOS-050 operational amplifier make it an ideal choice for matching the impedances of video circuits to the impedances of transmission lines.

In this application, source and load terminating resistors will cause the output voltage to be halved at the end of the cable being driven by the op amp. This makes it necessary to set the gain of the circuit to provide twice the desired voltage.

Three different values of resistors and cables are "phantomed" into the figure as examples of possible characteristic impedances which might be used. Figure 8 is *not* meant to imply the HOS-050 can drive three cables simultaneously.

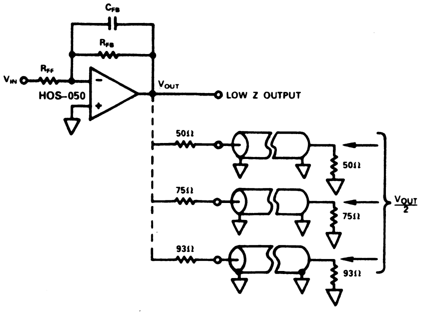


Figure 8. HOS-050 Impedance Matching

NONINVERTING OPERATION

The vast majority of video operational amplifiers display marked differences in settling times and bandwidths when operated in a noninverting mode instead of the inverting mode. There are a number of valid reasons for this characteristic.

Most high-speed op amps use feed-forward compensation for optimizing performance in the inverting mode. This is necessary to obtain wide gain-bandwidth products while maintaining dc performance in these types of devices. In effect, the op amp has a wideband ac channel which is not perfectly matched to the dc channel.

Feed-forward techniques enhance the performance of the op amp in the inverting mode by increasing the slew rate and small-signal bandwidth. These techniques, however, also decrease the amplifier's tolerance to stray capacitances, so must be employed judiciously.

The overall input capacitance of the op amp is kept as low as possible in the design; and any mismatch in the capacitance of the two channels appears as an error in the output. Because of the inherently low total input capacitance of the op amp, even a small capacitive mismatch between channels shows up as a large effective error signal.

Decreasing the channel mismatch can be achieved only by complicating the design of the op amp with additional components, and rigorous selection of those components in the manufacturing process.

As a consequence, the mismatch is reduced to the smallest practical value consistent with the economics of producing and using the op amp. But it remains a mismatch, and manifests itself as a difference in performance in the inverting versus noninverting modes.

There are video op amps available at low cost which use a 741-type amplifier for high dc open loop gain in the noninverting channel. The user of these kinds of designs may sometimes gain an economic advantage, but at a high cost in performance. Bandwidths for noninverting applications are often measured in kHz, not MHz, for this approach.

A video op amp is acting as a voltage mode device at both inputs when operating in the noninverting mode. This contrasts with the inverting mode, where it is operating as a current mode device.

The Analog Devices HOS-050 has different performance characteristics when operating as a noninverting amplifier, but the care used in the design makes the differences less pronounced than they are in many competing units.

The HOS-050 can be considered a true differential video op amp. It requires little or no external compensation because its rolloff characteristics approach a 6dB/octave slope. This helps the user determine summing errors and loop response; and helps assure the stability of the system.

The performance parameters for both inverting and noninverting operation are shown elsewhere in this data sheet (see SPECIFICATIONS section and figures). A comparison of the characteristics will highlight the similarities in performance, with the exceptions noted above.

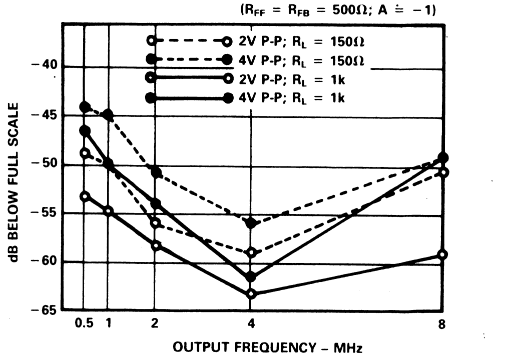


Figure 9. Harmonic Distortion – Inverting

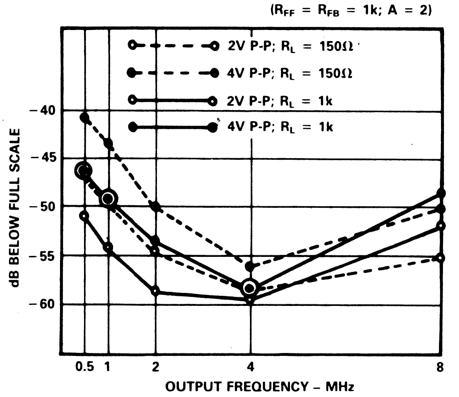


Figure 10. Harmonic Distortion – Noninverting

IN SUMMARY . . . A CAVEAT

Settling time specifications, bandwidth capabilities, harmonic distortion performance, and other parameters for video op amps cannot possibly include all possible situations and applications.

A multitude of seemingly insignificant conditions can have a major impact on the unit and its ability to operate in any given circuit.

The potential user is strongly urged to evaluate the effectiveness of the HOS-050 in the actual circuit in which it will be used. In many instances, the application conditions are different from the conditions used in specifying; there is no substitute for a trial in the proposed circuit to determine if the op amp will provide the desired results.

ANALOG DEVICES

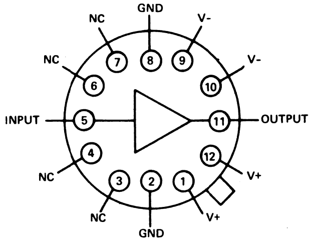
Wide Bandwidth, High Speed Buffer Amplifiers

HOS-100AH, 100SH

FEATURES
- Wide Bandwidth – dc to 125MHz
- High Slew Rate – 1500V/µs
- Operation Guaranteed -55°C to +125°C (SH)
- High Output Drive – ±10V with 100Ω Load
- MIL-STD-883 Processing Available

APPLICATIONS
- Current Boosters
- High Speed A/D Input Buffers
- Nuclear Instrumentation Amplifiers
- Coaxial Cable Drive
- High Speed Line Drivers
- Video Impedance Transformation

HOS-100SH/HOS-100AH
FUNCTIONAL BLOCK DIAGRAM



TO-8 PACKAGE
BOTTOM VIEW

GENERAL DESCRIPTION

The HOS-100SH and HOS-100AH Bipolar Buffer Amplifiers are high-speed, voltage follower/buffers designed to provide high-current drive at frequencies from dc to over 125MHz, as well as providing ±10mA into 1kΩ loads (±100mA peak) at slew rates of 1500V/µs. Both units also exhibit excellent phase linearity (2°), and low distortion (<0.1%).

For commercial temperature ranges the HOS-100AH is specified for operation over the range of -25°C to +85°C (case). The HOS-100SH is specified for operation over the military range of -55°C to +125°C (case). Further, the HOS-100SH may be processed to the requirements of MIL-STD-883.

The HOS-100SH and HOS-100AH are intended to fulfill a wide range of buffer applications, such as video impedance transformation, high impedance input buffers for A/D converters and comparators, as well as high-speed line drivers and nuclear instrumentation amplifiers. Additionally, both amplifiers will continuously drive 50Ω coaxial cables or serve as yoke drives in high resolution CRT displays.

They are particularly well suited for current booster applications (Figure 2) within an op-amp loop where input impedance and bias current requirements are less stringent than in FET design.

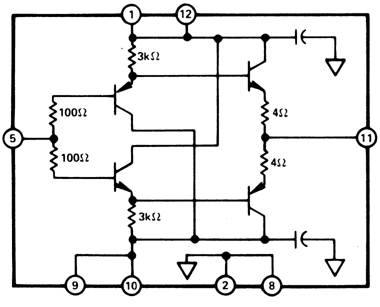


Figure 1. Schematic Diagram HOS-100

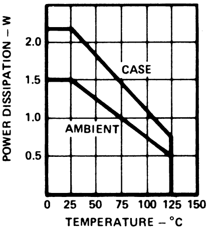


Figure 2. Power Derating

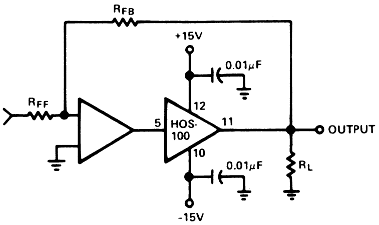


Figure 3. Current Booster

SPECIFICATIONS

PARAMETER	CONDITIONS	HOS-100SH MIN	HOS-100SH TYP	HOS-100SH MAX	HOS-100AH MIN	HOS-100AH TYP	HOS-100AH MAX	UNITS
DC ELECTRICAL CHARACTERISTICS[1,2]								
Input Bias Current	$T_C = 25°C$		5	20		5	25	μA
				25				μA
Input Impedance	V_{IN} = 1V rms, f = 1kHz R_L = 1k, $T_C = 25°C$	100	200		100	200		kΩ
Voltage Gain	V_{IN} = 1V rms, f = 1kHz R_L = 1k, $T_C = 25°C$	0.95	0.97	1.0	0.94	0.96	1.0	V/V
Output Offset Voltage	$R_S = 50Ω$, $T_C = 25°C$		5	10		10	25	mV
				25			35	mV
Output Offset Voltage T_C	$R_S = 50Ω$		25	75		25	75	μV/°C
Output Impedance	V_{IN} = 1V rms, f = 1kHz $R_S = 500Ω$, R_L = 1k		8	12		8	12	Ω
Output Voltage Swing	$R_S = 50Ω$, R_L = 1k	±12	±13		±12	±13		V
	V_S = ±5V, R_L = 1k		6			6		V
Supply Current	V_{IN} = 0V, $T_C = 25°C$							
	V_S = ±15		13	16		15	20	mA
	V_S = ±5		10			10		mA
Power Consumption	V_{IN} = 0V, V_S = ±15V $T_C = 25°C$		390	480		450	600	mW
AC ELECTRICAL CHARACTERISTICS[3]								
Slew Rate	V_{IN} = ±10V	1000	1500		1000	1400		V/μs
Bandwidth	V_{IN} = 1V rms	100	125		100	125		MHz
Rise Time	$ΔV_{IN}$ = 0.5V		2			2		ns
Propagation Delay	$ΔV_{IN}$ = 0.5V		1.5			1.5		ns
Phase Nonlinearity	BW = 1 to 20MHz		2			2		Degrees
Harmonic Distortion			<0.1			<0.1		%
MFBF[4]	>550,000 hours							
PACKAGE OPTION[5]	H12A							

NOTES

[1] Unless otherwise noted, these specifications apply for +15V applied to Pin 12, and −15V applied to Pin 10.

[2] Unless otherwise noted, specifications apply over a temperature range, $-55°C \leq T_C \leq +125°C$ for the HOS-100SH, and $-25°C \leq T_C \leq +85°C$ for the HOS-100AH. Typical values shown are for $T_C = +25°C$.

[3] These specifications all measured with following conditions: $T_C = +25°C$, $V_S = ±15V$, $R_S = 50Ω$, $R_L = 1k$.

[4] HOS-100SH/883 calculated using MIL Handbook 217. Ground: Fixed, Temperature (case) = 70°C.

[5] See Section 20 for package outline information.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V+ − V−)	40V
Maximum Power Dissipation	1.5W
Input Voltage	Equal to Supply Voltage
Maximum Continuous Output Current	±100mA
Maximum Peak Output Current	±250mA
Operating Temperature Range (Case)	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C
Maximum Junction Temperature	+175°C

ORDERING INFORMATION

Model	Temperature Range
HOS-100AH	−25°C to +85°C
HOS-100SH	−55°C to +125°C
HOS-100SH/883[1]	−55°C to +125°C

[1] Specifies 100% processing to MIL-STD-883 per Method 5008.

ANALOG DEVICES

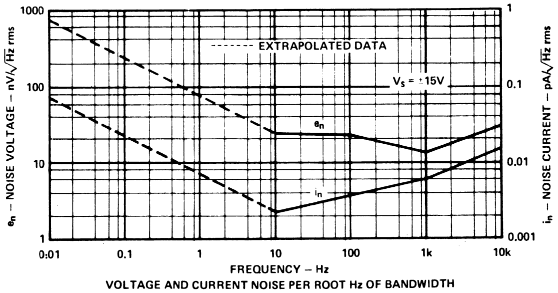
Low Noise, Low Drift Precision FET Amplifier

MODEL 52

FEATURES
Guaranteed Low Noise 1.5μV p-p max (0.01 to 1Hz)
Low Voltage Drift: 1μV/°C max (52K)
Low Bias Current: 3pA, max
High CMR: 100dB, min
High Voltage Gain: 120dB, min
Wide Power Supply Range: ±9V to ±18V
Excellent Long Term Stability: 5μV/month
Fast Thermal Response

APPLICATIONS
Low Level Instrumentation Preamp
High Impedance Precision Buffer
Long Term Integrator
Current to Voltage Converter
Precision Voltage Regulator
Preamp for 16-Bit Resolution V/F Converters

VOLTAGE AND CURRENT NOISE PER ROOT Hz OF BANDWIDTH



GENERAL DESCRIPTION
Model 52, a low noise, high accuracy FET input operational amplifier was designed for handling microvolt signals from high impedance (>100kΩ) sources. It features guaranteed low voltage noise (1.5μV p-p max, 0.01 to 1Hz bandwidth) with low input offset voltage drift (3μV/°C max, 52J; 1μV/°C max 52K). Unlike most available low drift amplifiers, model 52 voltage drift is unaffected by trimming the initial offset voltage (0.5mV max). The low input bias current (3pA max) is held constant over the entire ±10V common mode voltage range. High voltage gain (120dB, min) and high CMR (100dB, min) complete the performance profile. Model 52 is an excellent choice for high accuracy, high resolution linear signal processing applications.

By incorporating a new low noise N-channel monolithic FET input stage, thermal stability, voltage noise and differential signal performance are improved to a level previously obtainable only in the best bipolar amplifier designs. Model 52 is an excellent choice to replace chopper stabilized amplifiers where significant sources of error are introduced from zero beating, "chopper spikes" and ground loop currents.

The guaranteed accuracy performance of model 52 suggests critical applications such as low noise, low drift "front-end" preamplifiers for A to D converters and DVM's. For high impedance buffering applications, model 52 offers low input bias current, high linear common mode rejection, complete protection from input transients (offset voltage and bias current will not degrade due to reverse breakdown) and freedom from latch up when the common mode voltage range is exceeded. Model 52 is supplied in a reliable, compact epoxy module package. Output is protected from shorts to ground and/or supply voltage and is capable of driving up to 0.01μF load capacitance.

IMPROVED OFFSET VOLTAGE STABILITY
Model 52 has been designed for the lowest possible input voltage drift over the 0 to +70°C temperature range. In most operational amplifier designs, trimming is accomplished by unbalancing the current in the input stage. This trimming technique introduces an additional 2 to 12μV/°C for each millivolt of E_{OS} that is nulled. To provide performance consistent with low offset voltage drift, model 52 incorporates a three-point trim (see connection diagram) whereby a compensating voltage is introduced without unbalancing the input stage currents. By virtue of this trim scheme, there is no degradation in T.C. when E_{OS} is nulled and the specified performance is achieved.

IMPROVED NOISE PERFORMANCE
Input noise limits signal resolution in low level signal processing applications. The FET input stage of model 52 reduces noise current significantly from that of bipolar amplifiers, permitting high source impedance applications. Model 52 also offers voltage noise levels appreciably below that of other FET amplifiers. To illustrate the excellent low noise performance of model 52, Figure 1 shows typical input voltage noise in a 0.01 to 1Hz bandwidth. Noise is typically less than 1μV p-p and is free of noise spikes.

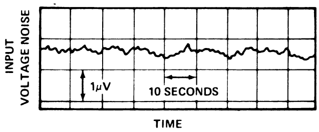


Figure 1. Voltage Noise 0.01 to 1Hz Bandwidth

For detailed information, contact factory.

SPECIFICATIONS (typical @ +25°C and ±15V unless otherwise noted)

MODEL	52J	52K
OPEN LOOP GAIN		
DC 2kΩ Load	120dB min (130dB typ)	*
RATED OUTPUT[1]		
Voltage, 2kΩ Load	±10V min	*
Current	±5mA min	*
Maximum Load Capacitance	0.01μF	*
Impedance, Open Loop	75Ω	*
FREQUENCY RESPONSE		
Unity Gain, Small Signal	500kHz	*
Full Power	4kHz min	*
Slew Rate	0.25V/μs min	*
Overload Recovery	130μs	*
Settling Time, ±0.1%, ±10V Step	100μs	*
Settling Time, ±0.01%, ±10V Step	150μs	*
INPUT OFFSET VOLTAGE		
Initial[2], @ +25°C	±500μV max	*
With External Trim Potentiometer	Adjustable to Zero	*
vs. Temperature (0 to +70°C)	±3μV/°C max	±1μV/°C max
vs. Supply Voltage	±2μV/%	*
vs. Time	±5μV/Month	*
Warm-Up Drift, 5 Minutes	±5μV	*
INPUT BIAS CURRENT		
Initial, @ +25°C	-3pA max (-1pA typ)	*
vs. Temperature (0 to +70°C)	x2/+10°C	*
vs. Supply Voltage	±0.01pA/%	*
INPUT DIFFERENCE CURRENT		
Initial, @ +25°C	±1pA	*
vs. Temperature (0 to +70°C)	x2/+10°C	*
INPUT IMPEDANCE		
Differential	$10^{12}\Omega \| 3.5$pF	*
Common Mode	$10^{12}\Omega \| 3.5$pF	*
INPUT NOISE		
Voltage, 0.01Hz to 1Hz	1.5μV p-p max (1μV p-p typ)	*
10Hz to 10kHz	3μV rms max (2μV rms typ)	*
f = 1Hz	70nV/$\sqrt{\text{Hz}}$ rms	*
f = 10Hz	25nV/$\sqrt{\text{Hz}}$ rms	*
f = 100Hz	20nV/$\sqrt{\text{Hz}}$ rms	*
f = 1kHz	13nV/$\sqrt{\text{Hz}}$ rms	*
Current, 0.01Hz to 1Hz	0.1pA p-p	*
f = 1Hz	7fA/$\sqrt{\text{Hz}}$ rms	*
f = 10Hz	2.5fA/$\sqrt{\text{Hz}}$ rms	*
f = 100Hz	3.5fA/$\sqrt{\text{Hz}}$ rms	*
f = 1kHz	6fA/$\sqrt{\text{Hz}}$ rms	*
INPUT VOLTAGE RANGE		
Common Mode Voltage	±10V min	*
Common Mode Rejection, CMV = ±10V	100dB min (106dB typ)	*
Max Safe Differential Voltage	$\pm V_S$	*
POWER SUPPLY[3]		
Voltage, Rated Performance	±15V	*
Voltage, Operating	±(9 to 18)V	*
Current, Quiescent	±5mA	*
TEMPERATURE RANGE		
Rated Performance	0 to +70°C	*
Operating	-25°C to +85°C	*
Storage	-55°C to +125°C	*
MECHANICAL		
Case Size	1.12" x 1.12" x 0.4"	*
Weight	16g	*
Mating Socket	AC1008	*

*Specifications same as model 52J.

[1] Protected for short circuit to ground.

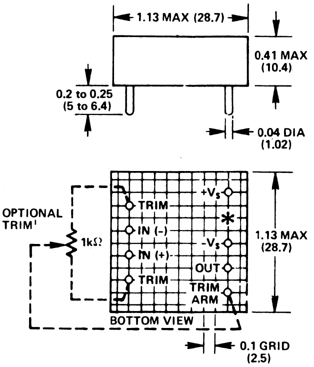
[2] With no external trim potentiometer connected.

[3] Recommended power supply, ADI model 904, ±15V @ 50mA output.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

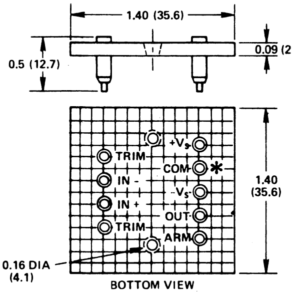
Dimensions shown in inches and (mm).



[1] Optional 1kΩ external trim pot. Input offset voltage may be adjusted to zero with trim pot connected as shown. With trim pins left open, input offset voltage will be ±0.5mV, maximum.

***Common Supply connection not required.**

MATING SOCKET AC1008



*No connection required on Model 52.

FREQUENCY RESPONSE

From the plot of Open Loop Voltage Gain and Phase Shift (see Figure 2) versus Frequency, it can be seen that model 52 is stable for all closed loop gains. Even at the crossover frequency of 500kHz, model 52 has a phase margin of 75°.

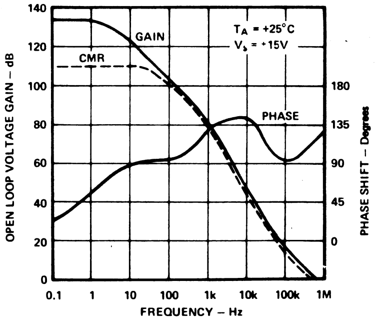


Figure 2. Open Loop Frequency Response and CMR

ANALOG DEVICES

High Voltage Differential FET Amplifier

MODEL 171

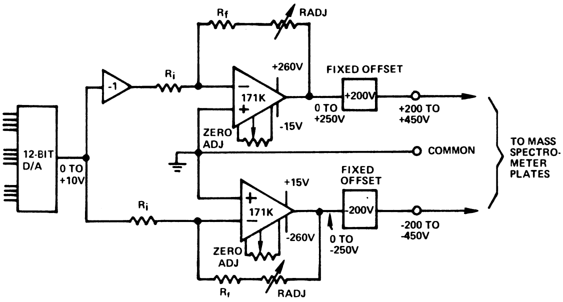
FEATURES

High Output Voltage: ±140V
High CMR: 100dB min
Operates With a Wide Range of Power Supplies
High CMV: ±(|V_S| - 10V)

APPLICATIONS

High Voltage Compliance Current Source
High Voltage Follower With Gain
High Voltage Integrator
Diff. Amp for High CMV Bridge Applications
Reference Power Supply

171 APPLICATION
PROGRAMMABLE MASS SPECTROMETER
VOLTAGE SOURCE



GENERAL DESCRIPTION

Model 171 is a high performance FET input op amp designed for operation over a wide range of supply voltages. This module features an output range of ±15V to ±140V at 10mA, a minimum CMRR of 100dB and a high common mode voltage rating of ±(V_S - 10V) min. DC offset is less than ±1mV, and maximum drift of either ±50 or ±15μV/°C is available in the J or K versions. Bias current is less than 50pA (171J) or 20pA (171K), doubling per +10°C increase of temperature. The model 171 also features small signal bandwidth of 3MHz for unity gain, full-power bandwidth of 15kHz, and slew rate of 10V/μs. These operating characteristics make model 171 an excellent choice for high voltage buffer applications, followers with gain, off-ground signal measurements and reference power supplies.

Excellent power supply rejection of 7μV/V enables model 171 to be powered by inexpensive, low regulation supplies, without sacrificing any of the 171's inherent high performance. The supplies also need not be symmetrical. Any combination of power supply voltages between the limits of 15 to +300V for the positive side and 15 to -300V for negative side is acceptable provided the total voltage across the amplifier is within the range of 30 to 300V.

Model 171's output is completely short circuit protected by the use of a current limit scheme. This type of protection provides a short circuit output that is only slightly greater than the rated output current for normal operation. With this design the module and external circuitry are protected, internal heat dissipation and the associated high temperature rise are limited, and added reliability is built in.

POWER SUPPLY VOLTAGES

Model 171 offers the flexibility of operating with an extensive range and combination of power supply voltage. The chart above shows a chart of permissible combinations of supply voltages for the 171. The model 171 maintains its normal operating characteristics when using asymmetrical power supply configurations.

For detailed information, contact factory.

SPECIFICATIONS (typical @ +25°C and ±125V unless otherwise noted)

MODEL	171J	171K
OPEN LOOP GAIN	10^6 min	*
RATED OUTPUT		
Voltage	$\pm(\lvert V_S \rvert -10V)$ min	*
Current	±10mA min	*
Maximum Load Capacitance	1000pF	*
FREQUENCY RESPONSE		
Unity Gain, Small Signal	3MHz	*
Slewing Rate	10V/μs min	*
Full Power	15kHz min	*
Settling Time to ±0.1%, ±10V Step	25μs	*
Overload Recovery	5μs	*
INPUT OFFSET VOLTAGE		
Initial Offset, +25°C[1]	±1mV	*
Avg. vs. Temp (0 to +70°C)	±50μV/°C max	±15μV/°C max
vs. Supply Voltage	±7μV/V	*
vs. Time	±250μV/mo	*
INPUT BIAS CURRENT		
Initial Bias, +25°C	-50pA max	-20pA max
vs. Temp (0 to +70°C)	x 2/10°C	*
Difference Current	±10pA	±5pA
INPUT IMPEDANCE		
Differential	$10^{11}\Omega \parallel 3.5pF$	*
Common Mode	$10^{11}\Omega \parallel 3.5pF$	*
INPUT NOISE		
Voltage, 0.01 to 1.0Hz	4μV p-p	*
10Hz to 10kHz	2.5μV rms	*
5Hz to 50kHz	6μV rms	*
INPUT VOLTAGE RANGE		
Common Mode Voltage	$\pm(\lvert V_S \rvert -10V)$ min	*
Common Mode Rejection	100dB min	*
Common Mode Rejection	114dB	*
Max Safe Differential Voltage	$\pm V_S$	*
POWER SUPPLY		
Voltage, Rated Specification	±25 to ±150V dc	*
Voltage, Operating	±15 to ±150V dc	*
Current, Quiescent	±6mA typ	*
TEMPERATURE RANGE		
Rated Specification	0 to +70°C	*
Operating	-25°C to +85°C	*
Storage	-40°C to +100°C	*
MECHANICAL		
Case Size	2.41" x 1.82" x 0.61"	*
Weight	80g	*
Mating Socket	AC1037	*

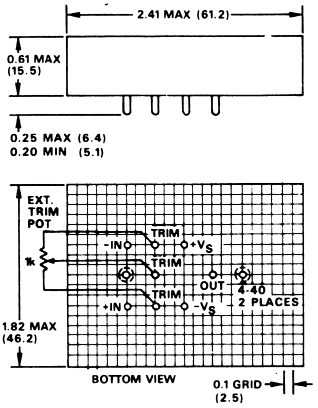
*Specifications same as 171J

[1] No external trim connection required.

Specifications subject to change without notice.

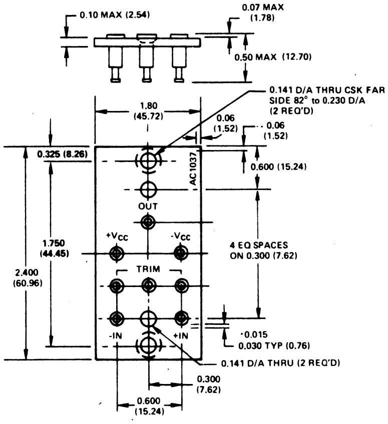
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



MATING SOCKET

Dimensions shown in inches and (mm).



MATING SOCKET AC1037

SINGLE SUPPLY OPERATION

The model 171 requires at least ±15 volts applied across it in order to operate properly. The 171 may be operated from a single floating supply voltage by using the power supply offsetting scheme shown in Figure 1. When this configuration is used, the 171 is capable of operating over its specified input and output voltage range.

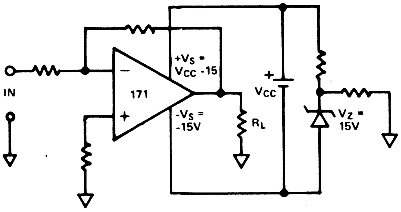


Figure 1. Single Supply Operation

ANALOG DEVICES

Low Noise Chopper Stabilized Amplifiers

MODELS 234, 235

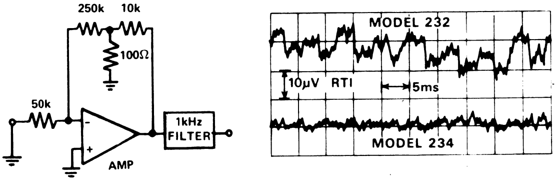
FEATURES

Ultra-Low Noise: 0.7μV p-p, 0.01Hz to 1Hz BW (234)
0.5μV p-p, 0.01Hz to 1Hz BW (235)
Very Low Offset Drift: 0.1μV/°C, 1pA/°C (234L)
0.1μV/°C, 0.5pA/°C (235L)
Excellent Long Term Stability: 5μV/year (235)
Fast Settling: 4μs to 0.01%, 2.5MHz BW (235)

APPLICATIONS

Precision Integration
Servo/Null Detector Loops
Microvolt/Picoamp Measurements
Bridge Amplifier
Controlled Current Source
Balance Scales and Weighing Instruments

MODEL 234 COMPARATIVE INPUT NOISE (RTI) PERFORMANCE IN A DC TO 1kHz BANDWIDTH



GENERAL DESCRIPTION

Analog Devices' models 234, 235 are high performance, economy chopper-stabilized op amps that meet the demands of critical laboratory and industrial applications requiring ultra-low noise, exceptional long term offset stability and versatility. Both models feature compact plug-in modular design, and are ideally suited for new design applications, or upgrading of existing systems, where both improved performance and cost savings can be realized.

Model 234: The model 234 is designed for wideband applications and features 10^7 V/V open loop gain, 2.5MHz unity gain bandwidth, full power response to 500kHz and settling time of 4μs (to 0.01%, 10V step, 20kΩ load). The model 234 also features low input voltage noise of 0.7μV p-p (0.01Hz to 1Hz BW), low offset voltage drift of 1μV/°C (234J), 0.03μV/°C (234K) or 0.1μV/°C (234L) and long term stability of ±2μV/month.

Incorporating MOSFET choppers and discrete components (vs. IC op amps) for the main and stabilizing amplifier channels, this inverting design is virtually free of input chopper spikes and offers reduced modulation ripple for quieter wideband performance. These characteristics are especially desirable when operating from high source impedances (above 100kΩ) at wide bandwidths. To illustrate the improvements in noise and bandwidth performance, over previous Analog Devices' designs, comparative data is set forth in the following sections comparing models 232 and 233 with 234.

Model 235: The model 235 is recommended for applications where lowest cost and lowest noise are required. The model 235 features low input voltage noise of 0.5μV p-p (0.01Hz to 1Hz BW), low offset voltage drift of 0.5μV/°C (235J), 0.25μV/°C (235K), 0.1μV/°C (235L) and a long term stability of 5μV/year.

This combination of noise and drift performance makes model 235 ideally suited for demanding applications such as balance scales and weighing instruments requiring high accuracy and excellent long-term stability without the use of "front panel" balance pots or periodic internal adjustment.

Model 235 has been designed to virtually eliminate intermodulation problems caused by "beating" against power line frequencies. The chopper's ultra-stable oscillator is precisely set at the factory to a frequency that minimizes ineractions with harmonics of 50Hz, 60Hz and 400Hz power lines.

APPLICATIONS

In general, the models 234, 235 inverting amplifiers should be considered where long term stability of offset voltage must be maintained with time and temperature for precision designs, or wherever maintenance-free operation of instruments and remote circuits is essential. Typical applications include low drift amplification of microvolt signals, integration of low duty-cycle pulse trains and analog computing for general purpose designs. Low input noise and stable offset voltages also make 234, 235 an ideal preamp for precision low frequency applications such as DVMs, 12- to 16-bit A to D converters, and for error amplifiers in servo and null detector systems.

For detailed information, contact factory.

SPECIFICATIONS (typical @ +25°C and ±15V unless otherwise noted)

MODEL	234J	234K	234L	235J	235K	235L
OPEN LOOP GAIN						
DC, 2k ohm load	10^7 V/V min	*	*	5 x 10^7V/V min	**	**
RATED OUTPUT						
Voltage	±10V min	*	*	*	*	*
Current	±5mA min	*	*	*	*	*
Load Capacitance Range	0-1000pF min	*	*	0.01µF	**	**
FREQUENCY[1]						
Unity Gain, Small Signal	2.5MHz	*	*	1MHz	**	**
Full Power Response	500kHz min	*	*	5kHz min	**	**
Slew Rate	30V/µs	*	*	0.3V/µs min	**	**
SETTLING TIME to 0.01%						
20kΩ load, 10V step	4µs	*	*	N/A	N/A	N/A
INPUT OFFSET VOLTAGE						
Initial Offset[2]	±50µV max	±20µV max	±20µV max	±25µV max	**	±15µV max
vs. Temp, 0 to +70°C	±1.0µV/°C max	±0.3µV/°C max	±0.1µV/°C max	±0.5µV/°C max	±0.25µV/°C max	±0.1µV/°C max
vs. Supply Voltage	±0.2µV/%	*	*	±0.1µV/%	**	**
vs. Time	±2µV/month	*	*	±5µV/year	**	**
vs. Turn On, 10 sec to 10 min	±3µV	*	*	*	*	*
INPUT BIAS CURRENT						
Initial, @ +25°C	±100pA max	*	*	*	±50pA max	±50pA max
vs. Temp, 0 to +70°C	±4pA/°C max	±2pA/°C max	±1pA/°C max	1pA/°C max	0.5pA/°C max	0.5pA/°C max
vs. Supply Voltage	±0.5pA/%	*	*	0.2pA/%	**	**
INPUT IMPEDANCE						
Inverting Input to Signal Ground	300k ohms	*	*	*	*	*
INPUT NOISE						
Voltage, 0.01 to 1Hz	0.7µV p-p	*	*	0.5µV p-p	2µV p-p max	2µV p-p max
0.1 to 10Hz	1.5µV p-p	*	*	3.5µV p-p	**	**
10Hz to 10kHz	2µV rms	*	*	5µV rms	**	**
Current, 0.01 to 1Hz	2pA p-p	*	*	10pA p-p	**	**
0.1 to 10Hz	4pA p-p	*	*	30pA p-p	**	**
INPUT VOLTAGE RANGE						
(-) Input to Signal Ground	±15V max	*	*	*	*	*
POWER SUPPLY (V dc)[3]						
Rated Performance	±15V @ 5mA	*	*	*	*	*
Operating	±(12 to 18)V	*	*	*	*	*
TEMPERATURE RANGE						
Rated Specifications	0 to +70°C	*	*	*	*	*
Operating	-25°C to +85°C	*	*	*	*	*
Storage	-25°C to +100°C	*	*	-55°C to +125°C	**	**

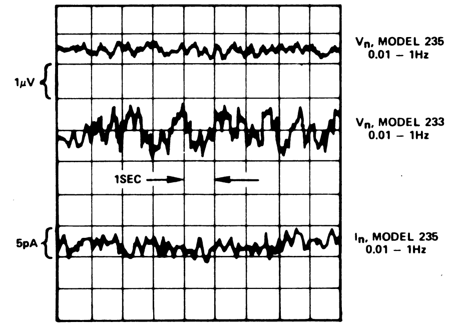
NOTES
*Specifications same as model 234J.
**Specifications same as model 235J.

[1] Model 235 overload recovery, 10 sec typ.

[2] Externally adjustable to zero.

[3] Recommended power supply: Analog Devices model 904, ±15V dc @ 50mA.

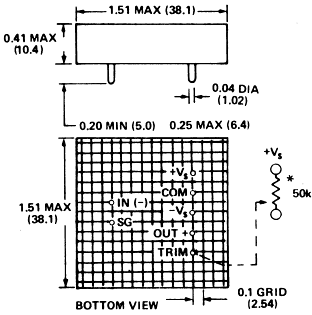
Specifications subject to change without notice.



Model 235 Voltage and Current Noise. Model 233 Voltage Noise Shown for Comparison.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



NOTES:
*Connect Trim Terminal to Common if Trim Pot is not used.

1. SG Tied to Common.
2. Mating Socket AC1010.
3. Weight: 27 grams.

ANALOG
DEVICES

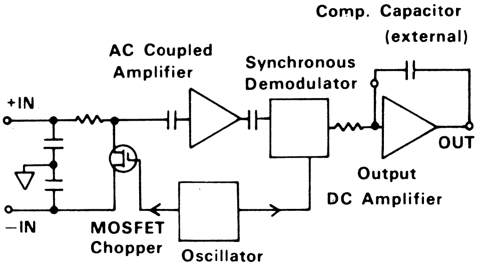
Low Noise Non-Inverting Chopper Amplifier

MODEL 261

FEATURES
Non-Inverting Input
$10^9\,\Omega$ Common Mode Impedance
Protected MOSFET Chopper
Ultra Low Drift $0.1\mu V/^\circ C$, Max (261K)
Guaranteed Low Noise of $0.4\mu Vp$-p (0.01 to 1Hz)
Low Cost

APPLICATIONS
Microvolt & Millivolt Measurements
Meter & Recorder Preamplifier
Semiconductor Strain Gage Amplifier
Biological Sensors
Potentiometer Buffer

MODEL 261 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION
Model 261 is a low cost non-inverting chopper amplifier featuring ultra low drift of $0.1\mu V/^\circ C$, open loop gain of greater than 10 million V/V and guaranteed low noise performance of $0.4\mu V$ p-p max in a 0.01 to 1Hz bandwidth. It is ideally suited for low level pre-amplifier applications where high input impedance and low noise are essential.

Model 261 also offers a solution to beat frequency problems caused by a low frequency carrier mixing with harmonics of the ac line. Its carrier frequency of 3500Hz is nearly a decade higher than that of models previously available. The required harmonic of the ac line that could cause interference with a 3500Hz carrier has negligible energy content and beat frequencies are eliminated. As a further protection against interfering signals, model 261 has been completely shielded internally. This protective shield reduces interference due to RF signals, as well as carrier signals from adjacent chopper amplifiers.

Still another advantage of the 261 due to its higher chopper frequency and shielded design is an output signal that is free from both distortion and chopper spikes. The result is a design that can process low level signals while maintaining low distortion and high signal to noise ratios.

CHOPPER VS. CHOPPER-STABILIZED
Most conventional ultra-stable amplifiers are chopper-stabilized to achieve low drift. In these units, the higher frequency signal components are separated and directly amplified, while the low frequency and dc components are separately chopped, amplified, demodulated, and then summed with the high frequency components in an output stage. This method provides wide bandwidth and excellent performance at the expense of increased cost and complexity. Since many requirements for ultra-low drift amplification involve only dc and low frequency signals, the additional high frequency amplifier stage found in most chopper-stabilized amplifiers has been eliminated from the model 261. This design approach has made it possible to achieve a practical non-inverting configuration, which retains the advantages of low cost and small size. The input stage of the model 261 chops the signal at a 3500Hz rate, resulting in a maximum useful −3dB bandwidth of about 100Hz. For increased flexibility in meeting specific design requirements, terminals are provided for an external compensation capacitor, which determines the amplifier's gain-bandwidth product.

INPUT IMPEDANCE
One of the prime advantages of the non-inverting amplifier is the capability of bootstrapping the input impedance up to the level of the common mode impedance. For the model 261, this means that the $40k\Omega$ open loop input resistance will be multiplied by the open loop gain times the feedback factor. With a typical open loop gain of 40×10^6, closed loop gains of up to 1600 will allow the user to realize $10^9\,\Omega$ input resistance. Even at a gain of 10,000, the effective input resistance will be over 100 megohms. (i.e.) $(40k\Omega)\frac{40 \times 10^6}{10^4} = 160M\Omega$.

This two-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be found in Volume II, page 4–27.

SPECIFICATIONS (typical @ +25°C and ±15V dc unless otherwise noted)

Model	261J	261K
OPEN LOOP GAIN		
DC rated load	10^7V/V min	*
RATED OUTPUT		
Voltage	±10V min	*
Current	±5mA min	*
Load Capacitance Range	0 to 0.001μF	*
FREQUENCY RESPONSE		
Small Signal, -3dB	100Hz	*
Full Power Response	2-50Hz min	*
Slewing Rate	100V/s min	*
Overload Recovery	300ms	*
INPUT OFFSET VOLTAGE[1]		
External Trim Pot	50kΩ	*
Initial Offset, +25°C	±25μV max	*
Avg vs Temp (0 to +70°C)	±0.3μV/°C max	±0.1μV/°C max
Supply Voltage	±0.1μV/%	*
Time	±½μV/month	*
Warm-Up Drift	<3μV in 20 minutes	*
INPUT BIAS CURRENT		
Initial Bias, +25°C, + Input	±300pA max	*
Avg vs Temp (0 to +70°C)	±10pA/°C max	*
Initial Bias, +25°C, - Input	±10nA max	*
Avg vs Supply Voltage	±3pA/%	*
INPUT IMPEDANCE		
Differential	40kΩ‖0.01μF	*
Common Mode	10^9Ω‖0.02μF	*
INPUT NOISE		
Voltage, 0.01 to 1Hz, p-p	0.4μV max	*
0.01 to 10Hz, p-p	1.0μV max	*
Current, 0.01 to 1Hz, p-p	8pA	*
0.01 to 10Hz, p-p	20pA	*
INPUT VOLTAGE RANGE		
Common Mode Voltage	±0.5V min	±1.0V min
Common Mode Rejection	300,000	*
Max Safe Differential Voltage	±20V	*
Max Safe Common Mode Voltage	±20V	*
POWER SUPPLY[2]		
Voltage, Rated Specification	±(14 to 16)V	*
Voltage, Operating	±(13 to 18)V	*
Current, Quiescent	±7mA	*
TEMPERATURE RANGE		
Rated Specifications	0 to +70°C	*
Operating	-25°C to +85°C	*
Storage	-55°C to +125°C	*
MECHANICAL		
Case Size	1.5" x 1.5" x 0.62"	*
Mating Socket	AC1022	*
Weight	1.75 oz. (50g)	*

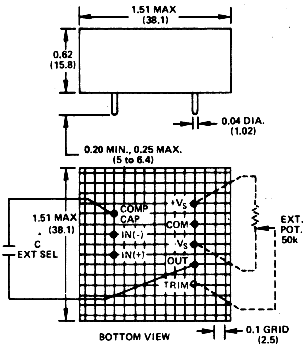
[1] Ground trim terminal if trim potentiometer is not used.

[2] Recommended power supply, ADI model 904, ±15V @ 50mA output.

*Specifications same as for model 261J.
Specifications subject to change without notice.

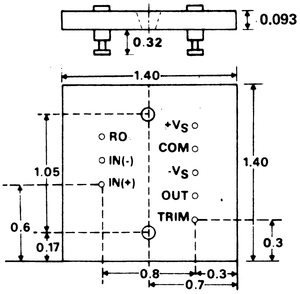
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



1. Trim terminal should be grounded if potentiometer is not used.
2. See Note 1 below for cap value. Use Polycarbonate, Mylar, Mica, Glass, or Polystyrene capacitor for best performance.

MATING SOCKET
AC1022



Notes
1. R.O. is connection for compensation capacitor.
2. Bottom View Shown.
3. Mounting holes 0.141 Dia., countersunk 82° to 0.23" Dia.
4. All in line pins spaced 0.2".
5. Dimensions in inches.
6. Markings printed on socket.

Instrumentation & Isolation Amplifiers

Contents

	Page
Selection Guide	5-2
Orientation and Definitions of Specifications	5-4
AD521J/K/L/S Monolithic IC Resistor-Programmable Amplifiers	5-9
AD522A/B/S Hybrid IC Resistor-Programmable Amplifiers	5-15
•AD524J/K/L/S Precision Instrumentation Amplifier	5-19
AD612A/B/C/D/E Hybrid IC Jumper-Programmable Amplifiers	5-23
AD614A/B/C/D/E Hybrid IC Jumper-Programmable Amplifiers	5-23
•AD293A/B/S Hybrid Industrial Isolation Amplifier	5-27
•AD294A Hybrid Medical Isolation Amplifier	5-27
289J/K/L High-Performance Synchronizable Self-Contained Isolation Amplifier	5-35

•New product since *1980 Data-Acquisition Components and Subsystems Catalog*

Selection Guide
Instrumentation & Isolation Amplifiers

The abbreviated specifications listed here permit a choice on the basis of the key parameters of instrumentation amplifiers, depending on which parameters are critical for the application. Complete and detailed specifications can be found in the data-sheet section.

Descriptive information on instrumentation and isolation amplifiers and a guide to specifications are provided on the following pages. Devices that perform instrumentation-amplifier functions can also be found in section 15 (Data Acquisition Subsystems).

All specifications are typical at rated supply voltage and load, and $T_A = 25^\circ C$, unless otherwise noted.

SELECTION GUIDE – INSTRUMENTATION AMPLIFIERS

	Monolithic IC AD521J(K)(L)(S)[1]	Hybrid IC AD522A(B)(S)[1]	Monolithic AD524J(K)(L)(S)	Hybrid IC AD612A(B)(C)	Hybrid IC AD614A(B)
GAIN					
Range V/V	0.1 to 1000	1 to 1000	1 to 1000	1 to 1024	1 to 1024
Nonlinearity (G = 100) – % max	0.2(0.2)(0.1)(0.2)	0.01(0.005)(0.005)	0.02(0.01)(0.005)(0.02)	0.001	0.001
RATED OUTPUT – V dc/mA	±10/±10	±10/±5	±10/±5	±10/±5	±10/±5
DYNAMIC RESPONSE					
Small Signal (-3dB)					
G = 1000	40kHz	300Hz	25kHz	10kHz	20kHz
Full Power Frequency	100kHz	1.5kHz	–	–	–
Slew Rate – V/μs	10	0.1	5	1	1
OFFSET VOLTAGE					
Input Offset Voltage	3(1.5)(1)(1.5)μV max	±400(200)(200)μV max	250(100)(25)(100)μV	±200μV	±200μV
vs. Temperature	15(15)(2)(5)μV/°C	±6(2)(6)μV/°C	3(1.5)(0.5)(1.5)μV/°C	±5(2)(1)μV/°C	±5(2)μV/°C
Output Offset Voltage	400(1200)(100)(200)μV max		1mV(500μV)(250μV)(500μV)		
vs. Temperature	400(150)(75)(150)μV/°C		50(20)(10)(20)μV/°C		
INPUT BIAS CURRENT – nA max	±80(40)(40)(40)	±25(15)(25)	50(70)(10)(50)	+100	+100
INPUT IMPEDANCE					
Common Mode – Ω	6×10^{10}	10^9	10^9	10^9	10^9
COMMON MODE REJECTION RATIO					
min @ 1kΩ Source Unbalance,					
CMV = ±10V					
G = 1 – dB	70(74)(74)(74)[2]	75(80)(85) dc to 30Hz	70(75)(80)(70)	74	74
G = 10 – dB	90(94)(94)(94)[2]	90(95)(90) dc to 10Hz	90(95)(100)(90)	80	80
G = 1000 – dB	100(110)(110)(110)[2]	100(110)(100) dc to 1Hz	115(125)(130)(190)	94	94
Volume I					
Page	5-9	5-15	5-19	5-23	5-23

[1] Processing to MIL-STD-883B available.
[2] DC to 60Hz.

SELECTION GUIDE – ISOLATION AMPLIFIERS

		WIDE BAND, PRECISION	LOWEST COST		±6500V MAX DIFF INPUT		UNCOMMITTED OP AMP	HYBRID		
								INDUSTRIAL	MEDICAL	MILITARY
		289	290A	292A	284J	286J	277	AD293	AD294A	AD294S/883B
Max Input/Output CMV	±2500V dc pk max	●			●	●	●	●	●	●
	±1500V dc pk max		●	●						
	±850V dc pk max									
Nonlinearity	±0.012%	●								
	±0.025%						●			
	±0.050%				●	●		●	●	
	±0.100%		●	●						●
Output Voltage	±5V				●					
	±10V	●	●	●		●	●	●	●	●
Gain Range	1–1000V/V						●	●	●	●
	1–100V/V	●	●	●		●				
	1–10V/V				●					
Synchronized Operation	With External Oscillator			●		●				
	With Internal Oscillator	●						●	●	
Output Amplifier		●					●	●	●	●
Isolated Power Out		●	●	●	●	●	●			
Defibrillation Protection					●	●			●	
Three Port Isolation		●						●	●	●
Volume I Page		5-35	–	–	–	–	–	5-27	5-27	5-27
Volume II Page		5-23	5-27	5-27	5-17	5-17	5-15	5-7	5-7	5-7

See *Signal Conditioners* for other analog/analog products with input/output isolation–including current-output devices.

Orientation

Instrumentation & Isolation Amplifiers

An instrumentation amplifier is a committed "gain block" that measures the difference between the voltages existing at its two input terminals, amplifies it by a precisely set gain – usually from 1V/V to 1000V/V or more – and causes the result to appear between a pair of terminals in the output circuit. Referring to Figure 1,

$$V_S - V_R = G\,(V^+ - V^-)$$

An ideal instrumentation amplifier responds only to the *difference* between the input voltages. If the input voltages are equal ($V^+ = V^- = V_{CM}$, the *common-mode voltage*), the output of the ideal instrumentation amplifier will be zero.

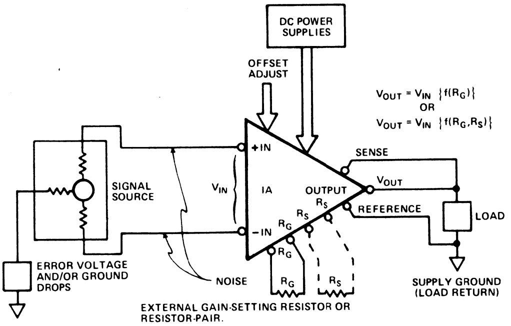

DC POWER SUPPLIES
OFFSET ADJUST
$V_{OUT} = V_{IN}\ \{f(R_G)\}$
OR
$V_{OUT} = V_{IN}\ \{f(R_G, R_S)\}$
+IN
SENSE
SIGNAL SOURCE
V_{IN}
IA
OUTPUT
V_{OUT}
R_S
R_S
REFERENCE
R_G
LOAD
−IN
R_G
ERROR VOLTAGE AND/OR GROUND DROPS
NOISE
R_G
R_S
SUPPLY GROUND (LOAD RETURN)
EXTERNAL GAIN-SETTING RESISTOR OR RESISTOR-PAIR.

Figure 1. Basic Instrumentation Amplifier Functional Diagram

An amplifier circuit which is optimized for performance as an instrumentation-amplifier gain block has high input impedance, low offset and drift, low nonlinearity, stable gain, and low effective output impedance. It is commonly used for applications which capitalize on these advantages. Examples include: transducer amplification – for thermocouples, strain-gage bridges, current shunts, and biological probes, preamplification of small differential signals superimposed on high common-mode voltages, signal conditioning and (moderate) isolation for data acquisition, and signal translation for differential and single-ended signals wherever the common "ground" is noisy or of questionable integrity.

Instrumentation-amplifiers are usually chosen in preference to user-assembled op-amp circuitry, because they offer optimized, specified performance in low-cost, easy-to-use, compact packages. If the application calls for high common-mode voltages (typically, voltages in excess of the amplifier supply voltage), or if isolation impedances must be very high (e.g., $10^{10}\,\Omega$, with galvanic isolation, as in medical and industrial applications), the designer should consider an isolation amplifier.

SPECIFYING INSTRUMENTATION AMPLIFIERS

The instrumentation amplifier chosen for a given application will be the lowest-cost device that satisfies the performance and environmental requirements. In addition to the products listed here, which are recommended for new designs, a number of older products are still available; data sheets are available upon request. It is essential that the designer have a firm understanding of the specifications of instrumentation amplifiers and of the contributions of the various sources of error to the total error. The data sheets provide much useful application data on these devices, as well as examples of basic error analyses.

Definitions of the key specifications follow a brief discussion of instrumentation-amplifier architectures. For more-complete information on the fundamentals and applications of instrumentation amplifiers, a number of publications are available from Analog Devices.[1,2,3]

INSTRUMENTATION-AMPLIFIER ARCHITECTURE

All Analog Devices instrumentation amplifiers have two high-impedance input terminals, a set of terminals for gain-programming, an "output" terminal, and a pair of feedback terminals, labeled *sense* and *reference*, as well as terminals for power supply and offset trim.*

Two basic circuit concepts are employed. The AD522, AD612 and AD524 use variations of the well-known three-op-amp configuration, consisting of a differential input-output gain stage and subtractor stage. Gain ($\geqslant$1V/V) is set by the choice of a single gain-setting resistor, R_G. When the *sense* (V_S) feedback terminal is connected to the output terminal, and the *reference* terminal (V_R) is connected to power common, the output voltage appears between the output terminal and power common.

The V_S and V_R terminals may be used for remote sensing – to establish precise outputs in the presence of line drops; they may be used with an inside-the-loop booster follower to obtain power amplification without loss of accuracy; and they may be used to establish an output current that is precisely proportional to the difference signal. A voltage applied to the V_R terminal will bias the output by a predetermined amount. It is important always to maintain very low impedance (in relation to the specified V_S and V_R input impedances), when driving the V_S and V_R inputs, in order not to introduce common-mode, gain, and/or offset errors. In devices using the 3-amplifier configuration, the V_R terminal is sometimes used for "tweaking" common-mode rejection.

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[1] *"Isolation and Instrumentation Amplifiers Designer's Guide*, 1978 edition, available upon request.

[2] "A User's Guide to IC Instrumentation Amplifiers," by J. Riskin, 1978, available upon request.

[3] *Transducer Interfacing Handbooks*, D.H. Sheingold, ed., 1980, \$14.50, Analog Devices, Inc., P.O. Box 796, Norwood, MA 02062.

*In Model 612, *sense* is internally connected to the output terminal.

SPECIFICATIONS

Specification tables are generally headed by the legend: "specifications are typical at $V_S = \pm 15V$, $T_A = +25^\circ C$, and rated load, unless otherwise noted." This tells the user that these are the normal operating conditions under which the device is tested. Deviations from these conditions might degrade (or improve) performance. When deviations from the "normal" conditions are likely (such as a change in temperature), the significant effects are usually indicated within the specs. "Typical" means that the manufacturer's characterization process has shown this number to be "average," but individual devices vary.

Specifications not discussed in detail are self-explanatory and require only a basic knowledge of electronic measurements. Such specs are not uniquely applicable to instrumentation amps.

GAIN These specifications refer to the linear transfer function of the device; for example, the AD522 gain equation is: $G = 1 + \frac{200{,}000}{R_G}$ V/V. The value of R_G for a given gain value is: $R_G = \frac{200{,}000}{G - 1}\,\Omega$. For example, if G is to be 100 V/V, $R_G = 2020.2$ ohms.

Gain Range Specified at 1 to 1000, for example, the device may work at higher gains (1 V/V is minimum, except for the AD521), but the manufacturer does not specify performance outside the range. In practice, noise and drift may make higher gains impractical for a given device.

Equation Error (or "Gain Accuracy") The number given by this specification describes deviation from the gain equation when R_G is at its nominal value (or, in the case of model 612, when connected for a given gain). The user can trim the gain or compensate for gain error elsewhere in the overall system. Systems using microprocessors (or computers, or other digital "intelligence") can be made self-calibrating, to take into account the lumped gain errors of all the stages in the analog portion of the system, from transducer to a/d converter.

Nonlinearity (or Gain Nonlinearity) Nonlinearity is defined as the deviation from a straight line on the plot of output vs. input. The magnitude of linearity error is the maximum deviation from a "best straight line," with the output swinging through its full-scale range. Nonlinearity is usually specified in percent of full-scale output range.

Gain vs. Temperature These numbers give the deviations from the gain equation as a function of temperature.

SETTLING TIME is defined as that length of time required for the output voltage to approach and remain within a certain (±) tolerance of its final value. It is usually specified for a fast step that will drive the output through its full-scale range and it includes slewing time. Since several factors contribute to the overall settling time, fast settling to 0.1% does not necessarily mean proportionally fast settling to 0.01%, nor is settling time necessarily proportional to gain. Principal contributing factors include slew-rate limiting, underdamping (ringing), and thermal gradients ("long tails").

VOLTAGE OFFSET Voltage offset and common-mode rejection (see below) specifications are often considered the key figures of merit for instrumentation amplifiers. While initial offset can be adjusted to zero, shifts in offset voltage with time and temperature introduce errors. Systems that involve "intelligent" processors can correct for offset errors in the whole measurement chain, but such applications are still relatively infrequent; in most applications, the instrumentation amplifier's contribution to system offset error must be defined.

Voltage offset and offset drift in instrumentation amplifiers are functions of gain.[4] The offset, measured at the output, is equal to a constant plus a term proportional to gain. For an amplifier with specified performance over a gain range from 1 to 1000, the constant is essentially the offset at unity gain, and the proportionality term (or slope) is equal to the change in output offset between G = 1 and G = 1000, divided by 999. To refer offset to the input (RTI), divide the total output offset by the gain. Since offset at a gain of 1000 is dominated by the proportional term, the slope is often called the "RTI offset, G = 1000." At any value of gain, the offset is equal to the unity-gain offset plus the product of the gain and the "RTI offset, G = 1000".

The same considerations apply to the offset drift. For example, the maximum RTI drift of the AD522B is specified at $25\mu V/^\circ C$ at G = 1, $2\mu V/^\circ C$ at G = 1000, and $(\frac{25}{G} + 2)\,\mu V/^\circ C$ at any arbitrary gain in the range. Thus, the output drift is $(25 + 2G)\mu V/^\circ C$ at any gain, G, in the range. The data sheets provide offset-vs.-gain plots, but the function is easily computed in the manner described above.

Voltage offset as a function of power supply level is also specified RTI at one or more gain settings.

INPUT BIAS AND OFFSET CURRENTS Input bias currents are those currents needed to bias the input transistors of a dc amplifier or to supply the junction-leakage of FET's. FET-input devices have lower bias currents than those using bipolar transistors, but FET leakage currents increase dramatically with temperature, approximately doubling every 11°C. Since bias currents can be considered as a source of voltage offset (when multiplied by source resistance), the change in bias currents is of more concern than the magnitude of the bias currents. Input offset current is the difference between the two input bias currents.

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[4] There is a good explanation of the specification of offset in instrumentation amplifiers in ANALOG DIALOGUE 6–2 (1972), p. 14

Important Note
Although instrumentation amplifiers have differential inputs, there *must* be a return path for the bias currents. If it is not provided, those currents will charge stray capacitances, causing the output to drift uncontrollably or to saturate. Therefore, when amplifying outputs of "floating" sources, such as transformers and thermocouples, as well as ac-coupled sources, there must still be a dc path from each input to common, or to the *guard* terminal. If a dc return path is impracticable, an *isolator* must be used.

COMMON-MODE REJECTION (CMR) is a measure of the change in output voltage when both inputs are changed by equal amounts. CMR is usually specified for a full-range common-mode voltage change (CMV), at a given frequency, and a specified imbalance of source impedance (e.g. 1kΩ source unbalance, at 60Hz). CMR is a logarithmic expression of the *common-mode rejection ratio* (CMRR): CMR = 20 $\log_{10}$ (CMRR). The common-mode rejection ratio is defined as the ratio of the signal gain, G, to the ratio of common mode signal appearing at the output to the input CMV.

In most instrumentation amplifiers, the CMR increases with gain, because the front-end configuration does not amplify common-mode signals, and the amount of common-mode signal appearing at the output stays relatively constant as the signal gain (G) increases.

However, at higher gains, amplifier bandwidth decreases. Since differences in phase shift through the differential input stage will show up as common-mode errors, CMR becomes more frequency-dependent at high gains.

ISOLATION AMPLIFIERS

The *isolation amplifier* (or *isolator*) has an input circuit that is galvanically isolated from the power supply and the output circuit. Isolators are intended for applications requiring safe, accurate measurement of dc and low-frequency voltage or current in the presence of high common-mode voltage (to thousands of volts) with high CMR, line-receiving of signals transmitted at high impedance in noisy environments, and for safety in general-purpose measurements where dc and line-frequency leakage must be maintained at levels well below certain mandated minima.* Principal applications are in electrical environments of the kind associated with medical equipment, conventional and nuclear power plants, automatic test equipment, and industrial process-control systems.

Analog Devices Isolators described in this catalog use electromagnetically coupled high-frequency carrier techniques for communication of power to and signals from the input circuit.

CHOOSING AN ISOLATOR

The choice of an isolator depends on the desired *functional characteristics* and the required *specifications*. Functional characteristics include such considerations as number of channels, range of output common-mode (output to power supply), nature of the front-end amplifier (amplification only or general op-amp functioning), and the availability of isolated power for additional external front-end circuitry. Key specifications include performance specs and "absolute max/min" mandated safety specifications. Definitions of specifications follow this section. In addition to the products listed here, which are recommended for new designs, a number of older products are still available; data sheets are available upon request. In addition to the useful applications information on the data sheets published here, a designers' guide[1], available upon request, provides information useful to the circuit designer.

Functional Characteristics The basic design of both amplifiers is identical. As shown in Figure 1, an amplifier is divided into three isolated sections—input, output, and power—coupled together by a single transformer. A power oscillator (which may be powered by system power or a separate power source) furnishes isolated power to the input amplifier, plus a carrier, which is modulated by the amplified input signal, coupled across the isolation barrier to the output section, demodulated, and buffer-amplified by a system-powered output amplifier.

Two significant innovations are responsible for the small size and excellent performance of these amplifiers. The first is an ultra-compact transformer, using screened wiring and well-conceived assembly technology. The second is an improvement in the use of the flyback (unclamped) portion of a blocking-oscillator waveform as the modulated signal carrier (U.S. Patent 4,286,225).

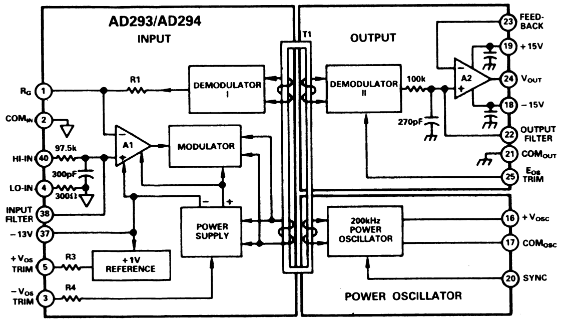

Figure 1. AD293/AD294 Block Diagram

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*Examples of such requirements may be found in UL STD 544 and SWC (Surge Withstand Capability) in IEEE Standard for Transient Voltage Protection 472-1974.

[1] *Analog Devices Isolation and Instrumentation Amplifiers Designer's Guide"* (1980)

As the block diagram shows, the synchronizable oscillator requires a two-wire power supply, which may be different (and (and isolated) from the power supply for the output amplifier, A2. The oscillator's output is coupled to (and loaded by, but isolated from) the circuitry connected to the other five identical transformer windings. One winding delivers power to the input amplifier, A1.

The flyback portion of the oscillator waveform is amplitude-modulate by A1's output signal, then coupled through separate transformer windings to a demodulator (I) in the amplifier's feedback path. Since A1 is an operational amplifier, the feedback signal must replicate the input signal (gain, from 1 to 100V/V, is equal to $1 + R_8/R_G$), and the transformer flux during flyback must be whatever is necessary to make this happen. The common flux, through an identical winding, applied to an identical demodulator (II), causes its output to be very nearly identical to the voltage at the output of the first demodulator, i.e., an accurately amplified version of the input signal. The other winding connected to Demodulator II provides a reference signal. The output of the demodulator is filtered and buffered by output amplifier, A2, which may be connected for gain values from 1 to 10V/V.

The AD293 and AD294 are *3-port* isolators; the input, output, and power sections are mutually isolated from one another. The use of separate substrates for the spiral-winding triplets of the transformer makes possible isolation of ±2500V (peak or continuous) for the AD293, and ±8000V (peak, 10ms pulse) for the AD294, between the input and output/power circuits. The high-temperature-fired dielectrics between the individual windings permit 500V rms of isolation between the output and power ports.

ANALOG DEVICES

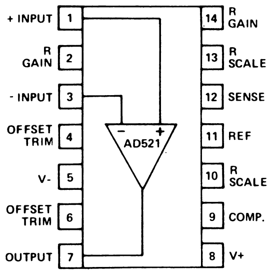
Integrated Circuit Precision Instrumentation Amplifier

AD521

FEATURES

Programmable Gains from 0.1 to 1000
Differential Inputs
High CMRR: 110dB min
Low Drift: 2μV/°C max (L)
Complete Input Protection, Power ON and Power OFF
Functionally Complete with the Addition of Two Resistors
Internally Compensated
Gain Bandwidth Product: 40MHz
Output Current Limited: 25mA
Very Low Noise: 0.5μV p-p, 0.1Hz to 10Hz, RTI @ G = 1000
Extremely Low Cost

AD521 FUNCTIONAL BLOCK DIAGRAM



TO-116

PRODUCT DESCRIPTION

The AD521 is a second generation, low cost, monolithic IC instrumentation amplifier developed by Analog Devices. As a true instrumentation amplifier, the AD521 is a gain block with differential inputs and an accurately programmable input/output gain relationship.

The AD521 IC instrumentation amplifier should not be confused with an operational amplifier, although several manufacturers (including Analog Devices) offer op amps which can be used as building blocks in variable gain instrumentation amplifier circuits. Op amps are general-purpose components which, when used with precision-matched external resistors, can perform the instrumentation amplifier function.

An instrumentation amplifier is a precision differential voltage gain device optimized for operation in a real world environment, and is intended to be used wherever acquisition of a useful signal is difficult. It is characterized by high input impedance, balanced differential inputs, low bias currents and high CMR.

As a complete instrumentation amplifier, the AD521 requires only two resistors to set its gain to any value between 0.1 and 1000. The ratio matching of these resistors does not affect the high CMRR (up to 120dB) or the high input impedance ($3 \times 10^9 \Omega$) of the AD521. Furthermore, unlike most operational amplifier-based instrumentation amplifiers, the inputs are protected against overvoltages up to ±15 volts beyond the supplies.

The AD521 IC instrumentation amplifier is available in four different versions of accuracy and operating temperature range. The economical "J" grade, the low drift "K" grade, and the lower drift, higher linearity "L" grade are specified from 0 to +70°C. The "S" grade guarantees performance to specification over the full MIL-temperature range: -55°C to +125°C and is available screened to MIL-STD-883, Class B. All versions are packaged in a hermetic 14-pin DIP.

PRODUCT HIGHLIGHTS

1. The AD521 is a true instrumentation amplifier in integrated circuit form, offering the user performance comparable to many modular instrumentation amplifiers at a fraction of the cost.
2. The AD521 has low guaranteed input offset voltage drift (2μV/°C for L grade) and low noise for precision, high gain applications.
3. The AD521 is functionally complete with the addition of two resistors. Gain can be preset from 0.1 to more than 1000.
4. The AD521 is fully protected for input levels up to 15V beyond the supply voltages and 30V differential at the inputs.
5. Internally compensated for all gains, the AD521 also offers the user the provision for limiting bandwidth.
6. Offset nulling can be achieved with an optional trim pot.
7. The AD521 offers superior dynamic performance with a gain-bandwidth product of 40MHz, full peak response of 100kHz (independent of gain) and a settling time of 5μs to 0.1% of a 10V step.

SPECIFICATIONS (typical @ V_S = ±15V, R_L = 2kΩ and T_A = 25°C unless otherwise specified)

MODEL	AD521JD	AD521KD	AD521LD	AD521SD (AD521SD/883B)
GAIN				
Range (For Specified Operation, Note 1)	1 to 1000	*	*	*
Equation	$G = R_S/R_G$ V/V	*	*	*
Error from Equation	(±0.25–0.004G)%	*	*	*
Nonlinearity (Note 2)				
$1 \leq G \leq 1000$	0.2% max	*	0.1% max	*
Gain Temperature Coefficient	±(3 ±0.05G)ppm/°C	*	*	±(15 ±0.4G)ppm/°C
OUTPUT CHARACTERISTICS				
Rated Output	±10V, ±10mA min	*	*	*
Output at Maximum Operating Temperature	±10V @ 5mA min	*	*	*
Impedance	0.1Ω	*	*	*
DYNAMIC RESPONSE				
Small Signal Bandwidth (±3dB)				
G = 1	>2MHz	*	*	*
G = 10	300kHz	*	*	*
G = 100	200kHz	*	*	*
G = 1000	40kHz	*	*	*
Small Signal, ±1.0% Flatness				
G = 1	75kHz	*	*	*
G = 10	26kHz	*	*	*
G = 100	24kHz	*	*	*
G = 1000	6kHz	*	*	*
Full Peak Response (Note 3)	100kHz	*	*	*
Slew Rate, $1 \leq G \leq 1000$	10V/μs	*	*	*
Settling Time (any 10V step to within 10mV of Final Value)				
G = 1	7μs	*	*	*
G = 10	5μs	*	*	*
G = 100	10μs	*	*	*
G = 1000	35μs	*	*	*
Differential Overload Recovery (±30V Input to within 10mV of Final Value) (Note 4)				
G = 1000	50μs	*	*	*
Common Mode Step Recovery (30V Input to within 10mV of Final Value) (Note 5)				
G = 1000	10μs	*	*	*
VOLTAGE OFFSET (may be nulled)				
Input Offset Voltage (V_{OS_I})	3mV max (2mV typ)	1.5mV max (0.5mV typ)	1.0mV max (0.5mV typ)	**
vs. Temperature	15μV/°C max (7μV/°C typ)	5μV/°C max (1.5μV/°C typ)	2μV/°C max	**
vs. Supply	3μV/%	*	*	*
Output Offset Voltage (V_{OS_O})	400mV max (200mV typ)	200mV max (30mV typ)	100mV max	**
vs. Temperature	400μV/°C max (150μV/°C typ)	150μV/°C max (50μV/°C typ)	75μV/°C max	**
vs. Supply (Note 6)	$0.005V_{OS_O}$/%	*	*	*
INPUT CURRENTS				
Input Bias Current (either input)	80nA max	40nA max	**	**
vs. Temperature	1nA/°C max	500pA/°C max	**	**
vs. Supply	2%/V	*	*	*
Input Offset Current	20nA max	10nA max	**	**
vs. Temperature	250pA/°C max	125pA/°C max	**	**
INPUT				
Differential Input Impedance (Note 7)	3×10^9 Ω‖1.8pF	*	*	*
Common Mode Input Impedance (Note 8)	6×10^{10} Ω‖3.0pF	*	*	*
Input Voltage Range for Specified Performance (with respect to ground)	±10V	*	*	*
Maximum Voltage without Damage to Unit, Power ON or OFF Differential Mode (Note 9)	30V	*	*	*
Voltage at either input (Note 9)	V_S ±15V	*	*	*
Common Mode Rejection Ratio, DC to 60Hz with 1kΩ source unbalance				
G = 1	70dB min (74dB typ)	74dB min (80dB typ)	**	**
G = 10	90dB min (94dB typ)	94dB min (100dB typ)	**	**
G = 100	100dB min (104dB typ)	104dB min (114dB typ)	**	**
G = 1000	100dB min (110dB typ)	110dB min (120dB typ)	**	**
NOISE				
Voltage RTO (p-p) @ 0.1Hz to 10Hz (Note 10)	$\sqrt{(0.5G)^2 + (225)^2}\,\mu V$	*	*	*
RMS RTO, 10Hz to 10kHz	$\sqrt{(1.2G)^2 + (50)^2}\,\mu V$	*	*	*
Input Current, rms, 10Hz to 10kHz	15pA (rms)	*	*	*
REFERENCE TERMINAL				
Bias Current	3μA	*	*	*
Input Resistance	10MΩ	*	*	*
Voltage Range	±10V	*	*	*
Gain to Output	1	*	*	*
POWER SUPPLY				
Operating Voltage Range	±5V to ±18V	*	*	*
Quiescent Supply Current	5mA max	*	*	*
TEMPERATURE RANGE				
Specified Performance	0 to +70°C	*	*	−55°C to +125°C
Operating	−25°C to +85°C	*	*	−55°C to +125°C
Storage	−65°C to +150°C	*	*	*
PACKAGE OPTION:[1] TO-116 Style (D14A)	AD521JD	AD521KD	AD521LD	AD521SD

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[1] See Section 20 for package outline information.

*Specifications same as AD521JD.
**Specifications same as AD521KD.
Specifications subject to change without notice.

NOTES:

1. Gains below 1 and above 1000 are realized by simply adjusting the gain setting resistors. For best results, voltage at either input should be restricted to ±10V for gains equal to or less than 1.

2. Nonlinearity is defined as the ratio of the deviation from the "best straight line" through a full scale output range of ±9 volts. With a combination of high gain and ±10 volt output swing, distortion may increase to as much as 0.3%.

3. Full Peak Response is the frequency below which a typical amplifier will produce full output swing.

4. Differential Overload Recovery is the time it takes the amplifier to recover from a pulsed 30V differential input with 15V of common mode voltage, to within 10mV of final value. The test input is a 30V, 10μs pulse at a 1kHz rate. (When a differential signal of greater than 11V is applied between the inputs, transistor clamps are activated which drop the excess input voltage across internal input resistors. If a continuous overload is maintained, power dissipated in these resistors causes temperature gradients and a corresponding change in offset voltage, as well as added thermal time constant, but will not damage the device.)

5. Common Mode Step Recovery is the time it takes the amplifier to recover from a 30V common mode input with zero volts of differential signal to within 10mV of final value. The test input is 30V, 10μs pulse at a 1kHz rate. (When a common mode signal greater than V_S -0.5V is applied to the inputs, transistor clamps are activated which drop the excessive input voltage across internal input resistors. Power dissipated in these resistors causes temperature gradients and a corresponding change in offset voltage, as well as an added thermal time constant, but will not damage the device.)

6. Output Offset Voltage versus Power Supply Change is a constant 0.005 times the unnulled output offset per percent change in either power supply. If the output offset is nulled, the output offset change versus supply change is substantially reduced.

7. Differential Input Impedance is the impedance between the two inputs.

8. Common Mode Input Impedance is the impedance from *either* input to the power supplies.

9. Maximum Input Voltage (differential or at either input) is 30V when using ±15V supplies. A more general specification is that neither input may exceed either supply (even when $V_S = 0$) by more than 15V and that the difference between the two inputs must not exceed 30V. (See also Notes 4 and 5.)

10. 0.1Hz to 10Hz Peak-to-Peak Voltage Noise is defined as the maximum peak-to-peak voltage noise observed during 2 of 3 separate 10 second periods with the test circuit of Figure 10.

DESIGN PRINCIPLE

Figure 1 is a simplified schematic of the AD521. A differential input voltage, V_{IN}, appears across R_G causing an imbalance in the currents through Q_1 and Q_2, $\Delta I = V_{IN}/R_G$. That imbalance is forced to flow in R_S because the collector currents of Q_3 and Q_4 are constrained to be equal by their biasing (current mirror). These conditions can only be satisfied if the differential voltage across R_S (and hence the output voltage of the AD521) is equal to $\Delta I \times R_S$. The feedback amplifier, A_{FB} performs that function. Therefore, $V_{OUT} = \frac{V_{IN}}{R_G} \times R_S$ or $\frac{V_{OUT}}{V_{IN}} = \frac{R_S}{R_G}$.

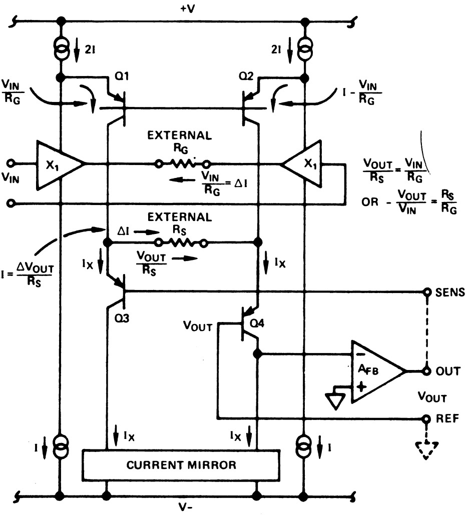
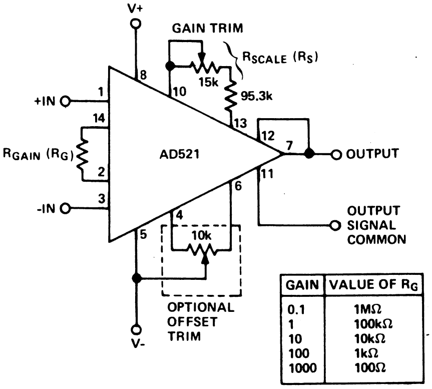


Figure 1. Simplified AD521 Schematic

APPLICATION NOTES FOR THE AD521

These notes ensure the AD521 will achieve the high level of performance necessary for many diversified IA applications.

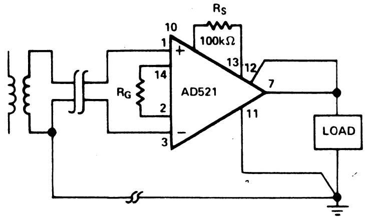
1. Gains below 1 and above 1000 are realized by adjusting the gain setting resistors as shown in Figure 2 (the resistor, R_S between pins 10 and 13 should remain 100kΩ ±15%, see application note 3). For best results, the input voltage should be restricted to ±10V especially for gain equal to or less than 1.
2. Provide a return path to ground for input bias currents. The AD521 is an instrumentation amplifier, not an isolation amplifier. When using a thermocouple or other "floating" source, this return path may be provided directly to ground or indirectly through a resistor to ground from pins 1 and/or 3, as shown in Figure 3. If the return path is not provided, bias currents will cause the output to saturate. The value of the resistor may be determined by dividing the maximum allowable common mode voltage for the application by the bias current of the instrumentation amplifier.



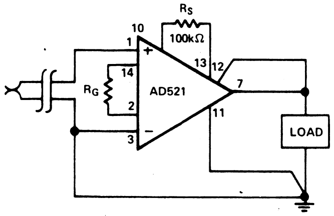
GAIN	VALUE OF R_G
0.1	1MΩ
1	100kΩ
10	10kΩ
100	1kΩ
1000	100Ω

Figure 2. Operating Connections for AD521

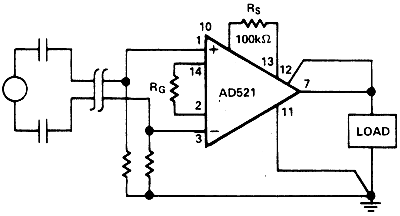
3. The resistors between pins 10 and 13, (R_{SCALE}) must equal 100kΩ ±15% (Figure 2). If R_{SCALE} is too low (below 85kΩ) the output swing of the AD521 is reduced. At values below 80kΩ and above 120kΩ the stability of the AD521 may be impaired.
4. Do not exceed the allowable input signal range. The linearity of the AD521 decreases if the inputs are driven within 5 volts of the supply rails, particularly when the device is used at a gain less than 1. To avoid this possibility, attenuate the input signal through a resistive divider network and use the AD521 as a buffer, as shown in Figure 4. The resistor R/2 matches the impedance seen by both AD521 inputs so that the voltage offset caused by bias currents will be minimized.



a). Transformer Coupled, Direct Return

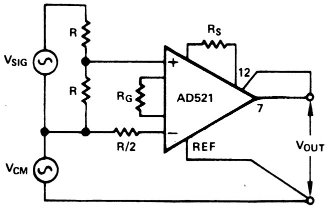


b). Thermocouple, Direct Return



c). AC Coupled, Indirect Return

Figure 3. Ground Returns for "Floating" Transducers



1. INCREASE R_G TO PICK UP GAIN LOST BY R DIVIDER NETWORK
2. INPUT SIGNAL MUST BE REDUCED IN PROPORTION TO POWER SUPPLY VOLTAGE LEVEL

Figure 4. Operating Conditions for $V_{IN} \approx V_S = 10V$

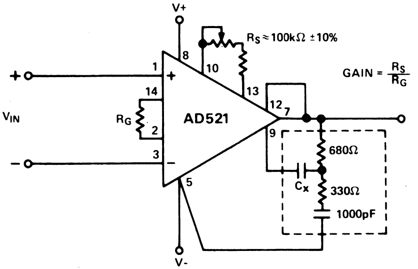
5. Use the compensation pin (pin 9) and the applicable compensation circuit when the amplifier is required to drive a capacitive load. It is worth mentioning that coaxial cables can "invisibly" provide such capacitance since many popular coaxial cables display capacitance in the vicinity of 30pF per foot.

This compensation (bandwidth control) feature permits the user to fit the response of the AD521 to the particular application as illustrated by Figure 5. In cases of extremely high load capacitance the compensation circuit may be changed as follows:

1. Reduce 680Ω to 24Ω
2. Reduce 330Ω to 7.5Ω
3. Increase 1000pF to 0.1μF
4. Set C_X to 1000pF if no compensation was originally used. Otherwise, do not alter the original value.

This allows stable operation for load capacitances up to 3000pF, but limits the slew rate to approximately 0.16V/μs.

6. Signals having frequency components above the Instrumentation Amplifier's output amplifier closed-loop bandwidth will be transmitted from V- to the output with little or no attenuation. Therefore, it is advisable to decouple the V- supply line to the output common or to pin 11.[1]



$C_X = \frac{1}{100\pi f_t}$ *when f_t is the desired bandwidth.*

(f_t in kHz, C_X in μF)

Figure 5. Optional Compensation Circuit

INPUT OFFSET AND OUTPUT OFFSET

When specifying offsets and other errors in an operational amplifier, it is often convenient to refer these errors to the inputs. This enables the user to calculate the maximum error he would see at the output with any gain or circuit configuration. An op amp with 1mV of input offset voltage, for example, would produce 1V of offset at the output in a gain of 1000 configuration.

In the case of an instrumentation amplifier, where the gain is controlled in the amplifier, it is more convenient to separate errors into two categories. Those errors which simply add to the output signal and are unaffected by the gain can be classified as output errors. Those which act as if they are associated with the input signal, such that their effect at the output is proportional to the gain, can be classified as input errors.

As an illustration, a typical AD521 might have a +30mV output offset and a -0.7mV input offset. In a unity gain configuration, the *total* output offset would be +29.3mV or the sum of the two. At a gain of 100, the output offset would be -40mV or: 30mV + 100(-0.7mV) = -40mV.

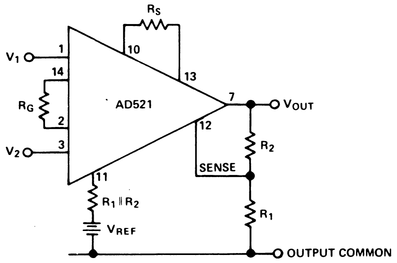
By separating these errors, one can evaluate the total error independent of the gain settings used, similar to the situation with the input offset specifications on an op amp. In a given gain configuration, both errors can be combined to give a total error *referred to the input* (R.T.I.) or *output* (R.T.O.) by the following formula:

Total Error R.T.I. = input error + (output error/gain)

Total Error R.T.O. = (Gain x input error) + output error

The offset trim adjustment (pins 4 and 6, Figure 2) is associated primarily with the output offset. At any gain it can be used to introduce an output offset equal and opposite to the input offset voltage multiplied by the gain. As a result, the total output offset can be reduced to zero.

As shown in Figure 6, the gain range on the AD521 can be extended considerably by adding an attenuator in the sense terminal feedback path (as well as adjusting the ratio, R_S/R_G). Since the sense terminal is the inverting input to the output amplifier, the additional gain to the output is controlled by R_1 and R_2. This gain factor is $1 + R_2/R_1$.



$$V_{OUT} = \left[V_{REF} + \left(\frac{R_S}{R_G}\right)\left(V_1 - V_2\right)\right]\left[\frac{R_1 + R_2}{R_1}\right]$$

Figure 6. Circuit for utilizing some of the unique features of the AD521. Note that gain changes introduced by changing R1 and R2 will have a minimum effect on output offset if the offset is carefully nulled at the highest gain setting.

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[1] For further details, refer to "An I.C. User's Guide to Decoupling, Grounding, and Making Things Go Right for a Change," by A. Paul Brokaw. This application note is available from Analog Devices without charge upon request.

Where offset errors are critical, a resistor equal to the parallel combination of R_1 and R_2 should be placed between pin 11 and V_{REF}. This minimizes the offset errors resulting from the input current flowing in R_1 and R_2 at the sense terminal. Note that gain changes introduced by changing the R_1/R_2 attenuator will have a minimum effect on output offset if the offset is carefully nulled at the highest gain setting.

When a predetermined output offset is desired, V_{REF} can be placed in series with pin 11. This offset is then multiplied by the gain factor $1 + R_2/R_1$ as shown in the equation of Figure 6.

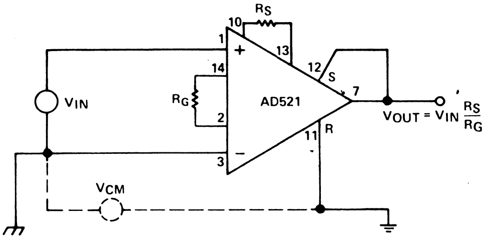


Figure 7. Ground loop elimination. The reference input, Pin 11, allows remote referencing of ground potential. Differences in ground potentials are attenuated by the high CMRR of the AD521.

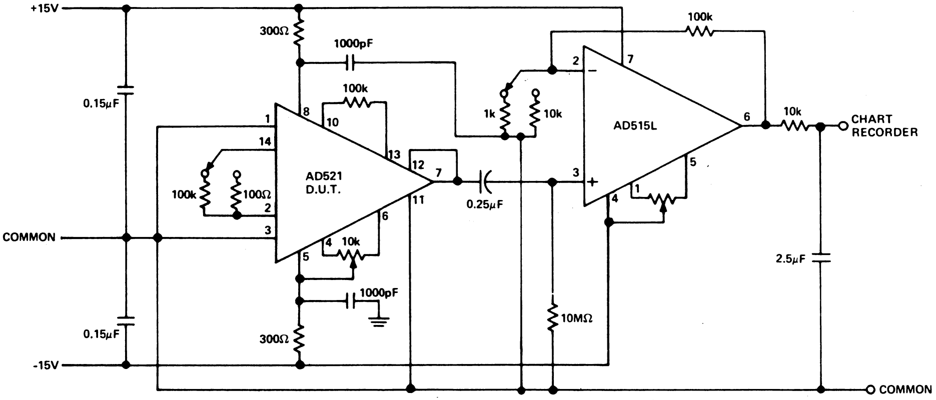


Figure 8. Test circuit for measuring peak to peak noise in the bandwidth 0.1Hz to 10Hz. Typical measurements are found by reading the maximum peak to peak voltage noise of the device under test (D.U.T.) for 3 observation periods of 10 seconds each.

ANALOG DEVICES

High Accuracy Data Acquisition Instrumentation Amplifier

AD522

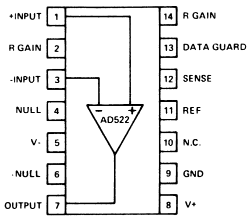
FEATURES

Performance
- Low Drift: 2.0μV/°C (AD522B)
- Low Nonlinearity: 0.005% (G = 100)
- High CMRR: >110dB (G = 1000)
- Low Noise: 1.5μV p-p (0.1 to 100Hz)
- Low Initial V_{OS}: 100μV (AD522B)

Versatility
- Single-Resistor Gain Programmable: 1 ⩽ G ⩽ 1000
- Output Reference and Sense Terminals
- Data Guard for Improving ac CMR

Value
- Internally Compensated
- No External Components except Gain Resistor
- Active Trimmed Offset, Gain, and CMR

AD522 FUNCTIONAL BLOCK DIAGRAM



14-PIN DIP

PRODUCT DESCRIPTION

The AD522 is a precision IC instrumentation amplifier designed for data acquisition applications requiring high accuracy under worst-case operating conditions. An outstanding combination of high linearity, high common mode rejection, low voltage drift, and low noise makes the AD522 suitable for use in many 12-bit data acquisition systems.

An instrumentation amplifier is usually employed as a bridge amplifier for resistance transducers (thermistors, strain gauges, etc.) found in process control, instrumentation, data processing, and medical testing. The operating environment is frequently characterized by low signal-to-noise levels, fluctuating temperatures, unbalanced input impedances, and remote location which hinders recalibration.

The AD522 was designed to provide highly accurate signal conditioning under these severe conditions. It provides output offset voltage drift of less than 10μV/°C, input offset voltage drift of less than 2.0μV/°C, CMR above 80dB at unity gain (110dB at G = 1000), maximum gain nonlinearity of 0.001% at G = 1, and typical input impedance of $10^9\Omega$.

This excellent performance is achieved by combining a proven circuit configuration with state-of-the-art manufacturing technology which utilizes active laser trimming of tight-tolerance thin-film resistors to achieve low cost, small size and high reliability. This combination of high value with no-compromise performance gives the AD522 the best features of both monolithic and modular instrumentation amplifiers, thus providing extremely cost-effective precision low-level amplification.

The AD522 is available in three versions with differing accuracies and operating temperature ranges; the "A", and "B" are specified from -25°C to +85°C, and the "S" is guaranteed over the military/aerospace temperature range of -55°C to +125°C. All versions are packaged in a 14-pin DIP and are supplied in a pin configuration similar to that of the popular AD521 instrumentation amplifier.

SPECIFICATIONS[1] (typical @ +V_S = ±15V, R_L = 2kΩ & T_A = +25°C unless otherwise specified)

MODEL	AD522AD	AD522BD	AD522S[2]
GAIN			
Gain Equation	$1 + \frac{2(10^5)}{R_g}$	*	*
Gain Range	1 to 1000	*	*
Equation Error			
G = 1	0.2% max	0.05% max	**
G = 1000	1.0% max	0.2% max	**
Nonlinearity, max (see Fig. 4)			
G = 1	0.005%	0.001%	**
G = 1000	0.01%	0.005%	**
vs. Temp, max			
G = 1	2ppm/°C (1ppm/°C typ)	*	*
G = 1000	50ppm/°C (25ppm/°C typ)	*	*
OUTPUT CHARACTERISTICS			
Output Rating	±10V @ 5mA	*	*
DYNAMIC RESPONSE (see Fig. 6)			
Small Signal (-3dB)			
G = 1	300kHz	*	*
G = 100	3kHz	*	*
Full Power GBW	1.5kHz	*	*
Slew Rate	0.1V/μs	*	*
Settling Time to 0.1%, G = 100	0.5ms	*	*
to 0.01%, G = 100	5ms	*	*
to 0.01%, G = 10	2ms	*	*
to 0.01%, G = 1	0.5ms	*	*
VOLTAGE OFFSET			
Offsets Referred to Input			
Initial Offset Voltage (adjustable to zero)			
G = 1	±400μV max (±200μV typ)	±200μV max (±100μV typ)	±200μV max (±100μV typ)
vs. Temperature, max (see Fig. 3)			
G = 1	±50μV/°C (±10μV/°C typ)	±25μV/°C (±5μV/°C typ)	±100μV/°C (±10μV/°C typ)
G = 1000	±6μV/°C	±2μV/°C	±6μV/°C
$1 < G < 1000$	$\pm(\frac{50}{G} + 6)$μV/°C	$\pm(\frac{25}{G} + 2)$μV/°C	$\pm(\frac{100}{G} + 6)$μV/°C
vs. Supply, max			
G = 1	±20μV/%	*	*
G = 1000	±0.2μV/%	*	*
INPUT CURRENTS			
Input Bias Current			
Initial max, +25°C	±25nA	±15nA	±25nA
vs. Temperature	±100pA/°C	±50pA/°C	±100pA/°C
Input Offset Current			
Initial max, +25°C	±20nA	±10nA	±20nA
vs. Temperature	±100pA/°C	±50pA/°C	±100pA/°C
INPUT			
Input Impedance			
Differential	10^9Ω	*	*
Common Mode	10^9Ω	*	*
Input Voltage Range			
Maximum Differential Input, Linear	±10V	*	*
Maximum Differential Input, Safe	±20V	*	*
Maximum Common Mode, Linear	±10V	*	*
Maximum Common Mode Input, Safe	±15V	*	*
Common Mode Rjection Ratio, Min @ ±10V, 1kΩ Source Imbalance (see Fig. 5)			
G = 1 (dc to 30Hz)	75dB (90dB typ)	80dB (100dB typ)	75dB (90dB typ)
G = 10 (dc to 10Hz)	90dB (100dB typ)	95dB (110dB typ)	90dB (110dB typ)
G = 100 (dc to 3Hz)	100dB (110dB typ)	100dB (120dB typ)	100dB (120dB typ)
G = 1000 (dc to 1Hz)	100dB (120dB typ)	110dB (>120dB typ)	100dB (>120dB typ)
G = 1 to 1000 (dc to 60Hz)	75dB (88dB typ)	80dB (88dB typ)	*
NOISE			
Voltage Noise, RTI (see Fig. 4)			
0.1Hz to 100Hz (p-p)			
G = 1	15μV	*	*
G = 1000	1.5μV	*	*
10Hz to 10kHz (rms)			
G = 1	15μV	*	*
TEMPERATURE RANGE			
Specified Performance	-25°C to +85°C	*	-55°C to +125°C
Operating	-55°C to +125°C	*	*
Storage	-65°C to +150°C	*	*
POWER SUPPLY			
Power Supply Range	±(5 to 18)V	*	*
Quiescent Current, max @ ±15V	±10mA	±8mA	**
PACKAGE OPTIONS[3,4]			
Hermetic, Metal (HY14D)	AD522AD	AD522BD	AD522SD

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[1] Specifications guaranteed after 10 minute warm-up.

[2] The AD522SD is available processed to MIL-STD-883, Level B.

[3] See Section 20 for package outline information.

[4] Analog Devices reserves the right to ship ceramic packages (H14A) in lieu of metal packages (HY14D).

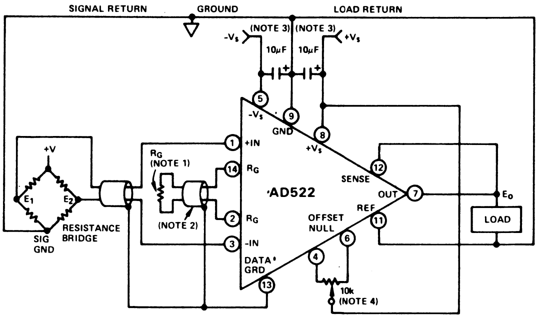
*Specifications same as AD522A.

**Specifications same as AD522B.

Specifications subject to change without notice.

GENERAL APPLICATION CONSIDERATIONS

Figure 1 illustrates the AD522 wiring configuration when used in a typical bridge amplifier application. In any low-level, high impedance, noise-dominated environment, proper shielding and grounding are requisite for optimum performance; a recommended technique is shown.



$$E_O = \left(1 + \frac{200k}{R_G}\right)\left[\left(E_1 - E_2\right) - \left(\frac{E_1 + E_2}{2} \times \frac{1}{CMR}\right)\right]$$

NOTES:
1. GAIN RESISTOR R_G SHOULD BE <5ppm/°C (VISHAY TYPE RECOMMENDED).
2. SHIELDED CONNECTIONS TO R_G RECOMMENDED WHEN MAXIMUM SYSTEM BANDWIDTH AND AC CMR IS REQUIRED, AND WHEN R_G IS LOCATED MORE THAN SIX INCHES FROM AD522. NO INSTABILITIES ARE CAUSED BY REMOTE R_G LOCATIONS. WHEN NOT USED, THE DATA GUARD PIN CAN BE LEFT UNCONNECTED.
3. POWER SUPPLY FILTERS ARE RECOMMENDED FOR MINIMUM NOISE IN NOISY ENVIRONMENTS.
4. NO TRIM REQUIRED FOR MOST APPLICATIONS. IF REQUIRED, A 10kΩ, 25ppm/°C, 25 TURN TRIM POT (SUCH AS VISHAY 1202-Y-10k) IS RECOMMENDED.

Figure 1. Typical Bridge Application

Direct coupling of the AD522 inputs makes it necessary to provide a signal ground return for input amplifier bias currents. This can be achieved by direct connection as shown, or through an indirect path of less than 1MΩ resistance such as other system interconnections.

To minimize noise, shielding should be provided for the input leads and gain resistor connections. A passive data guard is provided to improve ac common mode rejection by "bootstrapping" the capacitance of the input cabling, thus minimizing differential phase shift. This will also reduce degradation of system bandwidth.

Balanced design eliminates the need for external bypass capacitors for most applications. If, however, the power supplies are remotely located (farther than 10 feet or so) or if they are likely to carry more than a few millivolts of noise, local filtering will enable the user to retain optimal performance.

Reference and sense pins are provided to permit remote load sensing. These points can also be used to trim the device CMR, add an output booster, or to offset the output to a reference level. These applications are illustrated in following sections.

It is good practice to place R_G within several inches of the AD522. Longer leads will increase stray capacitance and cause phase shifts that will degrade CMR at higher frequencies. For frequencies below 10Hz, a remote R_G is generally acceptable; no stability problems are caused. Bear in mind that a leakage impedance of 200MΩ between R_G pins will cause an 0.1% gain error at G = 1. Unity gain is not trimmable.

TYPICAL APPLICATION AND ERROR BUDGET ANALYSIS (See Figure 1 and Table 1)

A floating transducer with a 0 to 1 volt output has a 1kΩ source imbalance. A noisy environment induces a one volt 0 to 60Hz common mode signal in the ground return. This signal must be amplified to interface with a data acquisition system calibrated for a 0 to 10 volt signal range. The operating temperature range is 0 to +50°C and an AD522B is to be used. Table 1 lists error sources and their effect on system accuracy.

The total effect on absolute accuracy is less than ±0.2%, allowing adjustment-free 8-bit operation. In computer or microprocessor controlled data-acquisition systems, automatic recalibration can nullify gain and offset drifts leaving noise, distortion and CMR as the only error sources. In this case, full 12-bit operation is achieved.

Gain Errors: Absolute gain errors can be nulled by trimming R_G. Gain drift is a linear effect, not detrimental to resolution and is caused by the change in value of internal resistors over the operating temperature range. An "intelligent" system can correct for these errors with an automatic calibration cycle. Gain nonlinearity never exceeds 0.002% at G = 10.

Offset Drift & Pins Current Errors: Special care has been taken in the design of the AD522 input stage to minimize offset drift. Unless transducer impedances are unbalanced by more than 2kΩ, errors caused by offset current drift are negligible compared to offset voltage drift. Although initial offset voltages are laser-nulled for most applications, provisions have been made to allow further adjustment to correct for initial system offset. In this example, all offset drifts amount to ±0.014% and do not effect resolution (can be corrected with an automatic calibration cycle).

CMR and Noise Errors: Common mode rejection and noise performance of instrumentation amplifiers are critical because

Error Source	Specification	Effect on Absolute Accuracy, % of F.S.	Effect on Resolution % of F.S.
Gain Nonlinearity	±0.002% max, G = 10 (from Spec. Sheet and Fig. 4)	±0.002	±0.002
Voltage Drift	$\frac{25\mu V/^\circ C}{Gain} + 2.0\mu V/^\circ C = 4.5\mu V/^\circ C$ R.T.I. = 0.00055%/°C (from Spec. Sheet)	±0.011	---
CMR	86dB (from Spec. Sheet, CMR vs. F vs. G, typical curve)	±0.005	±0.005
Noise, R.T.O. (0.1 to 100Hz)	15μV (p-p) R.T.O. (from Spec. Sheet, Noise vs. G typical curve)	±0.0015	±0.0015
Offset Current Drift	±50pA/°C x 1k source imbalance (Spec. Sheet) = ±50μV/°C = ±1.25μV R.T.I.	±0.000125	---
Gain Drift (add 10ppm/°C for external R_G)	60ppm/°C (Spec. Sheet)	±0.15	---

Table 1. Error Sources

these errors can not be corrected by calibration. Common mode rejection of the AD522 is active laser-trimmed to the limits of thin-film resistor stability. Further trimming could improve CMR on a short term basis, but regular readjustment would be necessary to maintain this improvement (see Figure 2). In this example, untrimmed CMR and noise cause a total error of ±0.0065% of full scale and are the major contributors to resolution error.

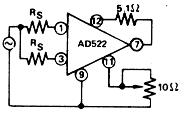


Figure 2. Optional CMR Trim

PERFORMANCE CHARACTERISTICS

Offset Voltage and Current Drift: The AD522 is available in four drift selections. Figure 3 is a graph of maximum RTO offset voltage drift vs. gain for all versions. Errors caused by offset voltage drift can thus be determined for any gain. Offset current drift will cause a voltage error equal to the product of the offset current drift and the source impedance unbalance.

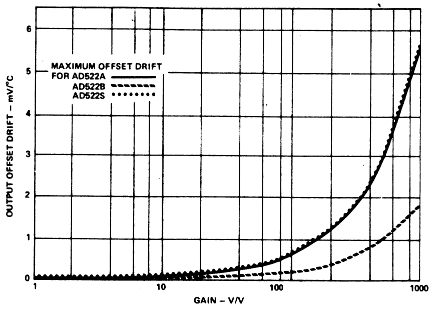


Figure 3. Output Offset Drift (RTO) vs. Gain

Gain Nonlinearity and Noise: Gain nonlinearity increases with gain as the device loop-gain decreases. Figure 4 is a plot of typical nonlinearity vs. gain. The shape of the curve can be safely used to predict worst-case nonlinearity at gains below 100. Noise vs. gain is shown on the same graph.

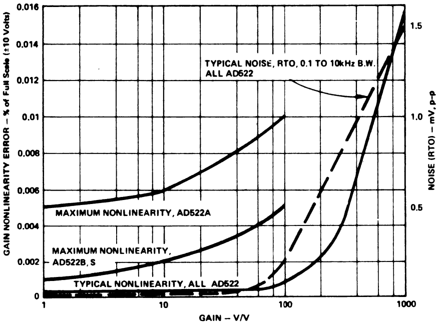


Figure 4. Gain Nonlinearity and Noise (RTO) vs. Gain

Common Mode Rejection: CMR is rated at ±10V and 1kΩ source imbalance. At lower gains, CMR depends mainly on thin-film resistor stability but due to gain-bandwidth considerations, is relatively constant with frequency to beyond 60Hz. The dc CMR improves with increasing gain and is increasingly subject to phase shifts in limited bandwidth high-gain amplifiers. Figure 5 illustrates CMR vs. Gain and Frequency.

Dynamic Performance: Settling time and unity gain bandwidth are directly proportional to gain. As a result, dynamic performance can be predicted from the well-behaved curves of Figure 6.

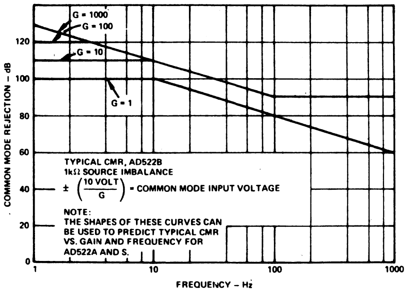


Figure 5. Common Mode Rejection vs. Frequency and Gain

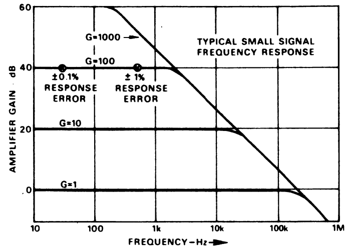


Figure 6. Small Signal Frequency Response (-3dB)

SPECIAL APPLICATIONS

Offset and Gain Trim: Gain accuracy depends largely on the quality of R_G. A precision resistor with a 10ppm/°C temperature coefficient is advised. Offset, like gain, is laser-trimmed to a level suitable for most applications. If further adjustment is required, the circuit shown in Figure 1 is recommended. Note that good quality (25ppm) pots are necessary to maintain voltage drift specifications.

CMR Trim: A short-term CMR improvement of up to 10dB at low gains can be realized with the circuit of Figure 2. Apply a low-frequency 20/G volt peak-to-peak input signal to *both* inputs through their equivalent source resistances and trim the pot for an ac output null.

Sense Output: A sense output is provided to enable remote load sensing or use of an output current booster. Figure 7 illustrates these applications. Being "inside the loop", booster drift errors are minimized. When not used, the sense output should be tied to the output.

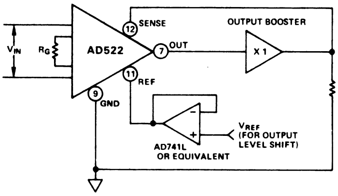


Figure 7. Output Current Booster and Buffered Output Level Shifter

Reference Output: The reference terminal is provided to permit the user to offset or "level shift" the output level to a datum compatible with his load. It must be remembered that the total output swing is ±10 volts to be shared between signal and reference offset. Furthermore, any reference source resistance will unbalance the CMR trim by the ratio $10k/R_{ref}$. For example, if the reference source impedance is 1Ω, CMR will be reduced to 80dB (10kΩ/1Ω = 10,000 = 80dB). A buffer amplifier can be used to eliminate this error, as shown in Figure 7, but the drift of the buffer will add to output offset drift. When not used, the reference terminal should be grounded.

ANALOG DEVICES

Precision Instrumentation Amplifier

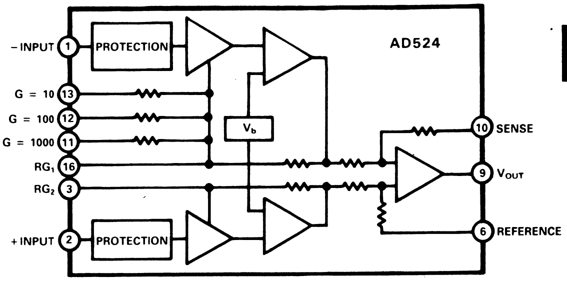
AD524

ADVANCE TECHNICAL DATA

FEATURES

- **Low Nonlinearity: 0.005% (G = 1)**
- **High CMRR: 130dB (G = 1000)**
- **Low Offset Voltage: 50µV**
- **Low Offset Voltage Drift: 0.5µV/°C**
- **Gain Bandwidth Product: 25MHz**
- **Pin Programmable Gains of 1, 10, 100, 1000**
- **Complete Input Protection, Power On – Power Off**
- **No External Components Required**
- **Internally Compensated**

AD524 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD524 is a precision monolithic instrumentation amplifier designed for data acquisition applications requiring high accuracy under worst-case operating conditions. An outstanding combination of high linearity, high common mode rejection, low offset voltage drift, and low noise makes the AD524 suitable for use in many data acquisition systems.

The AD524 has an output offset voltage drift of less than 20µV/°C, input offset voltage drift of less than 0.5µV/°C, CMR above 90dB at unity gain (120dB at G = 1000) and maximum nonlinearity of 0.005% at G = 1. In addition to the outstanding dc specifications the AD524 also has a 25MHz gain bandwidth product (G = 100). To make it suitable for high speed data acquisition systems the AD524 has an output slew rate of 5V/µs and settles in 15µs up to a gain of 100.

As a complete amplifier the AD524 does not require any external components for fixed gains of 1, 10, 100 and 1,000. For other gain settings between 1 and 1000 only a single resistor is required. The AD524 input is fully protected for both power on and power off fault conditions.

The AD524 IC instrumentation amplifier is available in four different versions of accuracy and operating temperature range. The economical "J" grade, the low drift "K" grade and lower drift, higher linearity "L" grade are specified from 0 to +70°C. The "S" grade guarantees performance to specification over the full MIL-temperature range: −55°C to +125°C and is available screened to MIL-STD-883, Class B.

PRODUCT HIGHLIGHTS

1. The AD524 has low guaranteed offset voltage, offset voltage drift and low noise for precision high gain applications.
2. The AD524 is functionally complete with pin programmable gains of 1, 10, 100 and 1000.
3. Input and output offset nulling terminals are provided for very high precision applications and to minimize offset voltage changes in gain ranging applications.
4. The AD524 is fully input protected for both power on and power off fault conditions.
5. The AD524 offers superior dynamic performance with a gain bandwidth product of 25MHz, full peak response of 75kHz and a settling time of 15µs to 0.01% of a 10V step (G = 100).

SPECIFICATIONS (typical @ V_S = ±15V, R_L = 2KΩ and T_A = +25°C unless otherwise specified)

Model	AD524J	AD524K	AD524L	AD524S
GAIN				
Gain Equation				
(External Resistor Gain Programming)	$\frac{40{,}000}{R_G} + 1 \pm 20\%$	*	*	*
Gain Range	1 to 1000	*	*	*
Pin Programmable				
Gain Error, Max				
G = 1	±0.05%	±0.02%	±0.02%	*
G = 10	±0.25%	±0.1%	±0.05%	*
G = 100	±0.5%	±0.25%	±0.1%	*
G = 1000	±5%	±2.5%	±1%	*
Nonlinearity, max				
G = 1	±0.01%	*	±0.005%	*
G = 10	±0.01%	*	±0.005%	*
G = 100	±0.01%	*	*	*
G = 1000	±0.01%	*	*	*
Gain vs. Temperature				
G = 1	5ppm/°C	*	*	*
G = 10	5ppm/°C	*	*	*
G = 100	10ppm/°C	*	*	*
G = 1000	25ppm/°C	*	*	*
OUTPUT RATING	±10V @ 5mA	*	*	*
DYNAMIC RESPONSE				
Small Signal − 3dB				
G = 1	1MHz	*	*	*
G = 10	400kHz	*	*	*
G = 100	150kHz	*	*	*
G = 1000	25kHz	*	*	*
Slew Rate				
G = 1	2.5V/µs	*	*	*
G = 10–1000	5.0V/µs	*	*	*
Settling Time to 0.01%				
G = 1 to 10	15µs	*	*	*
G = 100	15µs	*	*	*
G = 1000	75µs	*	*	*
VOLTAGE OFFSET (May be Nulled)				
Input Offset Voltage, max	250µV	100µV	50µV	**
vs. Temperature, max	2µV/°C	1µV/°C	0.5µV/°C	2µV/°C
Output Offset Voltage, max	1mV	500µV	250µV	**
vs. Temperature, max	100µV/°C	50µV/°C	20µV/°C	20µV/°C
Offset Referred to the Input vs. Supply				
G = 1	75dB	80dB	85dB	**
G = 10	85dB	95dB	100dB	**
G = 100	90dB	100dB	105dB	**
G = 1000	100dB	110dB	115dB	**
INPUT CURRENT				
Input Bias Current, max	±50nA	±20nA	±10nA	*
vs. Temperature	±100pA/°C	*	*	*
Input Offset Current, max	±35nA	±15nA	±10nA	*
vs. Temperature	±100pA/°C	*	*	*
INPUT				
Input Impedance				
Differential	$10^9\Omega$	*	*	*
Common Mode	$10^9\Omega$	*	*	*
Input Voltage Range				
Max Differ. Input Linear	±10V	*	*	*
Max Common Mode Linear	±10V	*	*	*
Common Mode Rejection Ratio dc to 60Hz with 1kΩ Source Imbalance, min				
G = 1	70	75	80	*
G = 10	90	95	100	*
G = 100	110	115	120	*
G = 1000	115	125	130	*
NOISE				
Voltage Noise, 1kHz				
R.T.I.	$\sqrt{(7nV/\sqrt{Hz})^2 + \left(\frac{90nV/\sqrt{Hz}}{G}\right)^2}$	*	*	*
R.T.O	$\sqrt{(90nV/\sqrt{Hz})^2 + (7nV/\sqrt{Hz} \times G)^2}$	*	*	*
TEMPERATURE RANGE				
Specified Performance	0 to +70°C	*	*	−55°C to +125°C
Storage	+65°C to +150°C	*	*	*
POWER SUPPLY				
Power Supply Range	±6V to ±18V	*	*	*
Quiescent Current	5mA max	3.5mA	**	**
PACKAGE OPTIONS[1]				
Hermetic 16-Pin Ceramic DIP	D16A	*	*	*
Plastic 16-Pin DIP	N16A	*	*	–

NOTES
[1] See Section 20 for package outline information.
*Specifications same as AD524J.
**Specifications same as AD524K.
Specifications subject to change without notice.

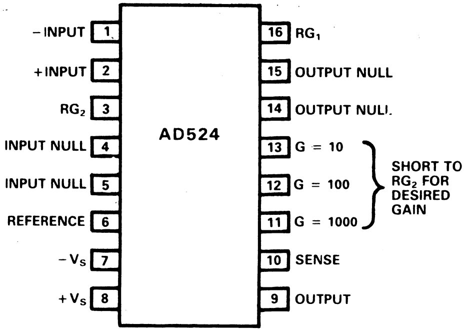


Figure 1. Pin Configuration

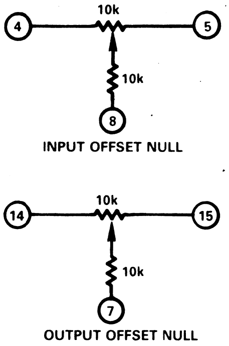


Figure 2. Offset Null Circuits

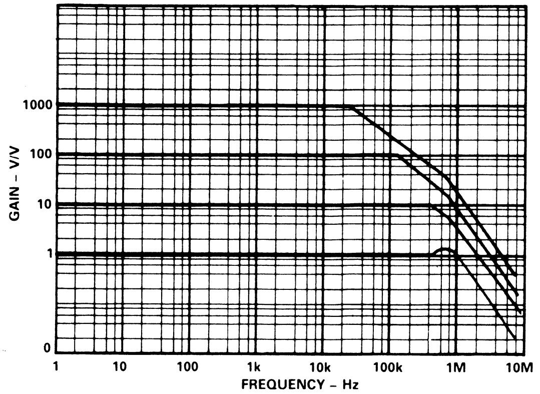


Figure 3. Gain vs. Frequency

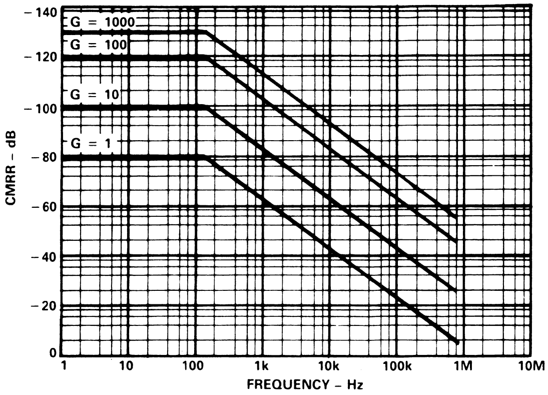


Figure 4. CMRR vs. Frequency RTI, Zero to 1k Source Imbalance

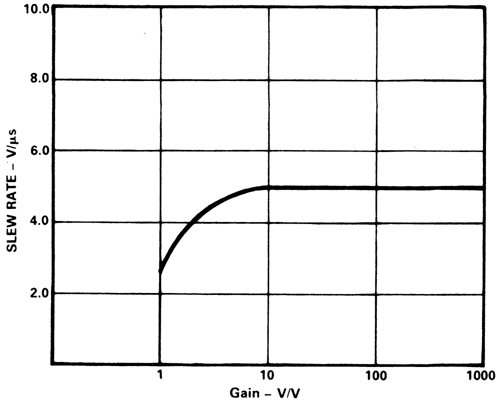


Figure 5. Slew Rate vs. Gain

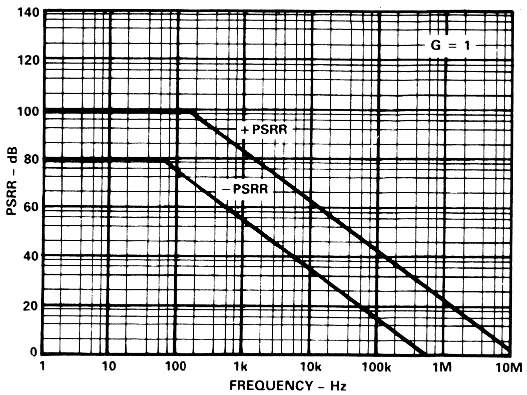


Figure 6. PSRR vs. Frequency

APPLICATION NOTES ON THE AD524

1. The AD524 has internal high accuracy pretrimmed resistors for pin programmable gains of 1, 10, 100 and 1000. One of the preset gains can be selected by pin strapping the appropriate gain terminal and RG$_2$ together.

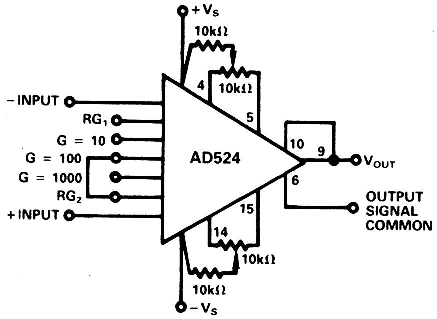


Figure 7. Operating Connections for G = 100

2. The AD524 can be configured for gains other than those that are internally preset. There are two methods to do this. The first shown in Figure 8a uses just an external resistor to program the gain.

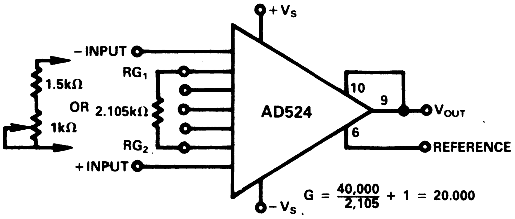


Figure 8a. Operating Connections for G = 20

The second technique uses the internal resistors in parallel with an external resistor Figure 8b. This technique minimizes the gain adjustment range and reduces the effects of temperature coefficient sensitivity.

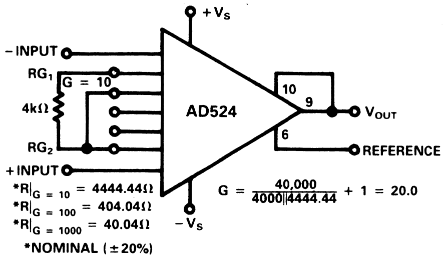


Figure 8b. Operating Connections for G = 20, Low Gain T.C. Technique

3. The AD524 may also be configured to provide gain in the output stage. Figure 9 shows an H pad attenuator connected to the reference and sense lines of the AD524. R1, R2 and R3 should be made as low as possible to minimize the gain variation and reduction of CMRR. Varying R2 will precisely set the gain without affecting CMRR. CMRR is determined by the match of R1 and R3.

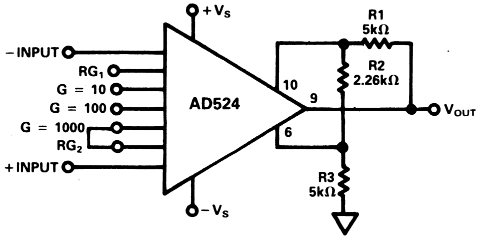


Figure 9. Gain of 2000

Output Gain	R1, R3	R2	Nominal Gain
2	5kΩ	2.26kΩ	2.02
5	2.05kΩ	1.05kΩ	5.01
10	1kΩ	4.42kΩ	10.1

Table 1. Output Gain Resistor Values

4. To minimize noise, shielding should be provided for the inputs. An active data guard is configured to improve ac common mode rejection by "bootstrapping" the capacitances of the input cabling, thus minimizing differential phase shift. This will also reduce degradation of system bandwidth.

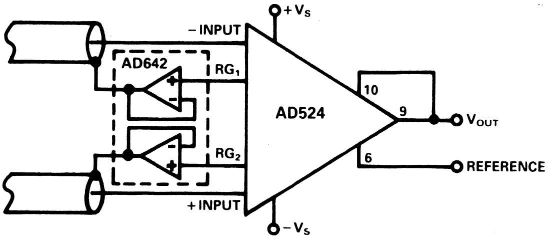


Figure 10. Differential Shield Drivers

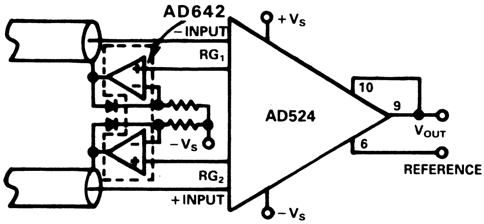


Figure 11. Improved Differential Shield Driver

ANALOG DEVICES

Self-Contained High Performance Wide Band Instrumentation Amplifiers

AD612, AD614

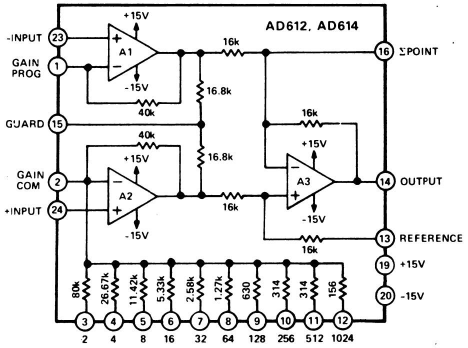
FEATURES

Pin-Programmable Gain: 1 to 1,024 in Binary Steps
Fast Settling: 20μs max to 0.05%, @ G = 128 (AD614A,B)
High Gain Accuracy: ±0.02% max (AD612C)
Gain Nonlinearity: ±0.001%
Low Gain TC: ±10ppm/°C max
Low Offset Drift: ±1μV/°C max, RTI, G = 1024 (AD612C)
High CMR: 94dB min @ G = 1,024
Hybrid Construction

APPLICATIONS

Low Level High Speed Data Acquisition Systems
Bridge Amplifiers for Resistance Transducers
Precision Current Amplifiers
Preamplifier for Recorder Instrumentation

AD612, AD614 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD612, AD614 are self-contained, high accuracy, high speed hybrid instrumentation amplifiers designed for data acquisition applications requiring speed and accuracy under worst-case operating conditions. Three versions (A, B, C) of the AD612 are available which provide superior dc characteristics with good dynamic performance, while the AD614 (A & B) versions provide superior dynamic performance with good dc characteristics.

The AD612, AD614 contain precision thin-film resistor networks that allows the user to set the gain in binary steps from 1 to 1024V/V by strapping the appropriate gain pins. In addition the excellent tracking characteristics of the active laser-trimmed thin-film resistors provide maximum gain drift of ±10ppm/°C max.

The AD612, AD614 are designed to provide high speed and high accuracy signal conditioning. They feature input offset drift of 1μV/°C max, output offset drift of ±75μV/°C max, CMR of 74dB min at unity gain (94dB min at G = 1024) in the highest accuracy version (AD612C) or 160kHz small signal bandwidth and settling time to 0.01% of 30μs max in the high speed version (AD614A or B).

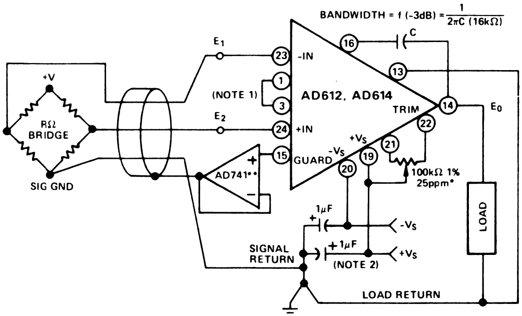
APPLICATIONS

The AD612, AD614 offer exceptional quality and value to the data acquisition designer, either as a signal conditioner per channel or as a high speed instrumentation amplifier in multichannel data acquisition systems, analytical instruments and transducer interfacing.

High CMR, input protection, low noise and excellent temperature stability make the AD612, AD614 an excellent choice for precise measurement and control in harsh industrial environments. The high speed of the AD612, AD614 provide higher throughput rates in multichannel data acquisition systems.

INTERCONNECTION DIAGRAM AND SHIELDING TECHNIQUES

Figure 1 shows the interconnection diagram for the AD612, AD614 along with the recommended shielding and grounding techniques. Because the AD612, AD614 are direct coupled, a ground return path for amplifier bias currents must be provided either by direct connection (as shown) or by an implicit ground path having up to 1MΩ resistance between signal ground and amplifier common. For best performance, sensitive input and gain setting terminals should be shielded from noise sources especially at high gains. The AD612, AD614 provide a guard terminal to drive the input cable shield at the input common mode voltage. This feature greatly reduces noise pickup and improves CMRR by maintaining the shield at the common mode voltage.



$$E_0 = \underbrace{(2)}_{\substack{\text{GAIN}\\ \text{(NOTE 1)}}} \times \left[\underbrace{(E_1 - E_2)}_{\substack{\text{INPUT}\\ \text{SIGNAL}}} + \underbrace{\left(\frac{E_1 + E_2}{2}\right) \times \left(\frac{1}{CMR}\right)}_{\text{CMR ERROR}}\right]$$

NOTES
*OPTIONAL INITIAL OFFSET TRIM POT.
**RECOMMENDED FOR LONG LEAD LENGTHS OR HIGH BANDWIDTHS.
1. GAIN SHOWN IS EQUAL TO 2. GAIN IS SELECTABLE, IN BINARY STEPS, BY PIN STRAPPING.
2. IN NOISY ENVIRONMENTS BYPASS CAPACITORS ARE RECOMMENDED.

Figure 1. Typical Bridge Application

For detailed information, contact factory.

SPECIFICATIONS (typical @ +25°C and V_S = ±15V, unless otherwise noted)

MODEL	HIGH ACCURACY AD612A	AD612B	AD612C	HIGH SPEED AD614A	AD614B
GAIN					
Gain Range, in Binary Steps	1 to 1024V/V	*	*	1 to 1024V/V	**
Gain Temperature Coefficient	±10ppm/°C max	*	*	±10ppm/°C max	**
Gain Accuracy, R_L = 10kΩ	±0.1% max	±0.04% max	±0.02% max	±0.1% max	±0.04% max
Gain Nonlinearity	±0.001%	*	*	±0.001%	**
RATED OUTPUT					
Voltage	±10V min	*	*	±10V min	**
Current	±5mA min	*	*	±5mA min	**
Impedance	0.15Ω	*	*	0.15Ω	**
INPUT CHARACTERISTICS					
Absolute Max Voltage	±V_S	*	*	±V_S	**
Common Mode Voltage	±10V min	*	*	±10V min	**
Differential and Common Mode Impedance	10^9 Ω‖3pF	*	*	10^9 Ω‖3pF	**
OFFSET VOLTAGES					
Input Offset Voltage					
Initial @ +25°C (Adjustable to Zero)[1]	±200μV	*	*	±200μV	**
vs. Temperature (G = 1024)(−25°C to +85°C)	±5μV/°C max	±2μV/°C max	±1μV/°C max	±5μV/°C max	±2μV/°C max
vs. Supply (G = 1024)	±25μV/V	*	*	±25μV/V	**
Output Offset Voltage G = 1					
Initial @ +25°C (Adjustable to Zero)	±2mV	*	*	±2mV	**
vs. Temperature (−25°C to +85°C)	±200μV/°C max	±150μV/°C max	±75μV/°C max	±200μV/°C max	±150μV/°C max
INPUT BIAS CURRENT					
Initial @ +25°C	+100nA max	*	*	+100nA max	**
vs. Temperature (−25°C to +85°C)	±0.5nA/°C	*	*	±0.5nA/°C	**
INPUT DIFFERENCE CURRENT					
Initial @ +25°C	±2nA	*	*	±2nA	**
vs. Temperature (−25°C to +85°C)	±10pA/°C	*	*	±10pA/°C	**
INPUT VOLTAGE NOISE, G = 1024					
0.01Hz to 10Hz	1μV p-p	*	*	1μV p-p	**
10Hz to 10kHz	2μV rms	*	*	2μV rms	**
OUTPUT VOLTAGE NOISE, (G = 1)					
0.01Hz to 10Hz	20μV p-p	*	*	20μV p-p	**
10Hz to 10kHz	50μV rms	*	*	50μV rms	**
COMMON MODE REJECTION RATIO					
1kΩ Source Imbalance, dc to 60Hz					
G = 1	74dB min	*	*	74dB min	**
G = 1024	94dB min	*	*	94dB min	**
DYNAMIC RESPONSE					
Slew Rate	1V/μs	*	*	1V/μs	**
Small Signal Bandwidth (−3dB)					
G = 1	100kHz	*	*	100kHz	**
G = 128	60kHz	*	*	160kHz	**
G = 1024	10kHz	*	*	20kHz	**
Settling Time to 0.01% 20V p-p Output Step					
G = 1	200μs max	*	*	40μs max	**
G = 128	100μs max	*	*	30μs max	**
Settling Time to 0.05% 20V p-p Output Step					
G = 1 to 128	60μs max	*	*	20μs max	**
G = 1024	150μs max	*	*	70μs max	**
POWER SUPPLY[2]					
Voltage, Rated Performance	±15V	*	*	±15V	**
Voltage, Operating	±8V to ±18V	*	*	±8V to ±18V	**
Current, Quiescent	±8mA	*	*	±8mA	**
TEMPERATURE RANGE					
Rated Performance	−25°C to +85°C	*	*	−25°C to +85°C	**
Storage	−55°C to +125°C	*	*	−55°C to +125°C	**

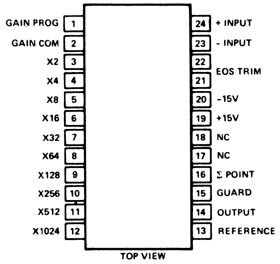
*Specifications same as AD612A.
**Specifications same as AD614A.

[1] One minute warm-up.

[2] Recommend model 904, ±15V @ ±50mA.

Specifications subject to change without notice.

PIN CONFIGURATION



TYPICAL ERROR BUDGET ANALYSIS

The error calculations for a typical transducer application shown in Figure 1 (350Ω bridge, 1mV/V FS, 10V excitation) are listed in Table 1.

Assumptions: AD612C is used, G = 1024V/V, temperature range is +25°C ±10°C, source imbalance is 100Ω, common mode noise is 0.05V rms (60Hz) on the ground return.

Error	% of FS (10V)	Calculations
Gain Nonlinearity	±0.001%	
Gain Accuracy	±0.02%	
Gain Drift	±0.01%	
Voltage Offset Drift	±0.11%	±11mV/°C (RTO) x ΔT x 1/10V
Offset Current Drift	±0.0004%	±10pA/°C x G x ΔT x 350Ω x 1/10V
Noise	±0.01%	
Total Output Error	±0.15% Worst Case	

Table 1. Error Budget Analysis

OPERATING INSTRUCTIONS

Install AD612, AD614 as shown in the diagram of Figure 1. Gain setting, offset trim and use of reference and guard terminals are described below.

Gain Setting: The AD612, AD614 operates at G = 1 without pin strapping. For binary gains 2 thru 256, strap appropriate gain pin (3 thru 10) to the gain programming pin (1). For gain 512, strap both pins 10 and 11 to pin 1; for gain 1024, strap pins 10, 11 and 12 to pin 1. The exceptional gain accuracy and gain drift of the AD612, AD614 are provided by the internal laser-trimmed thin-film resistor network.

If a nonbinary gain is required, an external resistor (R_G) can be connected between pins 1 and 2 to set the gain according to the formula $G = 1 + (80k/R_G)$. For R_G a precision resistor with a 10ppm/°C temperature coefficient is recommended.

Figure 2 shows a way to reduce the effects of R_G on gain accuracy and drift by using part of the internal resistor network in parallel with an external resistor to set the gain. Since the current flowing through the external resistor in Figure 2 is a small part of the total current, the effect of the external resistor is reduced by the ratio.

$$\left(\frac{R_{\text{internal}}}{R_{\text{internal}} + R_{\text{external}}}\right)$$

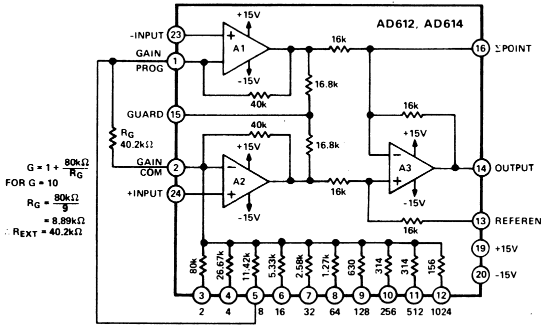


Figure 2. Nonbinary Gain Setting

Reference Output: Normally tied to load low, the reference terminal (pin 13) may be connected to a stable reference voltage, E_{REF}, to permit adjustment of the output level between ±10V, independent of initial offset adjustments. Source impedance of E_{REF} will be critical to CMR rating since the impedance at pin 13 is 16kΩ and forms a balanced bridge network around the output amplifier stage. (For example, a 60Ω imbalance results in a CMR of 49dB; 16kΩ/60Ω = 49dB). The use of a buffer amplifier, as shown below, will eliminate these difficulties. Reference source stability becomes critical when operating at low gains since any shifts may be referred to the input as RTI offset errors; i.e., $\Delta E_{REF}/G$ = Offset Error (RTI).

Common Mode Rejection: CMR is dependent on source impedance imbalance, signal frequency and amplifier gain. CMR is specified at gains 1 and 1024 with ±10V CMV and 1kΩ source imbalance over the frequency range of dc to 60Hz. Figure 5 shows the typical CMR performance vs. gain and frequency. For AD612, AD614 CMR is typically 26dB above the specified minimum.

Figures 6 and 7 illustrate the effect of source imbalance on CMR performance at dc (Figure 6) and at 60Hz (Figure 7) for several gains. CMR is typically 120dB at 60Hz and a 1kΩ source imbalance. At Gain = 1, CMR is maintained greater than 80dB for source imbalances up to 100kΩ.

Output Noise: As one would expect, total output voltage noise increases with gain and frequency. Figure 9 shows the typical wideband (10Hz to 10kHz) output noise performance vs. gain for 0Ω and 100kΩ source resistances.

Figure 10 shows output noise for several source resistances.

Bandwidth and Settling Time: Bandwidth (-3dB) is relatively constant with gain (see Figure 11) and is typically 100kHz at gain 1. At 4V/V and below, gain starts peaking at about 20kHz. Full power response and slew rate are 16kHz and 1V/μs (typ) respectively, independent of gain.

Settling time response to ±10V step output is relatively constant and gain insensitive, except for gains below 4V/V. AD612, AD614 have two speed selections with the AD612A, B, C being the slower versions and the AD614A, B, the faster versions. Settling times are specified to 0.01% for gains 1 and 128, and 0.05% for gains 1, 128 and 1024. Figure 12 shows typical settling times vs. gain for both versions to 0.01% and 0.05% accuracies. Settling time to 0.01% for gains greater than 128 are not shown because of the effects of voltage noise at the higher gains.

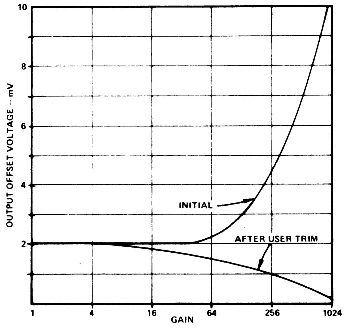


Figure 3. Total Offset Voltage (Typical) vs. Gain (RTO)

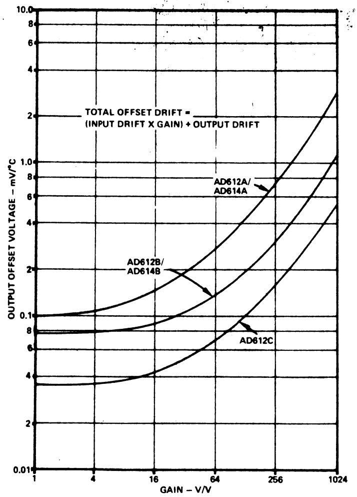


Figure 4. Total Offset Voltage Drift (Typical) vs. Gain (RTO)

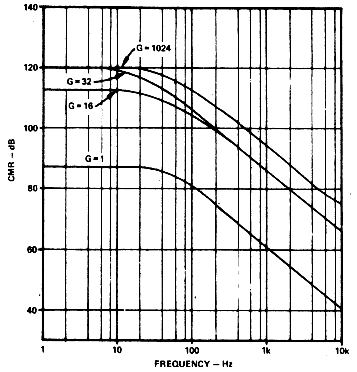


Figure 5. Common-Mode Rejection vs. Frequency and Gain

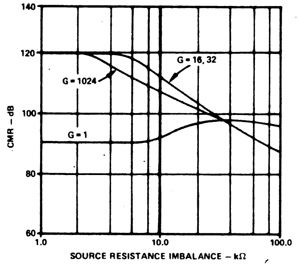


Figure 6. DC Common-Mode Rejection vs. Source Resistance Imbalance

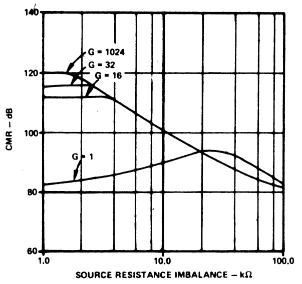


Figure 7. 60Hz Common-Mode Rejection vs. Source Resistance Imbalance

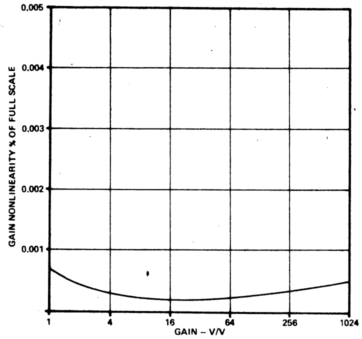


Figure 8. Gain Nonlinearity vs. Gain

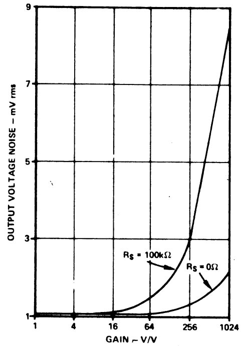


Figure 9. Wideband Output Voltage Noise vs. Gain

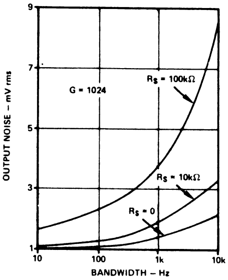


Figure 10. Output Voltage Noise vs. Bandwidth

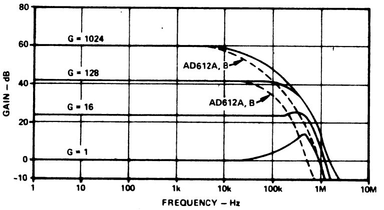


Figure 11. Small Signal Frequency Response

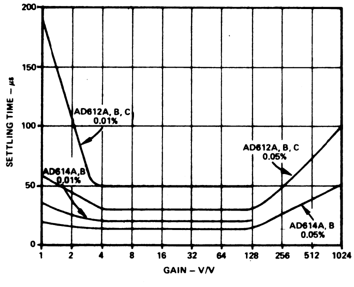


Figure 12. Settling Time vs. Gain

ANALOG DEVICES

Hybrid Industrial/ Medical Isolation Amplifier

AD293/AD294

FEATURES

High Common Mode Voltage: AD293 ±2500V peak max
AD294 ±8000V peak max
Nonlinearity: ±0.05% max (AD293B)
Adjustable Input & Output Gain: 1V/V to 1000V/V
Complies with NEMA ICS1-111
Meets UL Std 544 Leakage: 2.0μA max @ 115V ac, 60Hz
Hermetically Sealed Hybrid Construction
Military Versions Available
Low Cost:

APPLICATIONS

Off Ground Signal Measurement
Industrial Control
Nuclear & Military Instrumentation
High Voltage Protection for Data Acquisition Systems
Medical Diagnostic and Patient Monitoring Equipment

GENERAL DESCRIPTION

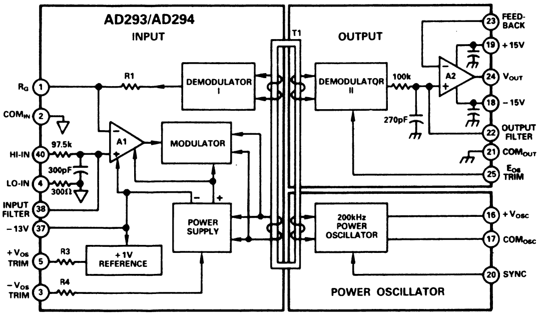
The AD293/AD294 are low-cost, high-accuracy, high reliability hybrid isolation amplifiers designed specifically for industrial, medical and military applications. The AD293 is available in three selected versions for industrial and military use; two of which are graded for nonlinearity, the AD293A (±0.1% max) and the AD293B (±0.05% max). The third version, AD293S/883B, is designed for extended temperature operation (−55°C to +125°C) offering screening and testing per MIL-STD-883B. The AD294A provides low leakage and higher CMV capability required for medical applications. Using modulation techniques with a proprietary hybrid magnetic transformer, the AD293/AD294 provides isolation from ground loop and leakage paths and guarantees common mode voltage protection up to ±2500V/±8000V peak respectively. All versions provide a small signal (−3dB) frequency response from dc to 2.5kHz and a large signal (full power) frequency response from dc to 250Hz at a gain of 1V/V. Gain, from 1V/V to 1000V/V, can be programmed at either the input section or output section allowing for user flexibility.

The AD293/AD294 are available in hermetically sealed 40 pin DIP ceramic packages that insure quality performance, high stability, and high reliability. Input/output pin spacing comply with NEMA (ICS1-111) separation specifications which is necessary for many industrial applications.

WHERE TO USE THE AD293/AD294

Industrial: In process control systems, high CMV instrumentation and multi-channel computer interface systems, the AD293 provides guaranteed protection against high transient voltages, lethal ground fault currents and high common mode voltages.

AD293, AD294 FUNCTIONAL BLOCK DIAGRAM



Medical: In biomedical and patient monitoring equipment such as ECG recorders, diagnostic systems and blood pressure monitors, the AD294A offers protection from lethal ground fault currents as well as 8kV peak defibrillator pulse inputs.

Low level signal recording and monitoring is achieved with the AD294A's low input noise (10μV p-p @ G = 100V/V) high CMR (100dB min @ 60Hz).

Military: In servo systems and instrumentation the AD293S/883B provides isolation from both ground loops and high common mode voltages.

DESIGN FEATURES AND USER BENEFITS

Adjustable Gain: Gain can be selected at either the input, output, or both. Thus, circuit response can be tailored to the user's application. The input gain can be selected from 1V/V to 100V/V with a single resistor. The output gain can be selected from 1V/V to 10V/V with or without compensation. The AD293/AD294 provides the user with flexibility for circuit optimization without requiring external active components.

Buffered Output: The AD293/AD294 prevent inaccuracies related to low impedance loads by providing an uncommitted output amplifier capable of supplying ±10V @ 2mA min.

Isolated Power: Low level isolated power provides −13V @ 200μA. This feature permits the AD293/AD294 to enhance system designs by eliminating the need for a separate isolated dc/dc converter.

SPECIFICATIONS (typical @ + 25°C, & V_S = 15V unless otherwise noted)

MODEL	AD293A	AD293B	AD293S/883B†	AD294A
GAIN				
Range	1 to 1000V/V	*	*	*
Formula (Input)	$G_{IN} = \left(1 + \frac{100k}{R_G}\right)$; $R_G \geq 1k\Omega$; G_{IN} max = 100			
(Output)	$G_{OUT} = \left(1 + \frac{R_A}{R_B}\right)$; $1 \leq G_{OUT} \leq 10$; G_{OUT} max = 10			
Deviation from Formula	± 1.0%	*	*	*
vs. Temperature (– 25°C to + 85°C)[1] (Gain = 1)	± 50ppm/°C max	*	*	*
(Gain > 1)	± 100ppm/°C max	*	*	*
Nonlinearity (± 5V swing)[2,3]	± 0.1% max	± 0.05% max	*	*
INPUT VOLTAGE RATINGS				
Linear Differential Range	± 10V min	*	*	*
Max Safe Differential Input				
Continuous	120V rms max	*	*	*
1 Minute	240V rms max	*	*	*
Max CMV (Inputs to Outputs)				
Continuous (ac or dc)	± 2500V peak	*	*	± 3500V peak
ac, 60Hz, 1 minute Duration	2500V rms	*	*	3500V rms
Pulse, 10ms Duration, 1 pulse/10 sec	—	—	—	± 8000V peak
CMR				
$R_S \leq 1k\Omega$ Balanced Source Impedance	115dB	*	*	*
$R_S \leq 1k$ Source Impedance Imbalance	100dB min	*	*	*
$R_S \leq 5k$ Balanced Source Impedance	—	—	—	115dB
$R_S \leq 5k$ Source Impedance Imbalance	—	—	—	100dB min
Leakage Current, Input to Output				
@ 115V ac, 60Hz	2μA rms max	*	*	*
Input Impedance, G = 1				
Differential	150pF‖$10^8\Omega$	*	*	*
Overload	100kΩ	*	*	*
Common Mode	30pF‖($5 \times 10^{10}\Omega$)	*	*	*
Input Difference Current				
Initial @ + 25 °C	2nA (7nA max)	*	*	*
vs. Temperature	2pA/°C	*	*	*
Input Noise (G = 100V/V)				
Voltage				
0.05Hz to 100Hz	10 μV p-p	*	*	*
10Hz to 1kHz	5μV rms	*	*	*
Current				
0.05Hz to 100Hz	50pA p-p	*	*	*
FREQUENCY RESPONSE				
Small Signal (– 3dB) G = 1V/V to 100V/V	2.5kHz	*	*	*
Full Power, 20V p-p Output				
G = 1V/V (G_{IN} = 1V/V, G_{OUT} = 1V/V)	250Hz	*	*	*
G = 100V/V (G_{IN} = 100V/V, G_{OUT} = 1V/V)	250Hz	*	*	*
G = 10V/V (G_{IN} = 1V/V, G_{OUT} = 10V/V)	2.5kHz	*	*	*
Slew Rate	9.1V/ms	*	*	*
OFFSET VOLTAGE, REFERRED TO INPUT				
Initial, @ + 25°C, max	$\left(\pm 8 \pm \frac{10}{G}\right)$mV	*	*	*
vs. Temperature				
(– 25°C to + 85°C) max	$\left(\pm 25 \pm \frac{150}{G}\right)\mu V/°C$	$\left(\pm 5 \pm \frac{100}{G}\right)\mu V/°C$	*	*
vs. Supply Voltage	75μV/V	*	*	*
RATED OUTPUT				
Voltage, 5kΩ Load	± 10V min	*	*	*
Output Impedance	< 1Ω	*	*	*
Output Ripple, (dc to 100kHz) Bandwidth	4mV p-p	*	*	*
POWER SUPPLY				
Voltage, Rated Performance	± 15V dc ± 5%	*	*	*
Voltage, Operating	± 15V dc ± 10%	*	*	*
Current, Quiescent (@ V_S = ± 15V)	+ 10mA, – 1mA	*	*	*
ISOLATED POWER	– 13V dc @ 200μA	*	*	*
TEMPERATURE RANGE				
Rated Performance	– 25°C to + 85°C	*	– 55°C to + 125°C	*
Operating	– 40°C to + 100°C	*	– 55°C to + 125°C	*
CASE DIMENSIONS	2.64″ × 0.86″ × 0.35″	*	*	*

NOTES:

*Specifications same as AD293A

†883B MIL version to be available in January, 1982.

[1] Gain temperature drift is specified as a percentage of output signal level.

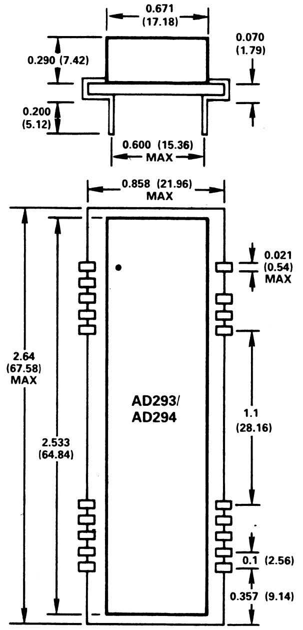
[2] Gain nonlinearity is specified as a percentage of 10V pk-pk output span.

[3] Recommended power supply, ADI Model 904, ± 15V @ 50mA output.

Specifications are subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



TOP VIEW

RECOMMENDED MATING SOCKET: AUGAT NO. 240-AG39D (TO PRESERVE THE HIGH CMV INTEGRITY OF THE AD293/AD294 REMOVE ALL UNUSED SOCKET PINS.)

PIN DESIGNATIONS

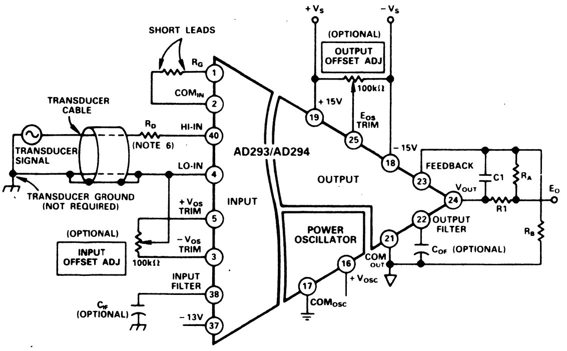
PIN	FUNCTION	PIN	FUNCTION
1	R_G	40	HI-IN
2	COM_{IN}		
3	$-V_{OS}$ TRIM	38	INPUT FILTER
4	LO-IN	37	– 13V
5	$+V_{OS}$ TRIM	36	NC
16	$+V_{OSC}$	25	E_{OS} TRIM
17	COM_{OSC}	24	V_{OUT}
18	– 15V	23	FEEDBACK
19	+ 15V	22	OUTPUT FILTER
20	SYNC	21	COM_{OUT}

Synchronization: Due to their hybrid transformer design and low power operation, RFI levels emitted by the AD293/AD294 are very low. A synchronization terminal is provided for use in high accuracy multi-channel applications. By connecting the synchronization terminals together and driving them with a TTL device, the AD293/AD294 internal oscillators will synchronize and "beat frequency" interference will be eliminated.

High Reliability: The AD293/AD294 are designed specifically to provide highly reliable operation in extremely harsh environments. These devices are available in hermetically sealed ceramic packages which use hybrid techniques and incorporate a revolutionary new hybrid magnetic transformer eliminating traditional wire wound methods. The AD293S/883B is manufactured and tested per MIL-STD-883B having a calculated MTBF of 1,682,369 hours.

INTERCONNECTIONS AND SHIELDING TECHNIQUE

To preserve the high CMR performance of the AD293/AD294, care must be taken to keep the capacitance balanced about the input terminals. Use twisted shielded cable, for the input signal, to reduce inductive and capacitive pickup. The cable shield should be connected to the common mode signal source and as close as possible to their respective terminal connections so pick-up can be minimized (shown in Figure 1).



NOTES:
1. GAIN RESISTORS R_G, R_A AND R_B, 1% 50ppm/°C METAL FILM TYPE.
2. INPUT GAIN $= 1 + \frac{100k}{R_G}$; $R_G \geq 1k$; MAX INPUT GAIN = 100V/V.

   $R_1 = 100\Omega$ AND $C_1 = 100pF$ (OPTIONAL); REQUIRED ONLY FOR CAPACITIVE LOADS $>1000pF$.
3. OUTPUT GAIN $= \frac{R_A \cdot R_B}{R_B}$; $1 \leq$ OUTPUT GAIN ≤ 10.
4. $C_{IF} = \frac{1}{2\pi F(97.5 \times 10^4)}$ FARADS.
5. $C_{OF} = \frac{1}{2\pi F(10^5)}$ FARADS.
6. R_D IS REQUIRED ONLY FOR THE AD294 TO PROVIDE PROTECTION AGAINST DEFIBRILLATOR PULSES. USE TWO 240kΩ 1/2 WATT RESISTORS. WHEN MOUNTING, PLACE THEM IN SERIES AND AWAY FROM THE PCB.

Figure 1. Basic Isolator Interconnection

THEORY OF OPERATION

The AD293/AD294 attribute their outstanding performance to the innovation of a hybrid magnetic ceramic transformer T1 (shown in the block diagram of Figure 2). Windings are screened on two ceramic alumina substrates which are placed together separated by a ceramic isolation barrier. Then an E-core is carefully fitted around the substrates to complete the transformer.

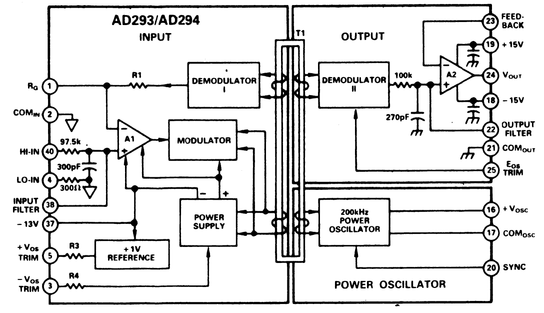


Figure 2. AD293/AD294 Block Diagram

Incorporating the carrier isolation technique, both power and signals are transferred between the amplifier's input stage and output circuitry via T1. The input signal is filtered and appears at the input of the inverting amplifier A1. This signal is then amplified by A1, with its gain (1V/V to 100V/V) determined by the value of resistance connected between R_G and COM_{IN}. The output of A1 is modulated, carried across the isolation barrier by signal transformer T1, and demodulated. The demodulator output voltage is filtered and then buffered by A2. Output gain (1V/V to 10V/V) and frequency compensation is determined by the value of resistance and capacitance selected between A2's feedback, V_{OUT}, and COM terminals. The 200kHz asymmetric square wave power oscillator drives the primary windings of transformer T1. The secondary windings of T1 then energizes the input power supply and drives both the modulator and demodulator.

INTERELECTRODE CAPACITANCE AND TERMINAL RATINGS

Capacitance: Interelectrode terminal capacitance effects are developed from stray capacitance that couple the input and output terminals together. The difference shown in Figure 3 between the AD293 and AD294 is a result of the separate transformer designs. Each terminal capacitance is shunted by leakage resistance exceeding $3.4 \times 10^9\Omega$.

Terminal Ratings: CMV performance is given in peak pulse and continuous ac or dc peak ratings. Continous peak ratings apply from dc up to the normal full power response frequencies. Figure 3 illustrates the AD293/AD294 ratings between terminals.

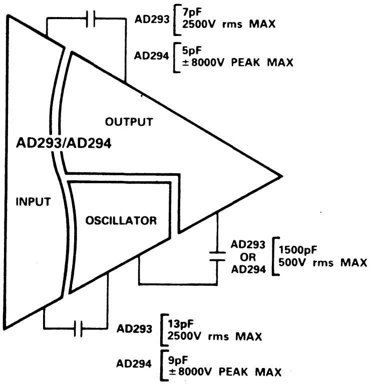

AD293 [7pF 2500V rms MAX
AD294 [5pF ±8000V PEAK MAX
OUTPUT
AD293/AD294
INPUT
OSCILLATOR
AD293 OR AD294 [1500pF 500V rms MAX
AD293 [13pF 2500V rms MAX
AD294 [9pF ±8000V PEAK MAX

Figure 3. Interelectrode Capacitance and Terminal Ratings

OFFSET AND GAIN TRIM PROCEDURES

The calibration procedure, shown in Figure 4, illustrates the recommended techniques which can be used to minimize output error. In this example, the output span is +10V to −10V and gain = 100V/V (G_{IN} = 10V/V; G_{OUT} = 10V/V).

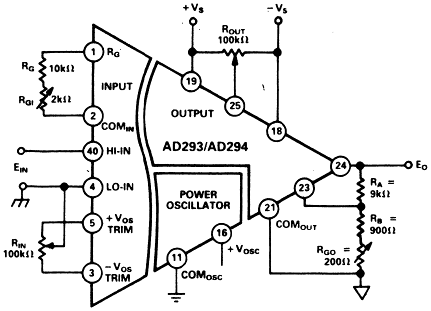


Figure 4. Recommended Offset & Gain Adjustments

Offset Adjustment

1. Set G_{OUT} = 1V/V by disconnecting R_B from COM.
2. Apply E_{IN} = 0 volts and adjust R_{IN} for E_O = 0 volts.
3. Connect R_B to COM.
4. Adjust R_{OUT} for E_O = 0 volts.

Gain Adjustment

5. Set G_{OUT} = 1V/V by disconnecting R_B from COM.
6. Apply E_{IN} = +1.000V and adjust R_G for E_O = +10.000V.
7. Connect R_B to COM.
8. Apply E_{IN} = +0.100V and adjust R_G for E_O = +10.000V.

LEAKAGE CURRENT LIMITS

The low coupling capacitance between input and output yields a ground leakage current of less than 2μA rms of 115V ac, 60Hz in the AD293/AD294 which meet standards established by UL STD 544.

For medical applications, the AD294 is designed to improve on patient safety current limits proposed by the F.D.A., U.L., A.A.M.I. and other regulatory agencies.

In patient monitoring equipment, such as ECG recorders, the AD294A will provide adequate isolation without exposing the patient to potentially lethal microshock hazards. With the use of passive components for input protection, this design limits input fault currents even under amplifier failure conditions.

PERFORMANCE CHARACTERISTICS

Phase vs. Frequency: The phase vs. frequency responses, for the AD293/AD294, is shown in Figure 5. The bandwidth is sufficient for the majority of isolation applications where accurate signal measurements must be made in the presence of noise and high common mode voltages.

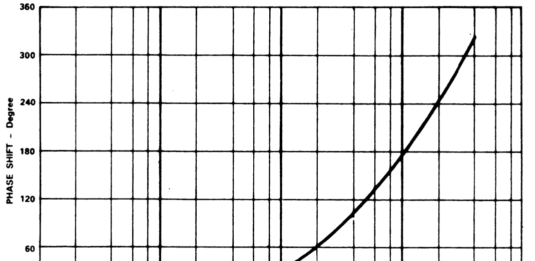


Figure 5. Typical AD293/AD294 – Phase vs. Frequency

Common Mode Rejection: Input-to-output CMR is dependent on source impedance imbalance, input signal frequency and amplifier gain. CMR is rated at 115V ac, 60Hz and 1kΩ (AD293)/5kΩ (AD294) source impedance imbalance at a gain of 1V/V. Figure 6 illustrates the CMR vs. frequency characteristics for the AD293/AD294. CMR approaches 144dB at dc with sources impedance as high as 1kΩ(AD293)/5kΩ (AD294).

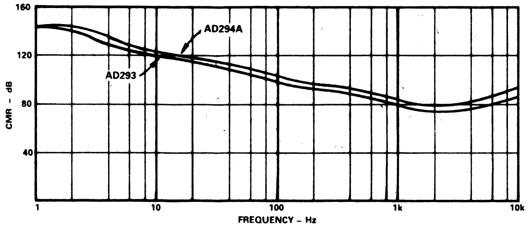


Figure 6. Typical AD293/AD294 – CMR vs. Frequency

Figure 7 illustrates the effect of source impedance imbalance on CMR performance at 60Hz for various gain settings. CMR is maintained greater than 60dB for source imbalances up to 100kΩ. As shown, increasing isolator gain increases CMR.

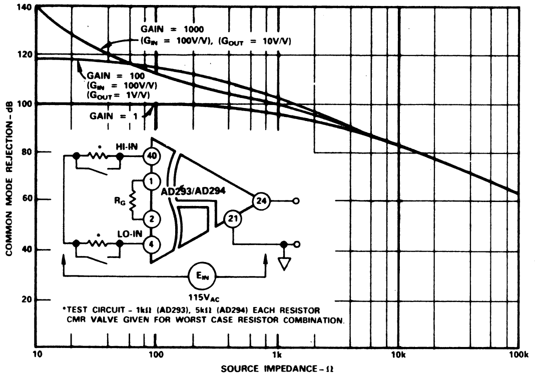


Figure 7. Typical AD293/AD294 – CMR vs. Source Impedance

Input Voltage Noise: Voltage noise, referred to input, is dependent on gain and bandwidth as illustrated in Figure 8. RMS voltage noise in a bandwidth from 0.05Hz to 100kHz is shown on the horizontal axis. The noise in a bandwidth from 0.05Hz to 100Hz is typically 5μV pk-pk at a gain of 1000V/V.

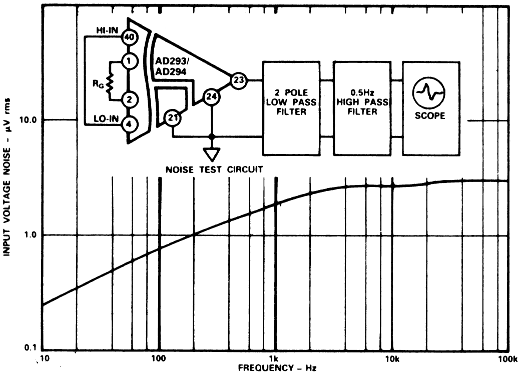


Figure 8. Typical AD293/AD294 – Input Noise vs. Frequency

The peak-to-peak value is derived by multiplying the rms value @ F = 100Hz ($0.75\mu V$ rms) by 6.6.

For applications requiring improved noise performance, additional low pass filters may be placed at either the input or output sections to selectively roll-off noise and undesired signals beyond the bandwidth of interest.

Gain Nonlinearity vs. Gain

Figure 9, shows the AD293/AD294 gain nonlinearity vs. gain as a function of output gain. As input gain is increased, gain nonlinearity increases. Although, as output gain is increased to ten, gain nonlinearity decreases.

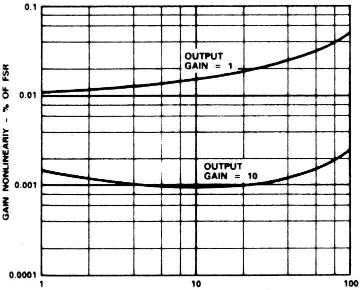


Figure 9. Typical AD293/AD294 – Gain Nonlinearity vs. Gain as a Function of Output Gain

Full Power Bandwidth vs. Gain

Figure 10 shows the –3dB full power bandwidth vs. gain with the input and output gain curves shown separately. As shown, the –3dB full power bandwidth with gain provided at the input is typically 330Hz. But with gain provided only at the output, the –3dB full power bandwidth approaches the small signal bandwidth.

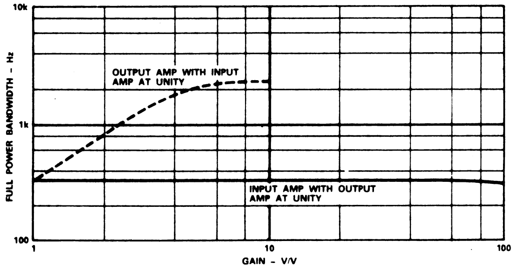


Figure 10. Typical AD293/AD294 - Full Power Bandwidth vs. Gain

Gain Nonlinearity vs. Output Swing

The gain nonlinearity vs. output swing, for the AD293/AD294, is illustrated in Figure 11. As shown, increasing either the input gain or the output swing will cause the gain nonlinearity to increase. Here the input gain is varied from 1V/V to 100V/V.

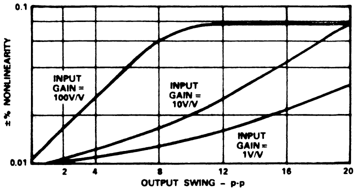


Figure 11. Typical AD293/AD294 - Gain Nonlinearity vs. Output Swing

OPTIMIZING THE AD293/AD294

The AD293/AD294 can be optimized for many applications as shown by the performance charts on the previous page. Gain and filtration can be implemented on both the input and output stages while providing true galvanic isolation. Provisions for an additional two poles of filtration are also available without the addition of external operational amplifiers. Due to their low power consumption and novel transformer design, the beat frequency problem normally associated with adjacent isolation amplifiers is eliminated. A sync terminal is provided for applications where ultra-sensitive circuitry might interpret the isolator carrier frequency.

SELECTING GAIN

The AD293/AD294 contain both input and output amplifiers (see Figures 1 and 2), the gains of which can be set independently. The selection of a particular combination tailors isolator properties to the application, minimizes errors, and optimizes frequency response.

Nonlinearity is the deviation of response from a straight line. This error arises from slight differences in responses of the input demodulator I and demodulator II, their respective transformer windings responses, and rectification of carrier signal in the input stage due to large signal amplitudes in this section. Hence, linearity is best obtained by raising output gain and lowering input gain.

Gain errors are deviations in slope from the predicted gain equation. Gain errors are attributable to the difference in gain between demodulators I and II. These errors are quite small, due to the highly predictable and uniform nature of the thick-film transformer. The gain drift of this portion of gain error is also small. Since this gain error source dominates at unity gain, the unity gain temperature coefficients of these units is very small. As input gain is taken, errors arise due to the inaccuracies of the internal feedback resistor R8, and user selected R_G. Failure of these resistors to temperature track introduces a gain TC. R8 is trimmed within ±2% and has a TC of ±100ppm/°C. Since the temperature coefficient of R8 is not user controllable, best gain TC at low gains is favored by taking output gain. The output stage also contributes gain error only when gain is taken. Here, both the feedback and gain resistors are user supplied and can be made as accurate as desired.

Offset errors are apparent both in the input stage and in the transformer-output stage combination. Provisions are available to eliminate these initial offset errors at both the input and output stages through trim potentiometers. These errors also have temperature dependence where at unity gain, output offset drift dominates. Taking output gain multiplies output drift by the gain taken. Taking input gain helps dilute output stage offset drift and is recommended where offset drift is to be minimized.

Errors due to small signal and large signal bandwidth limitations can also be optimized in the AD293/AD294. Small signal bandwidth is limited by lack of gain as frequency is raised, a condition caused by the necessity to limit bandwidth internally to preserve stability in the A1, modulator, input demodulator loop. The input stage contains most of the small signal bandwidth limitations thus, taking input gain limits small signal bandwidth (see Figure 10). The demodulators limit slew rate and large signal bandwidth. Apparent slew rate at the isolator output is multiplied by gain taken in the output stage. With maximum gain taken in the output stage, large signal bandwidth for moderate swings approaches small signal bandwidth (shown in Figure 10). Thus applying input gain, limits bandwidth while output gain enhances it.

FILTRATION

With the AD293/AD294, the addition of filtration can be implemented in a number of different configurations without the use of external operational amplifiers. Capacitors can be placed in series with the input or output terminals or configured in combination with the gain setting resistors to tailor performance. An input filter terminal and an output filter terminal are provided for user selectable filtration. Characteristics are determined by the formulas shown in Figure 1.

REDUCING NORMAL MODE VOLTAGE

A prime isolator function is the rejection of common mode signals. The extremely high input to output resistance of isolators allows excellent rejection of dc common mode voltages. As frequency rises, the small capacitance across the isolation barrier causes an ac common mode current to flow through that barrier, which is proportional to applied common mode voltage, frequency and barrier capacitance. Since the isolation mechanism (transformer T1) is more initimately connected to the input low terminal than the input high terminal, the bulk of common mode current flows through the input low terminal. Any resistance in series with the input source and the input low terminal then develops a normal mode voltage, which may constitute objectionable interference.

An isolator cannot separate normal mode interference from the desired signal without help, but interference can be rejected in several ways.

Conversion of common mode current to normal mode voltage can be reduced by minimizing resistance in the input low lead. In the AD293/AD294 CMR is enhanced and input trimming sacrificed by returning the input signal to pin 2. With known stable source resistances common mode current to normal mode voltage conversion can also be cancelled as shown in Figure 13.

ISOLATED INDUSTRIAL APPLICATIONS

As illustrated in Figure 14, the AD293 can be applied where differential signal sources are used such as an isolated strain gauge. With a third wire connected to the common mode potential of that source, a common mode current is forced to flow thorough the third wire and through the isolation barrier; thus, sparing the differential input wires the necessity of conducting the common mode current. In this manner, the isolator is responsive to only the differential inputs while ignoring the passage of common mode currents. Input gain is selected via R_G and determined by the input gain formula.

MEDICAL APPLICATIONS

In medical applications, a good connection to the patient, even on the third wire cannot be guaranteed due to electrode resistance to and through the skin. Illustrated in Figure 12 is a medical front end with right leg drive powered by the AD294A. Here the common mode drive amplifier helps force common mode current to flow in the third wire in preference to the differential input wires. The FET input has low noise current to avoid development of voltage noise in the input protection resistors. These resistors protect the input from defibrillator pulses with the AD294A having the capability of withstanding an 8kV pulse. The patient is also protected from fault currents due to input component failure. It is necessary to connect the third wire to establish the input common mode level. If not connected the input common mode level, with respect to common of the input section power supplies, will cause the isolator to drift out of its linear range. Layout is also very important, both for common mode rejection and isolation.

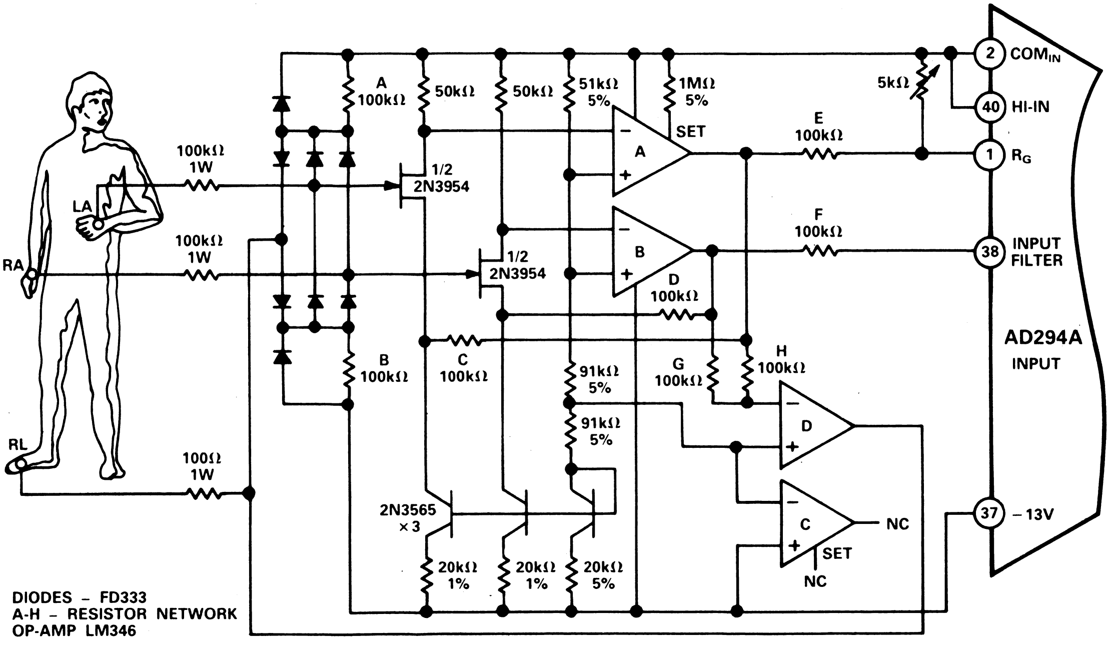


Figure 12. Multilead Medical Application Using the AD294A with Right Leg Drive

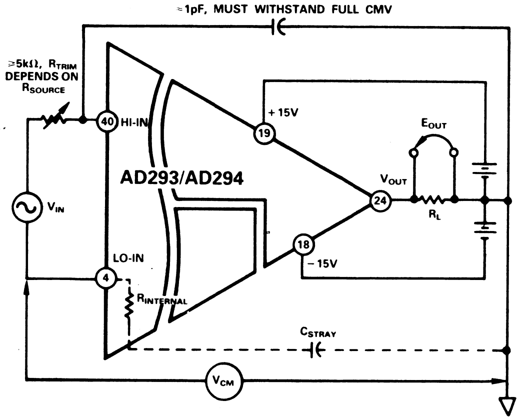
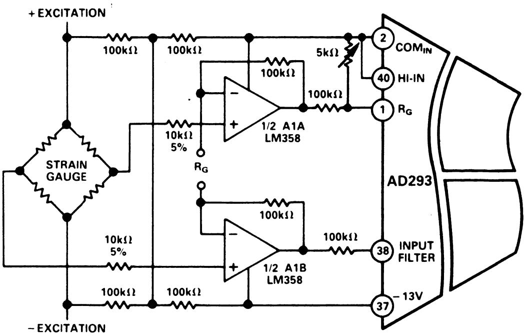


Figure 13. Improving CMR by Cancellation



ALL 100kΩ RESISTORS PART OF A RESISTOR NETWORK

Figure 14. Isolated Strain Gauge Using Front End of AD293

CURRENT LOOP INTERFACE

Illustrated in Figure 15, the AD293 provides an isolated sensor interface that is compatible with standard 4-to-20mA current loops. Here high common mode rejection and high common mode voltage suppression are easily attained with the AD293. The AD293 conditions the 0V to 10V input signal and provides a proportional voltage at the isolator's output. Then the circuitry shown converts it into a 4 to 20mA current, which in turn, may be applied to the loop load R_L.

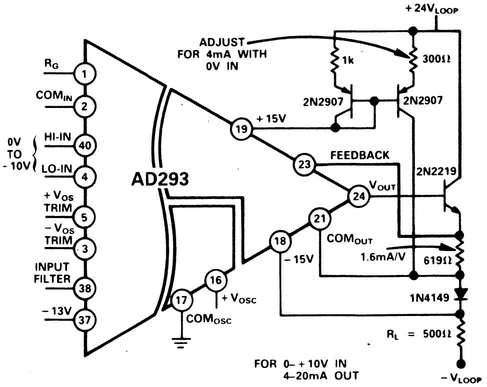


Figure 15. Isolated Current Loop Interface

TEMPERATURE MEASUREMENT AND COLD JUNCTION COMPENSATION

Illustrated in Figure 16, the AD293 can be used for isolated temperature measurements while providing cold junction compensation. With the circuitry connected as shown, the LM334 must be thermally connected to the cold junction terminal for an accurate temperature measurement to be made of this terminal. The 500Ω potentiometer will set the gain accuracy while the 100Ω potentiometer establishes offset trimming. Using this configuration, accurate temperature measurements of the industry's popular J type thermocouple can be made with the AD293 providing the added isolation feature. Gain and filtration can be addressed as required.

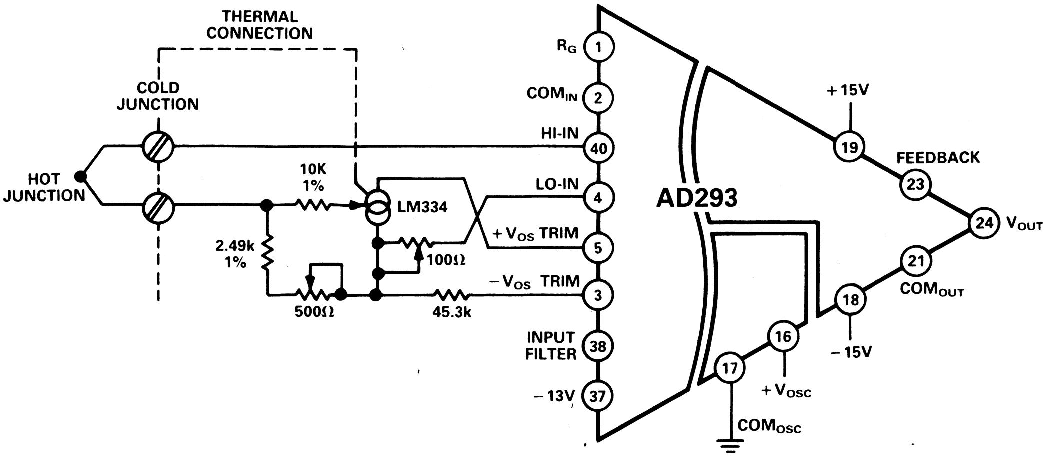


Figure 16. Temperature Measurement & Cold Junction Compensation

DRIVING CAPACITIVE LOADS

For driving capacitive loads greater than 1000pF, compensation should be implemented as shown in Figure 17. Here a 100pF capacitor and 100Ω resistor are used to insure that the AD293 output stage remains stable. These components can also be changed to tailor frequency response to the particular application. The 100Ω resistor isolates the output of the AD293 while the 100pF provides response lead.

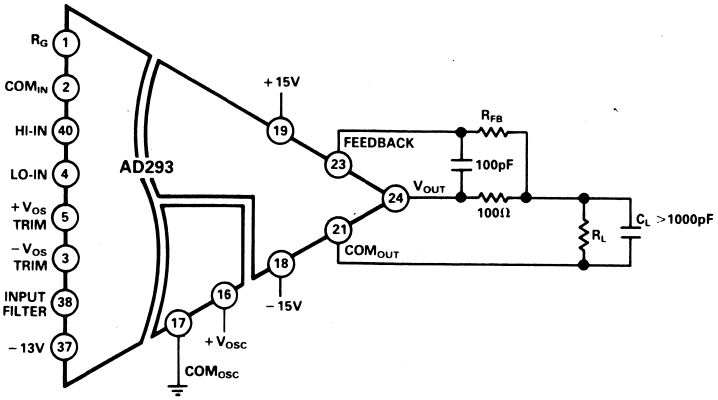


Figure 17. Driving Capacitive Loads

INCREASING OUTPUT DRIVE CAPABILITY

For applications requiring increased output drive, Figure 18 illustrates a single solution. Here the output voltage of the AD293 is conditioned and applied to the drive circuitry. R_A will supply the output stage with unity gain as connected. For gain to be added to the output stage, connect R_B as shown. Output gain will be determined by the output equation previously stated in the specifications. R_O and C_O should also be implemented so output stability will be insured. With this output drive circuitry, 200Ω loads can be easily driven with ±10V @ 50mA.

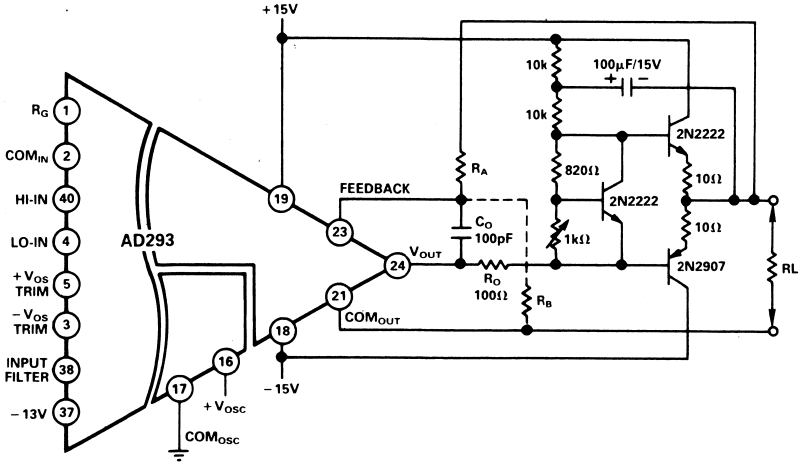


Figure 18. Increasing Output Drive Capability

ANALOG DEVICES

Precision, Wide Bandwidth, Synchronized Isolation Amplifier

MODEL 289

FEATURES

Low Nonlinearity: ±0.012% max (289L)
Frequency Response: (-3dB) dc to 20kHz
(Full Power) dc to 5kHz
Gain Adjustable 1 to 100V/V, Single Resistor
3-Port Isolation: ±2500V CMV Isolation Input/Output
Low Gain Drift: ±0.005%/°C max
Floating Power Output: ±15V @ ±5mA
120dB CMR at 60Hz: Fully Shielded Input Stage
Meets UL Std. 544 Leakage: 2μA rms max, @ 115V ac, 60Hz

APPLICATIONS

Multi-Channel Data Acquisition Systems
Current Shunt Measurements
Process Signal Isolator
High Voltage Instrumentation Amplifier
SCR Motor Control

GENERAL DESCRIPTION

Model 289 is a wideband, accurate, low cost isolation amplifier designed for instrumentation and industrial applications. Three accuracy selections are available offering guaranteed gain nonlinearity error at 10V p-p output: ±0.012% max (289L), ±0.025% max (289K), ±0.05% max (289J). All versions of the 289 provide a small signal frequency response from dc to 20kHz (-3dB) and a large signal response from dc to 5kHz (full power) at a gain of 1V/V. This new design offers true 3-port isolation, ±2500V dc between inputs and outputs (or power inputs), as well as 240V rms between power supply inputs and signal outputs. Using carrier modulation techniques with transformer isolation, model 289 interrupts ground loops and leakage paths and minimizes the effect of high voltage transients. It provides 120dB Common Mode Rejection between input and output common. The high CMV and CMR ratings of the model 289 facilitate accurate measurements in the presence of noisy electrical equipment such as motors and relays.

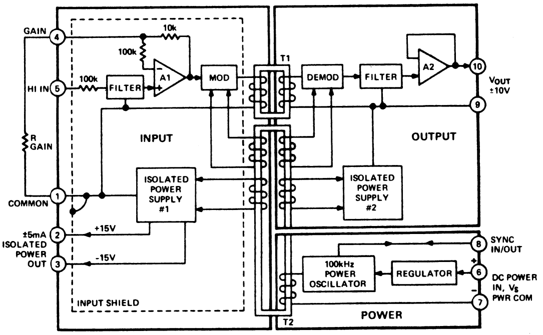
WHERE TO USE THE MODEL 289

The model 289 is designed to interface single and multichannel data acquisition systems with dc sensors such as thermocouples, strain gauges and other low level signals in harsh industrial environments. Providing high accuracy with complete galvanic isolation, and protection from line transients of fault voltages, model 289's performance is suitable for applications such as process controllers, current loop receivers, weighing systems, high CMV instrumentation and computer interface systems.

Use the model 289 when data must be acquired from floating transducers in computerized process control systems. The photograph above shows a typical multichannel application allowing potential differences or interrupting ground loops, among transducers, or between transducers and local ground.

This two-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be found in Volume II, page 5-23.

MODEL 289 FUNCTIONAL BLOCK DIAGRAM



DESIGN FEATURES AND USER BENEFITS

Isolated Power: The floating power supply section provides isolated ±15V outputs @ ±5mA. Isolated power is regulated to within ±5%. This feature permits model 289 to excite floating signal conditioners, front-end buffer amplifiers and remote transducers such as thermistors or bridges, eliminating the need for a separate isolated dc/dc converter.

Adjustable Gain: A single external resistor adjusts the model 289's gain from 1V/V to 100V/V for applications in high and low level transducer interfacing.

Synchronized: The model 289 provides a synchronization terminal for use in multichannel applications. Connecting the synchronization terminals of model 289s synchronizes their internal oscillators, thereby eliminating the problem of oscillator "beat frequency" interference that sometimes occurs when isolation amplifiers are closely mounted.

Internal Voltage Regulator: Improves power supply rejection and helps prevent carrier oscillator spikes from being broadcast via the isolator power terminal to the rest of the system.

Buffered Output: Prevents gain errors when an isolation amplifier is followed by a resistive load of low impedance. Model 289 can drive a 2kΩ load.

Three-Port Isolation: Provides true galvanic isolation between input, output and power supply ports. Eliminates need for power supply and output ports being returned through a common terminal.

Reliability: Model 289 is conservatively designed to be capable of reliable operation in harsh environments. Model 289 has a calculated MTBF of 271,835 hours. In addition, the model 289 meets UL Std. 544 leakage, 2μA rms @ 115V ac, 60Hz.

SPECIFICATIONS (typical @ +25°C and V_S = +14.4V to +25V dc unless otherwise noted)

Model	289J	289K	289L
GAIN (NONINVERTING)			
Range		1 to 100V/V	
Formula		$G = 1 + \frac{10k\Omega}{R_G (k\Omega)}$	
Deviation from Formula		±1.5% max	
vs. Temperature (0 to +70°C)[1]		15ppm/°C typ (50ppm/°C max)	
Nonlinearity, (±5V Swing)[2,3]	±0.05% max	±0.025% max	±0.012% max
INPUT VOLTAGE RATINGS			
Linear Differential Range (G = 1V/V)		±10V min	
Max Safe Differential Input			
Continuous		120V rms	
1 Minute		240V rms	
Max CMV (Inputs to Outputs)			
Continuous ac or dc		±2500V peak max	
ac, 60Hz, 1 Minute Duration		2500V rms	
CMR, Inputs to Outputs 60Hz			
$R_S \leqslant 1k\Omega$, Balanced Source Impedance		120dB	
$R_S \leqslant 1k\Omega$, HI IN Lead Only		104dB min	
Max Leakage Current, Input to Output @ 115V rms, 60Hz ac		2μA rms max	
INPUT IMPEDANCE			
Differential		$33pF \| 10^8 \Omega$	
Overload		100kΩ	
Common Mode		$20pF \| 5 \times 10^{10} \Omega$	
INPUT DIFFERENCE CURRENT			
Initial @ +25°C		10nA (75nA max)	
vs. Temperature (0 to 70°C)		0.15nA/°C	
INPUT NOISE (GAIN = 100V/V)			
Voltage			
0.05Hz to 100Hz		8μV p-p	
10Hz to 1kHz		3μV rms	
Current			
0.05Hz to 100Hz		3pA rms	
FREQUENCY RESPONSE			
Small Signal -3dB			
G = 1V/V		20kHz	
G = 100V/V		5kHz	
Full Power, 10V p-p Output			
G = 1V/V		5kHz	
G = 100V/V		3.5kHz	
Full Power, 20V p-p Output			
G = 1V/V		2.3kHz	
G = 100V/V		2.3kHz	
Slew Rate		0.14V/μs	
Settling Time[4] ±0.05%, ±10V Step		400μs	
OFFSET VOLTAGE, REFERRED TO INPUT			
Initial, @ +25°C		$\pm 5 \pm \frac{10}{G}$ mV max	
vs. Temperature (0 to +70°C)	$\pm 20 \pm \frac{200}{G}$ max	$\pm 15 \pm \frac{100}{G}$ max	$\pm 10 \pm \frac{50}{G}$ μV/°C max
vs. Supply Voltage (+15V to +20V change)		$\pm 2 \pm \frac{10}{G}$ μV/V	
RATED OUTPUT			
Voltage, 2kΩ Load		±10V min	
Output Impedance		<1Ω(dc to 100Hz)	
Output Ripple, 0.1MHz Bandwidth			
No Signal IN		5mV p-p	
$+10V_{IN}$		50mV p-p	
ISOLATED POWER SUPPLY			
Voltage		±15V dc	
Accuracy		±10%	
Current		±5mA, min	
Regulation No Load to Full Load		±5%	
Ripple, 0.1MHz Bandwidth, No Load		25mV p-p	
Full Load		75mV p-p	
POWER SUPPLY, SINGLE POLARITY[5]			
Voltage, Rated Performance		+14.4V to +25V	
Voltage, Operating		+8.5V to +25V	
Current, Quiescent (@ V_S = +15V)		+25mA	
TEMPERATURE RANGE			
Rated Performance		0 to +70°C	
Operating		-15°C to +75°C	
Storage		-55°C to +85°C	
CASE DIMENSIONS		1.5" X 2.0" X 0.75"	

NOTES:

[1] Gain temperature drift is specified as a percentage of output signal level.

[2] Gain nonlinearity is specified as a percentage of 10V pk-pk output span.

[3] When isolated power output is used, nonlinearity increases by ±0.002%/mA of current drawn.

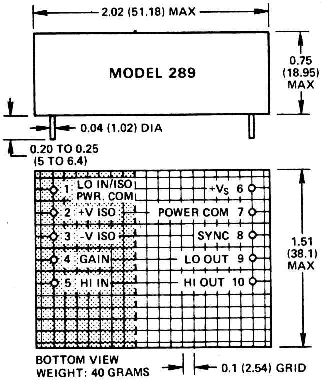
[4] G = 1V/V; with 2-pole, 5kHz output filter.

[5] Recommended power supply, ADI model 904, ±15V @ 50mA output.

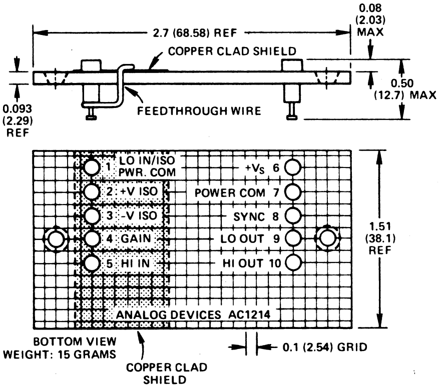
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



SHIELDED MATING SOCKET AC1214



INTERCONNECTIONS AND SHIELDING TECHNIQUE

To preserve the high CMR performance of model 289, care must be taken to keep the capacitance balanced about the input terminals. A shield should be provided on the printed circuit board under model 289 as illustrated in the outline drawing above (screened area). The LO IN/ISO PWR COM (pin 1) must be connected to this shield. This shield is provided with the mounting socket, model AC1214 (solder feedthrough wire to the socket pin 1 and copper foil surface). A recommended shielding technique using model AC1214 is illustrated in Figure 1.

Best CMR performance will be achieved by using twisted, shielded cable for the input signal to reduce inductive and capacitive pickup. To further reduce effective cable capacitance, the cable shield should be connected to the common mode signal source as close to signal low as possible.

Analog Computational Circuits

Contents

Page

Selection Guide 6-2
General Information and Definitions of Specifications 6-4
AD532J/K/S General-Purpose Internally Trimmed IC 4-Quadrant Multiplier/Divider 6-11
AD533J/K/L/S Lowest-Cost IC 4-Quadrant Multiplier/Divider 6-17
AD534J/K/L/S/T Highest-Performance Internally Trimmed IC 4-Quadrant Multiplier/Divider 6-21
AD535J/K High-Performance Internally Trimmed IC 2-Quadrant Divider 6-29
•AD539 Wideband Low-Distortion Dual-Channel Two-Quadrant Log/Linear Multiplier 6-35
429A/B Wideband 4-Quadrant Multiplier Module 6-37
433J/B Multifunction Device: $Y(Z/X)^m$ 6-39
755N/P 6-Decade, High Accuracy Log, Antilog Amplifiers 6-41
757N/P 6-Decade, High Accuracy Log, Antilog Amplifiers 6-43
759N/P Economy, Wideband Log/Antilog Amplifiers 6-41

•New product since *1980 Data-Acquisition Components and Subsystems Catalog*

Selection Guide
Analog Computational Circuits

In this Selection Guide, analog computational circuit products are partitioned into five categories:

1. General-purpose devices capable of optimization as multipliers or dividers
2. Internally trimmed devices optimized as multipliers
3. Internally trimmed devices optimized as dividers
4. Multifunction devices
5. Log/antilog amplifiers

Complete and detailed specifications, descriptions, and application information can be found in the data sheets. General information and definitions of important specifications can be found in the following pages.† Specifications are typical at rated supply voltage and load, and T_A = +25°C, unless noted otherwise.

1. GENERAL-PURPOSE EXTERNALLY TRIMMED DEVICES

Type	Characteristics	Vol I Page	Vol II Page
AD533J/K/L/S	Lowest cost general-purpose 4-quadrant multiplier, external trim to 0.5% max total error (L)	6–17	–

2. INTERNALLY TRIMMED MULTIPLIERS

Type	Characteristics	Vol I Page	Vol II Page
AD532J/K/S	General-purpose 4-quadrant multiplier, differential inputs, standard pinouts, internally trimmed to 1.0% max total error (K), 0.04%/°C max (S)	6–11	–
Model 429A/B	Wide-bandwidth 4-quadrant multiplier, full-power response to 2MHz min, slewing rate 120V/μs min, –3dB bandwidth 10MHz, small-signal, 1% settling-time 500ns; pretrimmed to 0.5% max error (B)	6–37	6–7
AD534J/K/L/S/T	High-accuracy internally trimmed 4-quadrant multiplier featuring 0.25% max total error (L), low noise (90μV rms, 10Hz – 10kHz), and versatile differential input configuration.	6–21	–
AD539J/S	Wideband low distortion dual-channel 2-quadrant log/linear multiplier, signal bandwidth 35MHz	6–35	–

3. INTERNALLY TRIMMED DIVIDERS

Type	Characteristics	Vol I Page	Vol II Page
Model 436A/B	High-accuracy 2-quadrant divider-only, pretrimmed to 0.25% max error (B, denominator [V_X] range from +0.1V to +10V [$\|V_Z\| \leqslant \|V_X\|$]), 2% max error over temperature (B), 1% max error 0 to +70°C.	–	6–15
AD535J/K#	2-quadrant divider, pretrimmed for 0.5% max total error (K version) for 10:1 denominator range. Differential inputs permit choice of denominator range. Differential inputs permit choice of denominator polarity.	6–29	–

4. MULTIFUNCTION DEVICES

Type	Characteristics	Vol I Page	Vol II Page
Model 433J/B	Programmable multifunction device, $Y(Z/X)^m$ (10V/E_{REF}), one quadrant, m adjustable from 0.2 to 5, max division error 25mV (B, V_Z from 0.01V to 10V, V_X from 0.1V to 10V, $V_Z \leqslant V_X$), 1% max over temperature.	6–39	6–11

†Letter suffixes denote temperature range and performance grade. J/K/L are specified for 0 to +70°C; A/B are specified for –25°C to +85°C; S/T are specified for –55°C to +125°C.

5. LOG/ANTILOG AMPLIFIERS

Type	Characteristics	Vol I Page	Vol II Page
Model 755N/P	High performance: ±1% max log-conformity error for 6 decades of current (1nA to 1mA) and 4 decades of voltage (1mV to 10V), and 0.5% max conformity error for 4 decades of current (10nA to 100μA) and 3 decades of voltage (1mV to 1V). Antilog output range: 4 decades, 1mV to 10V, K = 1, 2, 2/3 V/decade, I_{ref} = 10μA (externally adjustable).	6–41	8–7
Model 759N/P	Small size and low cost: 1.13″ X 1.13″ X 0.4″ module, wide bandwidth 200kHz @ 1μA, ±2% max log-conformity error for 5 decades of current (10nA to 1mA) or 4 decades of voltage (1.0mV to 10V), and ±1% max conformity error for 4 decades of current (20nA to 200μA). Log operating range: 6 decades of current (1nA to 1mA) and 4 decades of voltage (1mV to 10V). Antilog output range: 4 decades (1mV to 10V), K = 1, 2, 2/3 V/decade, I_{ref} = 10μA (externally adjustable).	6–41	8–7
Model 757N/P Log-ratio	Input dynamic range, 6 decades of current (1nA to 1mA), either channel, log conformity error ±1.0% max; for 4 decades (10nA to 100μA), log conformity error ±0.5% max. Log of voltage by using external resistors. K = 1 V/decade, ±1%, max, or externally programmable. Can be used for antilog operations.	6–43	8–11

Orientation
Analog Computational Circuits

The devices catalogued in this section accept analog voltages and multiply, divide, square, and/or square-root them, depending on device properties and connections.

Multiplication For two inputs, V_x and V_y, a multiplier will provide the output, $E_{out} = V_xV_y/E_{ref}$, where E_{ref} is a dimensional constant, usually of 10V nominal value. If E_{ref} = 10V, E_{out} = 10V when V_x and V_y are 10V. Multipliers are used for modulation and demodulation, fixed and variable remote gain adjustment, power measurement, and mathematical operations in analog computing, curve fitting, and linearizing.

If the inputs may be of either positive or negative polarity, and the output polarity is in a correct relationship for multiplication, the device is called a "four-quadrant" multiplier, reflecting the 4 quadrants of the X-Y plane.

Squaring If $V_x = V_y = V_{in}$, a multiplier's output will be V_{in}^2/E_{ref}. A four-quadrant multiplier, used as a squarer, will have an output that is positive, whether V_{in} is positive or negative. Squarers are useful in frequency doubling, power measurement of constant loads, and mathematical operations.

Division For a numerator input, V_z, and a denominator input, V_x, an analog divider will provide the output, $E_{out} = E_{ref}(V_z/V_x)$. If E_{ref} = 10V, E_{out} will be 10V or less for $V_z \leqslant V_x$. V_x is of a single polarity and will not provide meaningful results if it approaches zero too closely. If V_z may be of either positive or negative polarity, the device is described as a "two-quadrant" divider, and the output will reflect the polarity of V_z. Analog dividers are used to compute ratios—such as efficiency, attenuation, or gain; they are also used for fixed and variable remote gain adjustment, ratiometric measurements, and for mathematical operations in analog computing.

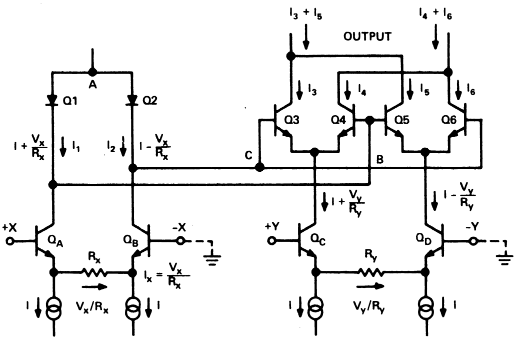
Square rooting For a numerator input, V_{in}, and a denominator input, E_o (the output fed back to the denominator input), the output of a divider is $E_o = E_{ref}(V_{in}/E_o)$; hence $E_o = \sqrt{E_{ref}V_{in}}$. A square-rooter works in one quadrant; some devices require external diode circuitry to prevent latchup if the input polarity changes, even momentarily. Square roots are used in vector and rms computation, to linearize flowmeters, and for mathematical operations in analog computing.

CHOOSING A MULTIPLIER, DIVIDER, etc.

A number of devices are listed here, differing in internal architecture, external functional configuration, device technology, and performance specifications. Some have essentially fixed references; others have an actively variable or programmable reference as a third input (*multifunction devices*), and one type (model 433) performs the one-quadrant operation, $E_o = V_z(V_y/V_x)^m$, where m is an exponent adjustable from 1/5 to 5. With one exception (model 436 precision 2-quadrant divider), all of the devices listed here can be used for any of the functions defined above.

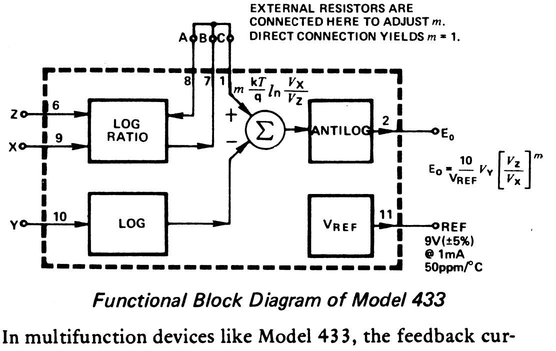
Considerable information on these functions, the nature of devices to perform them, and extensive discussions of their applications can be found in two publications available from Analog Devices.[1,2] A wealth of information is also to be found in the data sheets for the individual devices, published in this section. In addition to the products listed here, a number of popular earlier products are still available; data sheets are available upon request.

Internal Architecture All of the devices in this selection rely on the logarithmic properties of silicon P-N junctions. With the exception of models 433 and 436, the circuit employed is basically like that of the "Gilbert cell" (its 4-quadrant-multiplying circuitry and performance are described in (1) and (2), with further references to original sources). The input voltages are converted to currents, the currents are multiplied together and divided by a reference, and the net output current, I_xI_y/I_{ref}, is converted to voltage by feedback around the output amplifier. The feedback terminals are available as inputs for applications involving division. In the AD531[3], the I_{ref} terminals are available for external programming or variation; thus, the AD531 is a 3-variable "multifunction" IC which can divide without external feedback. This versatile feature offers greater bandwidth as a divider.



Basic 4-Quadrant Variable-Transconductance Multiplier Circuit

$$I_O = (I_3 + I_5) - (I_4 + I_6) = \frac{2\,V_X V_Y}{I\,R_X R_Y}$$



EXTERNAL RESISTORS ARE CONNECTED HERE TO ADJUST m. DIRECT CONNECTION YIELDS $m = 1$.
A
B
C
8
7
1
$m\frac{kT}{q}\ln\frac{V_X}{V_Z}$
Z
6
X
9
LOG RATIO
+
−
Σ
ANTILOG
2
E_o
$E_o = \frac{10}{V_{REF}} V_Y \left[\frac{V_Z}{V_X}\right]^m$
Y
10
LOG
V_{REF}
11
REF
9V(±5%)
@ 1mA
50ppm/°C

Functional Block Diagram of Model 433

In multifunction devices like Model 433, the feedback currents of the input op amps are used to develop logarithmic

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[1] *Multiplier Application Guide*, available upon request

[2] *Nonlinear Circuits Handbook*, D. H. Sheingold, ed., 1976, 536pp., $5.95, P.O. Box 796, Norwood MA 02062

[3] Data sheet available upon request.

voltages across transistor base-emitter junctions; these voltages are summed and differenced and produce an exponential current proportional to V_yV_z/V_x via another transistor junction in the input path of the output amplifier. Thus, the output voltage is proportional to V_yV_z/V_x; an internally generated reference voltage is available as a fixed reference for the odd input in two-variable operations. In the 433, the internal emitter-voltage difference proportional to log (V_z/V_x) can be amplified or attenuated by the appropriate connection of a resistive attenuator with an attenuation ratio, m; since the antilog of m(log V_z/V_x) is $(V_z/V_x)^m$, the output of the 433 is proportional to $V_y(V_z/V_x)^m$. In the model 436 divider, the inputs are scaled and linearly combined, before the log-antilog computation takes place; the result is that the numerator (of V_z/V_x) may have positive or negative values. The 436 circuit is optimized and trimmed for performance as a dedicated divider; it has a fixed reference. Its circuit principles are discussed in some detail on the data sheet.

External functional configuration As noted earlier, with the exception of the model 436 dedicated divider, all of the devices listed here can be used for multiplication, division, squaring, and/or square-rooting (MDSSR), by the appropriate connection of external jumpers. As an example, the AD534 is shown connected for multiplication, and the AD535, which has similar architecture but is optimized for division, is shown connected for division and square-rooting. Performance of pretrimmed devices is optimized in specified modes of operation, usually multiplication. The data sheets show how devices are connected for the various modes of operation; where appropriate, the trim circuits and procedures for optimizing performance are provided.

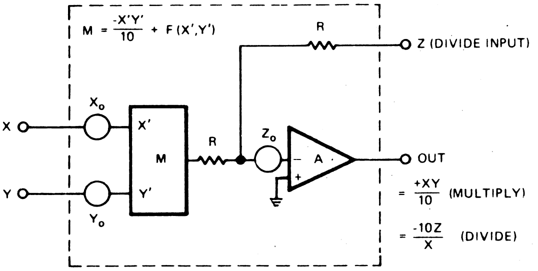
Some devices have differential inputs, which provide a great deal of flexibility. They permit polarity changes without external inversion, direct subtraction of inputs, insertion of bias voltages for additive constants, and direct multiplication of the results of differential measurements.

Technologies The devices described here are either monolithic integrated circuits or high-performance modules. For any application, the user will evaluate a device on the basis of its performance in the desired mode(s). The modules provide the highest performance: speed (model 429), accuracy as a divider (436), and accuracy in multifunction applications (433). On the other hand, the IC's provide economy of cost and space, and the availability of "mil-temp" range (−55°C to +125°C) versions. The pretrimmed IC's (AD534, AD535 and AD532) use laser trimming of thin-film-on-silicon chips at the wafer stage and buried-Zener reference circuitry, as well as thermally balanced input stages and "core" circuitry, for overall maximum errors to 0.25%, and linearities as yet unmatched in the industry.

Performance Multiplier performance, specifications and test circuitry are described in great detail in the NONLINEAR CIRCUITS HANDBOOK. Here is a brief digest of the factors relating to low-frequency performance.

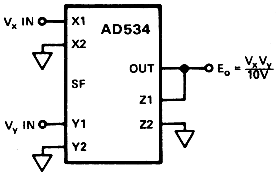
In theory, a multiplier has an output which is ideally the product of two input variables, X and Y, divided by the 10V scaling voltage. However, the practical multiplier is subject to various offset errors and nonlinearities, which must be accounted for in its application. This discussion is intended to assist the designer in understanding and interpreting multiplier and divider specifications and obtaining insight into device performance.

In practice (see the figure), the multiplier may be considered as having two parts, one (M) contains the input circuitry and the multiplying cell; the other is the gain-conditioning op amp, A.


M = $\frac{-X'Y'}{10}$ + F(X',Y')
R
Z (DIVIDE INPUT)
X_o
X
X'
M
R
Z_o
A
OUT
Y
Y'
Y_o
= $\frac{+XY}{10}$ (MULTIPLY)
= $\frac{-10Z}{X}$ (DIVIDE)

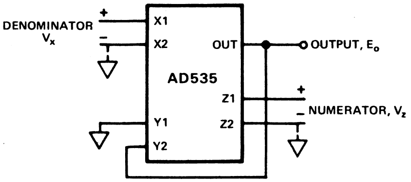
Functional Block Diagram of Typical Multiplier/Divider

Also summed at the op-amp input is the feedback variable, Z. In multiplication, Z is connected to the output circuit. In division, Z and X are the inputs, and Y is connected to the output. The figure shows a model used for considering errors. X_o and Y_o are input offset voltages, Z_o is the offset-referred-to-the-input of the output amplifier, and F(X', Y') is the nonlinearity, viewed as the departure from the ideal multiplication, $\frac{X'Y'}{10R}$. The output equation, including the errors is of the form



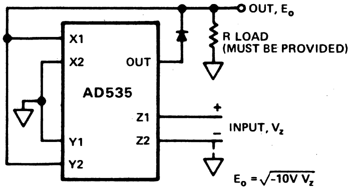
BASIC RELATIONSHIP: $(X_1 - X_2)(Y_1 - Y_2) = 10V(Z_1 - Z_2)$
$V_xV_y = 10V\ E_o$

Multiplier



$V_x(-E_o) = 10V\ V_z$ $E_o = -10\frac{V_z}{V_x}$

Divider



$E_o(-E_o) = 10V\ V_z$

Square Rooter

$$E_o = \underset{\text{Product}}{\frac{XY}{10B}} \pm \left[\underbrace{\underset{X_{\text{offset}}}{\frac{X_oY}{10B}} \pm \underset{Y_{\text{offset}}}{\frac{XY_o}{10B}}}_{\substack{\text{Linear}\quad\text{Feedthrough}\\ \text{``Y''}\qquad\quad\text{``X''}}} \pm \underset{\substack{\text{Output}\\ \text{offset}}}{Z_o} + \underset{\substack{\text{Nonlinearity}\\ \text{and feedthrough}}}{f(X,Y)} \right]$$

The errors are included in the bracketed term, except for gain error, which is the departure of "B", the gain-error term, from its nominal value of unity. The effects of input offsets (called "linear feedthrough") can be set to zero by applying external input biases, the output offset can be set to zero by biasing the output amplifier, and the gain can be externally calibrated by adjusting the reference or the feedback resistance. The remaining departure from the ideal output for any combination of input values is the irreducible *linearity error*, or *nonlinearity*, a function of X and Y that differs from device to device and, with temperature, within a given device. The component of nonlinearity for X = 0 is called "Y feedthrough" and for Y = 0, it is called "X feedthrough".

The "total error" specification includes the effects of all these errors. Although a guide to performance, it may produce an excessively conservative design in some applications. For example, output offset is not important if the output is to be capacitively coupled or the initial offset is nulled. Gain error is not important if system gain is to be adjusted elsewhere in the system or if gain is not a critical factor in system performance. If frequent calibration of offset and scale-factor errors is available (e.g., in a "smart" instrument, via software) nonlinearity becomes the limiting parameter. In such cases, improvements in predicted error can be achieved by using the approximate linearity equation:

$$f(X,Y) \cong |V_x|\,\epsilon_x + |V_y|\,\epsilon_y$$

were ϵ_x and ϵ_y are the specified fractional linearity errors (%/100) and V_x and V_y are the input signals.

When multipliers are fed back for use in division applications, it is important to recognize that maximum multiplication errors are increased approximately in proportion to the inverse of the denominator voltage ($10V/V_x$), and bandwidth is decreased in proportion to denominator voltage. Pretrimmed multipliers used in such applications, with wide dynamic range of X (e.g., 10:1), will always benefit greatly by the trimming of offsets, especially Z_o (affects offsets) and X_o (affects gain), for small values of X.

DEFINITIONS OF SPECIFICATIONS*

Accuracy is defined in terms of *total error* of the multiplier at room temperature and constant nominal supply voltage. *Total error* includes the sum of the effects of input and output dc offsets, nonlinearity, and feedthrough. *Temperature dependence* and *supply-voltage effects* are specified separately.

Scale Factor The *scale-factor error* (or *gain* error) is the difference between the average scale factor and the ideal scale factor (e.g., $(10V)^{-1}$). It is expressed in percent of the output signal. *Temperature dependence* is specified.

Output Offset refers to the offset voltage at the output-amplifier stage. This offset is usually minimized at manufacture and can be trimmed where high accuracy is desired. Output *offset vs. temperature* is also specified.

Linearity Error or *Nonlinearity* is the maximum difference between actual and "best-straight-line" theoretical output, for all pairs of input values, expressed as a percentage of full scale, with all other dc errors nulled. It is the irreducible minimum error. It is usually expressed in terms of X and Y nonlinearity, with the named input swinging over its full-scale range and the other input at (±) 10V. Y nonlinearity is considerably less than X nonlinearity in "Gilbert-cell" multipliers. This specification includes nonlinear feedthrough.

X or Y Feedthrough is the signal at the output for any value of X or Y input in the rated range, when the other input is zero. It has two components, a linear one, corresponding to an *input offset* at the zero input, which can be trimmed out (but can drift and has a *temperature specification*), and a nonlinear one, which is irreducible. *Feedthrough* is usually specified at one frequency (50Hz) for a 20V p-p sine wave input. It increases with frequency, and plots of typical feedthrough vs. frequency are provided on multiplier data sheets.

Noise is specified and measured with both inputs at zero signal and zero impedance (i.e., shorted). For low-frequency applications, filtering the output of the multiplier may improve small-signal resolution significantly.

Dynamic Parameters include: *small-signal bandwidth*, *full-power response*, *slew(ing) rate*, *small-signal amplitude error*, and *settling time*.

Small-signal bandwidth is the frequency at which the output is down 3dB from its low-frequency value (i.e., by about 30%) for a nominal output amplitude of 10% of full scale.

Full-power response is the maximum frequency at which the multiplier can produce full-scale voltage into its rated load without noticeable distortion.

Slew(ing) rate is the maximum rate of change of output voltage for the product of a full-scale dc voltage and a full-scale step input.

Small-signal amplitude error is defined in relation to the frequency at which the amplitude response, or scale factor, is in error by 1%, measured with a small (10% of full-scale) signal.

Settling time, for the product of a ±10V step and 10Vdc, is the total length of time the output takes to respond to an input change and stay within some specified error band of its final value. Settling time cannot be accurately predicted from any other dynamic specifications; it is specified in terms of a prescribed measurement.

Vector error is the most-sensitive measure of dynamic error. It is usually specified in terms of the frequency at which a phase error of 0.01 radians (0.57°) occurs.

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*These are general definitions. Further definitions are provided as footnotes to the specification tables; they should be read carefully.

LOGS AND LOG RATIOS

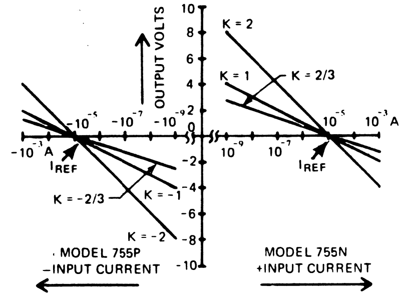
In the *logarithmic* mode, the ideal output equation is

$$E_o = -K \log_{10} \left(\frac{I_{in}}{I_{ref}}\right)$$

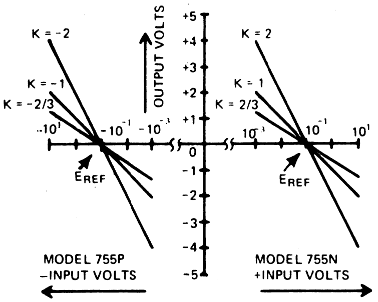
E_o can be positive or negative; it is zero when the ratio is unity, i.e., $I_{in} = I_{ref}$. K is the output scale constant; it is equal to the number of output volts corresponding to a decade* change of the ratio. In the 755 and 759 log amplifiers, K is pin-programmable to be either 1V, 2V, or 2/3V, or externally adjustable to any value $\geq$ 2/3V; in the model 757 log-ratio amplifier, K may be either a preset value of 1V, or an arbitrary value adjustable by an external resistance ratio.

I_{in} is a unipolar input current within a 6-decade range (1nA to 1mA); it may be applied directly, as a current, or derived from an input voltage via an input resistor (in which case, the ratio becomes $E_{in}/(R_{in}I_{ref}) = E_{in}/E_{ref}$. In models 755 and 759, the magnitude of I_{ref} is internally fixed at 10μA (E_{ref} = 0.1V) or externally adjusted; but model 757 is a *log-ratio* amplifier, in which both I_{in} and I_{ref} (or E_{in} and E_{ref}, using external scaling resistors) are input variables.

Each of the log amplifiers is available as a "P" or "N" option, depending on the polarity of the input voltage. Logarithms may be computed only for positive arguments, therefore the reference current must be of appropriate polarity to make the ratio positive. "N" indicates that the input current (or voltage) for the log mode is *positive;* "P" indicates that only *negative* voltage or current may be applied in the log mode. The polarity of K also differs: K is positive for "N" versions and negative for "P" versions. Thus, +10V applied to model 755N, with K = +1V, would produce an output voltage, E_o = -1V log (100) = -2V; on the other hand, -10V applied to model 755P, with K = 1V, would produce an output voltage, E_o = -(-1V) log (100) = +2V. The figure shows, in condensed form, the outputs of P and N log-amps, with differing K values, for voltage and current inputs.



Log of Current



Log of Voltage

Output vs. Input of Model 755N & 755P in Log Connection (Log Input Scales), Showing Voltages, and Polarity Relationships

Log amplifiers in the log mode are useful for applications requiring *compression* of wide-range analog input data, *linearization* of transducers having exponential outputs, and *analog computing*, ranging from simple translation of natural relationships in log form (e.g., computing absorbance as the log-ratio of input currents), to the use of logarithms in facilitating analog computation of terms involving arbitrary exponents and multi-term products and ratios.

ANTILOGS

In the *antilogarithmic* (exponential) mode, the ideal output equation is

$$E_o = E_{ref} \exp_{10} (-E_{in}/K)$$

E_{in} can be positive or negative; when it is zero, $E_o = E_{ref}$. However, E_o is always of single polarity, positive for "N" versions, negative for "P" versions. Thus, for 759P, connected for K = -2V, if E_{in} = +4V, and E_{ref} = -0.1V, then

$E_o = -0.1V \cdot 10^{-4/-2}$, or -10V; if E_{in} = -4V, then

$E_o = -0.1V \cdot 10^{-(-4)/-2}$ = -1mV. The figure on the next page shows, in condensed form, the outputs of P and N log amps, connected for antilogarithmic operation, with different K values.

Antilog amplifiers are useful for applications requiring *expansion* of compressed data, *linearization* of transducers having logarithmic outputs, *analog function fitting* or function generation, to obtain relationships or generate curves having voltage-programmable rates of growth or decay, and in *analog computing*, for such functions as compound multiplication and division of terms having differing exponents.

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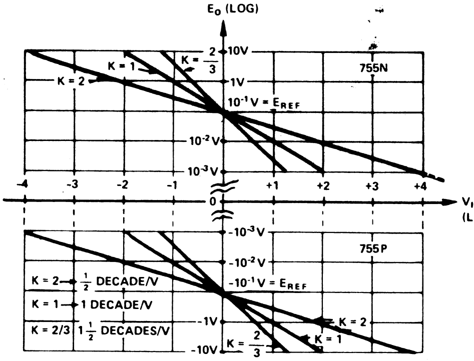
*A *decade* is a 10:1 ratio, two decades is 100:1, etc. For example, if K = 2, and the ratio is 10, the magnitude of the output would be 2V, and its polarity would depend on whether the ratio were greater or less than unity. If the input signal then changed by a factor of 1000 (3 decades), the output would change by 6V.

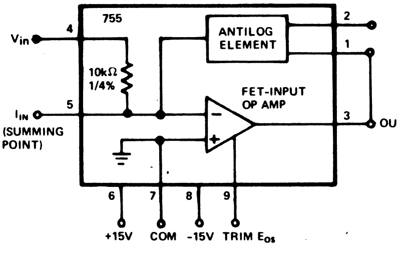


Antilog Operator Response Curves, Semilog Scale
$E_O = E_{REF}\,10^{V_{IN}/-K}$

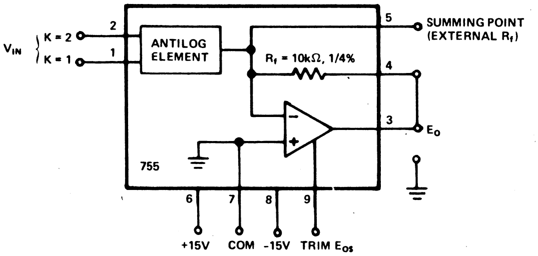
LOG-ANTILOG AMPLIFIER PERFORMANCE
Considerable information regarding log- and antilog-amplifier circuit design, performance, selection, and applications is to be found in the NONLINEAR CIRCUITS HANDBOOK[1]. Several salient points will be covered here, and specifications will be defined.

A log/antilog amplifier consists of an operational amplifier and an element with antilogarithmic transconductance (i.e., the voltage into the element produces a current that is an exponential function of the voltage). As the figure shows, for logarithmic operations, the input current is applied at the op-amp summing point, and the feedback circuit causes the amplifier output to produce whatever voltage is required to provide a feedback current that will exactly balance the input current.

In antilog operation, the input voltage is applied directly to the input of the antilog element, producing an exponential input current to the op-amp circuit. The feedback resistance transduces it to an output voltage.



a) Log/Antilog Amplifier Connected in the Log Mode (K = 1)



b) Log/Antilog Amplifier Connected in the Exponential Mode

The wide range of log/exponential behavior is made possible by the exponential current-voltage relationship of transistor base-emitter junctions,

$$I = I_0(\epsilon^{qV/kT} - 1) \cong I_0\epsilon^{qV/kT}$$

and $V = (kT/q)\ln(I/I_0)$

where I is the collector current, I_0 is the extrapolated current for V = 0, V is the base-emitter voltage, q/k (11605° K/V) is the ratio of charge of an electron to Boltzmann's constant, and T is junction temperature kelvin. In log/antilog devices, two matched transistors are connected so as to subtract the junction voltages associated with the input and reference currents, making the ratio independent of I_0's variation with temperature.

$$\begin{aligned}\Delta V &= (kT/q)\ln(I_{in}/I_0) - (kT/q)\ln(I_{ref}/I_0)\\ &= (kT/q)(\ln I_{in} - \ln I_{ref}) + (kT/q)(\ln I_0 - \ln I_0)\\ &= (kT/q)\ln(I_{in}/I_{ref})\end{aligned}$$

The temperature-dependence of gain is compensated for by a resistive attenuator that uses a temperature-sensitive resistor for compensation. The attenuator also produces amplification of K to the specified nominal values, e.g., from the basic 59mV/decade (kT/q) ln10 at room temperature) to 1V/decade.

Errors are introduced by the offset current of the amplifier, and the offset voltage, for voltage inputs; by inaccuracy of the reference current (or the effective reference voltage, for voltage inputs) in fixed-reference devices; and by inaccuracy of setting K. Additional errors are introduced by drift of these parameters with temperature. At any temperature, if these parameters are nulled out, there remains a final irreducible difference between the actual output and the theoretical output, called *log-conformity error*, which is manifested as a "nonlinearity" of the input-output plot on semilog paper. Best log conformity is realized away from the extremities of the rated signal range. For example, log-conformity error of model 755 is ±1% maximum, referred to the input, over the entire 6-decade range from 1nA to 1mA; but it is only ±0.5% maximum over the 4-decade range from 10nA to 100μA.

Errors occurring at the input, and log-conformity errors, can only be observed at the output, but it is useful to refer them to the input (RTI). Equal percentage errors at the input, at whatever input level, produce equal incremental errors at the output, for a given value of K. For example, if $K = 1$, and the RTI log-conformity error is +1%, the magnitude of the output error will be

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[1] *Nonlinear Circuits Handbook*, Analog Devices, Inc., 1974, 1976, 536pp, edited by D. H. Sheingold, $5.95; send check or complete MasterCard data to P.O. Box 796, Norwood MA 02062

$$\begin{aligned}\text{Error} &= \text{Actual output} - \text{ideal output}\\ &= 1\text{V}\cdot\log(1.01\ I/I_{ref}) - 1\text{V}\cdot\log(I/I_{ref})\\ &= 1\text{V}\cdot\log 1.01 = 0.0043\text{V} = 4.3\text{mV}\end{aligned}$$

If, in this example, the input range happens to be 5 decades, the corresponding output range will be 5 volts, and the 4.3mV log-conformity error, as a percentage of total *output* range, will be less than 0.1%. Because this ambiguity can prove confusing to the user, it is important that a manufacturer specify whether the error is referred to the input or the output. The table below indicates the conversion between RTI percentage and output error-magnitudes, for various percent errors, and various values of K.

LOG OUTPUT ERROR (mV)

% ERROR RTI	K = 1V	K = 2V	K = (2/3)V
0.1	0.43	0.86	0.28
0.5	2.2	4.3	1.4
1.0	4.3	8.6	2.9
2.0	8.6	17.	5.7
3.0	13.	26.	8.6
4.0	17.	34.	11.
5.0	21.	42.	14.
10.0	41.	83.	28.

For antilog operations, input and output errors are interchanged.

To arrive at the total error, an error budget should be made up, taking into account each of the error sources, and its contribution to the total error, over the temperature range of interest.

Dynamic response of log amps is a function of the input level. Small-signal bandwidths of ac input signals biased at currents above 1µA tend to be roughly comparable. However, below 1µA, bandwidth tends to be in rough proportion to current level. Similarly, rise time depends on step magnitude and direction – step changes in the direction of increasing current are responded to more quickly than step decreases of current.

DEFINITIONS OF SPECIFICATIONS

Log-Conformity Error When the parameters have been adjusted to compensate for offset, scale-factor, and reference errors, the *log-conformity error* is the deviation of the resulting function from a straight line on a semilog plot over the range of interest.

Offset Current (I_{os}) is the bias current of the amplifier, plus any stray leakage currents. This parameter can be a significant source of error when processing signals in the nanoampere region. Its contribution in antilog operation is negligible.

Offset Voltage (E_{os}) depends on the operational amplifier used for the log operation. Its effect is that of a small voltage in series with the input resistor. For current-logging operations, with high-impedance sources, its error contribution is negligible. However, for voltage logging, it modifies the value of V_{in}. Though it can be adjusted to zero at room temperature, its drift over the temperature range should be considered. In antilog operation, E_{os} appears at the output as an essentially constant voltage; its percentage effect on error is greatest for small outputs.

Reference Current (I_{ref}) is the effective internally-generated current-source output to which all values of input current are compared. I_{ref} tolerance appears as a dc offset at the output; it can be adjusted towards zero by adjusting the reference current, adding a voltage to the output by injecting a current into the scale-factor attenuator, or simply by adding a constant bias at the output's destination.

Reference Voltage (E_{ref}) is the effective internally generated voltage to which all input voltages are compared. It is related to I_{ref} by the equation: $E_{ref} = I_{ref}R_{in}$, where R_{in} is the value of input resistance. Typically, I_{ref} is less stable than R_{in}; therefore, practically all the tolerance is due to I_{ref}.

Scale Factor (K) is the voltage change at the output for a decade (i.e., 10:1) change at the input, when connected in the log mode. Error in scale factor is equivalent to a change in gain, or slope (on a semilog plot), and is specified in percent of the nominal value.

ANALOG DEVICES

Internally Trimmed Integrated Circuit Multiplier

AD532

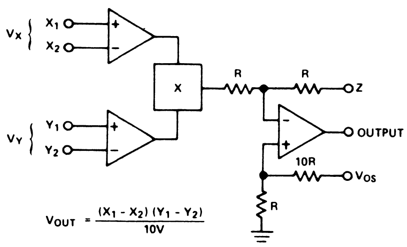
FEATURES

Pretrimmed To ±1.0% (AD532K)
No External Components Required
Guaranteed ±1.0% max 4-Quadrant Error (AD532K)
Diff Inputs For $(X_1-X_2)(Y_1-Y_2)/10V$ Transfer Function
Monolithic Construction, Low Cost

APPLICATIONS

Multiplication, Division, Squaring, Square Rooting
Algebraic Computation
Power Measurements
Instrumentation Applications

AD532 FUNCTIONAL BLOCK DIAGRAM



$$V_{OUT} = \frac{(X_1-X_2)(Y_1-Y_2)}{10V}$$

(WITH Z TIED TO OUTPUT)

PRODUCT DESCRIPTION

The AD532 is the first pretrimmed single chip monolithic multiplier/divider. It guarantees a maximum multiplying error of ±1.0% and a ±10V output voltage without the need for any external trimming resistors or output op amp. Because the AD532 is internally trimmed, its simplicity of use provides design engineers with an attractive alternative to modular multipliers, and its monolithic construction provides significant advantages in size, reliability and economy. Further, the AD532 can be used as a direct replacement for other IC multipliers that require external trim networks (such as the AD530).

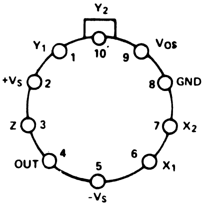
FLEXIBILITY OF OPERATION

The AD532 multiplies in four quadrants with a transfer function of $(X_1-X_2)(Y_1-Y_2)/10V$, divides in two quadrants with a $10VZ/(X_1-X_2)$ transfer function, and square roots in one quadrant with a transfer function of $\pm\sqrt{10VZ}$. In addition to these basic functions, the differential X and Y inputs provide significant operating flexibility both for algebraic computation and transducer instrumentation applications. Transfer functions, such as $XY/10V$, $(X^2-Y^2)/10V$, $\pm X^2/10V$, and $10VZ/(X_1-X_2)$ are easily attained, and are extremely useful in many modulation and function generation applications, as well as in trigonometric calculations for airborne navigation and guidance applications, where the monolithic construction and small size of the AD532 offer considerable system advantages. In addition, the high CMRR (75dB) of the differential inputs makes the AD532 especially well qualified for instrumentation applications, as it can provide an output signal that is the product of two transducer-generated input signals.

GUARANTEED PERFORMANCE OVER TEMPERATURE

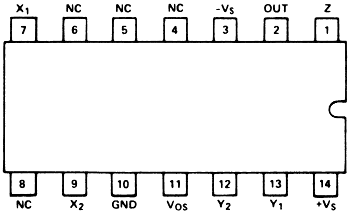
The AD532J and AD532K are specified for maximum multiplying errors of ±2% and ±1% of full scale, respectively at +25°C, and are rated for operation from 0 to +70°C. The AD532S has a maximum multiplying error of ±1% of full scale at +25°C; it is also 100% tested to guarantee a maximum error of ±4% at the extended operating temperature limits of -55°C and +125°C. All devices are available in either the hermetically-sealed TO-100 metal can or TO-116 ceramic DIP.

AD532H



TO-100
TOP VIEW

AD532D



TO-116
TOP VIEW

SPECIFICATIONS (typical @ +25°C with V_S = ±15V dc, V_{OS} grounded, unless otherwise specified)

PARAMETER	CONDITIONS	AD532J	AD532K	AD532S
ABSOLUTE MAX RATINGS				
Supply Voltage		±18V	*	±22V
Internal Power Dissipation		500mW	*	*
Input Voltage[1]				
X, Y, V_{os}, Z		$\pm V_S$	*	*
Rated Operating Temp Range		0 to +70°C	*	−55°C to +125°C
Storage Temp Range		−65°C to +150°C	*	*
Lead Temperature	60 Sec Soldering	+300°C	*	*
Output Short Circuit	To Ground	Indefinite	*	*
MULTIPLIER SPECIFICATIONS				
Transfer Function		$(X_1-X_2)(Y_1-Y_2)/10V$	*	*
Total Error (% F.S.)	V_X = 0/±10V, V_Y = 0/±10V	±2%max [±1.5% typ]	±1.0% max [±0.7% typ]	±1.0% max [±0.5% typ]
	T_A = min to max	±2.5%	±1.5%	±4.0% max
vs. Temperature	T_A = min to max	±0.04%/°C	±0.03%/°C	±0.04%/°C max [±0.01%/°C typ]
Nonlinearity				
X Input	V_X = 20V(p-p), V_Y = ±10V	±0.8%	±0.5%	**
Y Input	V_Y = 20V(p-p), V_X = ±10V	±0.3%	±0.2%	**
Feedthrough				
X Input	V_X = 20V(p-p), V_Y = 0, f = 50Hz	200mV(p-p) max [50mV(p-p) typ]	100mV(p-p) max [30mV(p-p) typ]	**
Y Input	V_Y = 20V(p-p), V_X = 0, f = 50Hz	150mV(p-p) max [30mV(p-p) typ]	80mV(p-p) max [25mV(p-p) typ]	**
vs. Temperature	T_A = min to max	2.0mV(p-p)/°C	1.0mV(p-p)/°C	**
DIVIDER SPECIFICATIONS				
Transfer Function		$10VZ/(X_1-X_2)$	*	*
Total Error[2]	$V_X = -10V$, V_Z = ±10V	±2%	±1%	**
	$V_X = -1V$, V_Z = ±10V	±4%	±3%	**
SQUARER SPECIFICATIONS				
Transfer Function		$(X_1-X_2)^2/10V$	*	*
Total Error		±0.8%	±0.4%	**
SQUARE ROOTER SPECIFICATIONS				
Transfer Function		$-\sqrt{10VZ}$	*	*
Total Error[2]	V_Z = 0/+10V	±1.5%	±1.0%	**
INPUT SPECIFICATIONS				
Input Resistance				
X, Y Inputs		10MΩ	*	*
Z Input		36kΩ	*	*
Input Bias Current				
X, Y Inputs		3μA	4μA max [1.5μA typ]	**
Z Input		±10μA	±15μA max [±5μA typ]	**
X, Y Inputs	T_A = min to max	10μA	8μA	**
Z Input	T_A = min to max	±30μA	±25μA	**
Input Offset Current				
X, Y Inputs		±0.3μA	±0.1μA	**
Input Voltage Diff/CM	T_A = min to max			
X, Y, Z Inputs	For Rated Accuracy	±10V	*	*
CMRR (X or Y Inputs)	X or Y = ±10V	40dB min	50dB min	**
DYNAMIC SPECIFICATIONS				
Small Signal, Unity Gain		1.0MHz	*	*
Full Power Bandwidth		750kHz	*	*
Slew Rate		45V/μs	*	*
Small Signal Amplitude Error		1% at 75kHz	*	*
Small Signal 1% Vector Error	0.5° phase shift	5kHz	*	*
Settling Time	±10V step	1μs to 2%	*	*
Overload Recovery		2μs to 2%	*	*
OUTPUT AMPLIFIER SPECIFICATIONS				
Output Impedance	Closed Loop	1Ω	*	*
Output Voltage Swing	T_A = min to max			
	$R_L \geqslant 2k\Omega$, $C_L \leqslant 1000pF$	±10V min [±13V typ]	*	*
Output Noise	f = 5Hz to 10kHz	0.6mV(rms)	*	*
	f = 5Hz to 5MHz	3.0mV(rms)	*	*
Output Offset Voltage				
Initial Offset	Trimmable To Zero	±40mV	±30mV max	**
vs. Temperature	T_A = min to max	0.7mV/°C	*	2.0mV/°C max
POWER SUPPLY SPECIFICATIONS				
Supply Voltage	Rated Performance	±15V	*	*
	Operating	±10V to ±18V	*	±10V to ±22V
Supply Current	Quiescent	±6mA max [±4mA typ]	*	*
Power Supply Variation				
Multiplier Accuracy		±0.05%/%	*	*
Output Offset		±2.5mV/%	*	*
Scale Factor		−0.03%/%	*	*
Feedthrough		±0.25mV/%	*	*

NOTES:
[1] Max input voltage is zero when supplies are turned off.
[2] With recommended external trim (see Applications).
*Specifications same as AD532J.
**Specifications same as AD532K.
Specifications subject to change without notice.

FUNCTIONAL DESCRIPTION

The functional block diagram for the AD532 is shown on the first page, and the complete schematic in Figure. 1. In the multiplying and squaring modes, Z is connected to the output to close the feedback around the output op amp. (In the divide mode, it is used as an input terminal.)

The X and Y inputs are fed to high impedance differential amplifiers featuring low distortion and good common mode rejection. The amplifier voltage offsets are actively laser trimmed to zero during production. The product of the two inputs is resolved in the multiplier cell using Gilbert's linearized transconductance technique. The cell is laser trimmed to obtain $V_{out} = (X_1 - X_2)(Y_1 - Y_2)/10$ volts. The built-in op amp is used to obtain low output impedance and make possible self-contained operation. The residual output voltage offset can be zeroed at V_{os} in critical applications . . . . otherwise the V_{os} pin should be grounded.

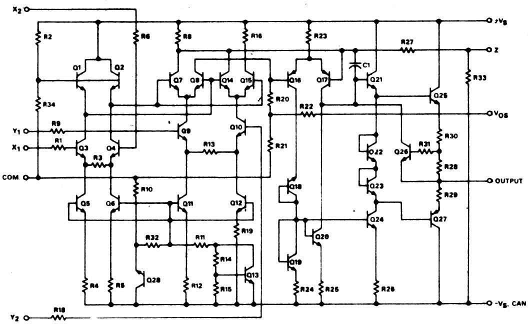


Figure 1. AD532 Schematic Diagram

ORDERING GUIDE

Model	Package Option[1]	Max Mult Error	Temperature Range
AD532JH	TO–100	±2.0%	0 to +70°C
AD532JD	TO–116 Style (D14A)	±2.0%	0 to +70°C
AD532KH	TO–100	±1.0%	0 to +70°C
AD532KD	TO–116 Style (D14A)	±1.0%	0 to +70°C
AD532SH	TO–100	±1.0%	-55°C to +125°C
AD532SD	TO–116 Style (D14A)	±1.0%	-55°C to +125°C

[1] See Section 20 for package outline information.

AD532 PERFORMANCE CHARACTERISTICS

Multiplication accuracy is defined in terms of total error at +25°C with the rated power supply. The value specified is in percent of full scale and includes X_{in} and Y_{in} nonlinearities, feedback and scale factor error. To this must be added such application-dependent error terms as power supply rejection, common mode rejection and temperature coefficients (although worst case error over temperature is specified for the AD532S). Total expected error is the rms sum of the individual components, since they are uncorrelated.

Accuracy in the divide mode is only a little more complex. To achieve division, the multiplier cell must be connected in the feedback of the output amp as shown in Figure 12. In this configuration, the multiplier cell varies the closed loop gain of the op amp in an inverse relationship to the denominator voltage. Thus, as the denominator is reduced, output offset, bandwdith and other multiplier cell errors are adversely affected. The divide error and drift are then $\epsilon_m \cdot 10V/X_1-X_2)$ where ϵ_m represents multiplier full scale error and drift, and (X_1-X_2) is the absolute value of the denominator.

NONLINEARITY

Nonlinearity is easily measured in percent harmonic distortion. The curves of Figures 2 and 3 characterize output distortion as a function of input signal level and frequency respectively, with one input held at plus or minus 10V dc. In Figure 3 the sine wave amplitude is 20V (p-p).

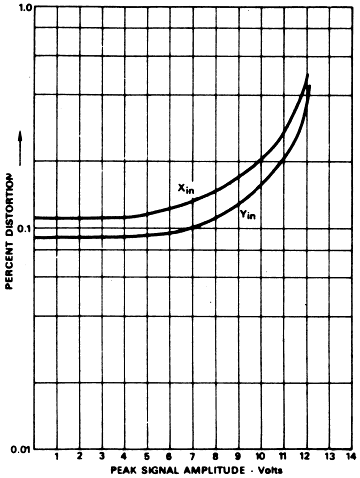


Figure 2. Percent Distortion vs. Input Signal

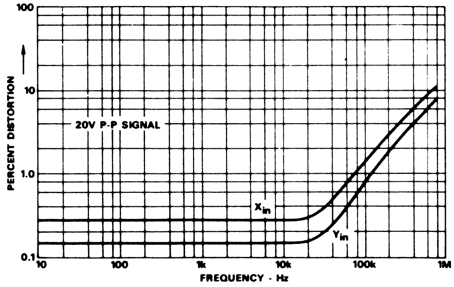


Figure 3. Percent Distortion vs. Frequency

AC FEEDTHROUGH

AC Feedthrough is a measure of the multiplier's zero suppression. With one input at zero, the multiplier output should be zero regardless of the signal applied to the other input. Feedthrough as a function of frequency for the AD532 is shown in Figure 4. It is measured for the condition $V_X = 0$, $V_Y = 20V(p\text{-}p)$ and $V_Y = 0$, $V_X = 20V(p\text{-}p)$ over the given frequency range. It consists primarily of the second harmonic and is measured in millivolts peak-to-peak.

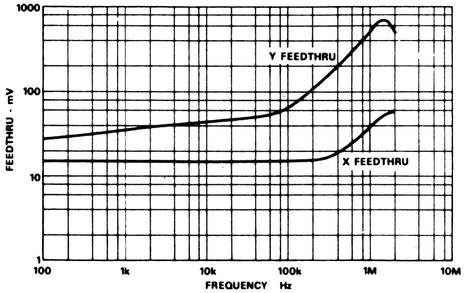


Figure 4. Feedthrough vs. Frequency

COMMON MODE REJECTION

The AD532 features differential X and Y inputs to enhance its flexibility as a computational multiplier/divider. Common mode rejection for both inputs as a function of frequency is shown in Figure 5. It is measured with $X_1 = X_2 = 20V\ (p\text{-}p)$, $(Y_1-Y_2) = \pm 10V$ dc and $Y_1 = Y_2 = 20V(p\text{-}p)$, $(X_1-X_2) = \pm 10V$ dc.

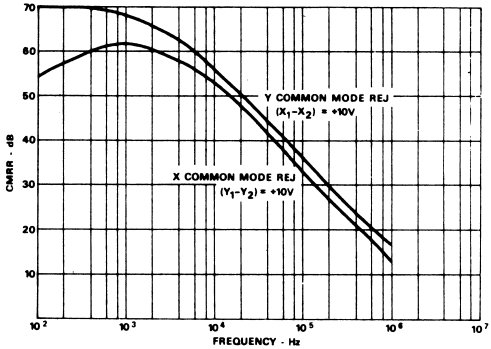


Figure 5. CMRR vs. Frequency

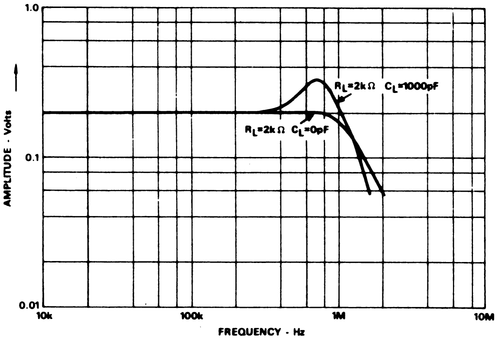


Figure 6. Frequency Response, Multiplying

DYNAMIC CHARACTERISTICS

The closed loop frequency response of the AD532 in the multiplier mode typically exhibits a 3dB bandwidth of 1MHz and rolls off at 6dB/octave thereafter. Response through all inputs is essentially the same as shown in Figure 6. In the divide mode, the closed loop frequency response is a function of the absolute value of the denominator voltage as shown in Figure 7.

Stable operation is maintained with capacitive loads to 1000pF in all modes, except the square root for which 50pF is a safe upper limit. Higher capacitive loads can be driven if a 100Ω resistor is connected in series with the output for isolation.

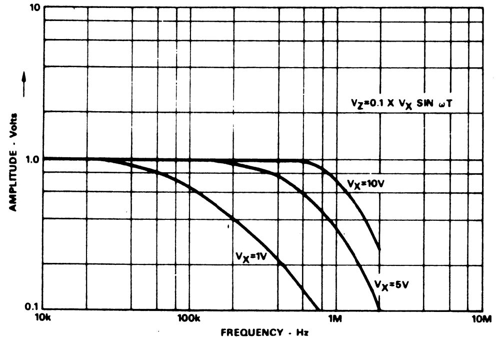


Figure 7. Frequency Response, Dividing

POWER SUPPLY CONSIDERATIONS

Although the AD532 is tested and specified with ±15V dc supplies, it may be operated at any supply voltage from ±10V to ±18V for the J and K versions and ±10V to ±22V for the S version. The input and output signals must be reduced proportionately to prevent saturation, however, with supply voltages below ±15V, as shown in Figure 8. Since power supply sensitivity is not dependent on external null networks as in the AD530 and other conventionally nulled multipliers, the power supply rejection ratios are improved from 3 to 40 times in the AD532.

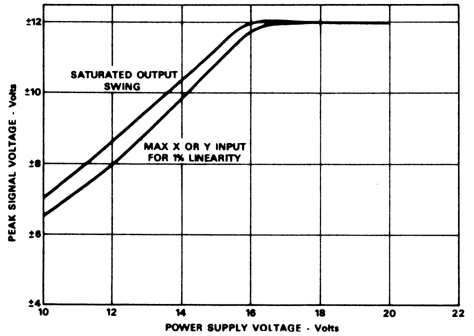


Figure 8. Signal Swing vs. Supply

NOISE CHARACTERISTICS

All AD532s are screened on a sampling basis to assure that output noise will have no appreciable effect on accuracy. Typical spot noise vs. frequency is shown in Figure 9.

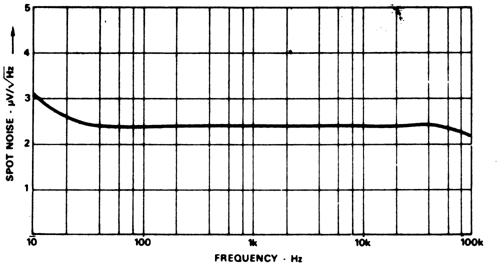


Figure 9. Spot Noise vs. Frequency

APPLICATIONS CONSIDERATIONS

The performance and ease of use of the AD532 is achieved through the laser trimming of thin film resistors deposited directly on the monolithic chip. This trimming-on-the-chip technique provides a number of significant advantages in terms of cost, reliability and flexibility over conventional in-package trimming of off-the-chip resistors mounted or deposited on a hybrid substrate.

First and foremost, trimming on the chip eliminates the need for a hybrid substrate and the additional bonding wires that are required between the resistors and the multiplier chip. By trimming more appropriate resistors on the AD532 chip itself, the second input terminals that were once committed to external trimming networks (e.g., AD530) have been freed to allow fully differential operation at both the X and Y inputs. Further, the requirement for an input attenuator to adjust the gain at the Y input has been eliminated, letting the user take full advantage of the high input impedance properties of the input differential amplifiers. Thus, the AD532 offers greater flexibility for both algebraic computation and transducer instrumentation applications.

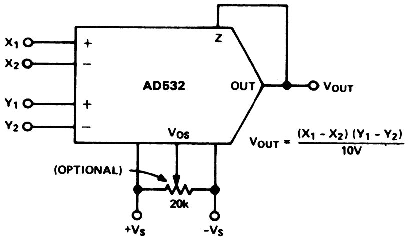
Finally, provision for fine trimming the output voltage offset has been included. This connection is optional, however, as the AD532 has been factory-trimmed for total performance as described in the listed specifications.

REPLACING OTHER IC MULTIPLIERS

Existing designs using IC multipliers that require external trimming networks (such as the AD530) can be simplified using the pin-for-pin replaceability of the AD532 by merely grounding the X_2, Y_2 and V_{OS} terminals. (The V_{OS} terminal should always be grounded when unused.)

APPLICATIONS

MULTIPLICATION



$$V_{OUT} = \frac{(X_1 - X_2)(Y_1 - Y_2)}{10V}$$

Figure 10. Multiplier Connection

For operation as a multiplier, the AD532 should be connected as shown in Figure 10. The inputs can be fed differentially to the X and Y inputs, or single-ended by simply grounding the unused input. Connect the inputs according to the desired polarity in the output. The Z terminal is tied to the output to close the feedback loop around the op amp (see first page). The offset adjust V_{OS} is optional and is adjusted when both inputs are zero volts to obtain zero out, or to buck out other system offsets.

SQUARE

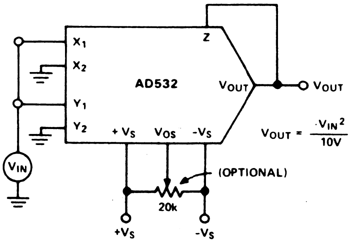


Figure 11. Squarer Connection

The squaring circuit in Figure 11 is a simple variation of the multiplier. The differential input capability of the AD532 can be used, however, to obtain a positive or negative output response to the input....a useful feature for control applications, as it might eliminate the need for an additional inverter somewhere else.

DIVISION

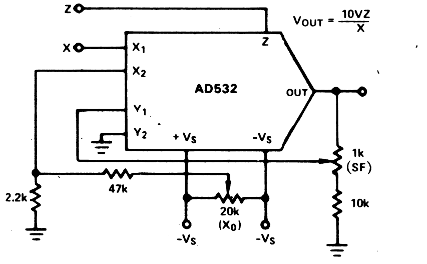


Figure 12. Divider Connection

The AD532 can be configured as a two-quadrant divider by connecting the multiplier cell in the feedback loop of the op amp and using the Z terminal as a signal input, as shown in Figure 12. It should be noted, however, that the output error is given approximately by $10V\epsilon_m/(X_1-X_2)$, where ϵ_m is the total error specification for the multiply mode; and bandwidth by $f_m \cdot (X_1-X_2)/10V$, where f_m is the bandwidth of the multiplier. Further, to avoid positive feedback, the X input is restricted to negative values. Thus for single-ended negative inputs (0V to -10V), connect the input to X and the offset null to X_2; for single-ended positive inputs (0V to +10V), connect the input to X_2 and the offset null to X_1. For optimum performance, gain (S.F.) and offset (X_0) adjustments are recommended as shown and explained in Table I.

For practical reasons, the useful range in denominator input is approximately $500mV \leqslant |(X_1-X_2)| \leqslant 10V$. The voltage offset adjust (V_{os}), if used, is trimmed with Z at zero and (X_1-X_2) at full scale.

SQUARE ROOT

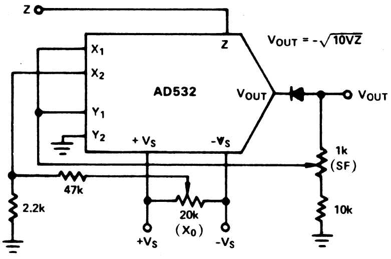


Figure 13. Square Rooter Connection

The connections for square root mode are shown in Figure 13. Similar to the divide mode, the multiplier cell is connected in the feedback of the op amp by connecting the output back to both the X and Y inputs. The diode D_1 is connected as shown to prevent latch-up as Z_{in} approaches 0 volts. In this case, the V_{os} adjustment is made with Z_{in} = +0.1V dc, adjusting V_{os} to obtain -1.0V dc in the output, $V_{out} = -\sqrt{10VZ}$. For optimum performance, gain (S.F.) and offset (X_0) adjustments are recommended as shown and explained in Table I.

DIFFERENCE OF SQUARES

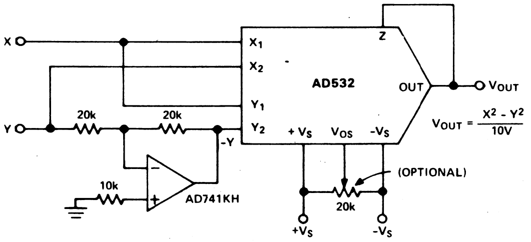


Figure 14. Differential of Squares Connection

The differential input capability of the AD532 allows for the algebraic solution of several interesting functions, such as the difference of squares, $X^2-Y^2/10V$. As shown in Figure 14, the AD532 is configured in the square mode, with a simple unity gain inverter connected between one of the signal inputs (Y) and one of the inverting input terminals ($-Y_{in}$) of the multiplier. The inverter should use precision (0.1%) resistors or be otherwise trimmed for unity gain for best accuracy.

TABLE I

ADJUST PROCEDURE (Divider or Square Rooter)

	DIVIDER			SQUARE ROOTER	
	With:	Adjust for:		With:	Adjust for:
Adjust	X	Z	V_{out}	Z	V_{out}
Scale Factor	−10V	+10V	±10V	+10V	−10V
X_o (Offset)	−1V	+0.1V	±10V	+0.1V	−1V

Repeat if required.

ANALOG
DEVICES

Low Cost IC Multiplier,Divider,Squarer,Square Rooter

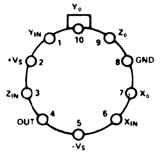
AD533

FEATURES

- Low Cost
- Simplicity of Operation: Only Four External Adjustments
- Max 4-Quadrant Error Below 0.5% (AD533L)
- Low Temperature Drift: 0.01%/°C (AD533L)
- Multiplies, Divides, Squares, Square Roots

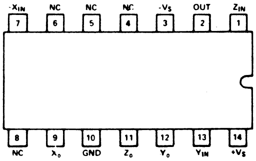
AD533 PIN CONFIGURATIONS

AD533H



TO-100
TOP VIEW

AD533D



TO-116
TOP VIEW

PRODUCT DESCRIPTION

The Analog Devices AD533 is a low cost integrated circuit multiplier comprised of a transconductance multiplying element, stable reference, and output amplifier on a monolithic silicon chip. Specified accuracy is easily achieved by the straight-forward adjustment of feedthrough, output zero, and gain trim pots. The AD533 multiplies in four quadrants with a transfer function of XY/10V, divides in two quadrants with a 10VZ/X transfer function, and square roots in one quadrant with a transfer function of $-\sqrt{10VZ}$. Several levels of accuracy are provided: the AD533J, AD533K, and AD533L, for 0 to +70°C operation, are specified for maximum multiplying errors of 2%, 1%, and 0.5% respectively at +25°C. The AD533S, for operation from -55°C to +125°C, is guaranteed for a maximum 1% multiplying error at +25°C. The maximum error specification is a true measure of overall accuracy since it includes the effects of offset voltage, feedthrough, scale factor, and nonlinearity in all four quadrants.

The low drift design of the AD533 insures that high accuracy is maintained with variations in temperature. The op amp output provides ±10 volts at 5mA, and is fully protected against short circuits to ground or either supply voltage: all inputs are fully protected against over-voltage transients with internal series resistors. The devices provide excellent ac performance, with typical small signal bandwidth of 1.0MHz, full power bandwidth of 750kHz, and slew rate of 45V/µs.

The low cost and simplicity of operation of the AD533 make it especially well suited for use in such widespread applications as modulation and demodulation, automatic gain control and phase detection. Other applications include frequency discrimination, rms computation, peak detection, voltage controlled oscillators and filters, function generation, and power measurements.

All models are available in the hermetically sealed TO-100 metal can and TO-116 ceramic DIP packages.

SPECIFICATIONS (typical @ +25°C, externally trimmed and V_S = ±15V dc unless otherwise specified)

PARAMETER	CONDITIONS	AD533J	AD533K	AD533L	AD533S
ABSOLUTE MAX RATINGS					
Internal Power Dissipation		500mW	*	*	*
Input Voltage[1]					
$X_{in}, Y_{in}, Z_{in}, X_O, Y_O, Z_O$		$\pm V_S$	*	*	*
Rated Operating Temp Range		0 to +70°C	*	*	-55°C to +125°C
Storage Temp Range		-65°C to +150°C	*	*	*
Output Short Circuit	To Ground	Indefinite	*	*	*
MULTIPLIER SPECIFICATIONS					
Transfer Function		XY/10V	*	*	*
	Untrimmed	XY/6V max [XY/10V min]	*	*	*
Total Error (of full scale)		±2.0% max	±1.0% max	±0.5% max	±1.0% max
	T_A = min to max	±3.0%	±2.0%	±1.0%	±1.5%
vs. Temperature	T_A = min to max	±0.04%/°C	±0.03%/°C	±0.01%/°C	±0.01%/°C
Nonlinearity					
X Input	$V_x = V_o$ = 20V(p-p)	±0.8%	±0.5%	**	**
Y Input	$V_y = V_o$ = 20V(p-p)	±0.3%	±0.2%	**	**
Feedthrough					
X Input	V_x = 20V(p-p), V_y = 0, f = 50Hz	150mV(p-p) max	200mV(p-p) max	50mV(p-p) max	100mV (p-p) max
Y Input	V_y = 20V(p-p), V_x = 0, f = 50Hz	200mV(p-p) max	150mV(p-p) max	50mV(p-p) max	100mV (p-p) max
DIVIDER SPECIFICATIONS					
Transfer Function		10VZ/X	*	*	*
	Untrimmed	10VZ/X max [6VZ/X min]	*	*	*
Total Error (of full scale)	V_x = -10V dc, V_z = ±10V dc	±1.0%	±0.5%	±0.2%	±0.5%
	V_x = -1V dc, V_z = ±10V dc	±3.0%	±2.0%	±1.5%	±2.0%
SQUARER SPECIFICATIONS					
Transfer Function		X^2/10V	*	*	*
	Untrimmed	X^2/6V max [X^2/10V min]	*	*	*
Total Error (of full scale)		±0.8%	±0.4%	±0.2%	±0.4%
SQUARE ROOTER SPECIFICATIONS					
Transfer Function		$-\sqrt{10VZ}$	*	*	*
	Untrimmed	$-\sqrt{10VZ}$ max [$-\sqrt{6VZ}$ min]	*	*	*
Total Error (of full scale)		±0.8%	±0.4%	±0.2%	±0.4%
INPUT SPECIFICATIONS					
Input Resistance					
X Input		10MΩ	*	*	*
Y Input		6MΩ	*	*	*
Z Input		36kΩ	*	*	*
Input Bias Current					
X, Y Inputs		3μA	7.5μA max	5μA max	7.5μA max
Z Input		±25μA	*	*	*
X, Y Inputs	T_A = min to max	12μA	10μA	7μA	7μA
Z Input	T_A = min to max	±35μA	*	*	*
Input Voltage	T_A = min to max				
V_x, V_y, V_z	For Rated Accuracy	±10V	*	*	*
DYNAMIC SPECIFICATIONS					
Small Signal, Unity Gain		1.0MHz	*	*	*
Full Power Bandwidth		750kHz	*	*	*
Slew Rate		45V/μs	*	*	*
Small Signal Amplitude Error		1% at 75kHz	*	*	*
Sm Sig 1% Vector Error	0.5° phase shift	5kHz	*	*	*
Settling Time	±10V step	1μs to 2%	*	*	*
Overload Recovery		2μs to 2%	*	*	*
OUTPUT AMPLIFIER SPECIFICATIONS					
Output Impedance		100Ω	*	*	*
Output Voltage Swing	T_A = min to max $R_L \geq 2k\Omega$, $C_L \leq 1000pF$	±10V min	*	*	*
Output Noise	f = 5Hz to 10kHz	0.6mV(rms)	*	*	*
	f = 5Hz to 5MHz	3.0mV(rms)	*	*	*
Output Offset Voltage		Trimmable To Zero	*	*	*
vs. Temperature	T_A = min to max	0.7mV/°C	*	*	*
POWER SUPPLY SPECIFICATIONS					
Supply Voltage	Rated Performance	±15V	*	*	*
	Operating	±15V to ±18V	±10V to ±18V	±10V to ±18V	±10V to ±22V
Supply Current	Quiescent	±6mA max	*	*	*
Power Supply Variation	*Includes* Effects of Recommended Null Pots				
Multiplier Accuracy		±0.5%/%	*	*	*
Output Offset		±10mV/%	*	*	*
Scale Factor		±0.1%/%	*	*	*
Feedthrough		±10mV/%	*	*	*

[1] Max input voltage is zero when supplies are turned off.

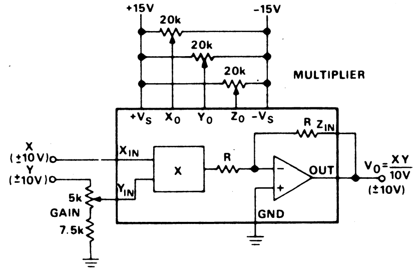
***Specifications same as AD533J.**

****Specifications same as AD533K.**

Specifications subject to change without notice.

MULTIPLIER

Multiplier operation is accomplished by closing the loop around the internal op amp with the Z input connected to the output. The X_O null pot balances the X input channel to minimize Y feedthrough and similarly the Y_O pot minimizes the X feedthrough. The Z_O pot nulls the output op amp offset voltage and the gain pot sets the full scale output level.



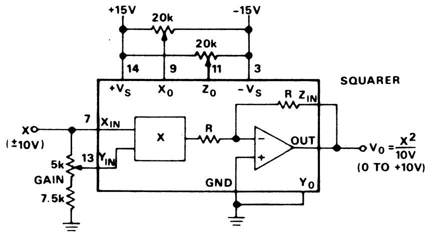
TRIM PROCEDURES

1. With X = Y = 0 volts, adjust Z_O for 0V dc output.
2. With Y = 20 volts p-p (at f = 50Hz) and X = 0V, adjust X_O for minimum ac output.
3. With X = 20 volts p-p (at f = 50Hz) and Y = 0V, adjust Y_O for minimum ac output.
4. Readjust Z_O for 0V dc output.
5. With X = +10V dc and Y = 20 volts p-p (at f = 50Hz), adjust gain for output = Y_{in}.

NOTE: For best accuracy over limited voltage ranges (e.g., ±5V), gain and feedthrough adjustments should be optimized with the inputs in the desired range, as linearity is considerably better over smaller ranges of input.

SQUARER

Squarer operation is a special case of multiplier operation where the X and Y inputs are connected together and two quadrant operation results since the output is always positive. When the X and Y inputs are connected together, a composite offset results which is the algebraic sum of the individual offsets which can be nulled using the X_O pot alone.

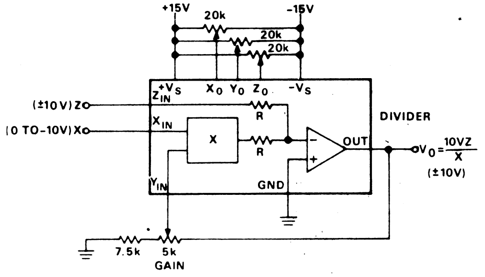


TRIM PROCEDURES

1. With X = 0 volts, adjust Z_O for 0V dc output.
2. With X = +10V dc, adjust gain for +10V dc output.
3. Reverse polarity of X input and adjust X_O to reduce the output error to ½ its original value, readjust the gain to take out the remaining error.
4. Check the output offset with input grounded. If nonzero, repeat the above procedure until no errors remain.

DIVIDER

The divide mode utilizes the multiplier in a fed-back configuration where the Y input now controls the feedback factor. With X = full scale, the gain (V_O/Z) becomes unity after trimming. Reducing the X input reduces the feedback around the op amp by a like amount, thereby increasing the gain. This reciprocal relationship forms the basis of the divide mode. Accuracy and bandwidth decrease as the denominator decreases.

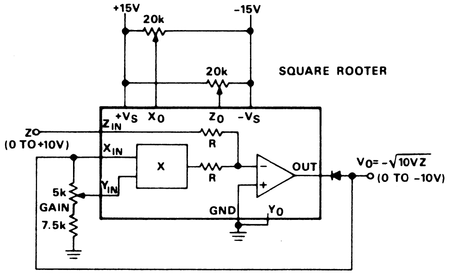


TRIM PROCEDURES

1. Set all pots at mid-scale.
2. With Z = 0V, trim Z_O to hold the output constant, as X is varied from -10V dc through -1V dc.
3. With Z = 0V, X = -10V dc, trim Y_O for 0V dc.
4. With Z = X or -X, trim X_O for the minimum worst-case variations as X is varied from -10V dc to -1V dc.
5. Repeat steps 2 and 3 if step 4 required a large initial adjustment.
6. With Z = X or -X, trim the gain for the closest average approach to ±10V dc output as X is varied from -10V dc to -3V dc.

SQUARE ROOTER

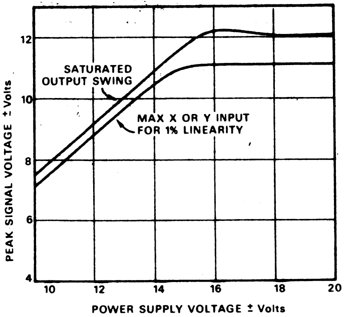
This mode is also a fed-back configuration with both the X and Y inputs tied to the op amp output through an external diode to prevent latchup. Accuracy, noise and frequency response are proportional to $\sqrt{Z}$, which implies a wider usable dynamic range than the divide mode.



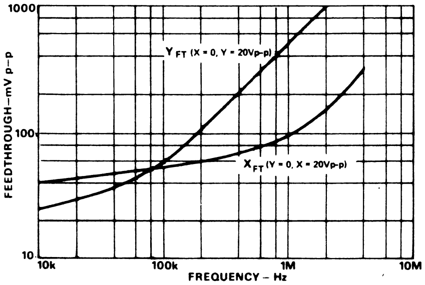
TRIM PROCEDURES

1. With Z = +0.1V dc, adjust Z_O for Output = -1.0V dc.
2. With Z = +10.0V dc, adjust gain for Output = -10.0V dc.
3. With Z = +2.0V dc, adjust X_O for Output = -4.47 ±0.1V dc.
4. Repeat steps 2 and 3, if necessary. Repeat step 1.

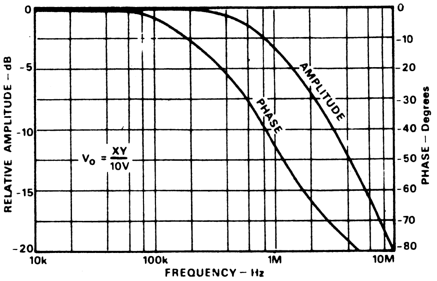
TYPICAL PERFORMANCE CHARACTERISTICS



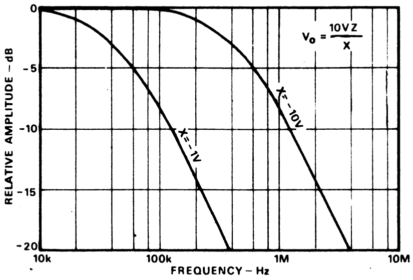
Allowable Signal Swing vs. Supply Voltage



Feedthrough vs. Frequency



Closed Loop Frequency and Phase Response



Divide Mode Frequency Response

ORDERING GUIDE

MODEL	MULT. ERROR (Max @ +25°C)	TEMP. RANGE	ORDER NUMBER	PACKAGE OPTIONS[1]
AD533J	±2.0%	0 to +70°C	AD533JH	TO-100
			AD533JD	TO-116 Style (D14A)
AD533K	±1.0%	0 to +70°C	AD533KH	TO-100
			AD533KD	TO-116 Style (D14A)
AD533L	±0.5%	0 to +70°C	AD533LH	TO-100
			AD533LD	TO-116 Style (D14A)
AD533S	±1.0%	-55°C to +125°C	AD533SH	TO-100
			AD533SD	TO-116 Style (D14A)

[1] See Section 20 for package outline information.

ANALOG DEVICES

Internally Trimmed Precision IC Multiplier

AD534

FEATURES

Pretrimmed to ±0.25% max 4-Quadrant Error (AD534L)
All Inputs (X, Y and Z) Differential, High Impedance for $[(X_1-X_2)(Y_1-Y_2)/10V]+Z_2$ Transfer Function
Scale-Factor Adjustable to Provide up to X100 Gain
Low Noise Design: 90µV rms, 10Hz-10kHz
Low Cost, Monolithic Construction
Excellent Long Term Stability

APPLICATIONS

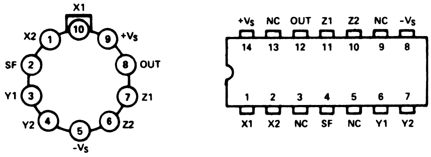
High Quality Analog Signal Processing
Differential Ratio and Percentage Computations
Algebraic and Trigonometric Function Synthesis
Wideband, High-Crest rms-to-dc Conversion
Accurate Voltage Controlled Oscillators and Filters

PRODUCT DESCRIPTION

The AD534 is a monolithic laser trimmed four-quadrant multiplier divider having accuracy specifications previously found only in expensive hybrid or modular products. A maximum multiplication error of ±0.25% is guaranteed for the AD534L without any external trimming. Excellent supply rejection, low temperature coefficients and long term stability of the on-chip thin film resistors and buried zener reference preserve accuracy even under adverse conditions of use. It is the first multiplier to offer fully differential, high impedance operation on all inputs, including the Z-input, a feature which greatly increases its flexibility and ease of use. The scale factor is pretrimmed to the standard value of 10.00V; by means of an external resistor, this can be reduced to values as low as 3V.

The wide spectrum of applications and the availability of several grades commend this multiplier as the first choice for all new designs. The AD534J (±1% max error), AD534K (±0.5% max) and AD534L (±0.25% max) are specified for operation over the 0 to +70°C temperature range. The AD534S (±1% max) and AD534T (±0.5% max) are specified over the extended temperature range, -55°C to +125°C. All grades are available in hermetically sealed TO-100 metal cans and TO-116 ceramic DIP packages.

AD534 PIN CONFIGURATIONS



TO-100 TO-116

TOP VIEW

PROVIDES GAIN WITH LOW NOISE

The AD534 is the first general purpose multiplier capable of providing gains up to X100, frequently eliminating the need for separate instrumentation amplifiers to precondition the inputs. The AD534 can be very effectively employed as a variable gain differential input amplifier with high common mode rejection. The gain option is available in all modes, and will be found to simplify the implementation of many function-fitting algorithms such as those used to generate sine and tangent. The utility of this feature is enhanced by the inherent low noise of the AD534: 90µV, rms (depending on the gain), a factor of 10 lower than previous monolithic multipliers. Drift and feedthrough are also substantially reduced over earlier designs.

UNPRECEDENTED FLEXIBILITY

The precise calibration and differential Z-input provide a degree of flexibility found in no other currently available multiplier. Standard MDSSR functions (multiplication, division, squaring, square-rooting) are easily implemented while the restriction to particular input/output polarities imposed by earlier designs has been eliminated. Signals may be summed into the output, with or without gain and with either a positive or negative sense. Many new modes based on implicit-function synthesis have been made possible, usually requiring only external passive components. The output can be in the form of a current, if desired, facilitating such operations as integration.

SPECIFICATIONS (typical at +25°C, with $\pm V_S$ = 15V, $R_L \geqslant 2k$, unless otherwise stated)

PARAMETER	CONDITIONS	AD534J	AD534K	AD534L	AD534S (AD534S/883B)[1]	AD534T (AD534T/883B)[1]
MULTIPLIER PERFORMANCE						
Transfer Function		$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}+Z_2$	•	•	•	•
Total Error[2]	$-10V \leqslant X, Y \leqslant +10V$	±1.0% max	±0.5% max	±0.25% max	•	••
	T_A = min to max					
	V_S = ±14V to ±16V	±1.5%	±1.0%	±0.5%	±2.0% max	±1.0% max
vs. Temperature		±0.022%/°C	±0.015%/°C	±0.008%/°C	±0.02%/°C max	±0.01%/°C max
Scale Factor Error	SF = 10.00V nominal[3]	±0.25%	±0.1%	••	•	••
Temperature-Coefficient of Scaling-Voltage	T_A = min to max	±0.02%/°C	±0.01%/°C	±0.005%/°C	•	±0.005%/°C max
Supply Rejection	$\pm V_S$ = (15V) ±1V	±0.01%	•	•	•	•
Nonlinearity, X	X = 20V pk-pk					
	Y = ±10V	±0.4%	±0.2% (0.3% max)	±0.1% (0.12% max)	•	••
Nonlinearity, Y	Y = 20V pk-pk					
	X = ±10V	±0.01%	±0.01%(±0.1% max)	±0.005% (±0.1% max)	•	••
Feedthrough[4], X	Y nulled					
	X = 20V pk-pk 50Hz	±0.3%	±0.15% (0.3% max)	±0.05% (0.12% max)	•	••
Feedthrough[4], Y	X nulled					
	Y = 20V pk-pk 50Hz	±0.01%	±0.01% (±0.1% max)	±0.003% (±0.1% max)	•	••
Output Offset Voltage,		±5mV (±30mV max)	±2mV (±15mV max)	±2mV (±10mV max)	•	••
Drift	T_A = min to max	200µV/°C	100µV/°C	••	500µV/°C max	300µV/°C max
DYNAMICS						
Small-Signal BW	V_{OUT} = 0.1V rms	1MHz	•	•	•	•
1% Amplitude Error	C_{LOAD} = 1000pF	50kHz	•	•	•	•
Slew Rate	V_{OUT} 20V pk-pk	20V/µs	•	•	•	•
Settling Time to ±1%	ΔV_{OUT} = 20V	2µs	•	•	•	•
NOISE						
Noise Spectral-Density	SF = 10V	$0.8\mu V/\sqrt{Hz}$	•	•	•	•
	SF = 3V (Note 5)	$0.4\mu V/\sqrt{Hz}$	•	•	•	•
Wideband Noise	f = 10Hz to 5MHz	1mV rms	•	•	•	•
	f = 10Hz to 10kHz	90µV rms	•	•	•	•
	f = 10Hz to 10kHz, SF = 3V (Note 5)	60µV rms	•	•	•	•
OUTPUT						
Output Voltage Swing	T_A = min to max	±11V min	•	•	•	•
Output Impedance	Unity-Gain, $f \leqslant 1kHz$	0.1Ω	•	•	•	•
Maximum Output Current	R_L = 0, T_A = min to max	30mA	•	•	•	•
Amplifier Open-Loop Gain	f = 50Hz	70dB	•	•	•	•
INPUT AMPLIFIERS (X, Y and Z)[6]						
Signal Voltage Range	Rated Accuracy (Diff. or CM)	±10V	•	•	•	•
	Operating (Diff.)	±12V	•	•	•	•
Offset Voltage, X, Y		±5mV (±20mV max)	±2mV (±10mV max)	••	•	••
Drift	T_A = min to max	100µV/°C	50µV/°C	••	•	150µV/°C
Offset Voltage, Z		±5mV (±30mV max)	±2mV (±15mV max)	±2mV (±10mV max)	•	••
Drift	T_A = min to max	200µV/°C	100µV/°C	••	500µV/°C max	300µV/°C max
CMRR (X, Y, Z)	50Hz, 20V pk-pk	80dB (60dB min)	90dB (70dB min)	••	•	••
Bias Current	Diff. Input = 0	0.8µA (2µA max)	•	•	•	•
Offset Current	Diff. Input = 0	0.1µA	•	0.05µA (0.2µA max)	•	•
Differential Resistance		10MΩ	•	•	•	•
DIVIDER PERFORMANCE[7]						
Transfer Function	$X_1 > X_2$	$10V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$	•	•	•	•
Total Error[2]	X = 10V					
	$-10V \leqslant Z \leqslant +10V$	±0.75%	±0.35%	±0.2%	•	••
	X = 1V					
	$-1V \leqslant Z \leqslant +1V$	±2.0%	±1.0%	±0.8%	•	••
	$0.1V \leqslant X \leqslant 10V$					
(Note 8)	$-10V \leqslant Z \leqslant +10V$	±2.5%	±1.0%	±0.8%	•	••
SQUARER PERFORMANCE						
Transfer Function		$\frac{(X_1-X_2)^2}{10V}+Z_2$	•	•	•	•
Total Error[2]	$-10V \leqslant X \leqslant +10V$	±0.6%	±0.3%	±0.2%	•	••
SQUARE-ROOTER PERFORMANCE[7]						
Transfer Function	$Z_1 \leqslant Z_2$	$\sqrt{10V(Z_2-Z_1)+X_2}$	•	•	•	•
Total Error[2]	$1V \leqslant Z \leqslant 10V$	±1.0%	±0.5%	±0.25%	•	••
POWER SUPPLY SPECIFICATIONS						
Supply Voltage	Rated Performance	±15V	•	•	•	•
	Operating	±8V to ±18V	•	•	±8V to ±22V	±8V to ±22V
Supply Current	Quiescent	4mA (6mA max)	•	•	•	•
PACKAGE OPTIONS[9]						
H: TO-100 Package		AD534JH	AD534KH	AD534LH	AD534SH	AD534TH
D: TO-116 Package (D14A)		AD534JD	AD534KD	AD534LD	AD534SD	AD534TD

NOTES

•Specifications same as AD534J.

••Specifications same as AD534K.

[1] The AD534S and AD534T are available fully processed to MIL-STD-883 Class B.

[2] Figures given are percent of full-scale, ±10V (i.e., 0.01% = 1mV).

[3] May be reduced down to 3V using external resistor between $-V_S$ and SF.

[4] Irreducible component due to nonlinearity: excludes effect of offsets.

[5] Using external resistor adjusted to give SF = 3V.

[6] See Functional Block Diagram, Figure 1, for definition of sections.

[7] The AD535 is a functional equivalent to the AD534, has guaranteed performance in the divider and square rooter modes and is recommended for such applications.

[8] With external Z-offset adjustment, $Z \leqslant \pm X$.

[9] See Section 20 for package outline information.

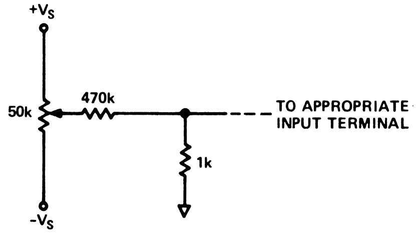
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

	AD534J, K, L	AD534S, T
Supply Voltage	±18V	±22V
Internal Power Dissipation	500mW	*
Output Short-Circuit to Ground	Indefinite	*
Input Voltages, X_1 X_2 Y_1 Y_2 Z_1 Z_2	$\pm V_S$	*
Rated Operating Temperature Range	0 to +70°C	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C	*
Lead Temperature, 60s soldering	+300°C	*

*Same as AD534J specs.

OPTIONAL TRIMMING CONFIGURATION



FUNCTIONAL DESCRIPTION

Figure 1 is a functional block diagram of the AD534. Inputs are converted to differential currents by three identical voltage-to-current converters, each trimmed for zero offset. The product of the X and Y currents is generated by a multiplier cell using Gilbert's translinear technique. An on-chip "Buried Zener" provides a highly stable reference, which is laser trimmed to provide an overall scale factor of 10V. The difference between XY/SF and Z is then applied to the high gain output amplifier. This permits various closed loop configurations and dramatically reduces nonlinearities due to the input amplifiers, a dominant source of distortion in earlier designs. The effectiveness of the new scheme can be judged from the fact that under typical conditions as a multiplier the nonlinearity on the Y input, with X at full scale (±10V), is ±0.005% of F.S.; even at its worst point, which occurs when X = ±6.4V, it is typically only ±0.05% of F.S. Nonlinearity for signals applied to the X input, on the other hand, is determined almost entirely by the multiplier element and is parabolic in form. This error is a major factor in determining the overall accuracy of the unit and hence is closely related to the device grade.

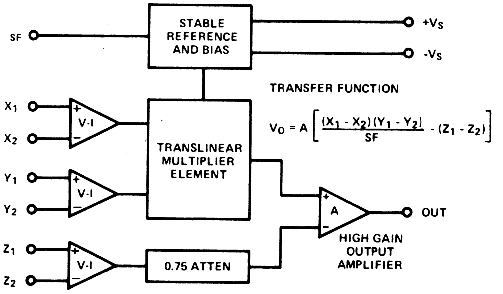

SF
STABLE REFERENCE AND BIAS
+Vs
-Vs
TRANSFER FUNCTION
$V_O = A\left[\frac{(X_1 - X_2)(Y_1 - Y_2)}{SF} - (Z_1 - Z_2)\right]$
X1
X2
V-I
Y1
Y2
V-I
Z1
Z2
V-I
TRANSLINEAR MULTIPLIER ELEMENT
0.75 ATTEN
A
OUT
HIGH GAIN OUTPUT AMPLIFIER

Figure 1. AD534 Functional Block Diagram

The generalized transfer function for the AD534 is given by:

$$V_{OUT} = A\left(\frac{(X_1 - X_2)(Y_1 - Y_2)}{SF} - (Z_1 - Z_2)\right)$$

where A = open loop gain of output amplifier, typically 70dB at dc

X, Y, Z = input voltages (full scale = ±SF, peak= ±1.25SF)

SF = scale factor, pretrimmed to 10.00V but adjustable by the user down to 3V.

In most cases the open loop gain can be regarded as infinite, and SF will be 10V. The operation performed by the AD534, can then be described in terms of equation:

$$(X_1 - X_2)(Y_1 - Y_2) = 10V (Z_1 - Z_2)$$

The user may adjust SF for values between 10.00V and 3V by connecting an external resistor in series with a potentiometer between SF and $-V_S$. The approximate value of the total resistance for a given value of SF is given by the relationship:

$$R_{SF} = 5.4K \frac{SF}{10 - SF}$$

Due to device tolerances, allowance should be made to vary R_{SF} by ±25% using the potentiometer. Considerable reduction in bias currents, noise and drift can be achieved by decreasing SF. This has the overall effect of increasing signal gain without the customary increase in noise. Note that the peak input signal is always limited to 1.25SF (i.e., ±5V for SF = 4V) so the overall transfer function will show a maximum gain of 1.25. The performance with small input signals, however, is improved by using a lower SF since the dynamic range of the inputs is now fully utilized. Bandwidth is unaffected by the use of this option.

Supply voltages of ±15V are generally assumed. However, satisfactory operation is possible down to ±8V (see curve 1). Since all inputs maintain a constant peak input capability of ±1.25SF some feedback attenuation will be necessary to achieve output voltage swings in excess of ±12V when using higher supply voltages.

OPERATION AS A MULTIPLIER

Figure 2 shows the basic connection for multiplication. Note that the circuit will meet all specifications without trimming.

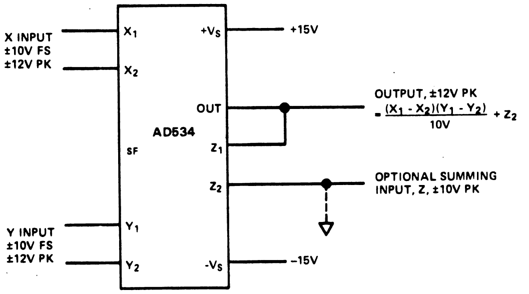


Figure 2. Basic Multiplier Connection

In some cases the user may wish to reduce ac feedthrough to a minimum (as in a suppressed carrier modulator) by applying an external trim voltage (±30mV range required) to the X or Y input (see Optional Trimming Configuration, previous page). Curve 4 shows the typical ac feedthrough with this adjustment mode. Note that the Y input is a factor of 10 lower than the X input and should be used in applications where null suppression is critical.

The high impedance Z_2 terminal of the AD534 may be used to sum an additional signal into the output. In this mode the output amplifier behaves as a voltage follower with a 1MHz small signal bandwidth and a 20V/µs slew rate. This terminal should always be referenced to the ground point of the driven system, particularly if this is remote. Likewise the differential inputs should be referenced to their respective ground potentials to realize the full accuracy of the AD534.

A much lower scaling voltage can be achieved without any reduction of input signal range using a feedback attenuator as shown in Figure 3. In this example, the scale is such that $V_{OUT} = XY$, so that the circuit can exhibit a maximum gain of 10. This connection results in a reduction of bandwidth to about 80kHz without the peaking capacitor C_F = 200pF. In addition, the output offset voltage is increased by a factor of 10 making external adjustments necessary in some applications. Adjustment is made by connecting a 4.7MΩ resistor between Z_1 and the slider of a pot connected across the supplies to provide ±300mV of trim range at the output.

Feedback attenuation also retains the capability for adding a signal to the output. Signals may be applied to the high impedance Z_2 terminal where they are amplified by +10 or to the common ground connection where they are amplified by +1. Input signals may also be applied to the lower end of the 10kΩ resistor, giving a gain of -9. Other values of feedback ratio, up to X100, can be used to combine multiplication with gain.

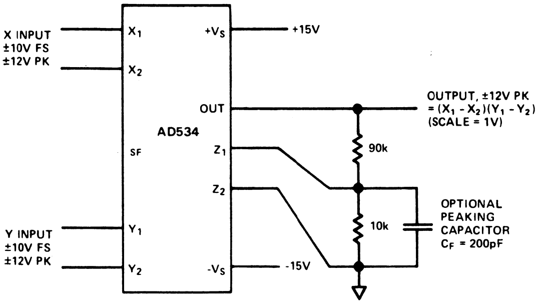


Figure 3. Connections for Scale-Factor of Unity

Occasionally it may be desirable to convert the output to a current, into a load of unspecified impedance or dc level. For example, the function of multiplication is sometimes followed by integration; if the output is in the form of a current, a simple capacitor will provide the integration function. Figure 4 shows how this can be achieved. This method can also be applied in squaring, dividing and square rooting modes by appropriate choice of terminals. This technique is used in the voltage-controlled low-pass filter and the differential-input voltage-to-frequency converter shown in the Applications Section.

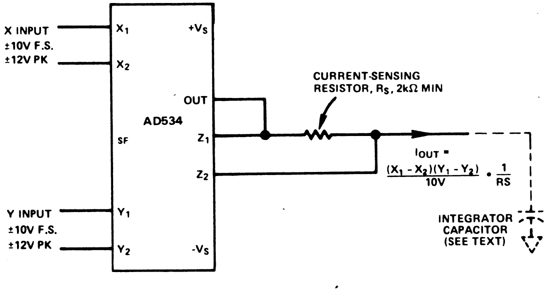


Figure 4. Conversion of Output to Current

OPERATION AS A SQUARER

Operation as a squarer is achieved in the same fashion as the multiplier except that the X and Y inputs are used in parallel. The differential inputs can be used to determine the output polarity (positive for $X_1 = Y_1$ and $X_2 = Y_2$, negative if either one of the inputs is reversed). Accuracy in the squaring mode is typically a factor of 2 better than in the multiplying mode, the largest errors occurring with small values of output for input below 1V.

If the application depends on accurate operation for inputs that are always less than ±3V, the use of a reduced value of SF is recommended as described in the FUNCTIONAL DESCRIPTION section (previous page). Alternatively, a feedback attenuator may be used to raise the output level. This is put to use in the difference-of-squares application to compensate for the factor of 2 loss involved in generating the sum term (see Figure 7).

The difference-of-squares function is also used as the basis for a novel rms-to-dc converter shown in Figure 14. The averaging filter is a true integrator, and the loop seeks to zero its input. For this to occur, $(V_{IN})^2 - (V_{OUT})^2 = 0$ (for signals whose period is well below the averaging time-constant). Hence V_{OUT} is forced to equal the rms value of V_{IN}. The absolute accuracy of this technique is very high; at medium frequencies, and for signals near full scale, it is determined almost entirely by the ratio of the resistors in the inverting amplifier. The multiplier scaling voltage affects only open loop gain. The data shown is typical of performance that can be achieved with an AD534K, but even using an AD534J, this technique can readily provide better than 1% accuracy over a wide frequency range, even for crest-factors in excess of 10.

OPERATION AS A DIVIDER

The AD535, a pin for pin functional equivalent to the AD534, has guaranteed performance in the divider and square-rooter configurations and is recommended for such applications.

Figure 5 shows the connection required for division. Unlike earlier products, the AD534 provides differential operation on both numerator and denominator, allowing the ratio of two floating variables to be generated. Further flexibility results from access to a high impedance summing input to Y_1. As with all dividers based on the use of a multiplier in a feedback loop, the bandwidth is proportional to the denominator magnitude, as shown in curve 8.

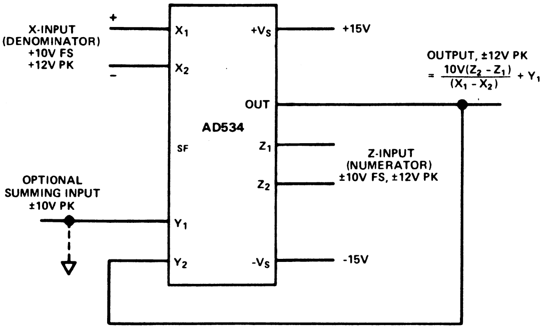

X-INPUT (DENOMINATOR) +10V FS +12V PK
+
-
X_1
X_2
$+V_S$
+15V
OUT
AD534
SF
Z_1
Z_2
Y_1
Y_2
$-V_S$
-15V
OUTPUT, ±12V PK
$= \frac{10V(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1$
Z-INPUT (NUMERATOR) ±10V FS, ±12V PK
OPTIONAL SUMMING INPUT ±10V PK

Figure 5. Basic Divider Connection

Without additional trimming, the accuracy of the AD534K and L is sufficient to maintain a 1% error over a 10V to 1V denominator range. This range may be extended to 100:1 by simply reducing the X offset with an externally generated trim voltage (range required is ±3.5mV max) applied to the unused X input (see Optional Trimming Configuration). To trim, apply a ramp of +100mV to +V at 100Hz to both X_1 and Z_1 (if X_2 is used for offset adjustment, otherwise reverse the signal polarity) and adjust the trim voltage to minimize the variation in the output.*

Since the output will be near +10V, it should be ac-coupled for this adjustment. The increase in noise level and reduction in bandwidth preclude operation much beyond a ratio of 100 to 1.

As with the multiplier connection, overall gain can be introduced by inserting a simple attenuator between the output and Y_2 terminal. This option, and the differential-ratio capability of the AD534 are utilized in the percentage-computer application shown in Figure 11. This configuration generates an output proportional to the percentage deviation of one variable (A) with respect to a reference variable (B), with a scale of one volt per percent.

OPERATION AS A SQUARE ROOTER

The operation of the AD534 in the square root mode is shown in Figure 6. The diode prevents a latching condition which could occur if the input momentarily changes polarity. As shown, the output is always positive; it may be changed to a negative output by reversing the diode direction and interchanging the X inputs. Since the signal input is differential, all combinations of input and output polarities can be realized, but operation is restricted to the one quadrant associated with each combination of inputs.

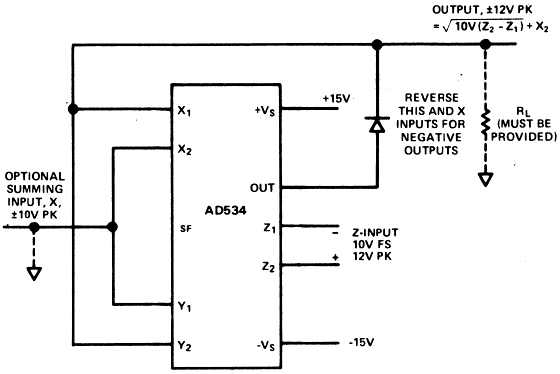


Figure 6. Square-Rooter Connection

In contrast to earlier devices, which were intolerant of capacitive loads in the square root modes, the AD534 is stable with all loads up to at least 1000pF. For critical applications, a small adjustment to the Z input offset (see Optional Trimming Configuration) will improve accuracy for inputs below 1V.

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*See the AD535 Data Sheet for more details.

Applications Section

The versatility of the AD534 allows the creative designer to implement a variety of circuits such as wattmeters, frequency doublers and automatic gain controls to name but a few. These applications along with many other such "idea stimulators" are described in detail in the *Multiplier Application Guide*, available upon request from Analog Devices.

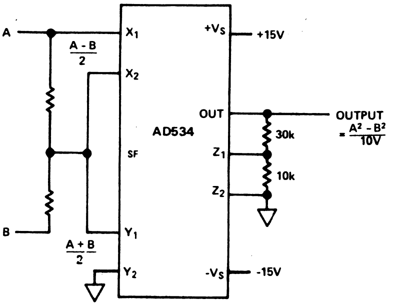
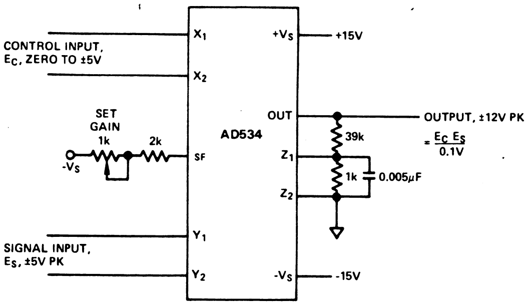
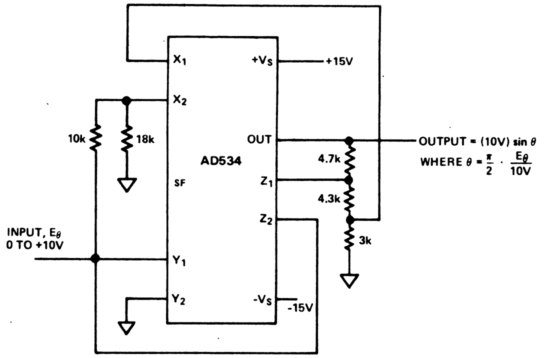


Figure 7. Difference-of-Squares



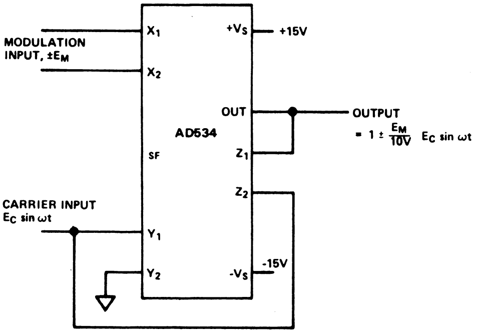
NOTES:
1) GAIN IS X10 PER VOLT OF E_C, ZERO TO X50
2) WIDEBAND (10Hz – 30kHz) OUTPUT NOISE IS 3mV RMS, TYP CORRESPONDING TO A F.S. S/N RATIO OF 70dB
3) NOISE REFERRED TO SIGNAL INPUT, WITH $E_C = \pm 5V$, IS 60µV RMS, TYP
4) BANDWIDTH IS DC TO 20kHz, -3dB, INDEPENDENT OF GAIN

Figure 8. Voltage-Controlled Amplifier



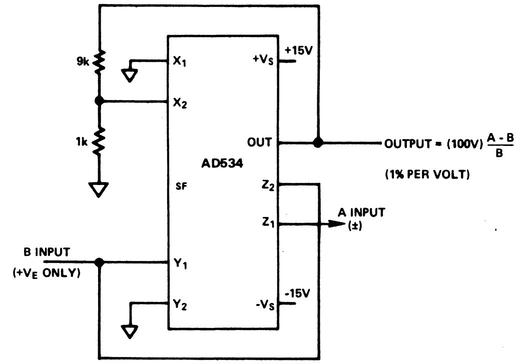
USING CLOSE TOLERANCE RESISTORS AND AD534L, ACCURACY OF FIT IS WITHIN ±0.5% AT ALL POINTS. θ IS IN RADIANS.

Figure 9. Sine-Function Generator



THE SF PIN OR A Z-ATTENUATOR CAN BE USED TO PROVIDE OVERALL SIGNAL AMPLIFICATION. OPERATION FROM A SINGLE SUPPLY IS POSSIBLE; BIAS Y_2 TO $V_S/2$.

Figure 10. Linear AM Modulator



OTHER SCALES, FROM 10% PER VOLT TO 0.1% PER VOLT CAN BE OBTAINED BY ALTERING THE FEEDBACK RATIO.

Figure 11. Percentage Computer

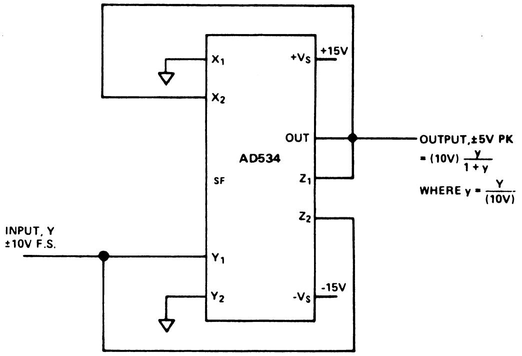
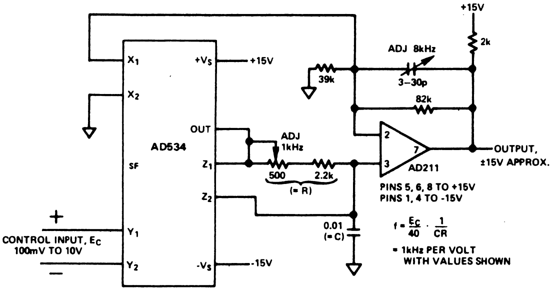


Figure 12. Bridge-Linearization Function



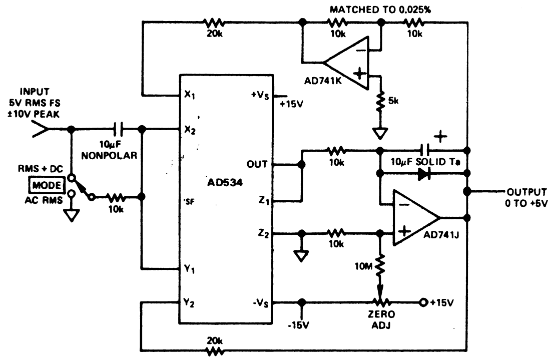
CALIBRATION PROCEDURE:

WITH E_C = 1.0V, ADJUST POT TO SET f = 1.000kHz. WITH E_C = 8.0V, ADJUST TRIMMER CAPACITOR TO SET f = 8.000kHz. LINEARITY WILL TYPICALLY BE WITHIN ±0.1% OF F.S. FOR ANY OTHER INPUT.

DUE TO DELAYS IN THE COMPARATOR, THIS TECHNIQUE IS NOT SUITABLE FOR MAXIMUM FREQUENCIES ABOVE 10kHz. FOR FREQUENCIES ABOVE 10kHz THE AD537 VOLTAGE TO FREQUENCY CONVERTER IS RECOMMENDED.

A TRIANGLE-WAVE OF ±5V PK APPEARS ACROSS THE 0.01µF CAPACITOR; IF USED AS AN OUTPUT, A VOLTAGE-FOLLOWER SHOULD BE INTERPOSED.

Figure 13. Differential-Input Voltage-to-Frequency Converter



CALIBRATION PROCEDURE:

WITH 'MODE' SWITCH IN 'RMS + DC' POSITION, APPLY AN INPUT OF +1.00VDC. ADJUST ZERO UNTIL OUTPUT READS SAME AS INPUT. CHECK FOR INPUTS OF ±10V; OUTPUT SHOULD BE WITHIN ±0.05% (5mV).

ACCURACY IS MAINTAINED FROM 60Hz to 100kHz, AND IS TYPICALLY HIGH BY 0.5% AT 1MHz FOR V_{IN} = 4V RMS (SINE, SQUARE OR TRIANGULAR WAVE).

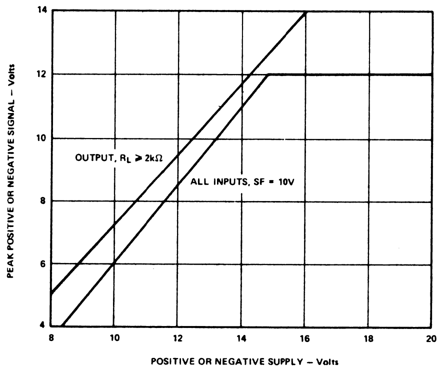
PROVIDED THAT THE PEAK INPUT IS NOT EXCEEDED, CREST-FACTORS UP TO AT LEAST TEN HAVE NO APPRECIABLE EFFECT ON ACCURACY.

INPUT IMPEDANCE IS ABOUT 10kΩ; FOR HIGH (10MΩ) IMPEDANCE, REMOVE MODE SWITCH AND INPUT COUPLING COMPONENTS.

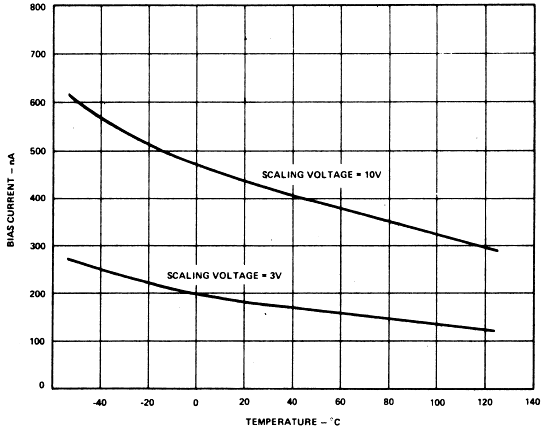
FOR GUARANTEED SPECIFICATIONS THE AD536A AND AD636 IS OFFERED AS A SINGLE PACKAGE RMS-TO-DC CONVERTER.

Figure 14. Wideband, High-Crest Factor, RMS-to-DC Converter

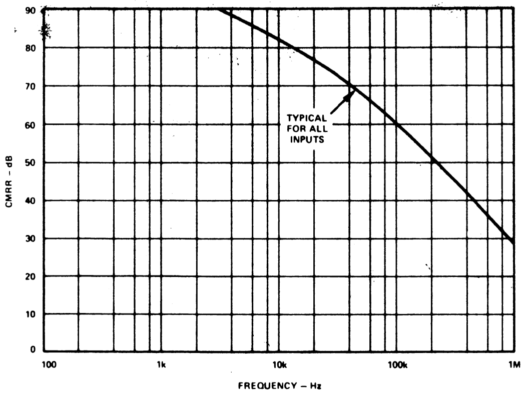
Typical Performance Curves (typical at +25°C, with V_S = ±15V dc, unless otherwise stated)



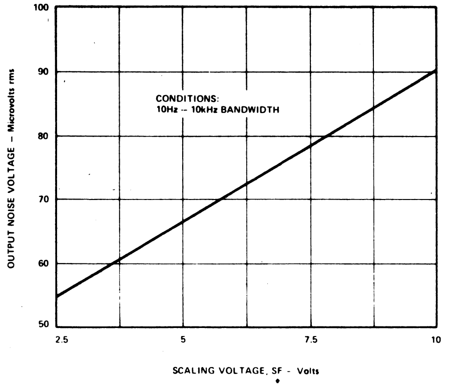
Curve 1. Input/Output Signal Range Vs. Supply Voltages



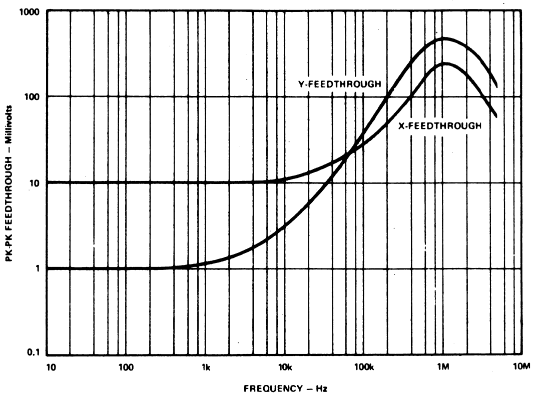
Curve 2. Bias Currents Vs. Temperature (X, Y or Z inputs)



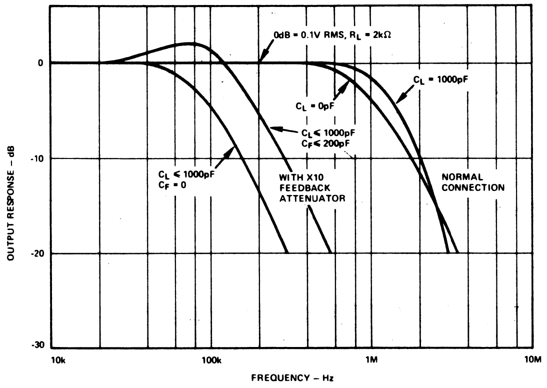
Curve 3. Common-Mode-Rejection-Ratio Vs. Frequency



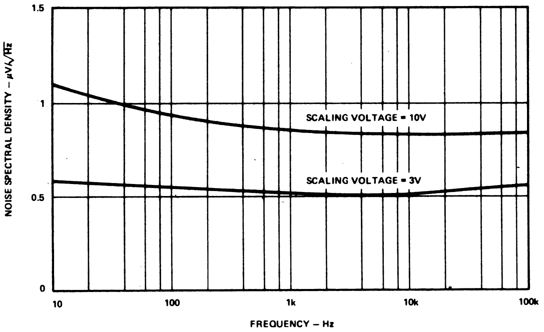
Curve 6. Wideband Noise Vs. Scaling Voltage



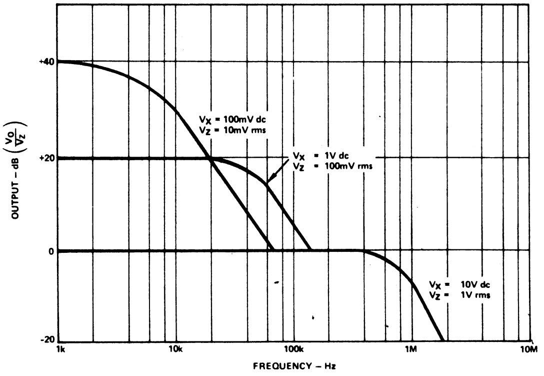
Curve 4. AC Feedthrough Vs. Frequency



Curve 7. Frequency Response as a Multiplier



Curve 5. Noise Spectral Density Vs. Frequency



Curve 8. Frequency Response Vs. Divider Denominator Input Voltage

ANALOG DEVICES

Internally Trimmed Integrated Circuit Divider

AD535

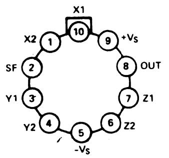
FEATURES

Pretrimmed to ±0.5% max Error, 10:1 Denominator Range (AD535K)
±2.0% max Error, 50:1 Denominator Range (AD535K)
All Inputs (X, Y and Z) Differential
Low Cost, Monolithic Construction

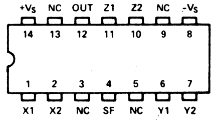
APPLICATIONS

General Analog Signal Processing
Differential Ratio and Percentage Computations
Precision AGC Loops
Square-Rooting

AD535 PIN CONFIGURATIONS



TO-100
(TOP VIEW)



TO-116
(TOP VIEW)

PRODUCT DESCRIPTION

The AD535 is a monolithic laser-trimmed two-quadrant divider having performance specifications previously found only in expensive hybrid or modular products. A maximum divider error of ±0.5% is guaranteed for the AD535K without any external trimming over a denominator range of 10:1; ±2.0% max error over a range of 50:1. A maximum error of ±1% over the 50:1 denominator range is guaranteed with the addition of two external trims. The AD535 is the first divider to offer fully differential, high impedance operation on all inputs, including the z-input, a feature which greatly increases its flexibility and ease of use. The scale factor is pretrimmed to the standard value of 10.00; by means of an external resistor, this can be reduced by any amount down to 3.

The extraordinary versatility and performance of the AD535 recommend it as the first choice in many divider and computational applications. Typical uses include square-rooting, ratio computation, "pin-cushion" correction and AGC loops. The device is packaged in a hermetically sealed, 10-pin TO-100 can or 14-pin TO-116 DIP and made available in a ±1% max error version (J) and a ±0.5% max error version (K). Both versions are specified for operation over the 0 to +70°C temperature range.

PRODUCT HIGHLIGHTS

1. Laser trimming at the wafer stage enables the AD535 to provide high accuracies without the addition of external trims (±0.5% max error over a 10:1 denominator range for the AD535K).
2. Improved accuracies over a wider denominator range are possible with only two external trims (±0.5% max error over a 20:1 denominator range for the AD535K).
3. Differential inputs on the X, Y and Z input terminals enhance the AD535's versatility as a generalized analog computational circuit.
4. Monolithic construction permits low cost and, at the same time, increased reliability.

SPECIFICATIONS (V_S = ±15V, $R_L \geq 2k\Omega$, T_A = +25°C unless otherwise stated)

PARAMETER	CONDITIONS	AD535J	AD535K
TRANSFER FUNCTION	Figure 2	$10V\frac{(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1$	*
TOTAL ERROR[1]	No External Trims, Figure 2		
	$1V \leq X \leq 10V, Z \leq \lvert X \rvert$	1.0% max	0.5% max
	$0.2V \leq X \leq 10V, Z \leq \lvert X \rvert$	5.0% max	2.0% max
	With External Trims, Figure 5		
	$0.5V \leq X \leq 10V, Z \leq \lvert X \rvert$	1.0% max	0.5% max
	$0.2V \leq X \leq 10V, Z \leq \lvert X \rvert$	2.0% max	1.0% max
TEMPERATURE COEFFICIENT	$1V \leq X \leq 10V, Z \leq \lvert X \rvert$	0.01%/°C typ	*
	$0.5V \leq X \leq 10V, Z \leq \lvert X \rvert$	0.02%/°C typ	*
	$0.2V \leq X \leq 10V, Z \leq \lvert X \rvert$	0.05%/°C typ	*
SUPPLY RELATED	$1V \leq X \leq 10V$	0.1%/V typ	*
Error	$0.5V \leq X \leq 10V$	0.2%/V typ	*
V_S = ±14V to ±16V	$0.2V \leq X \leq 10V$	0.5%/V typ	*
SQUARE ROOTER	No External Trims, Figure 11		
TOTAL ERROR[1]	$1V \leq Z \leq 10V$	0.4% typ	*
	$0.2V \leq Z \leq 10V$	0.7% typ	*
NOISE[2]	X = 0.2V, f = 10Hz to 10kHz	4.5mV rms typ	*
BANDWIDTH	X = 0.2V	20kHz typ	*
INPUT AMPLIFIERS[3]			
CMRR	f = 50Hz, 20V p-p	60dB min	*
Bias Current		2.0μA max	*
Offset Current		0.1μA typ	*
Differential Resistance		10MΩ typ	*
OUTPUT AMPLIFIER[3]			
Open-Loop Gain	f = 50Hz	70dB typ	*
Small Signal Gain-Bandwidth	V_{OUT} = 0.1V rms	1MHz typ	*
1% Amplitude Error	C_{LOAD} = 1000pF	50kHz typ	*
Output Voltage Swing	T_{min} to T_{max}	±11V min	*
Slew Rate	V_{OUT} = 20V p-p	20V/μs typ	*
Settling Time	V_{OUT} = 20V ±1%	2μs typ	*
Output Impedance	Unity Gain, $f \leq 1kHz$	0.1Ω typ	*
Wide-band Noise	f = 10Hz to 5MHz	1mV rms typ	*
	f = 10Hz to 10kHz	90μV rms typ	*
OUTPUT CURRENT	T_{min} to T_{max}, R_1 = 0	30mA max	*
POWER SUPPLIES			
Rated Performance		±15V	*
Operating		±8V min, ±18V max	*
Supply Current	Quiescent	6mA max	*
PACKAGE OPTIONS[4]			
H: TO-100		AD535JH	AD535KH
D: TO-116 Style (D14A)		AD535JD	AD535KD

NOTES:

*Specifications same as AD535J.

[1] Figures are given as a percent of full scale (i.e. 1.0% = 100mV).

[2] Noise may be reduced as shown in Figure 14.

[3] See Figure 1 for definition of section.

[4] See Section 20 for package outline information.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Internal Power Dissipation	500mW
Output Short-Circuit to Ground	Indefinite
Input Voltages, $X_1, X_2, Y_1, Y_2, Z_1, Z_2$	$\pm V_S$
Rated Operating Temp Range	0 to +70°C
Storage Temp Range	-65°C to +150°C
Lead Temp, 60s soldering	+300°C

FUNCTIONAL DESCRIPTION

Figure 1 is a functional block diagram of the AD535. Inputs are converted to differential currents by three identical voltage to current converters, each trimmed for zero offset. The product of the X and Y currents is generated by a multiplier cell using Gilbert's translinear technique with an internal scaling voltage.

The difference between XY/SF and Z is applied to the high gain output amplifier. The transfer function can then be expressed...

$$V_{OUT} = A\left[\frac{(X_1 - X_2)(Y_1 - V_{OUT})}{SF} - (Z_1 - Z_2)\right]$$

where A = open loop gain of output amplifier, typically 70dB at dc

X, Y, Z = input voltages

SF = scale factor, pretrimmed to 10.00V but adjustable by the user down to 3V.

In most cases the open loop gain can be regarded as infinite and SF will be 10V. Dividing both sides of the equation by A and solving the V_{OUT}, we get...

$$V_{OUT} = 10V\frac{(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1$$

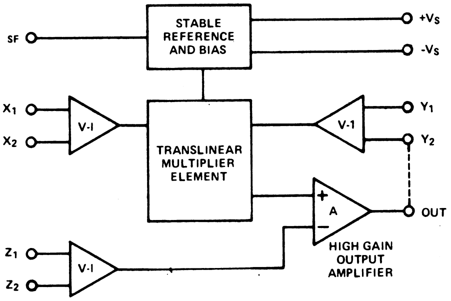

STABLE REFERENCE AND BIAS
SF
+Vs
-Vs
X1
X2
V-I
TRANSLINEAR MULTIPLIER ELEMENT
V-I
Y1
Y2
+
A
−
OUT
HIGH GAIN OUTPUT AMPLIFIER
Z1
Z2
V-I

Figure 1. AD535 Functional Block Diagram

SOURCES OF ERROR

Divider error is specified as a percent of full scale (i.e. 10.00V) and consists primarily of the effects of X, Y and Z offsets and scale factor (which are trimmable) as shown in the generalized equation....

$$V_{OUT} = (SF + \Delta SF)\left[\frac{(Z_2 - Z_1) + Z_{OS}}{(X_1 - X_2) + X_{OS}}\right] + Y_1 + Y_{OS}$$

Note especially that divider error is inversely proportional to X, that is, the error increases rapidly with decreasing denominator values. Hence, the AD535 divider error is specified over several denominator ranges on previous page. (See also Figure 12, AD535 Total Error as a function of denominator values.)

Overall accuracy of the AD535 can be significantly improved by nulling out X and Z offset as described in the applications sections. Figure 13 illustrates a factor of 2 improvement in accuracy with the addition of these external trims. The remaining errors stem primarily from scale factor error and Y offsets which can be trimmed out as shown in Figure 6.

Figure 14 illustrates the bandwidth and noise relationships versus denominator voltage. Whereas noise increases with decreasing denominator, bandwidth decreases, the net result given by the expression...

$$En_{OUT}\ (\text{wideband}) = \frac{1.26}{\sqrt{\left(\frac{X}{10}\right)}}\ \text{mV rms}$$

External filtering can be added to limit output voltage noise even further. In this case...

$$En_{OUT}\text{ (B.W. externally limited)} = \frac{0.9\sqrt{f}}{\left(\frac{X}{10}\right)}\text{ mV rms}$$

where f = bandwidth in MHz of an external filter whose bandwidth is less than the noise bandwidth of the AD535. Table 1 provides calculated values of the typical output voltage noise, both filtered and unfiltered for several denominator values.

X	Noise 10Hz to 5MHz	Noise Limited by External Filtering 10Hz to 10kHz
0.2V	8.9mV rms	4.5mV rms
0.5V	5.6mV rms	1.8mV rms
1V	4.0mV rms	0.9mV rms
10V	1.3mV rms	0.09mV rms

Table 1. AD535 Calculated Voltage Noise

APPLICATIONS

Figure 2 shows the standard divider connection without external trims. The denominator X, is restricted to positive values in this configuration. X, Y and Z inputs are differential with high (80dB typical) CMRR permitting the application of differential signals on X and Z (see Figure 3).

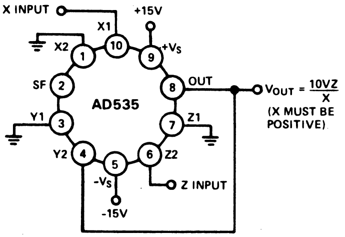


Figure 2. Divider Without External Trims

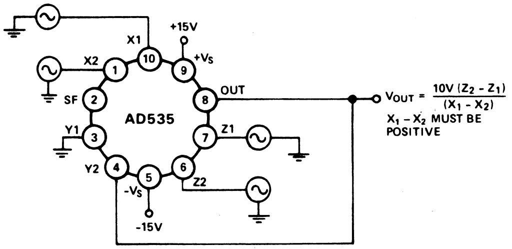

+15V
X1
X2
10
1
9
+Vs
SF
2
AD535
8
OUT
$V_{OUT} = \frac{10V(Z_2 - Z_1)}{(X_1 - X_2)}$
$X_1 - X_2$ MUST BE POSITIVE
Y1
3
7
Z1
Y2
4
5
6
Z2
-Vs
-15V

Figure 3. Differential Divider Connection

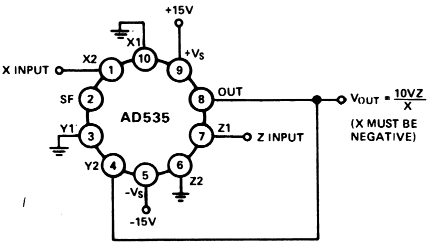


Figure 4. Divider Connection for Negative X Inputs

Negative denominator inputs are handled as shown in Figure 4. Note that in either configuration, operation is limited to two quadrants (i.e. Z is bipolar, X is unipolar).

A factor of two improvements in accuracy is possible by trimming the X and Z offsets as illustrated in Figure 5. To trim, set X to the smallest denominator value for which accurate computation is required (i.e., X = 0.2V). With Z = 0, adjust the Z_O trim for $V_{OUT} = 0$. Next, adjust the X_O trim for the best compromise when Z = +X (V_{OUT} = +10V) and Z = -X (V_{OUT} = -10V). Finally, readjust Z_O for the best compromise at Z = +X, Z = -X and Z = O. The remaining error (Figure 13) consists primarily of scale factor error, output offset and an irreducible nonlinearity component.

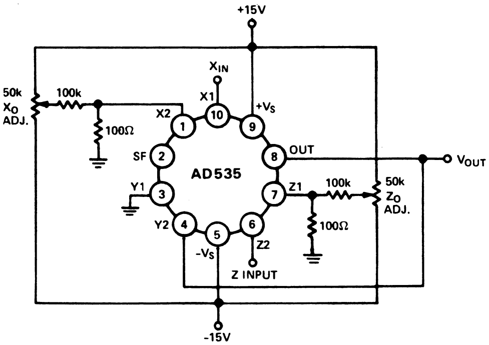


Figure 5. Precision Divider Using Two Trims

In certain applications, the user may elect to adjust SF for values between 10.00V and 3V by connecting an external resistor in series with a potentiometer between SF and $-V_S$. The approximate value of the total resistance for a given value of SF is given by the relationship:

$$R_{SF} = 5.4K\,\frac{SF}{10 - SF}$$

Due to device tolerances, allowance should be made to vary R_{SF} ±25% using the potentiometer. Note that the peak signal is always limited to 1.25 SF (i.e. ±5V for SF = 4).

The scale factor may also be adjusted using a feedback attenuator between V_{OUT} and Y2 as indicated in Figure 6. The input signal range is unaffected using this scheme.

Scale factor and output offset error can be minimized utilizing the four trim circuit of Figure 6. Adjustment is as follows:

1. Apply X = +0.2V (or the smallest required denominator value), Z = 0 and adjust Z_O for V_{OUT} = 0.
2. Apply X = 0.2V. Then adjust the X_O trim for the best compromise when Z = +X (V_{OUT} = +10V) and Z = -X (V_{OUT} = -10V.)
3. Apply X = +10V, Z = 0 and adjust Y_O for V_{OUT} = 0.
4. Apply X = +10V. Then adjust the scale factor (SF) trim for the best compromise when Z = +X (V_{OUT} = +10V) and Z = -X (V_{OUT} = -10V).
5. Repeat steps 1 and 2.
6. Apply X = 0.2V. Then adjust the Z trim for the best compromise when Z = X (V_{OUT} = +10V), Z = 0 (V_{OUT} = 0) and Z = -X (V_{OUT} = -10V).

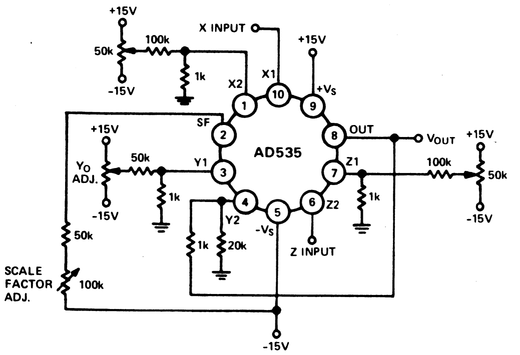


Figure 6. Precision Divider with Four External Adjustments

These trim adjustments can be made either by using two calibrated voltage sources and a DVM, or by using a differential scope, a low frequency generator, a voltage source and a precision attenuator. As shown in Figure 7, the differential scope subtracts the expected ideal output and thus displays only errors. Set the attenuation to $\frac{X}{10V}$.

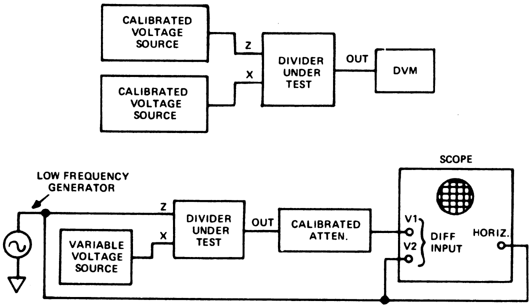


Figure 7. Alternate Trim Adjustment Set-Up

PIN-CUSHION CORRECTION

A pin-cushion corrector eliminates the distortion caused by flat screen CRT tubes. The correction equations are:

$$V_{OH} = \frac{V_{IH}}{\sqrt{V_{IH}^2 + V_{IV}^2 + L^2}}$$

and

$$V_{OV} = \frac{V_{IV}}{\sqrt{V_{IH}^2 + V_{IV}^2 + L^2}}$$

where: V_{OH} and V_{OV} are the horizontal and vertical output signals, respectively.

V_{IH} and V_{IV} are the horizontal and vertical input signals, respectively.

L is the length of the CRT tube.

In typical applications L (expressed in voltage) is roughly equal to full scale V_{IH} or V_{IV}. The result is that the expression, $\sqrt{(V_{IH}^2 + V_{IV}^2 + L^2)}$, varies less than 2:1 over the full range of values of V_{IH} and V_{IV}.

Major sources of divider error associated with small denominator values can thereby the minimized.

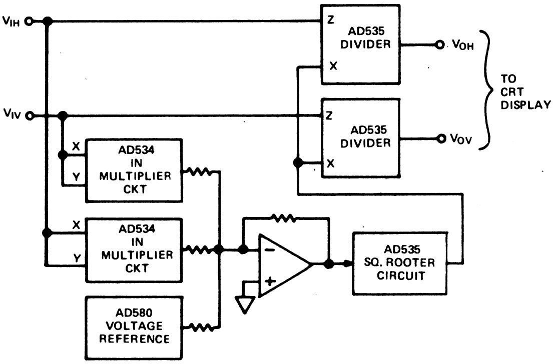


Figure 8. Pin-Cushion Corrector

Figure 9 shows an AGC loop using an AD535 divider. The AD535 lends itself naturally in this application since it is configured to provide gain rather than loss. Overall gain varies from 1 to ∞ as the denominator is servoed to maintain V_{OUT} at a constant level.

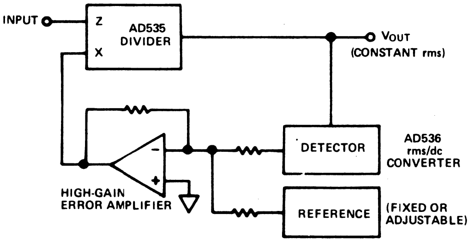


Figure 9. AGC Loop Using the AD536 rms/dc Converter as a Detector

Figure 10 shows a method for obtaining the time average as defined by:

$$\overline{X} = \frac{1}{T}\int_0^T X\,dt$$

where T is the time interval over which the average is to be taken. Conventional techniques typically provide only a crude approximation to the true time average, and furthermore, require a fixed time interval before the average can be taken. In Figure 10, the AD535 is used to divide the integrator output by the ramp generator output. Since the ramp is proportional to time, the integrator is divided by the time interval, thus allowing continuous, true time processing of signals over intervals varying by as much as 50:1.

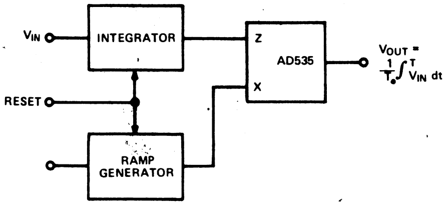


Figure 10. Time Average Computation Circuit

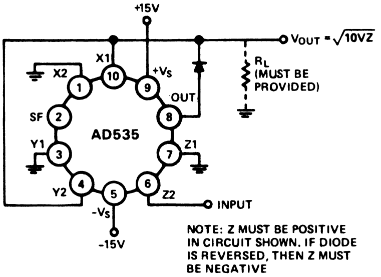

+15V
VOUT = √10VZ
X1
X2
+VS
OUT
RL (MUST BE PROVIDED)
SF
AD535
Y1
Z1
Y2
Z2
-VS
-15V
INPUT
1
2
3
4
5
6
7
8
9
10
NOTE: Z MUST BE POSITIVE IN CIRCUIT SHOWN. IF DIODE IS REVERSED, THEN Z MUST BE NEGATIVE

Figure 11. Square Rooter

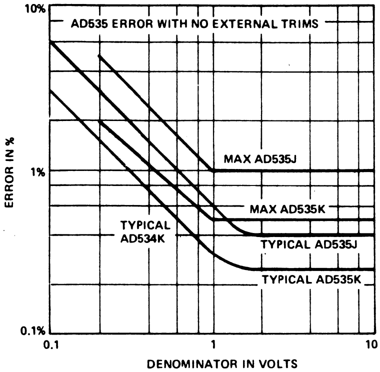


Figure 12. AD535 Error with No External Trims

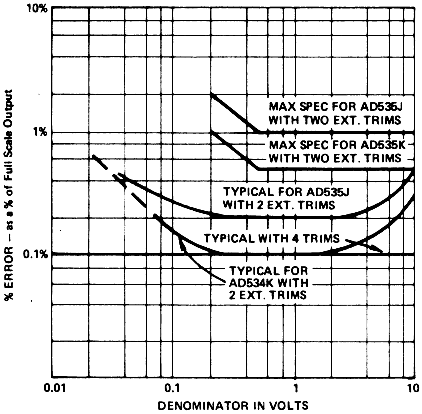


Figure 13. Errors with External Trims at 25°C

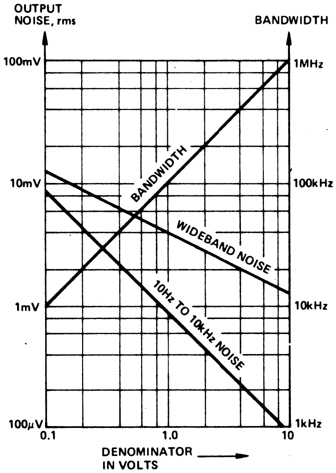


Figure 14. -3dB Bandwidth and Noise vs. Denominator

Wideband Low-Distortion Dual-Channel Two-Quadrant Log/Linear Multiplier

AD539

ADVANCE TECHNICAL DATA

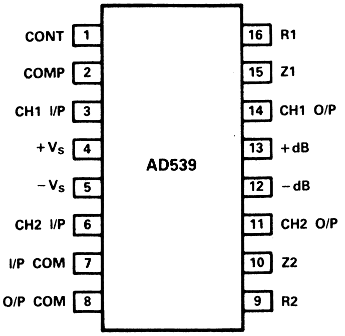
FEATURES

- **Low-Distortion Principle**
- **Two Independent Signal Channels**
- **Signal Bandwidth of 35MHz**
- **Linear Control BW of 5MHz**
- **Accurate Linear Multiplication**
- **Wide-Range (>100dB) Log Mode**

APPLICATIONS

- **Precise AGC and VCA Systems**
- **Noise Reduction Systems**
- **Distortion Analyzers**
- **Wide-Range VCOs**
- **Video Switching & Effects**
- **High-Speed Analog Division**
- **Logarithmic Signal Compression**

AD539 PIN CONFIGURATION



TO-116

PRODUCT DESCRIPTION

The AD539 is a wideband, low-distortion two quadrant multiplier intended for use in a variety of voltage-controlled amplifier and attenuator applications. It provides both linear and logarithmic control modes, with very low residual feedthrough of the signal. Two input channels are provided; these may be used independently, in which case a very high degree of channel isolation is maintained, or differentially, to achieve very low distortion and better dynamics in high-speed applications.

The AD539 also has applications in analog computation, and will be preferable to a four-quadrant multiplier in many cases, for example, where it is necessary to maintain low feedthrough of a signal when the other input is zero. It is also possible to operate each half of the AD539 as a four-quadrant multiplier if desired, thus providing much more bandwidth than previously possible from general-purpose analog multipliers. High static accuracy is ensured by the use of laser-trimmed thin-film resistors and bandgap reference generator which determine scaling.

SIGNAL CHANNELS

The input to each of the two signal channels is a voltage of nominally ±2V FS; the loading is approximately 350kΩ in parallel with 3pF. For supply voltages above the specified ±5V larger inputs (up to ±5V pk) can be tolerated with increased distortion. These inputs are with respect to the I/P COMM node (pin 7).

Each of the two signal outputs is a current of nominally ±1mA FS. This mode provides the maximum possible bandwidth and leaves the user free to choose either simple resistive loads, in which case an output swing of up to 2V pk-pk can be tolerated, or add external op-amps to provide large output swings at low-impedance. In many cases, a low-cost op-amp of modest bandwidth can be used. To facilitate the latter mode, trimmed applications resistors are provided on the chip to set the nominal scaling voltage to 1V, for example, to provide an output of 4V when both the signal and control inputs are 2V.

The intrinsic bandwidth of the signal channels (i.e., into low-impedance loads with no external active elements) is over 35MHz (rise-time 10ns) with no slew-rate limitations. The distortion depends on the drive mode and the combination of signal- and control-level; under optimum conditions of use the total harmonic distortion can be maintained below 0.05%.

LINEAR CONTROL INPUT

The linear control input is also in the voltage-mode, although it presents a rather low resistance of 500Ω to the source, a consequence of the high-speed design. The nominal full-scale control input is +3V, but linear gain response will continue for inputs up to +3.3V. Negative inputs can be accepted, but result in zero signal transmission. Recovery from overload or reverse inputs is rapid. The bandwidth of the control system is approximately 5MHz in the linear range. The control amplifier is compensated by one external capacitor which also serves to improve the HF response of the signal channel. This input is also with reference to the I/P COMM pin.

LOGARITHMIC CONTROL

Many signal-processing applications call for logarithmic control, of gain or loss. The AD539 provides this through the use of the +dB and −dB nodes (pins 12 & 13). The sensitivity is approximately 3mV/dB, and is not temperature-corrected. In many cases the linear control channel will not be needed in the logarithmic mode; in special applications, however, it can be combined with the logarithmic mode. For example, a linear perturbation of gain can be superimposed on a wide-range logarithmic control. As another example, a nonlinear control characteristic can be obtained by feeding the control signal to both the linear and logarithmic inputs.

SPECIFICATIONS (T_A @ +25°C and V_S = ±5V, unless otherwise noted)

PARAMETER	CONDITIONS	AD539	UNITS
SIGNAL INPUTS (Pins 3 & 6)			
Nominal Full Scale Input		±2	V
Peak (Clipping) Input	$-V_S > 7.5V$	±5	V
Input Resistance		350 min	kΩ
Bias Current		10	μA
Offset Voltage		5	mV
LINEAR CONTROL INPUT (Pin 1)			
Nominal Full Scale Input		+3	V
Peak (Clipping) Input		+3.3 min	V
Input Resistance		500	Ω
Offset Voltage		2	mV
Gain Linearity (V_X = +0.1V to +3.0V)		0.2	%
LOGARITHMIC CONTROL INPUTS (Pins 12 & 13)			
Assymptotic Sensitivity (High Attenuation)		3	mV/dB
Temperature Sensitivity		0.03	dB/°C
OUTPUTS (Pins 11 & 14)			
Nominal Full Scale Output Current (V_X = 3V, V_Y = 2V)		±1	mA
Source Resistance		1.25	kΩ
Scaling Resistance Z1, W1 to CH1 O/P Z2, W2 to CH2 O/P		6.25	kΩ
Voltage Outputs, V_{W1} & V_{W2} (Figure 2)			
Nominal Scaling Voltage		1.00	V
Accuracy		0.2	%
Offset Voltage		10 max	mV
Total Harmonic Distortion (Figure 2 Connections)			
(V_X = 0V to 3V, V_Y = 1V rms, 1kHz)		0.05	%
Feedthrough (V_X = 0, V_Y = 1V rms, 1kHz)		1	mV rms
(V_X = 0, V_Y = 1V rms 1MHz)		10	mV rms
(V_X = 0, V_Y = 2V rms 1kHz)		2	mV rms
(V_X = 0 to 3V, V_Y = 0, 1MHz)		20	mV rms
DYNAMIC CHARACTERISTICS			
(Outputs Loaded Directly with 50Ω to ground)			
Signal Bandwidth (V_X = 3V, V_Y = 1V rms)		35	MHz
Linear-Control Bandwidth (V_X = 1V to 2.0V, dc C_C = 3000F)		10	MHz
POWER SUPPLIES			
(Equal Positive & Negative) Range for Specified Performance			
Range for Specified Performance		4.5min	V
		7.5 max	V
Dissipation Limited (450mW at 25°C)		16 max	V
Current Consumption: $+V_S$		8.5	mA
$-V_S$		18.5	mA
TEMPERATURE RANGE			
AD539JD		0 to +70	°C
AD539SD		−55 to +125	°C
PACKAGE OPTION[1]			
16–Pin Hermetic Ceramic		D16A	

[1] See Section 20 for package outline information.

Specifications subject to change without notice.

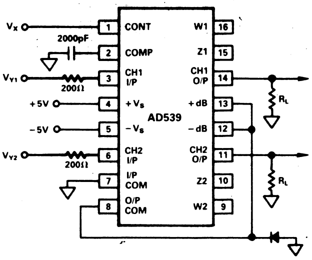


Figure 1. Minimal Configuration

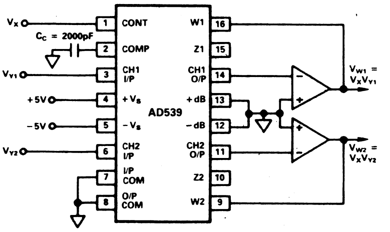


Figure 2. Linear 2-Channel Multiplication

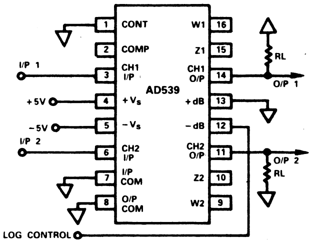


Figure 3. Minimal dB Control Configuration

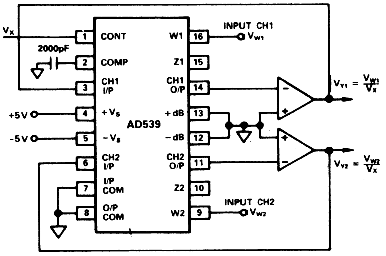


Figure 4. Two Quadrant Division

Pin #	Mnemonic	Function	Pin #	Mnemonic	Function
1	CONT	Linear-Mode CONT Input (Voltage)	9	W2	Feedback Resistor for CH2
2	COMP	HF Compensation for Control System	10	Z2	Aux. Access Resistor for CH2
3	CH1 I/P	CH1 Signal Input (Voltage)	11	CH2 O/P	CH 2 Signal Output (Current)
4	$+V_S$	Positive Supply	12	−dB	Decrementing dB Control Input
5	$-V_S$	Negative Supply	13	+dB	Incrementing dB Control Input
6	CH2 I/P	CH2 Signal Input (Voltage)	14	CH1 O/P	CH1 Signal Output (Current)
7	I/P COM	Analog Ground for Inputs	15	Z1	Aux. Access Resistor for CH1
8	O/P COM	Analog Ground for Outputs	16	W1	Feedback Resistor for CH1

Table 1. Pin Function Description

ANALOG DEVICES

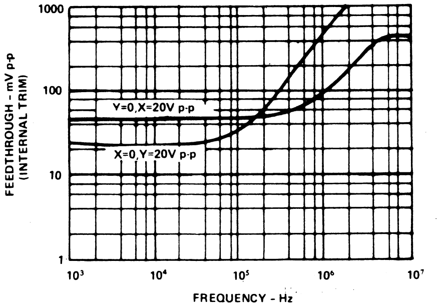
Accurate, Wideband, Multiplier, Divider, Square Rooter

MODEL 429

FEATURES:
- **1.0%/0.5% Accuracy without Trimming (429A/B)**
- **Low Drift to 1.0mV/°C max**
- **Wideband – 10MHz**
- **0.2% Nonlinearity max (429B)**
- **External Amplifiers not Required**
- **MTBF: 169, 268 Hours**

APPLICATIONS:
- **Fast Divider**
- **Modulation and Demodulation**
- **Phase Detection**
- **Instrumentation Calculations**
- **Analog Computer Functions**
- **Adaptive Process Control**
- **Trigonometric Computations**

FEEDTHROUGH VS. FREQUENCY



GENERAL DESCRIPTION

The model 429, an extremely fast multiplier/divider, should be considered if bandwidth, temperature coefficient, or accuracy are critical parameters. Based on the transconductance principle to achieve high speed, the model 429 offers a unique combination of features, those being ½% max error (429B) and 10MHz small signal bandwidth.

Both models 429A and 429B are internally trimmed achieving max errors of 1.0% and 0.5% respectively. By fine trimming the offset and feedthrough with external trim potentiometers typical performance may be improved to 0.5% for the 429A and 0.2% for the 429B.

In addition to high accuracy and high bandwidth, the model 429 offers exceptionally good stability for changes in ambient temperature. Model 429B is 100% temperature tested in order to guarantee an overall accuracy temperature coefficient of only 0.04%/°C max. Additionally, offset drift is held to only 1mV/°C max. To satisfy OEM requirements of low cost, the 429 uses transconductance principles with the latest design techniques and components to achieve guaranteed performance at competitive prices.

MULTIPLICATION ACCURACY

Multiplication accuracy is generally specified as a percentage of full scale output. This implies that error is independent of signal level. However, for signal levels less than 2/3 of full scale, error tends to decrease roughly in proportion to the input signal. A good approximation of error behavior is:

$f(X, Y) \cong |X|\,\epsilon_x + |Y|\,\epsilon_y$, where ϵ_x and ϵ_y are the fractional nonlinearities specified for the X and Y inputs

EXAMPLE: For model 429A, $\epsilon_x = 0.5\%$, $\epsilon_y = 0.3\%$. What maximum error can one expect for $x = 5V$, $y = 1V$, providing the offset is zeroed out? Can one get less by interchanging inputs?

1. Nominal output is XY/10 = (5)(1)/10 = 500mV
2. Expected error is (5) (0.5%) + (1) (0.3%) = 28mV, 5.6% of output (0.28% of F.S.)
3. Interchanging inputs (1) (0.5%) + (5) (0.3%) = 20mV, 4.0% of output (0.20% of F.S.)

Compare this with the overly conservative error predicted by the overall 1% of full scale specification: 100mV, or 20% of output.

FREQUENCY RELATED SPECIFICATIONS

Accuracy, and its components, feedthrough, linearity, gain, (and phase shift) are frequency dependent. Feedthrough is constant up to 100kHz for the Y input, and up to 400kHz for the X input. Beyond these frequencies it rises at approximately a 6dB/octave rate due to distributed capacitive coupling.

This two-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be found in Volume II, page 6-7.

SPECIFICATIONS (typical @ +25°C and ±15VDC unless otherwise noted)

MODEL	429A	429B
MULTIPLICATION CHARACTERISTICS		
Output Function	XY/10	*
Error, with Internal Trim, at +25°C	±1% max	±0.5% max
Error, with External Trim, at +25°C	±0.7%	±0.3%
Avg. vs. Temp (-25°C to +85°C)	±0.05%/°C	±0.04%/°C max
Avg vs. Supply	±0.05%/%	*
SCALE FACTOR		
Initial Error at +25°C	0.5%	0.25%
Avg vs. Temp (-25°C to +85°C)	0.03%/°C	0.02%/°C
Avg vs. Supply	0.03%/%	*
OUTPUT OFFSET		
Initial at +25°C (Adjustable to Zero)	±20mV max	±10mV max
Avg vs. Temp (-25°C to +85°C)	±2mV/°C	±1mV/°C max
Avg vs. Supply	±1mV/%	*
NONLINEARITY		
X Input		
(X = 20V p-p 50Hz, Y = ±10V)	0.5% max	0.2% max
Y Input		
(Y = 20V p-p 50Hz, X = ±10V)	0.3% max	0.2% max
FEEDTHROUGH		
X = 0, Y = 20V p-p, 50Hz	50mV p-p, max	20mV p-p, max
With External Trim	16mV p-p	10mV p-p
Y = 0, X = 20V p-p, 50Hz	100mV p-p, max	30mV p-p, max
With External Trim	50mV p-p	20mV p-p
BANDWIDTH		
-3dB	10MHz	*
Full Power Response	2MHz min	*
Slew Rate	120V/μs min	*
1% Amplitude Error	300kHz min	*
1% Vector Error (0.57°)	50kHz min	*
Differential Phase Shift ($\theta_x - \theta_y$)	1° @ 1MHz	*
Small Signal Rise Time 10-90%	40ns	*
Settling to ±1% (±10V step)	500ns	*
Overload Recovery	0.2μs	*
OUTPUT NOISE		
5Hz to 10kHz	0.6mV rms	*
5Hz to 10MHz	3.0mV rms	*
OUTPUT CHARACTERISTICS		
Voltage, 1kΩ load	±11V min	*
Current	±11mA min	*
Load Capacitance	0.01μF max	*
INPUT RESISTANCE		
X Input	10kΩ±5%	*
Y Input	11kΩ±2%	*
Z Input	27kΩ±10%	*
INPUT BIAS CURRENT		
Input X, Y, Z	±100nA	*
Z	±20μA	*
MAXIMUM INPUT VOLTAGE		
For Rated Accuracy	±10.5V	*
Maximum Safe	±16V	*
WARM UP		
To Rated Specifications	1 second	*
POWER SUPPLY[1]		
Rated Performance	±(14.8 to 15.3)V dc	*
Operating	±(14 to 16)V dc	*
Quiescent Current	±12mA	*
TEMPERATURE RANGE		
Rated Performance	-25°C to +85°C	*
Operating	-25°C to +85°C	*
Storage	-55°C to +125°C	*
MECHANICAL		
Weight	2 oz.	*
Socket	AC1023	*
Case Dimensions	1.5" x 1.5" x 0.62"	*

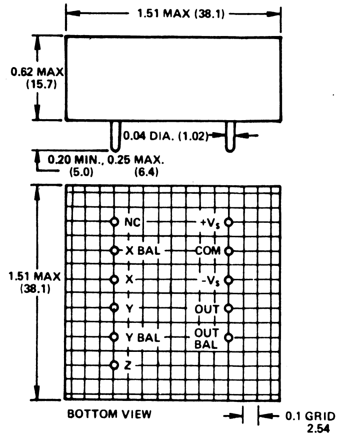
***Specifications same as model 429A.**

[1] Recommended power supply, ADI model 904, ±15V @ 50mA output.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

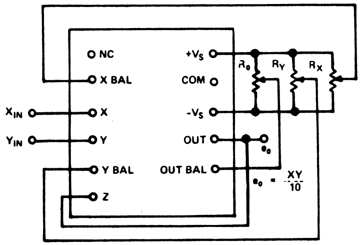
Dimensions shown in inches and (mm).



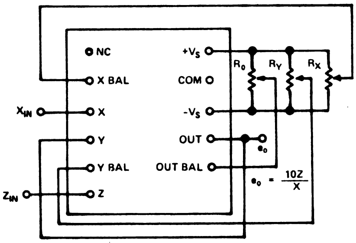
PIN CONNECTIONS

Bottom View Shown in all Figures.
Optional Trim Pots
Shown are not Required
for Rated Accuracy.

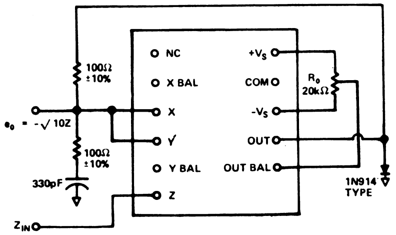
MULTIPLY MODE



DIVIDE MODE



SQUARE ROOT MODE



All trim pots 20kΩ.

ANALOG DEVICES

Programmable Multifunction Module

MODEL 433

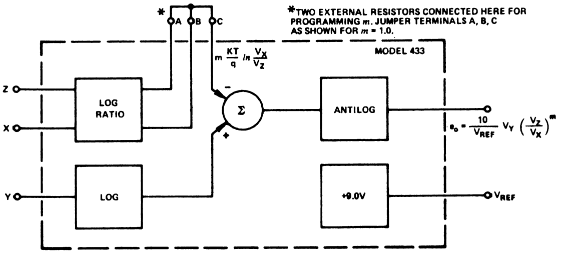
FEATURES

- **Versatility: Provides Transfer Characteristics of Several Function Modules**
- **Divides Over a 100:1 Range With a Max Error of 0.25% (433B)**
- **Internal Voltage Reference**
- **Hermetically Sealed Semiconductors**
- **No External Trims Required**
- **Low Cost**

APPLICATIONS

- **Transducer Linearization**
- **Signal Processing**
- **Raising to Arbitrary Powers**
- **Vector Functions**
- **Trigonometric Functions (Sine, Cosine, Arctangent)**

MODEL 433 FUNCTIONAL BLOCK DIAGRAM


*
A
B
C
MODEL 433
$m \frac{KT}{q} \ln \frac{V_X}{V_Z}$
Z
X
Y
LOG RATIO
LOG
Σ
−
+
ANTILOG
+9.0V
$e_o = \frac{10}{V_{REF}} V_Y \left(\frac{V_Z}{V_X}\right)^m$
V_{REF}

*TWO EXTERNAL RESISTORS CONNECTED HERE FOR PROGRAMMING *m*. JUMPER TERMINALS A, B, C AS SHOWN FOR *m* = 1.0.

GENERAL DESCRIPTION

The model 433 is an extremely versatile function module which implements the transfer function:

$$e_o = \frac{10}{V_{REF}} V_y \left(\frac{V_z}{V_x}\right)^m, \ 0.2 \leqslant m \leqslant 5.0$$

$V_{REF} = +9.0$ Volts

By either jumper connections on the pins, or selection of two external resistors the user can program the 433 to: multiply, divide, square, square root, root of a ratio, square of a ratio, or raise voltage ratios to an arbitrary power, *m*.

When used with a low cost op amp, such as AD741, the model 433 may be used to compute the true rms value of a varying signal. With two such op amps, the 433 can be used to perform accurate vector computations over wide ranges of the vector sum.

Due to its log/antilog circuit approach, signal levels of 100mV to 10V may be processed with a maximum output error of 0.25% F.S. (433B). The allowable input range for the three input variables is 0.01 to +10V, for which there is a typical error of ±5mV ±0.3% of the theoretical output voltage for model 433J, and ±1mV ±0.15% for 433B.

Because of its small size, accuracy, versatility, and speed (and all at low cost), the model 433 will prove to be an essential component in equipment requiring on-the-spot computations in real time, or for linearizing a wide range of transducer characteristics in medical, industrial, and process control equipment. Designed with the OEM's needs in mind, the model 433 is attractively priced for new equipment designs.

PRINCIPLE OF OPERATION

The model 433 is comprised of log and antilog circuits interconnected as shown in the Functional Block Diagram. The log ratio circuit provides the log of V_X/V_Z to terminals A, B, C where, for exponents other than unity, it is scaled by two external programming resistors (see hook-up diagrams for connection and values of these two resistors). The scaled log ratio from terminal C is subtracted from a signal proportional to the log of V_y. The resulting expression is operated on by the antilog circuit, yielding an output of

$$e_o = \frac{10}{V_{REF}} V_y \left(\frac{V_z}{V_x}\right)^m, \ V_{REF} = +9.0 \text{ Volts}$$

The voltage reference circuit is a high stability (0.005%/°C) voltage source which is generated internally. It is provided as an output terminal for user convenience, and may be used as a constant at any of the input terminals.

ONE-QUADRANT DIVIDER

When connected as a divider, the model 433B has less than ¼% output error over an input signal range of 100:1. This performance is obtained with no external trims, and is nearly twenty times better than that attainable with a 0.1% multiplier/divider connected in a feedback loop.

This two-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be found in Volume II, page 6-11.

SPECIFICATIONS (typical @ +25°C and ±15V unless otherwise noted)

Model	433J	433B
Transfer Function	$e_o = +\frac{10}{V_{REF}} V_y \left(\frac{V_z}{V_x}\right)^m$	*
Reference Terminal Voltage[1]		
V_{REF} (Internal Source)	+9.0V ±5% @ 1mA	*
vs Temp. Rated	±0.005%/°C	*
Rated Output[1]	+10.5V @ 5mA, min	*
Input		
Signal Range	$0 \leq V_x, V_y, V_z \leq +10V$,	*
Max Safe Input	$V_x, V_y, V_z \leq \pm 18V$	*
Resistance		
X Terminal	100kΩ ±1%	*
Y Terminal	90kΩ ±10%	*
Z Terminal	100kΩ ±1%	*
External Adjustment of the Exponent, m		
Range for m <1 (Root)	$1/5 \leq m < 1,\ m = \frac{R_2}{R_1 + R_2}$	*
Range for m > 1 (Power)	$1 \leq m < 5,\ m = \frac{R_1 + R_2}{R_2}$	*
	$(R_1 + R_2) \leq 200\Omega$	*
Accuracy (Divide Mode, m = 1, $V_y = V_{REF}$)[2,3]		
Total Output Error @ +25°C (for specified input range)		
Typical (RTO)	±5mV ±0.3% of output	±1mV ±0.15% of output
Max Error (RTO)	±50mV	±25mV
Input Range ($V_z \leq V_x$)	0.01V to 10V, V_z	*
	0.1V to 10V, V_x	*
Over Specified Temp. Range	±1%	±1% max
Output Offset Voltage (Not Adjustable)		
Initial @ +25°C	±5mV	±2mV max
Offset vs Temp.	±1mV/°C	±1mV/°C max
Noise, 10Hz to 1kHz		
$V_x = +10V$	100μV rms	*
$V_x = +0.1V$	500μV rms	*
Bandwidth, V_y, V_z		
Small Signal (-3dB), 10% of dc Level	V_y or V_z	*
$V_y = V_z = V_x = 10V$	100kHz	*
$V_y = V_z = V_x = 1V$	20kHz	*
$V_y = V_z = V_x = 0.1V$	1kHz	*
$V_y = V_z = V_x = 0.01V$	400Hz	*
Full Output (V_y or V_z = 5V dc, ±5V ac)	(V_x) x (5kHz)	*
Power Supply Range		
Rated Performance	±15V dc @ 10mA	*
Operating	±(12 to 18)V dc	*
Temperature Range		
Rated Performance	0 to +70°C	-25°C to +85°C
Storage	-55°C to +125°C	-55°C to +125°C
Mechanical		
Case Size	1.5" x 1.5" x 0.62"	*
Mating Socket	AC1038	*

*Same specifications as 433J.

[1] Terminals short circuit protected to ground.

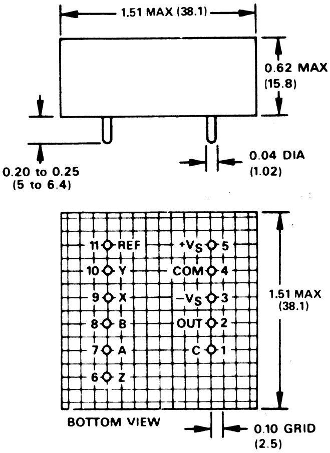
[2] Accuracy is specified in divide mode. Input range is 10mV to 10V for specified accuracy when connected as a multiplier.

[3] Error is defined as the difference between the measured output and the theoretical output for any given pair of specified input voltages.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

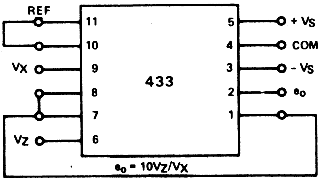
Dimensions shown in inches and (mm).



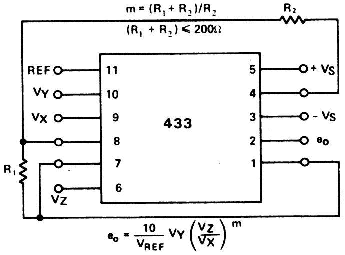
Mating Socket AC1038

WIRING CONNECTIONS
Bottom View Shown in All Cases

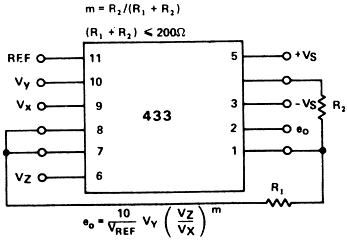
DIVIDE MODE (m = 1, $V_y = V_{REF}$)



POWERS m ⩾ 1



ROOTS m ⩽ 1



ANALOG DEVICES

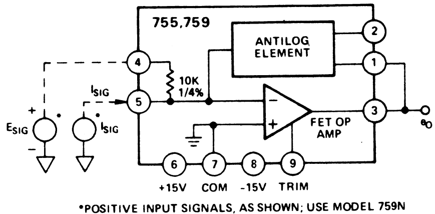
6-Decade, High Accuracy and Wideband Log, Antilog Amplifiers

MODELS 755N, 755P, 759N, 759P

FEATURES

- High Accuracy: Models 755N, 755P
- Wideband: Models 759N, 759P
- Complete Log/Antilog Amplifiers: External Components Not Required
- Temperature-Compensated Internal Reference
- 6 Decades Current Operation: 1nA to 1mA
- 1% max Error: 1nA to 1mA (755)
  - 20nA to 200μA (759)
- 4 Decades Voltage Operation: 1mV to 10V
- 1% max Error: 1mV to 10V (755)
  - 1mV to 2V (759)
- Small Size: 1.1" X 1.1" X 0.4"

MODELS 755, 759 FUNCTIONAL BLOCK DIAGRAM



*POSITIVE INPUT SIGNALS, AS SHOWN; USE MODEL 759N
NEGATIVE INPUT SIGNALS, USE MODEL 759P

GENERAL DESCRIPTION

The models 755N, 755P and 759N, 759P are low cost dc logarithmic amplifiers offering conformance to ideal log operation over 6 decades of current (1nA to 1mA) and 4 decades of voltage (1mV to 10V). For high accuracy requirements, models 755N, 755P offer maximum nonconformity of 0.5%, from 10nA to 1mA, and 1mV to 1V. For wideband applications, the models 759N, 759P provide fast response (300kHz @ I_{SIG} = 10μA to 1mA) and feature maximum nonconformity of 1% from 20nA to 200μA, and 1mV to 2V. The models 755N and 759N compute the log of positive (+) input signals, while the models 755P, 759P compute the log of negative (−) signals.

Designed for ease of use, the models 755N/P and 759N/P are complete, temperature compensated log/antilog amplifiers packaged in a compact epoxy-encapsulated module. External components are not required for logging currents over the complete 6 decade range of 1μA to 1mA. Both the scale factor (K=2, 1, or 2/3 volt/decade) and log/antilog operation are selected by simple pin connection. In addition, both the internal 10μA reference current as well as the offset voltage may be externally adjusted to improve overall accuracy.

The models 755 and 759 are ideally suited as an alternative to in-house designs of OEM applications. Advanced design techniques and superior performance place the 755 and 759 ahead of competitive designs in terms of price, performance and package design.

APPLICATIONS

When connected in the current or voltage logging configuration, as shown in Figure 1, the models 755 and 759 may be used in several key applications. A plot of input current versus output voltage is also presented to illustrate the log amplifier's transfer characteristics.

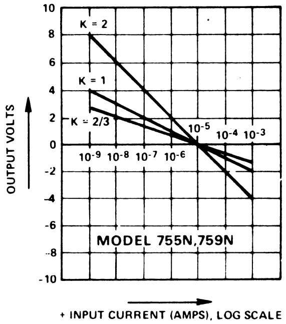


Figure 1. Transfer Function

This two-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be found in Volume II, page 8-7.

SPECIFICATIONS (typical @ +25°C and ±15V dc unless otherwise noted)

MODEL	755N/P	759N/P
TRANSFER FUNCTIONS		
Current Mode	$e_O = -K\log_{10}\frac{I_{SIG}}{I_{REF}}$	•
Voltage Mode	$e_O = -K\log_{10}\frac{E_{SIG}}{E_{REF}}$	•
Antilog Mode	$e_O = E_{REF}\ 10^{-\left(\frac{E_{SIG}}{K}\right)}$	•
TRANSFER FUNCTION PARAMETERS		
Scale Factor (K) Selections[1, 2]	2, 1, 2/3 Volt/Decade	•
Error @ +25°C	±1% max	•
vs. Temperature (0 to +70°C)	±0.04%/°C max	•
Reference Voltage (E_{REF})[2]	0.1V	•
Error @ +25°C	±3% max	±4% max
vs. Temperature (0 to +70°C)	±0.1%/°C max	±0.05%/°C
Reference Current (I_{REF})[2]	10μA	•
Error @ +25°C	±3% max	•
vs. Temperature (0 to +70°C)	±0.1%/°C max	

MAXIMUM LOG CONFORMITY ERROR

I_{SIG} RANGE	E_{SIG} RANGE	RTI	RTO (K=1)	RTI	RTO (K=1)
1nA to 10nA	–	±1%	±4.3mV	±5%	±21mV
10nA to 20nA	–	±0.5%	±2.17mV	±2%	±8.64mV
20nA to 100μA	1mV to 1V	±0.5%	±2.17mV	±1%	±4.3mV
100μA to 200μA	1V to 2V	±1%	±4.3mV	±1%	±4.3mV
200μA to 1mA	2V to 10V	±1%	±4.3mV	±2%	±8.64mV

INPUT SPECIFICATIONS		
Current Signal Range		
Model 755N, 759N	+1nA to +1mA min	•
Model 755P, 759P	-1nA to -1mA min	•
Max Safe Input Current	±10mA max	•
Bias Current @ +25°C	(0, +) 10pA max	(0, +) 200pA max
vs. Temperature (0 to +70°C)	x2/+10°C	•
Voltage Signal Range (Log Mode)		
Model 755N, 759N	+1mV to +10V min	•
Model 755P, 759P	-1mV to -10V min	•
Voltage Signal Range, Antilog Mode Model 755N, 755P	$-2 \leq \frac{E_{SIG}}{K} \leq 2$	•
Offset Voltage @ +25°C (Adjustable to 0)	±400μV max	±2mV max
vs. Temperature (0 to +70°C)	±15μV/°C max	±10μV/°C
vs. Supply Voltage	±15μV/%	•
FREQUENCY RESPONSE, Sinewave		
Small Signal Bandwidth, -3dB		
I_{SIG} = 1nA	80Hz	250Hz
I_{SIG} = 1μA	10kHz	100kHz
I_{SIG} = 10μA	40kHz	200kHz
I_{SIG} = 1mA	100kHz	200kHz
RISE TIME		
Increasing Input Current		
10nA to 100nA	100μs	20μs
100nA to 1μA	7μs	3μs
1μA to 1mA	4μs	2.5μs
Decreasing Input Current		
1mA to 1μA	7μs	3μs
1μA to 100nA	30μs	10μs
100nA to 10nA	400μs	80μs
INPUT NOISE		
Voltage, 10Hz to 10kHz	2μV rms	10μV rms
Current, 10Hz to 10kHz	2pA rms	10pA rms
OUTPUT SPECIFICATIONS[3]		
Rated Output		
Voltage	±10V min	•
Current		
Log Mode	±5mA	•
Antilog Mode	±4mA	•
Resistance	0.5Ω	•
POWER SUPPLY[4]		
Rated Performance	±15Vdc	•
Operating	±(12 to 18)Vdc	•
Current, Quiescent	±7mA	±4mA
TEMPERATURE RANGE		
Rated Performance	0 to +70°C	•
Operating	-25°C to +85°C	•
Storage	-55°C to +125°C	•
CASE SIZE[5] (W x L x H)	1.5" x 1.5" x 0.4" (38 x 38 x 10.4)	1.125" x 1.125" x 0.4" (29 x 29 x 10.4)

---

[1] Use terminal 1 for K = 1V/decade; terminal 2 for K = 2V/decade; terminals 1 or 2 (shorted together) for K = 2/3V/decade.

[2] Specification is + for models 755N, 759N; – for 755P, 759P.

[3] No damage due to any pin being shorted to ground.

[4] Recommended power supply, model 904, ±15V @ ±50mA output.

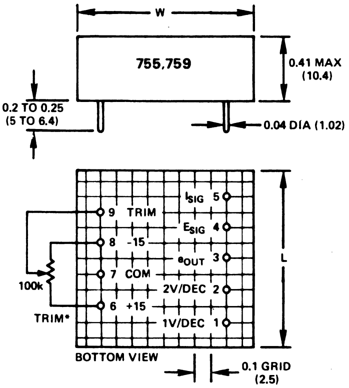
[5] Case size in inches (mm).

•Specifications same as 755N/P.

Specifications subject to change without notice.

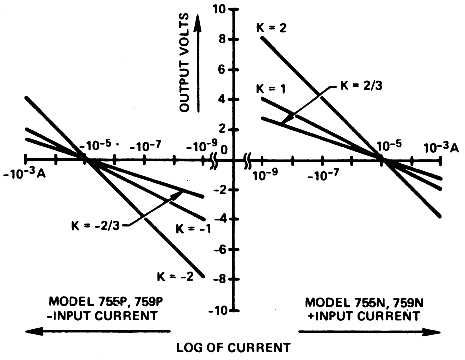
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

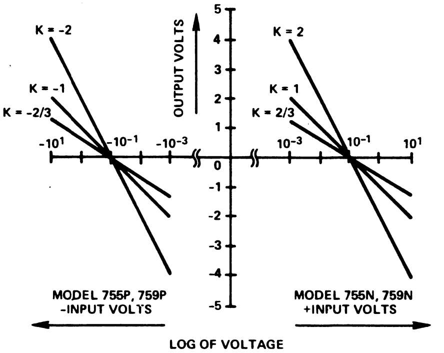


*Optional 100kΩ external trim pot. Input offset voltage may be adjusted to zero with trim pot connected as shown. With trim terminal 9 left open, input offset voltage will be ±0.4mV (755) or ±2mV (759) maximum.

MATING SOCKET AC1016



Plot of Output Voltage vs Input Current for Model 755 Connected in the Log Mode



Plot of Output Voltage vs Input Voltage for Models 755, 759 Connected in the Log Mode

Figure 2. Transfer Curves

ANALOG DEVICES

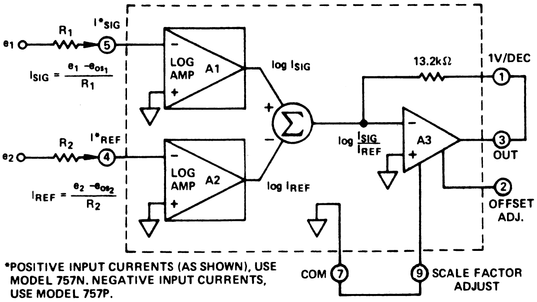
6-Decade, High Accuracy Log Ratio Amplifiers

MODEL 757N, 757P

FEATURES
- 6 Decade Operation – 1nA to 1mA
- 1/2% Log Conformity – 10nA to 100µA
- Symmetrical FET Inputs
- Voltage or Current Operation
- Temperature Compensated

APPLICATIONS
- Absorbence Measurements
- Log Ratios of Voltages or Currents
- Data Compression
- Transducer Linearization

757N, 757P FUNCTIONAL BLOCK DIAGRAM



*POSITIVE INPUT CURRENTS (AS SHOWN), USE MODEL 757N. NEGATIVE INPUT CURRENTS, USE MODEL 757P.

GENERAL DESCRIPTION

Model 757 is a complete, temperature compensated, dc-coupled log ratio amplifier. It is comprised of two input channels for processing signals spanning up to 6 decades in dynamic range (1nA to 1mA). By virtue of its symmetrical FET input stages, the 757 can accommodate this 6 decade signal range at either channel. Log conformity is maintained to within 1/2% over 4 decades of input (10nA to 100µA) and to within 1% over the full input range. Unlike other log ratio designs, model 757 does not restrict the relative magnitude of the two signal inputs to achieve rated performance. Either input can be operated within the specified range regardless of the signal level at the other channel.

The model 757 log-ratio amplifier design makes available both input amplifier summing junctions. As a result, it can directly interface with photo diodes operating in the short-circuit current mode without the need of additional input circuitry.

The excellent performance of model 757 can be further improved by means of external scale factor and output offset adjustments. A significant feature of model 757 not found on competing devices is that, when the offset adjustment is used to establish a fixed bias at the output, the output offset level does not vary as a function of input signal magnitude. On other designs, the sensitivity of output offset to input levels results in output effects resembling log conformity errors.

Model 757 can operate with either current or voltage inputs. Its excellent performance makes it ideally suited for log ratio applications such as blood analysis, chromatography, chemical analysis of liquids and absorbence measurements.

CURRENT LOG RATIO

Current log ratio is accomplished by model 757 when two currents, I_{SIG} and I_{REF}, are applied directly to the input terminals (see Functional Diagram). The two log amps process these signals providing voltages which are proportional to the log of their respective inputs. These voltages are then subtracted and applied to an output amplifier. The scale factor, when connected as shown, is 1V/dec. However, higher scale factors may be achieved by connecting external scale factor adjusting resistors.

VOLTAGE LOG RATIO

The principle of operation for voltage log ratio is identical to that of current log ratio after the voltage signal has been converted to a current. To accomplish this conversion, an external resistor is attached from the voltage signal to the appropriate input current terminal of the 757. Input currents are then determined by:

$$I_{SIG} = \frac{e_1 - e_{os_1}}{R_1}, \quad I_{REF} = \frac{e_2 - e_{os_2}}{R_2}$$

e_{os_1} = Input Offset Voltage (I_{SIG} Channel)

e_{os_2} = Input Offset Voltage (I_{REF} Channel)

This two-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be found in Volume II, page 8-11.

SPECIFICATIONS (typical @ +25°C and V_S = ±15V dc unless otherwise noted)

MODEL	757N/P
TRANSFER FUNCTION [1]	
Current Mode	$e_o = -K \log_{10} \frac{I_{SIG}}{I_{REF}}$
Voltage Mode	$e_o = -K \log_{10} \left[\frac{(e_1 - e_{os_1})}{(e_2 - e_{os_2})} \times \frac{R_2}{R_1} \right]$
ACCURACY	
Log Conformity[2]	
I_{SIG}, I_{REF} = 10nA to 100µA	±0.5%, max
I_{SIG}, I_{REF} = 1nA to 1mA	±1%, max
Scale Factor (1V/Dec)	(+0, -2%) max
vs. Temperature (0 to +70°C)	±0.04%/°C max
INPUT SPECIFICATIONS – Both Input Channels	
Current	
Signal Range, Rated Performance	
Model 757N	+1nA to +1mA min
Model 757P	-1nA to -1mA min
Max Safe	±10mA max
Bias Current, @ +25°C	(0, +) 10pA max
vs. Temperature (0 to +70°C)	x2/+10°C
Offset Voltage, @ +25°C	±1mV max
vs. Temperature (0 to +70°C)	
I_{SIG} Channel	±25µV/°C max
I_{REF} Channel	±25µV/°C max
vs. Supply Voltage	±5µV/%
FREQUENCY RESPONSE, Sinewave	
Small Signal Response (-3dB)	
Signal Channel	
I_{SIG} = 1nA	250Hz
I_{SIG} = 1µA	25kHz
I_{SIG} = 100µA	40kHz
Reference Channel	
I_{REF} = 1nA	100Hz
I_{REF} = 1µA	25kHz
I_{REF} = 100µA	40kHz

RISE TIME	Signal Channel (I_{REF} = 10µA)	Reference Channel (I_{SIG} = 10µA)
Increasing Input Current		
1nA to 10nA	250µs	80µs
10nA to 100nA	50µs	40µs
100nA to 1µA	30µs	30µs
1µA to 100µA	25µs	25µs
Decreasing Input Current		
100µA to 1µA	25µs	25µs
1µA to 100nA	30µs	30µs
100nA to 10nA	100µs	40µs
10nA to 1nA	600µs	70µs

INPUT NOISE	
Voltage (10Hz to 10kHz)	3µV rms
Current (10Hz to 10kHz)	0.1pA rms
OUTPUT SPECIFICATIONS	
Rated Output	
Voltage	±10V min
Current	±5mA min
Resistance	0.1Ω
Offset Voltage[3] (K = 1V/Decade)	±15mV max
vs. Temperature (0 to +70°C)	±0.3mV/°C
vs. Supply	±5µV/V
POWER SUPPLY[4]	
Rated Performance	±15V dc
Operating	±(12 to 18)V dc
Current, Quiescent	±8mA
TEMPERATURE RANGE	
Rated Performance	0 to +70°C
Operating	-25°C to +85°C
Storage	-55°C to +125°C
MECHANICAL	
Case Size	1.5" x 1.5" x 0.4"
Weight	21 grams

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[1] For model 757N, K = +1V/Decade and input currents must be positive. For model 757P, K = -1V/Decade and input currents must be negative. (Input currents are defined as positive when flowing into the input terminals, 4 and 5. Refer to TRANSFER CURVES.)

[2] The log conformity error is referred to input (RTI). 1% error RTI is equivalent to 4.3mV of error at the output for K = 1V/Dec.

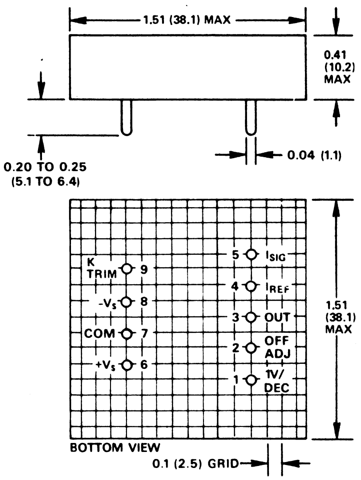
[3] Externally adjustable to zero.

[4] Recommended power supply: Analog Devices model 904, ±15V @ 50mA.

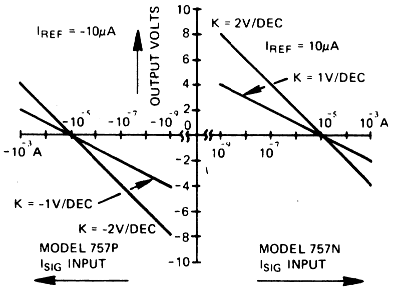
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



TRANSFER CURVES



Log mode output voltage vs. input current for I_{REF} = 10µA.

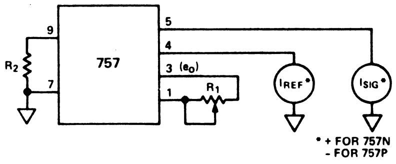


Figure 1. Scale Factor Adjustment

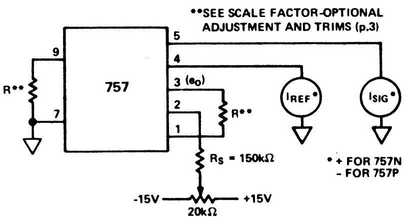


Figure 2. Output Voltage Offset Adjustments

RMS-to-DC Converters

Contents

Page

Selection Guide 7-3

General Information and Definitions of Specifications 7-4

AD536AJ/AK/AS Integrated Circuit True rms-to-dc Converter 7-7

●AD636J/K Low Level True rms-to-dc Converter 7-13

442J/K/L Wideband, High Accuracy True rms-to-dc Converter 7-19

●New product since *1980 Data-Acquisition Components and Subsystems Catalog*

Selection Guide

RMS-to-DC Converters

Model	Characteristics	Vol I Page	Vol II Page
AD536AJ/AK/AS	Monolithic IC rms/dB converter. Laser-wafer-trimmed for total max error ±2mV ±0.2% of reading (AD536AK), sine waves at 1kHz (20kHz typ), 0 to 7V rms. Crest factor of 7 for 1% additional error. ±3dB bandwidth 2MHz ($1V < V_{IN} \leqslant 7V$). Averaging time constant per μF of C_{ext}, 25ms/μF. Total-error tempco (±50μV ±0.005% rdg)/°C max (AK). Additional features include dB output with 60dB range, single-or dual-supply operation, and low power consumption – 1mA. AD536AJ/K are specified for 0 to +70°C, AD536AS for -55°C to +125°C.	7-7	–
AD636J/K	Monolithic IC rms/dB converter. Laser-wafer-trimmed for total max error ±0.2mV ±0.5% of reading (AD636K), 0 to 200mV rms. Crest factor of 6 for 0.5% additional error. ±3dB bandwidth 1.3MHz (200mV). Averaging time constant per μF of C_{ext}, 25ms/μF. Total-error tempco (±0.1μV ±0.005% rdg/°C) max. Additional features include dB output with 60dB range, single-or dual-supply operation, and low power consumption – 1mA.	7-13	–
442	A high performance true rms/dc converter featuring 8MHz bandwidth, low drift to ±3.5μV/°C ±0.01% of reading/°C maximum, and ±1% of reading error to 800kHz.	7-19	7-7

Orientation

RMS-to-DC Converters

The devices catalogued here are high-accuracy true-rms-to-dc-conversion ICs. Devices of this class compute the instantaneous square of the input signal, average it, and take the square root of the result, to provide a dc voltage that is proportional to the rms of the input and, in the case of the AD536A, AD636, an auxiliary dc voltage that is proportional to the *log* of the rms, for dB measurements.

Excellent pre-trimmed performance, improvable by simple optional trims, makes these devices ideal for all types of laboratory and OEM rms instrumentation where amplitude measurements must be made with high accuracy, independently of waveshape.

An alternative to rms that has been widely used in the past, principally for measurements on sine waves, is mean absolute-deviation, or "ac average." It is performed by taking the absolute value of (i.e., full-wave or half-wave rectifying) a signal, filtering it, and scaling it by the ratio of rms to m.a.d. for sine waves, 1.111, so that it reads correctly (for undistorted sine waves). Unfortunately, this ratio varies widely as a function of the waveform and will give grossly incorrect results in many cases. The table shows a few representative examples comparing rms with m.a.d.

Examples of applications include noise measurement – for example, thermal noise, transistor noise, and switch-contact noise. True-rms measurement is a technique that provides consistent theoretically valid measurements of noise amplitude (standard deviation) from different sources having different properties.

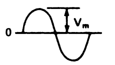
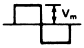
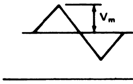
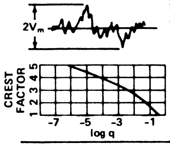
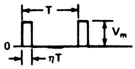
True-rms devices are also useful for measuring electrical signals derived from mechanical phenomena, such as strain, stress, vibration, shock, expansion, bearing noise, and acoustical noise. The electrical signals produced by these mechanical actions are often noisy, non-periodic, nonsinusoidal, and superimposed on dc levels, and require true-rms for consistent, valid, accurate measurements. RMS converters are also useful for accurate measurements on low-repetition-rate pulse-trains having high *crest factors* (ratio of peak to rms), and for measurements of the energy content of SCR waveforms at differing firing angles.

The basic approach used in these converters for computing the rms is to take the absolute value, square it, and divide by the fed-back output (using the logarithmic characteristics of transistor junctions), and filter the result. The resulting approximation

$$E_o = \text{Avg.}\left[\frac{V_{in}^2}{E_o}\right] \cong \sqrt{\text{Avg.}\,(V_{in}^2)}$$

is valid if the averaging time-constant is sufficiently long compared with the periods of the lowest-frequency ac components of the signal.

The simplest form of averaging involves a single-pole filter, using an external filtering capacitance. Increased values of capacitance for filtering will improve the accuracy for low frequency rms measurements and provide reduced ripple at the output, but at the cost of increased settling time. For fastest settling and minimum ripple, the data sheets show how an additional stage of 2-pole filtering is useful (the internal buffer amplifier of the AD536A and AD636 permits this to be accomplished without external active elements). The additional filtering permits improvement of settling time or reduction of ripple (or both) because of substantial reduction of C_{ext}.

WAVEFORM		RMS	MAD	$\frac{RMS}{MAD}$	CREST FACTOR
	SINE WAVE	$\frac{V_m}{\sqrt{2}}$ $0.707\ V_m$	$\frac{2}{\pi}V_m$ $0.637\ V_m$	$\frac{\pi}{2\sqrt{2}} = 1.111$	$\sqrt{2} = 1.414$
	SYMMETRICAL SQUARE WAVE OR DC	V_m	V_m	1	1
	TRIANGULAR WAVE OR SAWTOOTH	$\frac{V_m}{\sqrt{3}}$	$\frac{V_m}{2}$	$\frac{2}{\sqrt{3}} = 1.155$	$\sqrt{3} = 1.732$
	GAUSSIAN NOISE CREST FACTOR IS THEORETICALLY UNLIMITED. q IS THE FRACTION OF TIME DURING WHICH GREATER PEAKS CAN BE EXPECTED TO OCCUR	RMS	$\sqrt{\frac{2}{\pi}}$ RMS = 0.798 RMS	$\sqrt{\frac{\pi}{2}}$ 1.253	C.F. q 1 32% 2 4.6% 3 0.37% 3.3 0.1% 3.9 0.01% 4 63ppm 4.4 10ppm 4.9 1ppm 6 2×10^{-9}
 η: "DUTY CYCLE"	PULSE TRAIN η MARK/SPACE 1 ∞ 0.25 0.3333 0.0625 0.0667 0.0156 0.0159 0.01 0.0101	$V_m\sqrt{\eta}$ V_m $0.5V_m$ $0.25V_m$ $0.125V_m$ $0.1V_m$	$V_m\eta$ V_m $0.25V_m$ $0.0625V_m$ $0.0156V_m$ $0.01V_m$	$\frac{1}{\sqrt{\eta}}$ 1 2 4 8 10	$\frac{1}{\sqrt{\eta}}$ 1 2 4 8 10

PERFORMANCE SPECIFICATIONS

Considerable information regarding rms-to-dc converter circuit design, performance, selection, and applications is to be found in the NONLINEAR CIRCUITS HANDBOOK.[1] In addition, useful applications information on auxiliary filtering can be found in the article "Measure RMS with Less Ripple in Less Time,"[2] and a discussion of the design of the AD536A can be found in the 1976 IEEE International Solid-State Circuits Conference *Digest of Technical Papers,* page 10.

The most-salient feature of a true rms-to-dc converter is that it ideally has no error due to an indirect approximation to the rms. Static errors are due only to scale-factor, linearity, and offset errors; dynamic errors are due to insufficient averaging time at the low end and finite bandwidth and slewing rate at the upper end. Linearity errors affect crest factor in midband. Dynamic errors are also a function of signal amplitude, due in part to the variation of bandwidth of the "log" transistors with signal level.

Total Error A specification for quick reference, this is the maximum deviation of the dc component of the output voltage from the theoretical output value over a specified range of signal amplitude and frequency. It is shown as the sum of a fixed error and a component proportional to the theoretical output ("% of reading"). It is specified for a sinusoidal input in a given frequency and amplitude range. The fixed error-component includes all offset errors and irreducible nonlinearities; the %-of-reading component includes the linear scale-factor error.

Total Error, external trim (adjustment) is the amount by which the output may differ from the theoretical value when the output offset and scale factor have been trimmed. Note that the fixed error-component cannot be reduced to zero, even though the output offset can be nulled at zero input. This is because of residual input offsets and inherent nonlinearities in the converter.

Total Error vs. Temperature is the average change of %-of-full-scale error component plus the average change of percent of reading error component per degree Celsius, over the rated temperature range.

Frequency for 1%-of-Reading Error is the minimum value of frequency (at the high end) at which the error increases from the midband value by 1% of reading. It is a function of peak-to-peak input amplitude.

Frequency for ±3dB Reading Error is the minimum value of frequency (at the high end) at which the error may equal 30% of reading. It is a function of amplitude.

Crest Factor (a property of the signal) is the ratio of peak signal voltage to the ideal value of rms; the specified value of crest factor is that for which the error is maintained within specified limits at a given rms level for a worst-case – rectangular pulse – input signal.

Filter Time Constant and External Capacitor: The time constant of the internal averaging filter, and the increase of time constant per μF of added external capacitance.

Input: The voltage range over which specified operation is obtained, the maximum voltage for which the unit operates, the maximum safe input voltage, and the effective input resistance.

Output: The maximum output range for rated performance, the minimum current guaranteed available at full-scale output voltage, and the source resistance of the output circuit.

Power Supply: Power-supply range for specified performance, power-supply range for operation, and quiescent current drain. Note that the AD536 can be operated from single or dual supplies.

Temperature Range: The range of temperature variation for operation within specifications. Temperature coefficients are determined by three-point measurements ($T_H - 25^\circ C$), ($25^\circ C - T_L$), when measured.

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[1] *Nonlinear Circuits Handbook,* Analog Devices, Inc., 1974, 1976, 536pp, edited by D. H. Sheingold, $5.95; send check or complete MasterCard data to P.O. Box 796, Norwood MA 02062

[2] ANALOG DIALOGUE 9-3, 1975, pp 21-22

ANALOG DEVICES

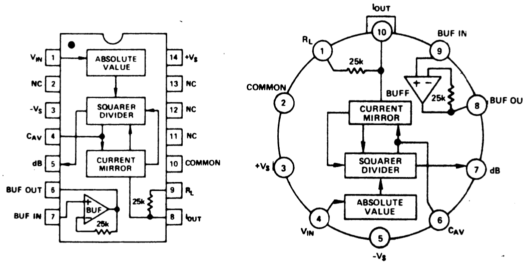
Integrated Circuit True rms-to-dc Converter

AD536A

FEATURES

- True rms-to-dc Conversion
- Laser-Trimmed to High Accuracy
  - 0.2% max Error (AD536AK)
  - 0.5% max Error (AD536AJ)
- Wide Response Capability:
  - Computes rms of ac and dc Signals
  - 300kHz Bandwidth: $V_{rms} > 100mV$
  - 2MHz Bandwidth: $V_{rms} > 1V$
  - Signal Crest Factor of 7 for 1% Error
- dB Output with 60dB Range
- Low Power: 1mA Quiescent Current
- Single or Dual Supply Operation
- Monolithic Integrated Circuit
- -55°C to +125°C Operation (AD536AS)
- Low Cost

AD536A FUNCTIONAL BLOCK DIAGRAMS



TO-116 TOP VIEW

TO-100 TOP VIEW

PRODUCT DESCRIPTION

The AD536A is a complete monolithic integrated circuit which performs true rms-to-dc conversion. It offers performance which is comparable or superior to that of hybrid or modular units costing much more. The AD536A directly computes the true rms value of any complex input waveform containing ac and dc components. It has a crest factor compensation scheme which allows measurements with 1% error at crest factors up to 7. The wide bandwidth of the device extends the measurement capability to 300kHz with 3dB error for signal levels above 100mV.

An important feature of the AD536A not previously available in rms converters is an auxiliary dB output. The logarithm of the rms output signal is brought out to a separate pin to allow the dB conversion, with a useful dynamic range of 60dB. Using an externally supplied reference current, the 0dB level can be conveniently set by the user to correspond to any input level from 0.1 to 2 volts rms.

The AD536A is laser trimmed at the wafer level for input and output offset, positive and negative waveform symmetry (dc reversal), and full scale accuracy. As a result, no external trims are required to achieve the rated accuracy of the unit.

There is full protection for both inputs and outputs. The input circuitry can take overload voltages well beyond the supply levels. Loss of supply voltage with inputs connected will not cause unit failure. The output is short-circuit protected.

The AD536A is available in two accuracy grades (J, K) for commercial temperature range (0 to +70°C) applications, and one grade (S) rated for the full -55°C to +125°C military range. The AD536AK offers a maximum total error of ±2mV ±0.2% of reading and the AD536AJ and AD536AS have maximum errors of ±5mV ±0.5% of reading.

PRODUCT HIGHLIGHTS

1. The AD536A computes the true root-mean-square level of a complex ac (or ac plus dc) input signal and gives an equivalent dc output level. The true rms value of a waveform is a more useful quantity than the average rectified value since it relates directly to the power of the signal. The rms value of a statistical signal also relates to its standard deviation.
2. The crest factor of a waveform is the ratio of the peak signal swing to the rms value. The crest factor compensation scheme of the AD536A allows measurement of highly complex signals with wide dynamic range.
3. The only external component required to perform measurements to the fully specified accuracy is the capacitor which sets the averaging period. The value of this capacitor determines the low frequency ac accuracy, ripple level and settling time.
4. The AD536A will operate equally well from split supplies or a single supply with total supply levels from 5 to 36 volts. The one milliampere quiescent supply current makes the device well-suited for a wide variety of remote controllers and battery powered instruments.
5. The AD536A directly replaces the AD536, and provides improved bandwidth and temperature drift specifications.

SPECIFICATIONS (typical @ +25°C and ±15V dc unless otherwise noted)

MODEL	AD536AJ	AD536AK	AD536AS
TRANSFER EQUATION	$V_{OUT} = \sqrt{avg. (V_{IN})^2}$	*	*
CONVERSION ACCURACY			
Total Error, Internal Trim[1] (Fig. 1)	±5mV ±0.5% of Reading, max	±2mV ±0.2% of Reading, max	*
vs. Temperature, T_{min} to +70°C	±(0.1mV ±0.01% Reading)/°C max	±(0.05mV ±0.005% of Reading)/°C max	±(0.1mV ±0.005% of Reading)/°C max
+70°C to +125°C	–	–	±(0.3mV ±0.005% of Reading)/°C max
vs. Supply Voltage	±(0.1mV ±0.01% Reading)/V	*	*
dc Reversal Error	±0.3% of Reading	*	*
Total Error, External Trim[1] (Fig. 2)	±3mV ±0.3 of Reading	±2mV ±0.1% of Reading	*
ERROR vs CREST FACTOR[2]			
Crest Factor 1 to 2	Specified Accuracy	*	*
Crest Factor = 3	-0.1% of Reading	*	*
Crest Factor = 7	-1% of Reading	*	*
FREQUENCY RESPONSE[3]			
Bandwidth for 1% additional error (0.1dB)			
$10mV < V_{IN} \leqslant 100mV$	6kHz	*	*
$100mV < V_{IN} \leqslant 1V$	40kHz	*	*
$1V < V_{IN} \leqslant 7V$	100kHz	*	*
±3dB Bandwidth			
$10mV < V_{IN} \leqslant 100mV$	50kHz	*	*
$100mV < V_{IN} \leqslant 1V$	300kHz	*	*
$1V < V_{IN} \leqslant 7V$	2MHz	*	*
AVERAGING TIME CONSTANT (Fig. 5)	25ms/μF C_{AV}	*	*
INPUT CHARACTERISTICS			
Signal Range, ±15V Supply	±20V Peak	*	*
Signal Range, +5V Supply	±5V Peak	*	*
Safe Input, All Supply Voltages	±25V max	*	*
Input Resistance	16.7kΩ ±25%	*	*
Input Offset Voltage	±2mV max	±1mV max	*
OUTPUT CHARACTERISTICS			
Offset Voltage	±2mV max	±1mV max	*
vs. Temperature	±0.1mV/°C	*	±0.2mV/°C max
vs. Supply Voltage	±0.1mV/V	*	±0.2mV/V max
Voltage Swing, ±15V Supplies	0 to +10V min	*	*
±5V Supply	0 to +2V min	*	*
Output Current	(+5mA, -130μA) min	*	*
Short Circuit Current	+20mA	*	*
Resistance	0.5Ω max	*	*
dB OUTPUT (Fig. 10)			
Error, V_{IN} 7mV to 7V rms, 0dB = 1V rms	±0.5dB	±0.2dB	*
Scale Factor	-3mV/dB	*	*
Scale Factor TC (Uncompensated, see Fig. 10 for Temperature Compensation)	-0.3% Reading/°C (-0.03dB/°C)	*	*
I_{REF} for 0dB = 1V rms	20μA (5μA min, 80μA max)	*	*
I_{REF} Range	1μA to 100μA	*	*
I_{OUT} TERMINAL			
I_{OUT} Scale Factor	40μA/Volt rms	*	*
I_{OUT} Scale Factor Tolerance	±25%	*	*
Output Resistance	10^8Ω	*	*
Voltage Compliance	$-V_S$ to $(+V_S$ -2.5V)	*	*
BUFFER AMPLIFIER			
Input and Output Voltage Range	$-V_S$ to $(+V_S$ -2.5V)min	*	*
Input Offset Voltage, R_S = 25k	±4mV max	*	*
Input Current	100nA typ, 300nA max	*	*
Input Resistance	10^8Ω	*	*
Output Current	(5mA, -130μA) min	*	*
Short Circuit Current	+20mA	*	*
Small Signal Bandwidth	1MHz	*	*
Slew Rate[4]	5V/μs	*	*
POWER SUPPLY			
Voltage, Rated Performance			
Dual Supply	±3.0V to ±18V	*	*
Single Supply	+5V to +36V	*	*
Quiescent Current			
Total V_S 5V to 36V, T_{min} to T_{max}	2mA max (1mA typ)	*	*
TEMPERATURE RANGE			
Rated Performance	0 to +70°C	*	-55°C to +125°C
Storage	-55°C to +150°C	*	*
PACKAGE OPTIONS[5]			
"H" Package: TO-100	AD536AJH	AD536AKH	AD536ASH
"D" Package: TO-116 Style (D14A)	AD536AJD	AD536AKD	AD536ASD

[1] Accuracy is specified for 0 to 7V rms, dc or 1kHz sinewave input with the AD536A connected as in the figure referenced.

[2] Error vs crest factor is specified as an additional error for 1V rms rectangular pulse input, pulse width = 200μs.

[3] Input voltages are expressed in volts rms, and error is percent of reading.

[4] With 2k external pulldown resistor.

[5] See Section 20 for package outline information.

*Specifications same as AD536AJ.

Specifications subject to change without notice.

STANDARD CONNECTION

The AD536A is simple to connect for the majority of high accuracy rms measurements, requiring only an external capacitor to set the averaging time constant. The standard connection is shown in Figure 1. In this configuration, the AD536A will measure the rms of the ac and dc level present at the input, but will show an error for low frequency inputs as a function of the filter capacitor, C_{AV}, as shown in Figure 5. Thus, if a 4μF capacitor is used, the additional average error at 10Hz will be 0.1%, at 3Hz it will be 1%. The accuracy at higher frequencies will be according to specification. If it is desired to reject the dc input, a capacitor is added in series with with the input, as shown in Figure 3; the capacitor must be non-polar. If the AD536A is driven with power supplies with a considerable amount of high frequency ripple, it is advisable to bypass both supplies to ground with 0.1μF ceramic discs as near the device as possible.

The input and output signal ranges are a function of the supply voltages; these ranges are shown in Figure 14. The AD536A can also be used in an unbuffered voltage output mode by disconnecting the input to the buffer. The output then appears unbuffered across the 25k resistor. The buffer amplifier can then be used for other purposes. Further the AD536A can be used in a current output mode by disconnecting the 25k resistor from ground. The output current is available at pin 8 (pin 10 on the "H" package) with a nominal scale of 40μA per volt rms input, positive out.

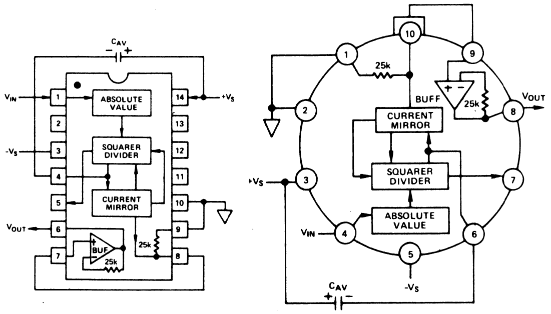


Figure 1. Standard rms Connection

OPTIONAL EXTERNAL TRIMS FOR HIGH ACCURACY

If it is desired to improve the accuracy of the AD536A, the external trims shown in Figure 2 can be added. R_4 is used to trim the offset. Note that the offset trim circuit adds 249Ω in series with the internal 25kΩ resistor. This will cause a 1% increase in scale factor, which is trimmed out by using R_1 as shown.

The trimming procedure is as follows:

1. Ground the input signal, V_{IN}, and adjust R_4 to give zero volts output from pin 6. Alternatively, R_4 can be adjusted to give the correct output with the lowest expected value of V_{IN}.
2. Connect the desired full scale input level to V_{IN}, either dc or a calibrated ac signal (1kHz is the optimum frequency); then trim R_1 to give the correct output from pin 6, i.e., 1.000V dc input should give 1.000V dc output. Of course, a ±1.000V peak-to-peak sinewave should give a 0.707V dc output. The remaining errors, as given in the specifications, are due to the nonlinearity.

The major advantage of external trimming is to optimize device performance for a reduced signal range; the AD536A is internally trimmed for a 7V rms full scale range.

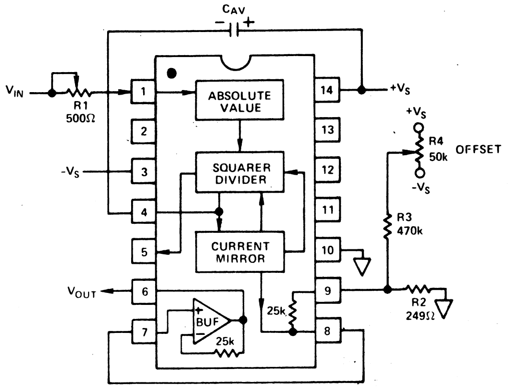


Figure 2. Optional External Gain and Output Offset Trims

SINGLE SUPPLY CONNECTION

The applications in Figures 1 and 2 require the use of approximately symmetrical dual supplies. The AD536A can also be used with only a single positive supply down to +5 volts, as shown in Figure 3. The major limitation of this connection is that only ac signals can be measured since the differential input stage must be biased off ground for proper operation. This biasing is done at pin 10; thus it is critical that no extraneous signals be coupled into this point. Biasing can be accomplished by using a resistive divider between $+V_S$ and ground. The values of the resistors can be increased in the interest of lowered power consumption, since only 5 microamps of current flows into pin 10 (pin 2 on the "H" package). AC input coupling requires only capacitor C_2 as shown; a dc return is not necessary as it is provided internally. C_2 is selected for the proper low frequency break point with the input resistance of 16.7kΩ; for a cut-off at 10Hz, C_2 should be 1μF. The signal ranges in this connection are slightly more restricted than in the dual supply connection. The input and output signal ranges are shown in Figure 14. The load resistor, R_L, is necessary to provide output sink current.

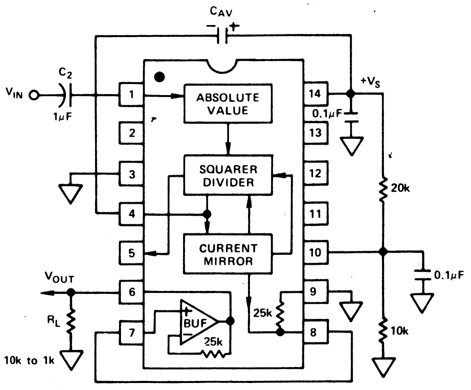


Figure 3. Single Supply Connection

CHOOSING THE AVERAGING TIME CONSTANT

The AD536A will compute the rms of both ac and dc signals. If the input is a slowly-varying dc, the output of the AD536A will track the input exactly. At higher frequencies, the average output of the AD536A will approach the rms value of the input signal. The actual output of the AD536A will differ from the ideal output by an average (or dc) error and some amount of ripple, as demonstrated in Figure 4.

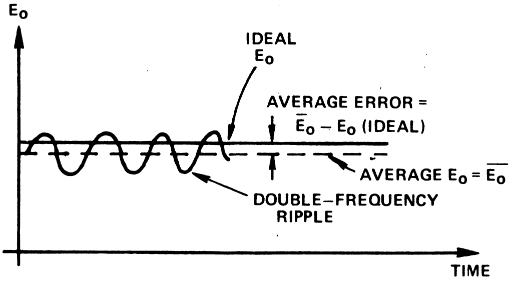

E_O
IDEAL E_O
AVERAGE ERROR = $\bar{E}_O - E_O$ (IDEAL)
AVERAGE $E_O = \overline{E_O}$
DOUBLE-FREQUENCY RIPPLE
TIME

Figure 4. Typical Output Waveform for Sinusoidal Input

The dc error is dependent on the input signal frequency and the value of C_{AV}. Figure 5 can be used to determine the minimum value of C_{AV} which will yield 1% or 0.1% dc error above a given frequency. For example, if a 60Hz waveform is to be measured with a dc error of less than 0.1%, C_{AV} must be greater than 0.65μF. If a 1% error can be tolerated, the minimum value of C_{AV} is 0.22μF.

The ac component of the output signal is the ripple. There are two ways to reduce the ripple. The first method involves using a large value of C_{AV}. Since the ripple is inversely proportional to C_{AV}, a tenfold increase in this capacitance will effect a tenfold reduction in ripple. When measuring waveforms with high crest factors, (such as low duty cycle pulse trains), the averaging time constant should be at least ten times the signal period. For example, a 100Hz pulse rate requires a 100ms time constant, which corresponds to a 4μF capacitor (time constant = 25ms per μF).

The primary disadvantage in using a large C_{AV} to remove ripple is that the settling time for a step change in input level is increased proportionately. Figure 5 shows that the relationship between C_{AV} and settling time is 100 milliseconds for each microfarad of C_{AV}. The settling time is twice as great for decreasing signals as for increasing signals (the values in Figure 5 are for decreasing signals). Settling time also increases for low signal levels, as shown in Figure 6.

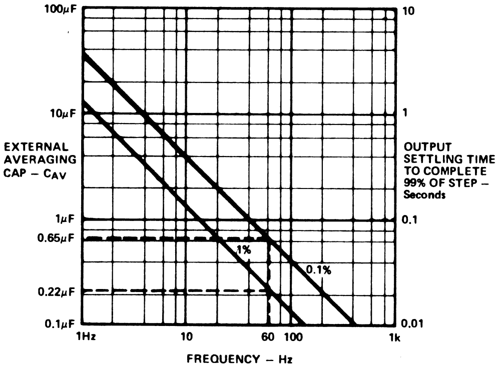


Figure 5. Lower Frequency for Stated % of Reading Error and Settling Time for Circuit Shown in Figure 1

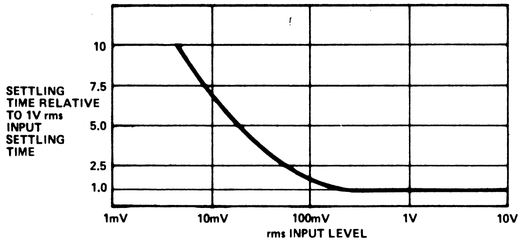


Figure 6. Settling Time vs Input Level

A better method for reducing output ripple is the use of a "post-filter". Figure 7 shows a suggested circuit. If a single-pole filter is used (C_3 removed, R_X shorted), and C_2 is approximately twice the value of C_{AV}, the ripple is reduced as shown in Figure 8, and settling time is increased. For example, with C_{AV} = 1μF and C_2 = 2.2μF, the ripple for a 60Hz input is reduced from 10% of reading to approximately 0.3% of reading. The settling time, however, is increased by approximately a factor of 3. The values of C_{AV} and C_2 can therefore be reduced to permit faster settling times while still providing substantial ripple reduction.

The two-pole post-filter uses an active filter stage to provide even greater ripple reduction without substantially increasing the settling times over a circuit with a one-pole filter. The values of C_{AV}, C_2, and C_3 can then be reduced to allow extremely fast settling times for a constant amount of ripple. Caution should be exercised in choosing the value of C_{AV}, since the dc error is dependent upon this value and is independent of the post filter.

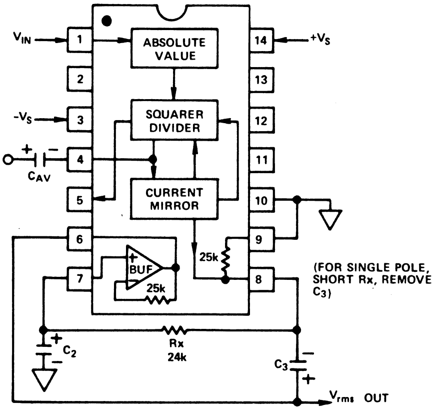


Figure 7. 2 Pole "Post" Filter

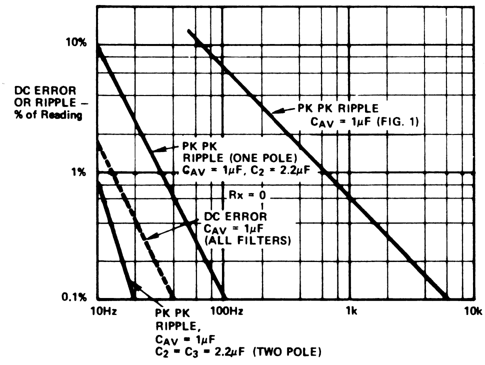


Figure 8. Performance Features of Various Filter Types

AD536A PRINCIPLE OF OPERATION

The AD536A embodies an implicit solution of the rms equation that overcomes the dynamic range as well as other limitations inherent in a straight-forward computation of rms. The actual computation performed by the AD536A follows the equation:

$$V_{rms} = \text{Avg.} \left[\frac{V_{IN}^2}{V_{rms}} \right]$$

Figure 9 is a simplified schematic of the AD536A; it is subdivided into four major sections: absolute value circuit (active rectifier), squarer/divider, current mirror, and buffer amplifier. The input voltage, V_{IN}, which can be ac or dc, is converted to a unipolar current I_1, by the active rectifier A_1, A_2. I_1 drives one input of the squarer/divider, which has the transfer function:

$$I_4 = I_1^2 / I_3$$

The output current, I_4, of the squarer/divider drives the current mirror through a low pass filter formed by R_1 and the externally connected capacitor, C_{AV}. If the R_1, C_{AV} time constant is much greater than the longest period of the input signal, then I_4 is effectively averaged. The current mirror returns a current I_3, which equals Avg. $[I_4]$, back to the squarer/divider to complete the implicit rms computation. Thus:

$$I_4 = \text{Avg.}\ [I_1^2/I_4] = I_1\ \text{rms}$$

The current mirror also produces the output current, I_{OUT}, which equals $2I_4$. I_{OUT} can be used directly or converted to a voltage with R_2 and buffered by A_4 to provide a low impedance voltage output. The transfer function of the AD536A thus results:

$$V_{OUT} = 2R_2\ I_{rms} = V_{IN\ rms}$$

The dB output is derived from the emitter of Q_3, since the voltage at this point is proportional to $-\log V_{IN}$. Emitter follower, Q_5, buffers and level shifts this voltage, so that the dB output voltage is zero when the externally supplied emitter current (I_{REF}) to Q_5 approximates I_3.

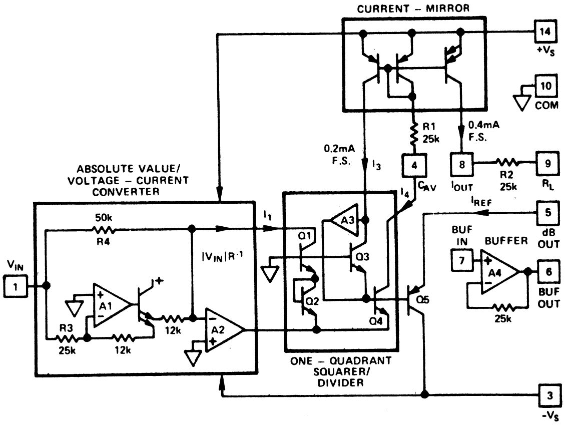


Figure 9. Simplified Schematic

CONNECTIONS FOR dB OPERATION

A powerful feature added to the AD536A, which is not available in any other computing rms circuit, is the logarithmic or decibel output. The internal circuit which computes dB is very accurate and works well over a 60dB range. The connection for dB measurements is shown in Figure 10. The user selects the 0dB level by setting R_1 for the proper 0dB reference current (which is set to exactly cancel the log output current from the squarer-divider at the desired 0dB point). The external op amp is used to provide a more convenient scale and to allow compensation of the 0.3%/°C temperature drift of the dB circuit. The special T.C. resistor, R_3, is available from Tel Labs, Londonderry, NH, type number Q-81. The linear rms output is available at pin 8 with an output impedance of 25kΩ; thus some applications may require an additional buffer amplifier if this output is desired.

dB Calibration:

1. Set V_{IN} = 1.00V dc
2. Adjust R_1 for dB out = 0.00V
3. Set V_{IN} = +0.1V dc
4. Adjust R_2 for dB out = -2.00V

Any other desired 0dB reference level can be used by setting V_{IN} and adjusting R_1 accordingly. Note that adjusting R_2 for the proper gain automatically gives the correct temperature compensation.

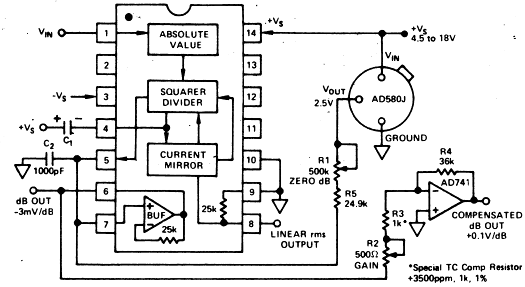


Figure 10. dB Connection

FREQUENCY RESPONSE

The AD536A utilizes a logarithmic circuit in performing the implicit rms computation. As with any log circuit, bandwidth is proportional to signal level. The solid lines in the graph below represent the frequency response of the AD536A at input levels from 10 millivolts to 1 volt rms. The dashed lines indicate the upper frequency limits for 1%, 10%, and 3dB of reading additional error. For example, note that a 1 volt rms signal will produce less than 1% of reading additional error up to 100kHz. A 10 millivolt signal can be measured with 1% of reading additional error (100μV) up to only 6kHz.

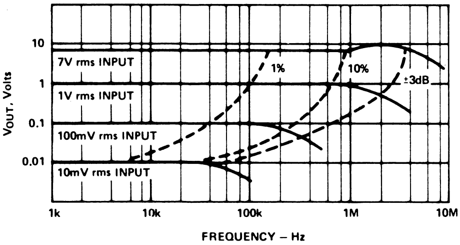


Figure 11. High Frequency Response

AC MEASUREMENT ACCURACY AND CREST FACTOR

Crest factor is often overlooked in determining the accuracy of an ac measurement. Crest factor is defined as the ratio of the the peak signal amplitude to the rms value of the signal (C.F. = V_p/V_{rms}). Most common waveforms, such as sine and triangle waves, have relatively low crest factors (<2). Waveforms which resemble low duty cycle pulse trains, such as those occurring in switching power supplies and SCR circuits, have high crest factors. For example, a rectangular pulse train with a 1% duty cycle has a crest factor of 10 (C.F. = $1/\sqrt{\eta}$).

Figure 12 is a curve of reading error for the AD536A for a 1 volt rms input signal with crest factors from 1 to 10. A rectangular pulse train (pulse width 100μs) was used for this test since it is the worst-case waveform for rms measurement (all the energy is contained in the peaks). The duty cycle and peak amplitude were varied to produce crest factors from 1 to 10 while maintaining a constant 1 volt rms input amplitude.

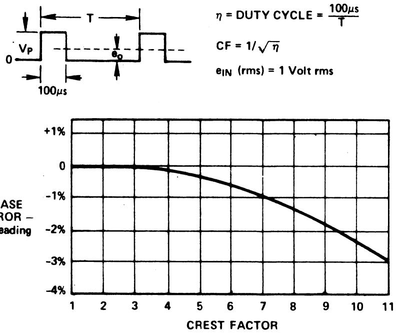


Figure 12. Error vs. Crest Factor

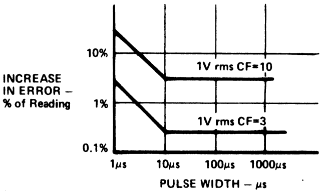


Figure 13. AD536A Error vs. Pulse Width Rectangular Pulse

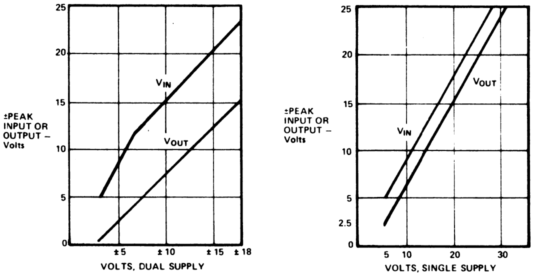


Figure 14. AD536A Input and Output Voltage Ranges vs. Supply

ANALOG DEVICES

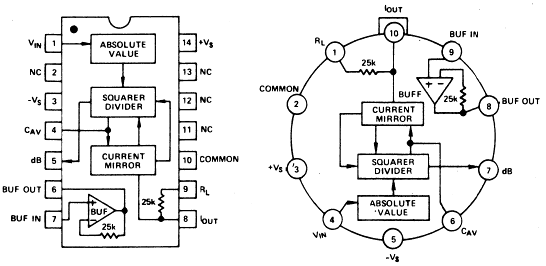
Low Level True rms-to-dc Converter

AD636

FEATURES

True rms-to-dc Conversion
200mV Full Scale
Laser-Trimmed to High Accuracy
  0.5% max Error (AD636K)
  1.0% max Error (AD636J)
Wide Response Capability:
  Computes rms of ac and dc Signals
  1MHz -3dB Bandwidth: $V_{rms}>100mV$
  Signal Crest Factor of 6 for 0.5% Error
dB Output with 50dB Range
Low Power: 800μA Quiescent Current
Single or Dual Supply Operation
Monolithic Integrated Circuit
Low Cost

AD636 FUNCTIONAL BLOCK DIAGRAMS



TO-116
TOP VIEW

TO-100
TOP VIEW

PRODUCT DESCRIPTION

The AD636 is a low power monolithic IC which performs true rms-to-dc conversion on low level signals. It offers performance which is comparable or superior to that of hybrid and modular converters costing much more. Similar in operation to the AD536A, the AD636 is specified for a signal range of 0 to 200 millivolts rms. Crest factors up to 6 can be accommodated with less than 0.5% additional error, allowing accurate measurement of complex input waveforms.

The low power supply current requirement of the AD636, typically 800μA, allows it to be used in battery-powered portable instruments. A wide range of power supplies can be used, from ±2.5V to ±12V or a single +5V to +24V supply. The input and output terminals are fully protected; the input signal can exceed the power supply with no damage to the device (allowing the presence of input signals in the absence of supply voltage) and the output buffer amplifier is short-circuit protected.

The AD636 includes an auxiliary dB output. This signal is derived from an internal circuit point which represents the logarithm of the rms output. The 0dB reference level is set by an externally supplied current and can be selected by the user to correspond to any input level from 0dBm (774.6mV) to -20dBm (77.46mV). Frequency response ranges from 1.2MHz at a 0dBm level to over 10kHz at -50dBm.

The AD636 is designed for ease of use. The device is factory-trimmed at the wafer level for input and output offset, positive and negative waveform symmetry (dc reversal), and full scale accuracy. Thus no external trims are required to achieve full rated accuracy.

The AD636 is available in two accuracy grades; the AD636J has a total error of ±0.5mV ±1.0% of reading, and the AD636K is accurate within ±0.2mV ±0.5% of reading. Both versions are specified for the 0 to 70°C temperature range, and are offered in either a hermetically sealed 14-pin DIP or a 10 pin TO-100 metal can.

PRODUCT HIGHLIGHTS

1. The AD636 computes the true root-mean-square of a complex ac (or ac plus dc) input signal and gives an equivalent dc output level. The true rms value of a waveform is a more useful quantity than the average rectified value since it is a measure of the power in the signal. The rms value of an ac-coupled signal is also its standard deviation.
2. The 200 millivolt full scale range of the AD636 is compatible with many popular display-oriented analog-to-digital converters. The low power supply current requirement permits use in battery-powered hand-held instruments.
3. The only external component required to perform measurements to the fully specified accuracy is the averaging capacitor. The value of this capacitor can be selected for the desired trade-off of low frequency accuracy, ripple, and settling time.
4. The on-chip buffer amplifier can be used to buffer either the input or the output. Used as an input buffer, it provides accurate performance from standard 10MΩ input attenuators. As an output buffer, it can supply up to 5 milliamps of output current.
5. The AD636 will operate over a wide range of power supply voltages, including single +5V to +24V or split ±2.5V to ±12V sources. A standard 9V battery will provide several hundred hours of continuous operation.

SPECIFICATIONS (typical @ +25°C, $+V_S = +3V$, $-V_S = -5V$, unless otherwise specified)

Model	AD636J	AD636K
TRANSFER EQUATION	$V_{OUT} = \sqrt{avg. (V_{IN})^2}$	•
CONVERSION ACCURACY		
Total Error, Internal Trim[1]	±0.5mV ±1.0% of Reading, max	±0.2mV ±0.5% of Reading, max
vs. Temperature, 0 to +70°C	±(0.1mV ±0.01% of Reading)/°C max	±(0.1mV ±0.005% of Reading)/°C max
vs. Supply Voltage	±(0.1mV ±0.01% of Reading)/V	•
dc Reversal Error	±0.2% of Reading	±0.1% of Reading
Total Error, External Trim[1]	±0.3mV ±0.3% of Reading	±0.1mV ±0.2% of Reading
ERROR vs. CREST FACTOR[2]		
Crest Factor 1 to 2	Specified Accuracy	•
Crest Factor = 3	-0.2%	•
Crest Factor = 6	-0.5%	•
FREQUENCY RESPONSE[3,4]		
Bandwidth for 1% Additional Error (0.1dB)		
V_{IN} = 10mV	12kHz	•
V_{IN} = 100mV	80kHz	•
V_{IN} = 200mV	130kHz	•
±3dB Bandwidth		
V_{IN} = 10mV	80kHz	•
V_{IN} = 100mV	800kHz	•
V_{IN} = 200mV	1.3MHz	•
AVERAGING TIME CONSTANT	25ms/μF	•
INPUT CHARACTERISTICS		
Signal Range		
+3, -5V Supply	±2.8V Peak	•
±2.5V Supply	±2V Peak	•
±5V Supply	±5V Peak	•
Safe Input, All Supply Voltage	±12V max	•
Input Resistance	6.7kΩ ±25%	•
Input Offset Voltage	0.5mV max	0.2mV max
OUTPUT CHARACTERISTICS[4]		
Offset Voltage	0.5mV max	0.2mV max
vs. Temperature	±10μV/°C	•
vs. Supply	±0.1mV/V	•
Voltage Swing		
+3, -5V Supply	0 to 1V typ (0.3V min)	•
±5V Supply	0 to 1.4V typ (0.3V min)	•
Output Impedance	10kΩ ±20% max	•
dB OUTPUT		
Error, 7mV ≤ V_{IN} ≤ 300mV rms	±0.5dB max	±0.2dB max
Scale Factor	-3mV/dB	•
Scale Factor Temperature Coefficient	+0.3%/°C(-0.03dB/°C)	•
I_{REF} for 0dB = 0.1V rms	4μA (2μA min, 8μA max)	•
I_{REF} Range	1μA to 50μA	•
I_{OUT} TERMINAL		
I_{OUT} Scale Factor	100μA/V rms	•
I_{OUT} Scale Factor Tolerance	±20%	•
Output Resistance	10^8Ω	•
Voltage Compliance	$-V_S$ to ($+V_S$ -2V)	•
BUFFER AMPLIFIER		
Input and Output Voltage Range	$-V_S$ to ($+V_S$ -2V) min	•
Input Offset Voltage, R_S = 10k	2mV max	1mV max
Input Current	100nA typ (300nA max)	•
Input Resistance	10^8Ω	•
Output Current	(+5mA, -130μA) min	•
Short Circuit Current	20mA	•
Small Signal Bandwidth	1MHz	•
Slew Rate[5]	5V/μs	•
POWER SUPPLY		
Voltage, Rated Performance	+3, -5V	•
Dual Supply	+2/-2.5V to ±12V	•
Single Supply	+5V to +24V	•
Quiescent Current[6]	800μA (1mA max)	•
TEMPERATURE RANGE		
Rated Performance	0 to +70°C	•
Storage	-55°C to +150°C	•
PACKAGE OPTIONS[7]		
"H Package: TO-100	AD636JH	AD636KH
"D" Package: TO-116 Style (D14A)	AD636JD	AD636KD

NOTES

[1] Accuracy is specified for 0 to 200mV rms, dc or 1kHz sinewave input. Accuracy is degraded at higher rms signal levels.

[2] Error vs. crest factor is specified as additional error for a 200mV rms rectangular pulse train, pulse width = 200μs.

[3] Input voltages are expressed in volts rms.

[4] Measured at pin 8 of DIP (I_{OUT}), with pin 9 tied to common.

[5] With 10kΩ pull-down resistor from pin 6 (BUF OUT) to $-V_S$.

[6] With BUF input tied to $-V_S$.

[7] See Section 20 for package outline information.

•Specifications same as AD636J.

Specifications subject to change without notice.

STANDARD CONNECTION

The AD636 is simple to connect for the majority of high accuracy rms measurements, requiring only an external capacitor to set the averaging time constant. The standard connection is shown in Figure 1. In this configuration, the AD636 will measure the rms of the ac and dc level present at the input, but will show an error for low frequency inputs as a function of the filter capacitor, C_{AV}, as shown in Figure 5. Thus, if a 4µF capacitor is used, the additional average error at 10Hz will be 0.1%, at 3Hz it will be 1%. The accuracy at higher frequencies will be according to specification. If it is desired to reject the dc input, a capacitor is added in series with with the input, as shown in Figure 3; the capacitor must be non-polar. If the AD636 is driven with power supplies with a considerable amount of high frequency ripple, it is advisable to bypass both supplies to ground with 0.1µF ceramic discs as near the device as possible. C_F is an optional output ripple filter, as discussed elsewhere in this data sheet.

The input and output signal ranges are a function of the supply voltages as detailed in the specifications. The AD636 can also be used in an unbuffered voltage output mode by disconnecting the input to the buffer. The output then appears unbuffered across the 10k resistor. The buffer amplifier can then be used for other purposes. Further, the AD636 can be used in a current output mode by disconnecting the 10k resistor from the ground. The output current is available at pin 8 (pin 10 on the "H" package) with a nominal scale of 100µA per volt rms input, positive out.

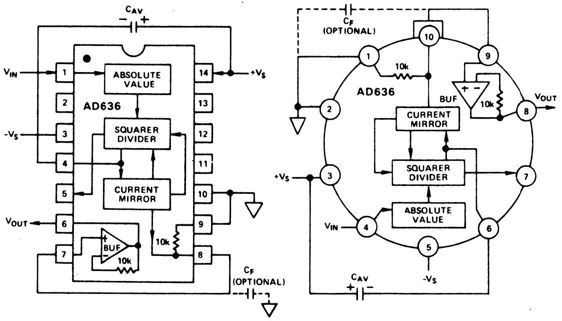


Figure 1. Standard rms Connection

OPTIONAL EXTERNAL TRIMS FOR HIGH ACCURACY

If it is desired to improve the accuracy of the AD636, the external trims shown in Figure 2 can be added. R_4 is used to trim the offset. The scale factor is trimmed by using R_1 as shown. The insertion of R_2 allows R_1 to either increase or decrease the scale factor.

The trimming procedure is as follows:

1. Ground the input signal, V_{IN}, and adjust R_4 to give zero volts output from pin 6. Alternatively, R_4 can be adjusted to give the correct output with the lowest expected value of V_{IN}.
2. Connect the desired full scale input level to V_{IN}, either dc or a calibrated ac signal (1kHz is the optimum frequency); then trim R_1 to give the correct output from pin 6, i.e., 200mV dc input should give 200mV dc output. Of course, a ±200mV peak-to-peak sinewave should give a 141.4mV dc output. The remaining errors, as given in the specifications, are due to the nonlinearity.

SINGLE SUPPLY CONNECTION

The applications in Figures 1 and 2 assume the use of dual power supplies. The AD636 can also be used with only a single positive supply down to +5 volts, as shown in Figure 3. The major limitation of this connection is that only ac signals can be measured since the input stage must be biased off ground for proper operation. This biasing is done at pin 10; thus it is critical that no extraneous signals be coupled into this point. Biasing can be accomplished by using a resistive divider between $+V_S$ and ground. The values of the resistors can be increased in the interest of lowered power consumption, since only 1 microamp of current flows into pin 10 (pin 2 on the "H" package). Alternately, the COM pin of some CMOS ADCs provides a suitable artificial ground for the AD636. AC input coupling requires only capacitor C_2 as shown; a dc return is not necessary as it is provided internally. C_2 is selected for the proper low frequency break point with the input resistance of 6.7kΩ; for a cut-off at 10Hz, C_2 should be 3.3µF. The signal ranges in this connection are slightly more restricted than in the dual supply connection. The load resistor, R_L, is necessary to provide current sinking capability.

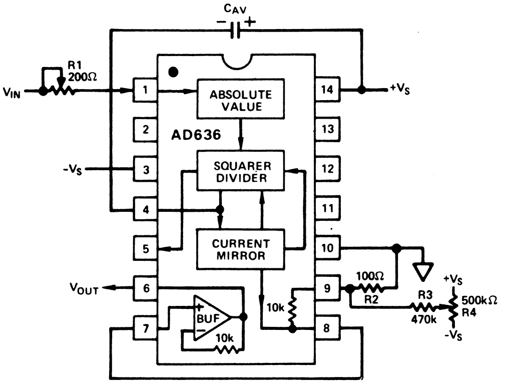


Figure 2. Optional External Gain and Output Offset Trims

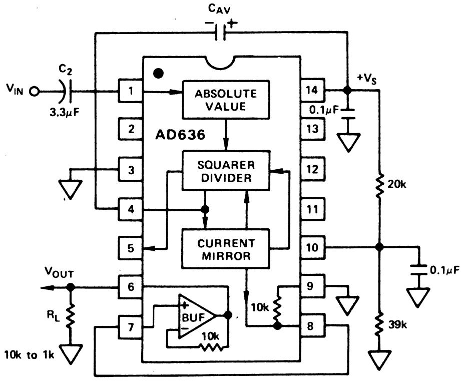
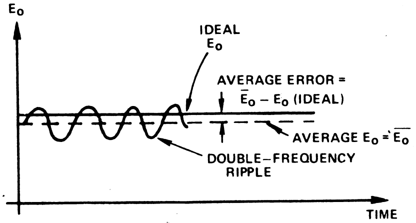


Figure 3. Single Supply Connection

CHOOSING THE AVERAGING TIME CONSTANT

The AD636 will compute the rms of both ac and dc signals. If the input is a slowly-varying dc voltage, the output of the AD636 will track the input exactly. At higher frequencies, the average output of the AD636 will approach the rms value of the input signal. The actual output of the AD636 will differ from the ideal output by an average (or dc) error and some amount of ripple, as demonstrated in Figure 4.



E₀
IDEAL E₀
AVERAGE ERROR = $\overline{E_0}$ – E₀ (IDEAL)
AVERAGE E₀ ≐ $\overline{E_0}$
DOUBLE–FREQUENCY RIPPLE
TIME

Figure 4. Typical Output Waveform for Sinusoidal Input

The dc error is dependent on the input signal frequency and the value of C_{AV}. Figure 5 can be used to determine the minimum value of C_{AV} which will yield 1% or 0.1% dc error above a given frequency. For example, if a 60Hz waveform is to be measured with a dc error of less than 0.1%, C_{AV} must be greater than 0.65μF. If a 1% error can be tolerated, the minimum value of C_{AV} is 0.22μF.

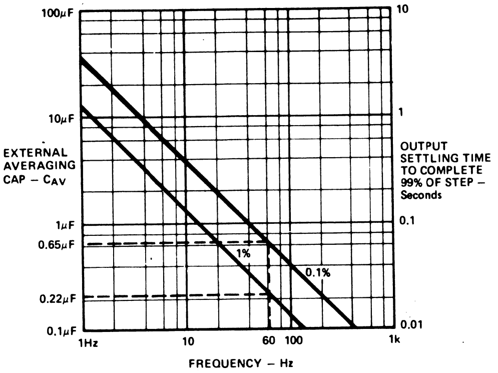


Figure 5. Lower Frequency for Stated % of Reading Error and Settling Time for Circuit Shown in Figure 1

The ac component of the output signal is the ripple. There are two ways to reduce the ripple. The first method involves using a large value of C_{AV}. Since the ripple is inversely proportional to C_{AV}, a tenfold increase in this capacitance will effect a tenfold reduction in ripple. When measuring waveforms with high crest factors, (such as low duty cycle pulse trains), the averaging time constant should be at least ten times the signal period. For example, a 100Hz pulse rate requires a 100ms time constant, which corresponds to a 4μF capacitor (time constant = 25ms per μF).

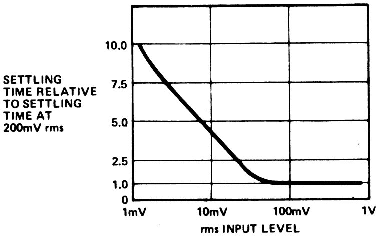


Figure 6. Settling Time vs. Input Level

The primary disadvantage in using a large C_{AV} to remove ripple is that the settling time for a step change in input level is increased proportionately. Figure 5 shows that the relationship between C_{AV} and settling time is 100 milliseconds for each microfarad of C_{AV}. The settling time is twice as great for decreasing signals as for increasing signals (the values in Figure 5 are for decreasing signals). Settling time also increases for low signal levels, as shown in Figure 6.

A better method for reducing output ripple is the use of a "post-filter". Figure 7 shows a suggested circuit. If a single-pole filter is used (C_3 removed, R_X shorted), and C_2 is approximately twice the value of C_{AV}, the ripple is reduced as shown in Figure 8, and settling time is increased. For example, with C_{AV} = 1μF and C_2 = 4.7μF, the ripple for a 60Hz input is reduced from 10% of reading to approximately 0.3% of reading. The settling time, however, is increased by approximately a factor of 3. The values of C_{AV} and C_2 can therefore be reduced to permit faster settling times while still providing substantial ripple reduction.

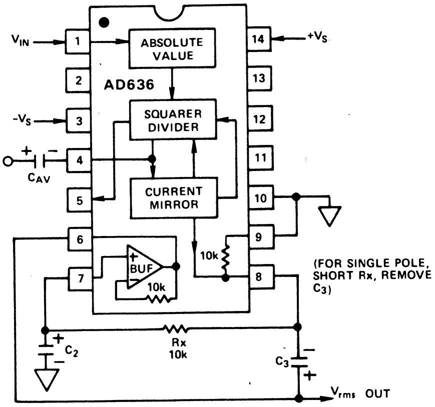


Figure 7. 2 Pole "Post" Filter

The two-pole post-filter uses an active filter stage to provide even greater ripple reduction without substantially increasing the settling times over a circuit with a one-pole filter. The values of C_{AV}, C_2, and C_3 can then be reduced to allow extremely fast settling times for a constant amount of ripple. Caution should be exercised in choosing the value of C_{AV}, since the dc error is dependent upon this value and is independent of the post filter.

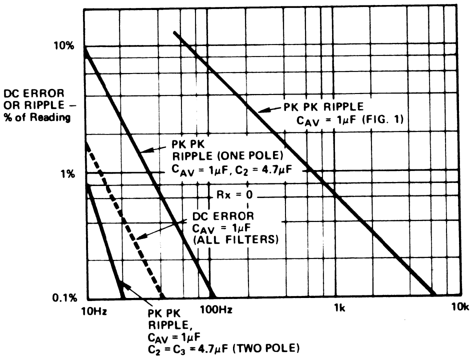


Figure 8. Performance Features of Various Filter Types

AD636 PRINCIPLE OF OPERATION

The AD636 embodies an implicit solution of the rms equation that overcomes the dynamic range as well as other limitations inherent in a straight-forward computation of rms. The actual computation performed by the AD636 follows the equation:

$$V_{rms} = \text{Avg.} \left[\frac{V_{IN}^2}{V_{rms}} \right]$$

Figure 9 is a simplified schematic of the AD636; it is subdivided into four major sections: absolute value circuit (active rectifier), squarer/divider, current mirror, and buffer amplifier. The input voltage, V_{IN}, which can be ac or dc, is converted to a unipolar current I_1, by the active rectifier A_1, A_2. I_1 drives one input of the squarer/divider, which has the transfer function:

$$I_4 = I_1^2 / I_3$$

The output current, I_4, of the squarer/divider drives the current mirror through a low pass filter formed by R_1 and the externally connected capacitor, C_{AV}. If the R_1, C_{AV} time constant is much greater than the longest period of the input signal, then I_4 is effectively averaged. The current mirror returns a current I_3, which equals Avg. $[I_4]$, back to the squarer/divider to complete the implicit rms computation. Thus:

$$I_4 = \text{Avg.}\ [I_1^2/I_4] = I_1\ \text{rms}$$

The current mirror also produces the output current, I_{OUT}, which equals $2I_4$. I_{OUT} can be used directly or converted to a voltage with R_2 and buffered by A_4 to provide a low impedance voltage output. The transfer function of the AD636 thus results:

$$V_{OUT} = 2R_2\ I_{rms} = V_{IN\ rms}$$

The dB output is derived from the emitter of Q_3, since the voltage at this point is proportional to $-\log V_{IN}$. Emitter follower, Q_5, buffers and level shifts this voltage, so that the dB output voltage is zero when the externally supplied emitter current (I_{REF}) to Q_5 approximates I_3.

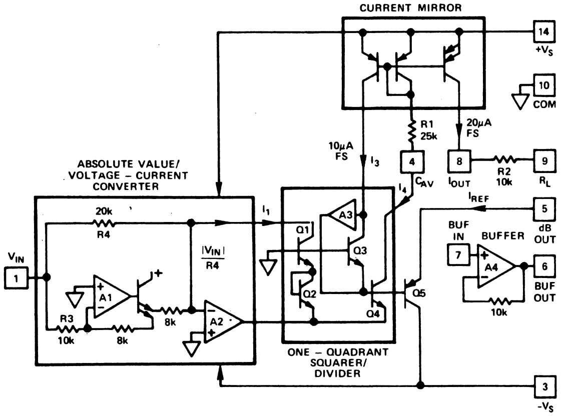


Figure 9. Simplified Schematic

THE AD636 BUFFER AMPLIFIER

The buffer amplifier included in the AD636 offers the user additional application flexibility. It is important to understand some of the characteristics of this amplifier to obtain optimum performance. Figure 10 shows a simplified schematic of the buffer.

Since the output of an rms-to-dc converter is always positive, it is not necessary to use a traditional complementary Class AB output stage. In the AD636 buffer, a Class A emitter follower is used instead. In addition to excellent positive output voltage swing, this configuration allows the output to swing fully down to ground in single-supply applications without the problems associated with most IC operational amplifiers.

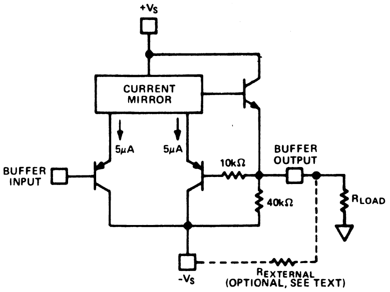


Figure 10. AD636 Buffer Amplifier Simplified Schematic

When this amplifier is used in dual-supply applications as an input buffer amplifier driving a load resistance referred to ground, steps must be taken to insure an adequate negative voltage swing. For negative outputs, current will flow from the load resistor through the 40kΩ emitter resistor, setting up a voltage divider between $-V_S$ and ground. This reduced effective $-V_S$ will limit the available negative output swing of the buffer. Addition of an external resistor in parallel with R_E alters this voltage divider such that increased negative swing is possible.

Figure 11 shows the value of $R_{EXTERNAL}$ for a particular ratio of V_{PEAK} to $-V_S$ for several values of R_{LOAD}. Addition of $R_{EXTERNAL}$ increases the quiescent current of the buffer amplifier by an amount equal to $R_{EXT}/-V_S$. Nominal buffer quiescent current with no $R_{EXTERNAL}$ is 30μA at $-V_S$ = -5V.

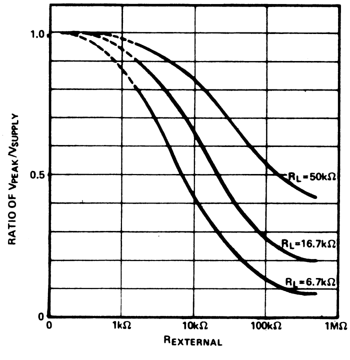


Figure 11. Ratio of Peak Negative Swing to $-V_S$ vs. $R_{EXTERNAL}$ for Several Load Resistances

FREQUENCY RESPONSE

The AD636 utilizes a logarithmic circuit in performing the implicit rms computation. As with any log circuit, bandwidth is proportional to signal level. The solid lines in the graph below represent the frequency response of the AD636 at input levels from 1 millivolt to 1 volt rms. The dashed lines indicate the upper frequency limits for 1%, 10%, and ±3dB of reading additional error. For example, note that a 1 volt rms signal will produce less than 1% of reading additional error up to 200kHz. A 10 millivolt signal can be measured with 1% of reading additional error (100μV) up to 12kHz.

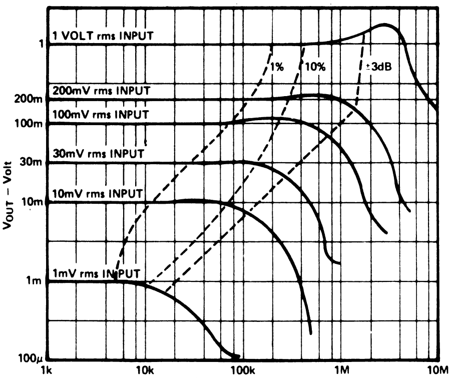


Figure 12. AD636 Frequency Response

AC MEASUREMENT ACCURACY AND CREST FACTOR

Crest factor is often overlooked in determining the accuracy of an ac measurement. Crest factor is defined as the ratio of the the peak signal amplitude to the rms value of the signal (C.F. = V_p/V_{rms}). Most common waveforms, such as sine and triangle waves, have relatively low crest factors (<2). Waveforms which resemble low duty cycle pulse trains, such as those occurring in switching power supplies and SCR circuits, have high crest factors. For example, a rectangular pulse train with a 1% duty cycle has a crest factor of 10 (C.F. = $1/\sqrt{\eta}$).

Figure 13 is a curve of reading error for the AD636 for a 200mV rms input signal with crest factors from 1 to 7. A rectangular pulse train (pulse width 200μs) was used for this test since it is the worst-case waveform for rms measurement (all the energy is contained in the peaks). The duty cycle and peak amplitude were varied to produce crest factors from 1 to 7 while maintaining a constant 200mV rms input amplitude.

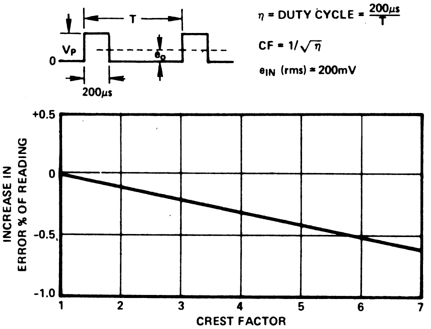


Figure 13. Error vs. Crest Factor

A COMPLETE AC DIGITAL VOLTMETER

Figure 14 shows a design for a complete low power ac digital voltmeter circuit based on the AD636. The 10MΩ input attenuator allows full scale ranges of 200mV, 2V, 20V and 200V rms. Signals are capacitively coupled to the AD636 buffer amplifier, which is connected in an ac bootstrapped configuration to minimize loading. The buffer then drives the 6.7kΩ input impedance of the AD636. The COM terminal of the ADC chip provides the false ground required by the AD636 for single supply operation. An AD589 1.2 volt reference diode is used to provide a stable 100 millivolt reference for the ADC in the linear rms mode; in the dB mode, a 1N4148 diode is inserted in series to provide correction for the temperature coefficient of the dB scale factor. Calibration of the meter is done by first adjusting offset pot R17 for a proper zero reading, then adjusting the R13 for an accurate readout at full scale.

Calibration of the dB range is accomplished by adjusting R9 for the desired 0dB reference point, then adjusting R14 for the desired dB scale factor (a scale of 10 counts per dB is convenient).

Total power supply current for this circuit is typically 2.8mA using a 7106-type ADC.

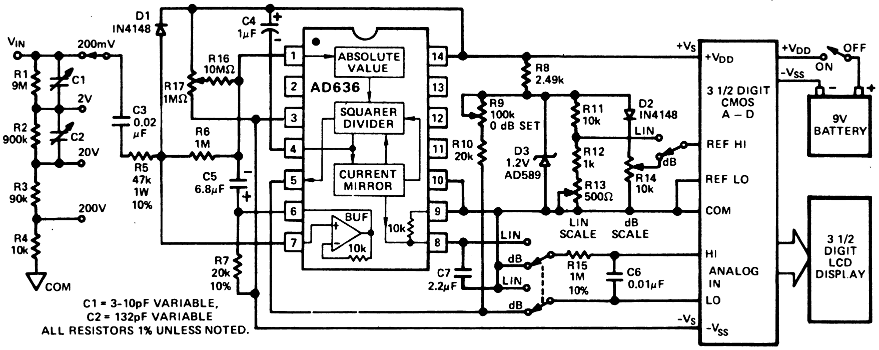


Figure 14. 3 1/2 Digit True rms ac Voltmeter

ANALOG DEVICES

Wideband, High Accuracy True rms-to-dc Converter

MODEL 442

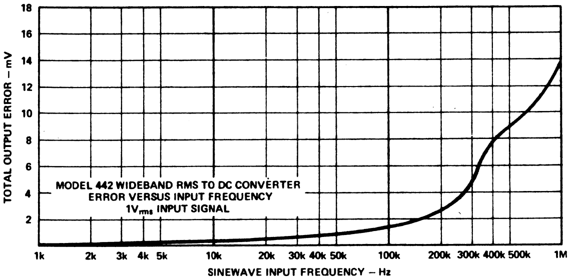
FEATURES

- DC to 8MHz Response (-3dB)
- High Accuracy:
  - With No Ext. Trim: ±2mV ±0.15% of Rdg., max
  - With Ext. Trim: ±1mV ±0.05% of Rdg., max
- Low Drift: ±(35μV ±0.01% of Reading)/°C max, 442L
- Fast Settling Time: 5ms to 1%
- Small Size: 1.5" x 1.5" x 0.4"
- All Hermetically Sealed Semiconductors

APPLICATIONS

- Wideband rms Instrumentation
- Telephone, Telegraph & Modem Test Equipment
- Vibration Analysis
- Sound & Noise Level Instrumentation
- Mean Square Measurements

MODEL 422
SIGNAL ACCURACY VS. INPUT FREQUENCY



GENERAL DESCRIPTION

Model 442 is a high performance true rms-to-dc converter featuring 8MHz bandwidth, low drift to ±35μV/°C ±0.01% of reading/°C maximum, and ±1% reading error to 800kHz. Unlike competing designs, model 442 achieves its high accuracy over a very wide input signal range. With no external adjustment, accuracy is held to within ±2mV ±0.15% of reading for input signals of 0 to $2V_{rms}$. If optional adjustments are performed, this accuracy can be improved to ±1mV ±0.05% of reading. Model 442 is designed to be used in high performance instrumentation where response to low level, high speed signals, is of greatest importance.

The compact, log-antilog circuit design of model 442 results in high accuracy measurements on sinewave signals and complex waveforms such as pulse trains. Reading error increases 0.2% for signals with crest factors up to 7. In addition, true rms measurement can be performed directly on signals containing both ac and dc components.

Model 442 is available in three low drift selections offering maximum drift performance over 0 to +70°C range; model 442L: ±(35μV ±0.01% of rdg.)/°C max; model 442K: ±(50μV ±0.01% of rdg.)/°C max; model 442J: ±(100μV ±0.01% of rdg.)/°C max.

WHERE TO USE MODEL 442

Excellent untrimmed performance along with simple, optional trims make model 442 the ideal component for all types of laboratory and OEM rms instrumentation where wideband measurements must be made with high accuracy. Model 442 is ideally suited for measuring thermal noise, transistor noise and switch contact noise. True rms measurement is the only technique to accurately measure system noise and thereby assist the designer in reducing this noise. Model 442 is also useful for measuring mechanical phenomena such as strain, stress, vibration, shock, expansion and contraction. The electrical signals produced by these mechanical actions are often noisy, nonperiodic, nonsinusoidal and superimposed on dc levels, therefore requiring true rms devices for accurate measurements.

Model 442 is also required for accurate measurements on low repetition rate pulse trains. For pulse trains with crest factors of 10, a 3dB bandwidth of 400 times the pulse rate is required to achieve 1% accuracy and 4000 times the pulse rate is needed for 0.1% accuracy.

Model 442 may also be connected (see Figure 3) to measure the MEAN SQUARE of a signal ($e_o = \overline{e_{in}^2} / V_R$). The Mean Square of a random signal is equal to the variance (σ^2).

TOTAL ACCURACY

Total output error is specified as the sum of two components; a fixed term plus a percentage of output signal. Model 442 has a rated sinewave accuracy of ±1mV ±0.05% max (externally trimmed), which for a one volt rms sinewave, results in a ±1.5mV maximum error (±1mV fixed error plus ±0.5mV reading error). The fixed error component is comprised of output offsets and linearity errors. Both of these error terms have been minimized in the model 442 as a result of special output circuit design and sophisticated factory offset trim procedures. Output offset can be adjusted for minimum error by means of an external adjustment (see Figure 2). The % of reading error is attributed to nonlinearity and scale factor errors. Scale factor error may also be reduced by external adjustment of an optional 5kΩ potentiometer (see Figure 2).

For detailed information, contact factory.

SPECIFICATIONS** (typical @ +25°C and V_S = ±15V dc, unless otherwise noted)

MODEL	442J	442K	442L
TRANSFER EQUATION	$e_o = \sqrt{\text{avg}\ (e_{in})^2}$	*	*
ACCURACY[1]			
Total Error, Sinewave Input, f ≤ 20kHz			
No External Adjustment			
Input Range: 0 to $2V_{rms}$	±2mV ±0.15% of Rdg., max	*	*
External Adjustment			
Input Range: 0 to $2V_{rms}$	±1mV ±0.05% of Rdg., max	*	*
$10mV_{rms}$ to $2V_{rms}$	±0.5mV ±0.05% of Rdg., max	*	*
Additional Error, Sinewave Input, 20kHz ≤ f ≤ 500kHz			
With or Without External Adjustment			
For Any Input Range	$(\pm 25\mu V \pm 0.0025\% \text{ of Rdg}) \times \left(\frac{f(kHz) - 20kHz}{1kHz}\right)$, max	*	*
vs. Temperature (0 to +70°C), max	±100μV/°C plus ±0.01% of Rdg./°C	±50μV/°C plus ±0.01% of Rdg./°C	±35μV/°C plus ±0.01% of Rdg./°C
vs. Supply Voltage	±0.1mV/%	*	*
Warm-Up Time	5 minutes	*	*
FREQUENCY RESPONSE, SINEWAVE INPUT			
±1% Reading Error			
Input: $7V_{rms}$	500kHz	*	*
$2V_{rms}$	700kHz	*	*
$1V_{rms}$	800kHz	*	*
$0.2V_{rms}$	120kHz	*	*
$0.1V_{rms}$	80kHz	*	*
$0.01V_{rms}$	25kHz	*	*
-3dB Reading Error			
Input: $7V_{rms}$	5MHz	*	*
$2V_{rms}$	8MHz	*	*
$1V_{rms}$	7MHz	*	*
$0.2V_{rms}$	3MHz	*	*
$0.1V_{rms}$	2MHz	*	*
$0.01V_{rms}$	300kHz	*	*
Internal Filter Time Constant	1.5ms	*	*
External Filter Time Constant[2]	15ms/μF	*	*
Total Averaging Time Constant[2]	1.5ms + 15ms/μF	*	*
CREST FACTOR			
±0.2% Additional Reading Error	7	*	*
±0.5% Additional Reading Error	10	*	*
INPUT SPECIFICATIONS			
Voltage			
Signal Range	$\pm 10V_{peak}$ min	*	*
Safe Input	$\pm V_S$	*	*
Impedance	2.5kΩ ±10%	*	*
OUTPUT SPECIFICATIONS[3]			
Rated Output			
Voltage	+10.0V min	*	*
Current	+5mA min	*	*
Impedance	0.1Ω	*	*
Offset Voltage, @ +25°C	±2mV max	*	*
With External 20kΩ Trim Pot	Adjustable to Zero	*	*
POWER SUPPLY[4]			
Voltage, Rated Specifications	±15V dc	*	*
Voltage, Operating	±(6 to 18)V dc	*	*
Current, Quiescent	±12mA	*	*
TEMPERATURE RANGE			
Rated Performance	0 to +70°C	*	*
Operating	-25°C to +85°C	*	*
Storage	-55°C to +125°C	*	*
CASE SIZE	1.5" x 1.5" x 0.4"	*	*

*Specifications same as model 442J.

**Contact sales office for complete 4 page data sheet.

[1] Error is specified as the sum of two components: a fixed term plus a percentage of output signal (reading). Refer to TOTAL ACCURACY.

[2] Connect optional filter capacitor between pin 1 and pin 2 (see Figure 2). Pin 1 is protected for shorts to ground and the positive supply voltage. Pin 1 is not protected for negative voltage greater than 1 volt.

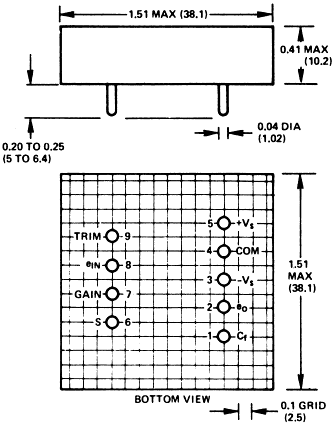
[3] Protected for short circuit to ground and/or either supply voltage.

[4] Recommended power supply: Analog Devices' model 904.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



Weight: 40 grams

MATING SOCKET AC1016

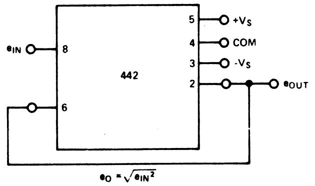
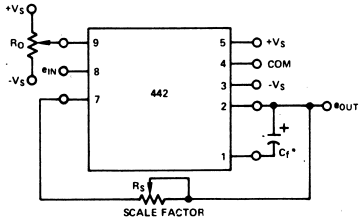


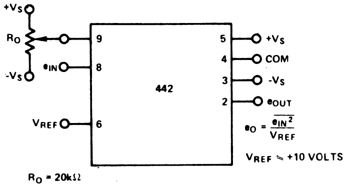
Figure 1. Wiring Connections for rms Measurements (No External Trim)



R_S = 5kΩ
R_O = 20kΩ

*SELECT C_f FOR INCREASED AVERAGING TIME CONSTANT. $\tau(ms) = 1.5 + 15C_f\ (\mu F)$

Figure 2. Optional External Adjustment for rms Measurements



R_O = 20kΩ

Figure 3. Wiring Connections for Mean Square Measurements with Adjustable Scale Factor (V_{REF})

Voltage References

Contents

	Page
Selection Guide	8–3
Orientation and Definitions of Specifications	8–4
AD580JH/KH/LH/MH/SH/TH/UH 2.5V Monolithic IC Positive Voltage References	8–5
AD581J/K/L/S/T/U 10V Pretrimmed Monolithic IC Voltage References	8–9
AD584J/K/L/S/T/U Pretrimmed 10V, 7.5V, 5V, 2.5V Monolithic IC Multiple-Voltage References	8–15
AD589JH/KH/LH/MH/SH/TH/UH Two-Terminal IC 1.2V References	8–21
AD1403/AD1403A +2.5V Monolithic IC Voltage References in Mini-DIP Package	8–25
AD2700J/L/S +10V Precision Hybrid IC Positive Voltage References	8–29
AD2701J/L/S −10V Precision Hybrid IC Negative Voltage References	8–29
AD2702J/L/S ±10V Precision Hybrid Dual Voltage References	8–29
•AD2710, AD2712KN/LN +10.000V, ±10.000 Volt Ultra High, Precision References	8–33

•New product since the *1980 Data-Acquisition Components and Subsystems Catalog*

Selection Guide
Voltage References

		AD589	AD580	AD1403	AD581	AD584	AD2700	AD2710
Output Voltage Range	1.235V	●				●		
	2.5V		●	●		●		
	5.0V					●		
	7.5V					●		
	+10.00V				●	●	●	●
	-10.00V						●	
	±10.00V						●	●
Output Voltage Tolerance	≤±0.4%		●	●				
	≤±0.05%				●	●		
	≤±0.025%						●	
	≤±0.012%							●
Temperature Stability	≤25ppm/°C	●		●				
	≤10ppm/°C		●					
	≤5ppm/°C				●	●	●	
	≤1ppm/°C							●
Temperature Range	0 to +70°C	●	●	●	●	●	●	●
	-55°C to +125°C	●	●		●	●	●	
Package Style	Hermetic Package	●	●		●	●	●	●
	Plastic Package			●				
Dice Available		●	●		●	●		
Volume I Page		8-21	8-5	8-25	8-9	8-15	8-29	8-33

Orientation

Voltage References

A voltage reference is used to provide an accurately known voltage which can be utilized in a circuit or system. For example, measurement systems rely on precision references in order to establish a basis for absolute measurement accuracy. Any reference inaccuracy will undermine the accuracy of the overall system. Thus, ideal references are characterized by accurately set (and traceable to recognized fundamental standards) constant output voltage, independent of temperature, load changes, input voltage variation, and time.

Types of References

The majority of available IC reference circuits use the bandgap principle: the V_{BE} of any silicon transistor has a negative tempco of about 2mV/°C, which can be extrapolated to approximately 1.2 volts at absolute zero (the *bandgap* voltage of silicon). Since identical transistors operating at constant current densities will have predictably different temperature coefficients of base-emitter voltage, it is possible to arrange circuit elements so as to null out the temperature coefficients associated with the two phenomena and produce a constant voltage (usually 1.2 volts). This temperature-invariant voltage can be amplified and buffered to produce a standard voltage value, such as 2.5V or 10.0V. The bandgap types catalogued here include the AD1403 and the AD580 (2.5V), the AD581 (10.0V), and the multi-output AD584 (2.5, 5.0, 7.5, and/or 10.0V).

Another popular form of reference circuit uses a selected low-drift Zener diode, followed by a buffer-amplifier-and-precision-gain stage to provide a standard output voltage. The AD2710, AD2712 families provide +10V and ±10V (dual output) using this technique. Laser-trimmed thin-film resistors are essential to secure ±1mV accuracy and ±1ppm/°C max drift in these hybrid devices.

The AD589 family are two-terminal 1.2V bandgap ICs used like Zener diodes. They are ideally suited to battery-powered instruments or portable equipment where low power consumption (and often low supply voltages) are essential. Power requirements as low as 60μW, combined with low temperature drift, provide precision performance at low cost.

Definitions of Specifications

Line regulation. The change in output voltage due to a specified change in input voltage. It is usually expressed in percent per volt or microvolts per volt of input change.

Load regulation. The change in output voltage for a specified change in load current. It is generally expressed in microvolts per milliampere, or ohms of dc output resistance. This specification includes the effect of self-heating due to increased power dissipation at higher load currents.

Output voltage tolerance. The deviation from the nominal output voltage at 25°C and specified input voltage as measured by a device traceable to a recognized fundamental voltage standard.

Output voltage change with temperature. The change in output voltage from the value at 25°C ambient; it is independent of variations in the other operating conditions. Analog Devices specifies both an error band and an equivalent temperature coefficient (in ppm/°C) for most references. The error band (e.g., ±5mV, -55°C to +125°C), is defined graphically in terms of a box (voltage vertically, temperature horizontally) whose diagonals extend from 25°C to T_{max} and 25°C to T_{min}, with a slope equal to the stated temperature coefficient. Thus, the total absolute error for a particular reference over its specified temperature range is equal to the output voltage tolerance at 25°C plus the error band.

Turn-on settling time. The time, from a cold start, for the reference output to settle within a specified error band. This definition relates only to the electrical turn-on of the chip, and does not include thermal settling time, which depends on the package, heat-sinking, and load-current change.

ANALOG DEVICES

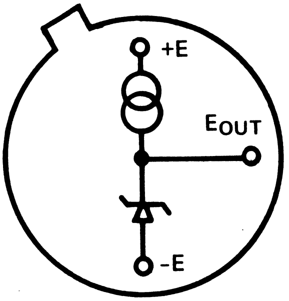
High Precision 2.5 Volt IC Reference

AD580*

FEATURES

Laser Trimmed to Higher Accuracy: 2.500V ±0.4%, Improved from ±1.0% (AD580M)
3-Terminal Device: Voltage In/Voltage Out
Excellent Temperature Stability: 10ppm/°C (AD580M, U)
Excellent Long Term Stability: 250μV (25μV/Month)
Low Quiescent Current: 1.0mA max
Small, Hermetic IC Package: TO-52 Can
3 MIL Temperature Grades (-55°C to +125°C) with MIL-STD-883, Class B Processing Available

AD580 FUNCTIONAL BLOCK DIAGRAM



TO-52
BOTTOM VIEW

PRODUCT DESCRIPTION

The AD580 is an improved three-terminal, low cost, temperature compensated, bandgap voltage reference which provides a fixed 2.5V output voltage for inputs between 4.5V and 30V. A unique combination of advanced circuit design and laser-wafer-trimmed thin-film resistors provide the AD580 with an improved initial tolerance of ±0.4%, a temperature stability of better than 10ppm/°C and long term stability of better than 250μV. In addition, the low quiescent current drain of 1.0mA max offers a clear advantage over classical zener techniques.

The AD580 is recommended as a stable reference for all 8-, 10- and 12-bit D-to-A converters that require an external reference. In addition, the wide input range of the AD580 allows operation with 5 volt logic supplies making the AD580 ideal for digital panel meter applications or whenever only a single logic power supply is available.

The AD580J, K, L and M are specified for operation over the 0 to +70°C temperature range; the AD580S, T and U are specified for operation over the extended temperature range of -55°C to +125°C.

*Covered by Patent Nos. 3,887,863; RE 30,586

PRODUCT HIGHLIGHTS

1. Laser-trimming the thin-film resistors has reduced the AD580 output error. For example, AD580L output tolerance is now ±10mV, improved from ±50mV.
2. The three-terminal voltage in/voltage out operation of the AD580 provides regulated output voltage without any external components.
3. The AD580 provides a stable 2.5V output voltage for input voltages between 4.5V and 30V. The capability to provide a stable output voltage using a 5-volt input makes the AD580 an ideal choice for systems that contain a single logic power supply.
4. Thin film resistor technology and tightly controlled bipolar processing provide the AD580 with temperature stabilities to 10ppm/°C and long term stability better than 250μV.
5. The low quiescent current drain of the AD580 makes it ideal for CMOS and other low power applications.
6. The three grades of AD580 rated for operation over the -55°C to +125°C "military" temperature range are available with processing to MIL-STD-883, Class B.

SPECIFICATIONS (typical @ +15V and 25°C unless otherwise specified)

MODEL	AD580JH	AD580KH	AD580LH	AD580MH
ABSOLUTE MAXIMUM RATINGS				
Input Voltage	40V E_{IN}	*	*	*
Power Dissipation @ +25°C				
Ambient Temperature	350mW	*	*	*
Derate Above +25°C	2.8mW/°C	*	*	*
Operating Junction Temperature Range	−55°C to +150°C	*	*	*
Storage Temperature Range	−65°C to +175°C	*	*	*
Lead Temperature (Soldering, 10 sec)	+300°C	*	*	*
Thermal Resistance				
Junction-to-Case	100°C/W	*	*	*
Junction-to-Ambient	360°C/W	*	*	*
Specified Operating Temperature Range	0 to +70°C	*	*	*
OUTPUT VOLTAGE TOLERANCE (Error from Nominal 2.500 Volt Output)	±75mV max	±25mV max	±10mV max	±10mV max
OUTPUT VOLTAGE CHANGE				
T_{min} to T_{max}	15mV max (85ppm/°C)	7mV max (40ppm/°C)	4.3mV max (25ppm/°C)	1.75mV max (10ppm/°C)
LINE REGULATION				
$7V \leq V_{IN} \leq 30V$	6mV max (1.5mV typ)	4mV max (1.5mV typ)	2mV max	2mV max
$4.5 \leq V_{IN} \leq 7V$	3mV max (0.3mV typ)	2mV max (0.3mV typ)	1mV max	1mV max
LOAD REGULATION				
$\Delta I = 10mA$, $V_{IN} = +15V$	10mV max	*	*	*
QUIESCENT CURRENT	1.5mA max (1.0mA typ)	*	*	*
NOISE (0.1Hz to 10Hz)	60μV (p-p)	*	*	*
STABILITY				
Long Term	250μV	*	*	*
Per Month	25μV	*	*	*
PACKAGE STYLE[1] TO-52	H	*	*	*

MODEL	AD580SH (AD580SH/883B)[2]	AD580TH (AD580TH/883B)[2]	AD580UH (AD580UH/883B)[2]
ABSOLUTE MAXIMUM RATINGS			
Input Voltage	40V E_{IN}	**	**
Power Dissipation @ +25°C			
Ambient Temperature	350mW	**	**
Derate Above +25°C	2.8mW/°C	**	**
Operating Junction Temperature Range	−55°C to +150°C	**	**
Storage Temperature Range	−65°C to +175°C	**	**
Lead Temperature (Soldering, 10 sec)	+300°C	**	**
Thermal Resistance			
Junction-to-Case	100°C/W	**	**
Junction-to-Ambient	360°C/W	**	**
Specified Operating Temperature Range	−55°C to +125°C	**	**
OUTPUT VOLTAGE TOLERANCE (Error from Nominal 2.500 Volt Output)	±25mV max	±10mV max	±10mV max
OUTPUT VOLTAGE CHANGE			
T_{min} to T_{max}	25mV max (55ppm/°C)	11mV max (25ppm/°C)	4.5mV max (10ppm/°C)
LINE REGULATION			
$7V \leq V_{IN} \leq 30V$	6mV max (1.5mV typ)	2mV max	2mV max
$4.5 \leq V_{IN} \leq 7V$	3mV max (0.3mV typ)	1mV max	1mV max
LOAD REGULATION			
$\Delta I = 10mA$, $V_{IN} = +15V$	10mV max	**	**
QUIESCENT CURRENT	1.5mA max (1.0mA typ)	**	**
NOISE (0.1Hz to 10Hz)	60μV (p-p)	**	**
STABILITY			
Long Term	250μV	**	**
Per Month	25μV	**	**
PACKAGE STYLE[1] TO-52	H	**	**

*Specifications same as AD580JH

**Specifications same as AD580SH

[1] See Section 20 for package outline information.

[2] The AD580SH, TH and UH are available processed and screened to the requirements of MIL-STD-883, Class B. When ordering, specify AD580XH/883B.

Specifications subject to change without notice.

Applying the AD580

THEORY OF OPERATION

Most precision IC references use complex multichip hybrid designs based on expensive temperature-compensated zener diodes. Others are monolithic with on-chip zener diodes; these often require more than one power supply and, with the zener breakdown occuring near 6.3 volts, will not operate from a low voltage logic supply.

The AD580 family (AD580, AD581, AD584, AD589) uses the "bandgap" concept to produce a stable, low-temperature-coefficient voltage reference suitable for high accuracy data-acquisition components and systems. The device makes use of the underlying physical nature of a silicon transistor base-emitter voltage in the forward-biased operating region. All such transistors have approximately a -2mV/°C temperature coefficient, unsuitable for use directly as a low TC reference; however, extrapolation of the temperature characteristic of any one of these devices to absolute zero (with emitter current proportional to absolute temperature) reveals that it will go to a V_{BE} of 1.205 volts 0°K, as shown in Figure 1. Thus, if a voltage could be developed with an opposing temperature coefficient to sum with V_{BE} to total 1.205 volts, a zero-TC reference would result and operation from a single, low-voltage supply would be possible. The AD580 circuit provides such a compensating voltage, V_1 in Figure 2, by driving two transistors at different current densities and amplifying the resulting V_{BE} difference (ΔV_{BE} – which now has a positive TC); the sum (V_Z) is then buffered and amplified up to 2.5 volts to provide a usable reference-voltage output. Figure 3 is the schematic diagram of the AD580.

The AD580 operates as a three-terminal reference, that means that no additional components are required for biasing or current setting. The connection diagram, Figure 4 is quite simple.

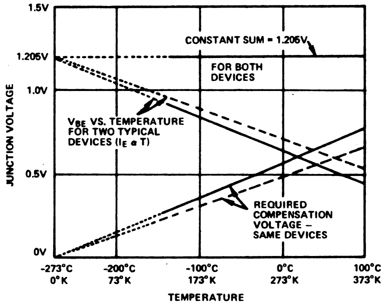


Figure 1. Extrapolated Variation of Base-Emitter Voltage with Temperature ($I_E \alpha T$), and Required Compensation, Shown for Two Different Devices

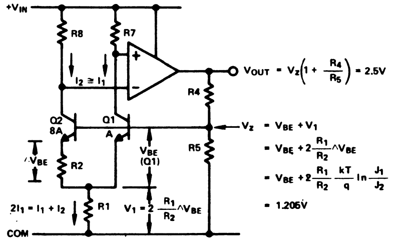


Figure 2. Basic Bandgap-Reference Regulator Circuit

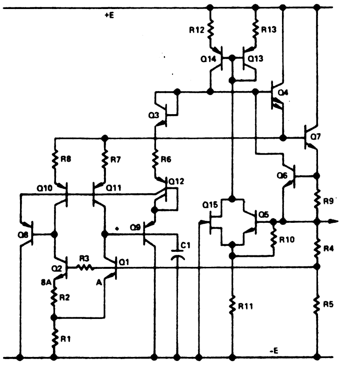


Figure 3. AD580 Schematic Diagram

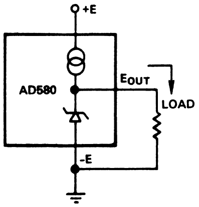


Figure 4. AD580 Connection Diagram

VOLTAGE VARIATION VS. TEMPERATURE

Some confusion exists in the area of defining and specifying reference voltage error over temperature. Historically, references are characterized using a maximum deviation per degree Centigrade; i.e., 10ppm/°C. However, because of the inconsistent nonlinearities in zener references (butterfly or "S" type characteristics), most manufacturers use a maximum limit error band approach to characterize their references. This technique measures the output voltage at 3 to 5 different temperatures and guarantees that the output voltage deviation will fall within the guaranteed error band at these discrete temperatures. This approach, of course, makes no mention or guarantee of performance at any other temperature within the operating temperature range of the device.

The consistent Voltage vs. Temperature performance of a typical AD580 is shown in Figure 5. Note that the characteristic is quasi-parabolic, not the possible "S" type characteristics of classical zener references. This parabolic characteristic permits a maximum output deviation specification over the device's full operating temperature range, rather than just at 3 to 5 discrete temperatures.

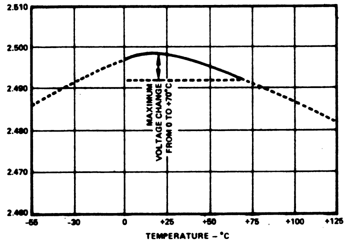


Figure 5. Typical AD580K Output/Voltage vs. Temperature

The AD580M guarantees a maximum deviation of 1.75mV over the 0 to +70°C temperature range. This can be shown to be equivalent to 10ppm/°C average maximum; i.e. . .

$$\frac{1.75\text{mV max}}{70^\circ\text{C}} \times \frac{1}{2.5\text{V}} = 10\text{ppm}/^\circ\text{C max average}$$

The AD580 typically exhibits a variation of 1.5mV over the power supply range of 7 to 30 volts. Figure 6 is a plot of AD580 line rejection versus frequency.

NOISE PERFORMANCE

Figure 7 represents the peak-to-peak noise of the AD580 from 1Hz (3dB point) to a 3dB high end shown on the horizontal axis. Peak-to-peak noise from 1Hz to 1MHz is approximately 600μV.

THE AD580 AS A CURRENT LIMITER

The AD580 represents an excellent alternative to current limiter diodes which require factory-selection to achieve a desired current. This approach often results in temperature coefficients of 1%/°C. The AD580 approach is not limited to a specially selected factory set current limit; it can be programmed from 1 to 10mA with the insertion of a single external resistor. The approximate temperature coefficient of current limit for the AD580 used in this mode is 0.13%/°C for I_{LIM} = 1mA and 0.01%/°C for I_{LIM} = 13mA (see Figure 9). Figure 8 displays the high output impedance of the AD580 used as a current limiter for I_{LIM} = 1, 2, 3, 4, 5mA.

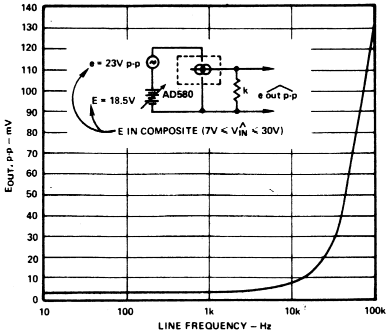


Figure 6. AD580 Line Rejection Plot

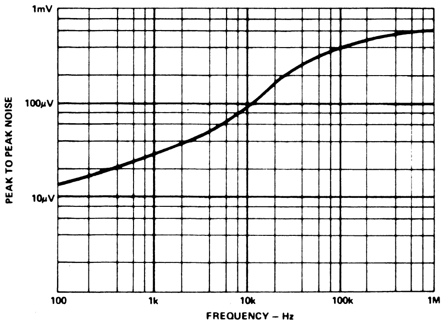


Figure 7. Peak-to-Peak Output Noise vs. Frequency

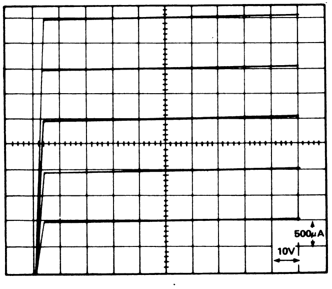


Figure 8. Input Current vs. Input Voltage (Integral Loads)

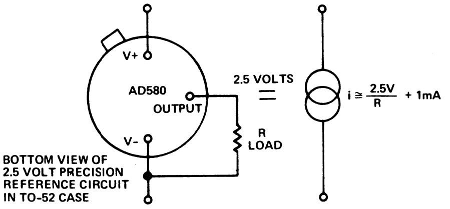


Figure 9. A Two-Component Precision Current Limiter

THE AD580 AS A LOW POWER, LOW VOLTAGE PRECISION REFERENCE FOR DATA CONVERTERS

The AD580 has a number of features that make it ideally suited for use with A/D and D/A data converters used in complex microprocessor-based systems. The calibrated 2.500 volt output minimizes user trim requirements and allows operation from a single low voltage supply. Low power consumption (1mA quiescent current) is commensurate with that of CMOS-type devices, while the low cost and small package complements the decreasing cost and size of the latest converters.

Figure 10 shows the AD580 used as a reference for the AD7542 12-bit CMOS DAC with complete microprocessor interface. The AD580 and the AD7542 are specified to operate from a single 5 volt supply; this eliminates the need to provide a +15 volt power supply for the sole purpose of operating a reference. The AD7542 includes three 4-bit data registers, a 12-bit DAC register, and address decoding logic; it may thus be interfaced directly to a 4-, 8- or 16-bit data bus. Only 8mA of quiescent current from the single +5 volt supply is required to operate the AD7542 which is packaged in a small 16-pin DIP. The AD544 output amplifier is also low power, requiring only 2.5mA quiescent current. Its laser-trimmed offset voltage preserves the ±1/2LSB linearity of the AD7542KN without user trims and it typically settles to ±1/2 LSB in less than 3μs. It will provide the 0 to −2.5 volt output swing from ±5 volt supplies.

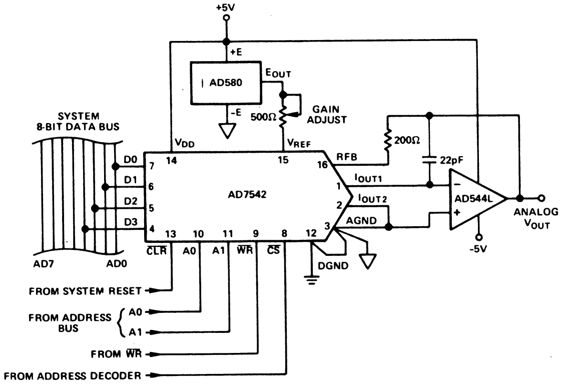


Figure 10. Low Power, Low Voltage Reference for the AD7542 Microprocessor-Compatible 12-Bit DAC

ANALOG DEVICES

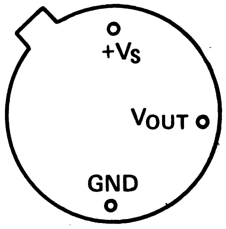
High Precision 10 Volt IC Reference

AD581*

FEATURES

Laser-Trimmed to High Accuracy:
10.000 Volts ±5mV (L and U)
Trimmed Temperature Coefficient:
5ppm/°C max, 0 to +70°C (L)
10ppm/°C max, -55°C to +125°C (U)
Excellent Long-Term Stability:
25ppm/1000 hrs. (Non-Cumulative)
Negative 10 Volt Reference Capability
Low Quiescent Current: 1.0mA max
10mA Current Output Capability
3-Terminal TO-5 Package
Low Cost

AD581 PIN CONFIGURATION



TO-5
BOTTOM VIEW

PRODUCT DESCRIPTION

The AD581 is a three-terminal, temperature compensated, monolithic band-gap voltage reference which provides a precise 10.00 volt output from an unregulated input level from 12 to 30 volts. Laser Wafer Trimming (LWT) is used to trim both the initial error at +25°C as well as the temperature coefficient, which results in high precision performance previously available only in expensive hybrids or oven-regulated modules. The 5mV initial error tolerance and 5ppm/°C guaranteed temperature coefficient of the AD581L represent the best performance combination available in a monolithic voltage reference.

The band-gap circuit design used in the AD581 offers several advantages over classical zener breakdown diode techniques. Most important, no external components are required to achieve full accuracy and stability of significance to low power systems. In addition, total supply current to the device, including the output buffer amplifier (which can supply up to 10mA) is typically 750μA. The long-term stability of the band-gap design is equivalent or superior to selected zener reference diodes.

The AD581 is recommended for use as a reference for 8-, 10- or 12-bit D/A converters which require an external precision reference. The device is also ideal for all types of A/D converters up to 14 bit accuracy, either successive approximation or integrating designs, and in general can offer better performance than that provided by standard self-contained references.

The AD581J, K, and L are specified for operation from 0 to +70°C; the AD581S, T, and U are specified for the -55°C to +125°C range. The AD581S, T, and U grades are also available processed to MIL-STD-883A, Level B. All grades are packaged in a hermetically-sealed three-terminal TO-5 metal can.

PRODUCT HIGHLIGHTS

1. Laser trimming of both initial accuracy and temperature coefficient results in very low errors over temperature without the use of external components. The AD581L has a maximum deviation from 10.000 volts of ±7.25mV from 0 to +70°C, while the AD581U guarantees ±15mV maximum total error without external trims from -55°C to +125°C.
2. Since the laser trimming is done on the wafer prior to separation into individual chips, the AD581 will be extremely valuable to hybrid designers for its ease of use, lack of required external trims, and inherent high performance.
3. The AD581 can also be operated in a two-terminal "Zener" mode to provide a precision negative 10 volt reference with just one external resistor to the unregulated supply. The performance in this mode is nearly equal to that of the standard three-terminal configuration.
4. Advanced circuit design using the band-gap concept allows the AD581 to give full performance with an unregulated input voltage down to 13 volts. With an external resistor, the device will operate with a supply as low as 11.4 volts.

***Covered by Patent Nos. 3,887,863; RE30,586**

SPECIFICATIONS (typical @ V_{IN} = +15V and +25°C unless otherwise noted)

MODEL	AD581J	AD581K	AD581L	AD581S	AD581T	AD581U
ABSOLUTE MAX RATINGS						
Input Voltage V_{IN} to Ground	40V	*	*	*	*	*
Power Dissipation @ +25°C	600mW	*	*	*	*	*
Operating Junction Temp. Range	−55°C to +150°C	*	*	*	*	*
Storage Temperature Range	−65°C to +175°C	*	*	*	*	*
Lead Temperature (Soldering, 10sec)	+300°C	*	*	*	*	*
Thermal Resistance Junction-to-Ambient	150°C/Watt	*	*	*	*	*
Operating Temperature Range	0 to +70°C	*	*	−55°C to +125°C	**	**
OUTPUT VOLTAGE TOLERANCE (Error from nominal 10.000V output)	±30mV max	±10mV max	±5mV max	±30mV max	±10mV max	±5mV max
OUTPUT VOLTAGE CHANGE Maximum Deviation from +25°C Value T_{min} to T_{max} (Temperature Coefficient)	±13.5mV (30ppm/°C)	±6.75mV (15ppm/°C)	±2.25mV (5ppm/°C)	±30mV (30ppm/°C)	±15mV (15ppm/°C)	±10mV (10ppm/°C)
LINE REGULATION						
$15V \leq V_{IN} \leq 30V$	3mV max (0.002%/V)	*	*	*	*	*
$13V \leq V_{IN} \leq 15V$	1mV max (0.005%/V)	*	*	*	*	*
LOAD REGULATION $0 \leq I_{OUT} \leq 5mA$	500μV/mA max 200μV/mA typ	* *	* *	* *	* *	* *
QUIESCENT CURRENT	1.0mA max 750μA typ	* *	* *	* *	* *	* *
TURN-ON SETTLING TIME TO 0.1%[1]	200μs	*	*	*	*	*
NOISE (0.1 to 10Hz)	50μV p-p	*	*	*	*	*
LONG-TERM STABILITY	25ppm/1000 Hrs. (Non-Cumulative)	*	*	*	*	*
SHORT CIRCUIT CURRENT	30mA	*	*	*	*	*
OUTPUT CURRENT						
Source @ +25°C	10mA min	*	*	*	*	*
Source T_{min} to T_{max}	5mA min	*	*	*	*	*
Sink T_{min} to T_{max}	5mA min	*	*	200μA min	**	**
Sink −55°C to +85°C	—	—	—	5mA min	**	**
PACKAGE STYLE:[2] TO-5	"H"	*	*	*	*	*

*Specifications same as AD581J.

**Specifications same as AD581S.

[1] See Figure 6.

[2] See Section 20 for package outline information.

Specification subject to change without notice.

APPLYING THE AD581

The AD581 is easy to use in virtually all precision reference applications. The three terminals are simply primary supply, ground, and output, with the case grounded. No external components are required even for high precision applications; the degree of desired absolute accuracy is achieved simply by selecting the required device grade. The AD581 requires less than 1mA quiescent current from an operating supply range of 12 to 30 volts.

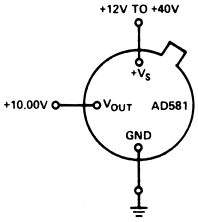
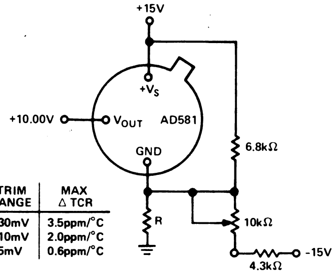


Figure 1. AD581 Pin Configuration (Top View)

An external fine trim may be desired to set the output level to exactly 10.000 volts within less than a millivolt (calibrated to a main system reference). System calibration may also require a reference slightly different from 10.00 volts. In either case, the optional trim circuit shown in Figure 2 can offset the output by up to ±30 millivolts (with the 22Ω resistor), if needed, with minimal effect on other device characteristics.



R	TRIM RANGE	MAX Δ TCR
22Ω	±30mV	3.5ppm/°C
12Ω	±10mV	2.0ppm/°C
3.9Ω	±5mV	0.6ppm/°C

Figure 2. Optional Fine Trim Configuration

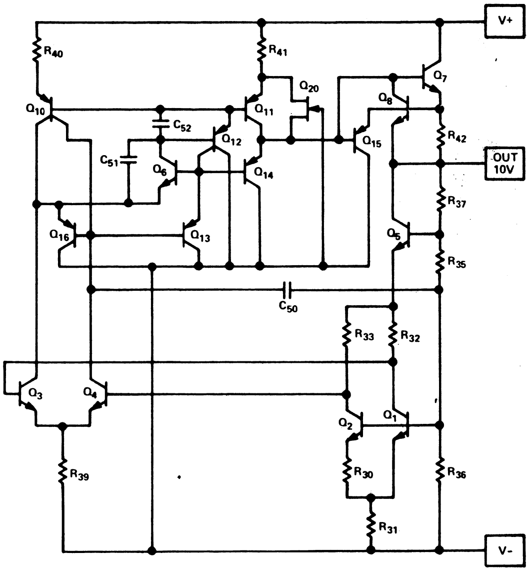


Figure 3. Simplified Schematic

VOLTAGE VARIATION vs. TEMPERATURE

Some confusion exists in the area of defining and specifying reference voltage error over temperature. Historically, references have been characterized using a maximum deviation per degree Centigrade; i.e., 10ppm/°C. However, because of nonlinearities in temperature characteristics, which originated in standard zener references (such as "S" type characteristics) most manufacturers have begun to use a maximum limit error band approach to specify devices. This technique involves measurement of the output at 3, 5 or more different temperatures to guarantee that the output voltage will fall within the given error band. The temperature characteristic of the AD581 consistently follows the S-curve shown in Figure 4. Five-point measurement of each device guarantees the error band over the -55°C to +125°C range; three-point measurement guarantees the error band from 0 to +70°C.

The error band which is guaranteed with the AD581 is the maximum deviation from the initial value at +25°C; this error band is of more use to a designer than one which simply guarantees the maximum total change over the entire range (i.e., in the latter definition, all of the changes could occur in the positive direction). Thus, with a given grade of the AD581, the designer can easily determine the maximum total error from initial tolerance plus temperature variation (e.g., for the AD581T, the initial tolerance is ±10mV, the temperature error band is ±15mV, thus the unit is guaranteed to be 10.000 volts ±25mV from -55°C to +125°C).

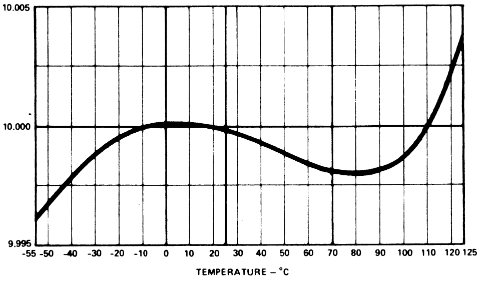


Figure 4. Typical Temperature Characteristic

OUTPUT CURRENT CHARACTERISTICS

The AD581 has the capability to either source or sink current and provide good load regulation in either direction, although it has better characteristics in the source mode (positive current into the load). The circuit is protected for shorts to either positive supply or ground. The output voltage vs. output current characteristics of the device are shown in Figure 5. Source current is displayed as negative current in the figure; sink current is positive. Note that the short circuit current (i.e., zero volts output) is about 28mA; when shorted to +15 volts, the sink current goes to about 20mA.

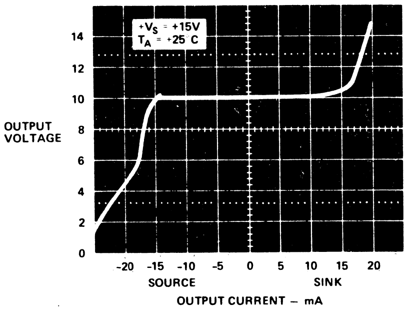


Figure 5. AD581 Output Voltage vs. Sink and Source Current

DYNAMIC PERFORMANCE

Many low power instrument manufacturers are becoming increasingly concerned with the turn-on characteristics of the components being used in their systems. Fast turn-on components often enable the end user to keep power off when not needed, and yet respond quickly when the power is turned on for operation. Figure 6 displays the turn-on characteristic of the AD581. This characteristic is generated from cold-start operation and represents the true turn-on waveform after an extended period with the supplies off. The figure shows both the coarse and fine transient characteristics of the device; the total settling time to within ±1 millivolt is about 180µs, and there is no long thermal tail appearing after the point.

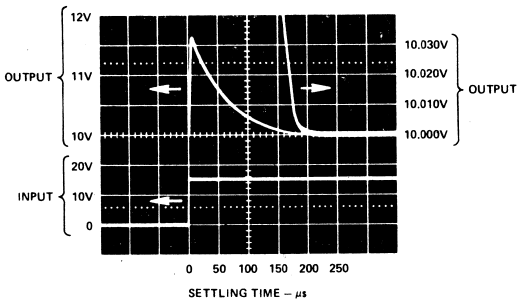


Figure 6. Output Settling Characteristic

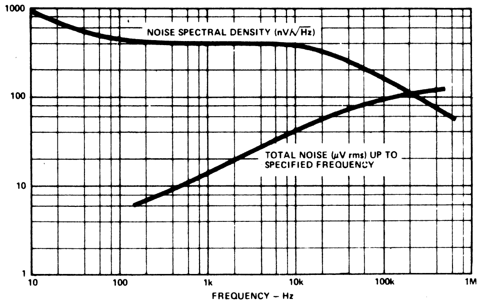


Figure 7. Spectral Noise Density and Total rms Noise vs. Frequency

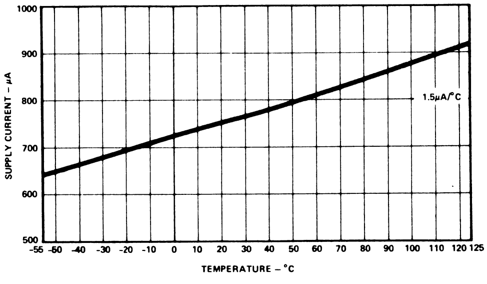


Figure 8. Quiescent Current vs. Temperature

PRECISION HIGH CURRENT SUPPLY

The AD581 can be easily connected with power pnp or power darlington pnp devices to provide much greater output current capability. The circuit shown in Figure 9 delivers a precision 10 volt output with up to 4 amperes supplied to the load. The 0.1µF capacitor is required only if the load has a significant capacitive component. If the load is purely resistive, improved high frequency supply rejection results from removing the capacitor.

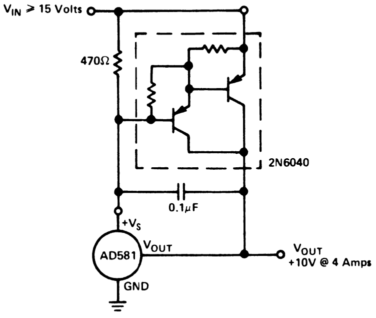


Figure 9. High Current Precision Supply

CONNECTION FOR REDUCED PRIMARY SUPPLY

While line regulation is specified down to 13 volts, the typical AD581 will work as specified down to 12 volts or below. The current sink capability allows even lower supply voltage capability such as operation from 12V ±5% as shown in Figure 10. The 560Ω resistor reduces the current supplied by the AD581 to a manageable level at full 5mA load. Note that other bandgap references, without current sink capability, may be damaged by use in this circuit configuration.

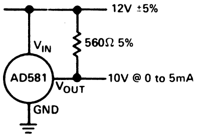


Figure 10. 12-Volt Supply Connection

THE AD581 AS A CURRENT LIMITER

The AD581 represents an alternative to current limiter diodes which require factory selection to achieve a desired current. This approach often results in temperature coefficients of 1%/°C. The AD581 approach is not limited to a defined set current limit; it can be programmed from 0.75 to 5mA with the insertion of a single external resistor. Of course, the minimum voltage required to drive the connection is 13 volts. The AD580, which is a 2.5 volt reference, can be used in this type of circuit with compliance voltage down to 4.5 volts.

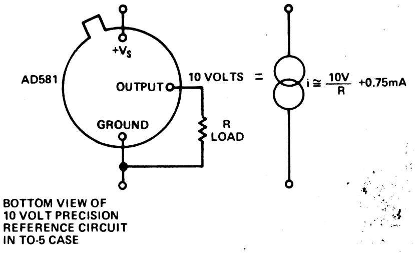


Figure 11. A Two-Component Precision Current Limiter

NEGATIVE 10-VOLT REFERENCE

The AD581 can also be used in a two-terminal "zener" mode to provide a precision -10.00 volt reference. As shown in Figure 12, the V_{IN} and V_{OUT} terminals are connected together to the high supply (in this case, ground). The ground pin is connected through a resistor to the negative supply. The output is now taken from the ground pin instead of V_{OUT}. With 1mA flowing through the AD581 in this mode, a typical unit will show a 2mV increase in output level over that produced in the three-terminal mode. Note also that the effective output impedance in this connection increases from 0.2Ω typical to 2 ohms. It is essential to arrange the output load and the supply resistor, R_S, so that the net current through the AD581 is always between 1 and 5mA. The temperature characteristics and long-term stability of the device will be essentially the same as that of a unit used in the standard three-terminal mode. The operating temperature range is limited to -55°C to +85°C.

The AD581 can also be used in a two-terminal mode to develop a positive reference. V_{IN} and V_{OUT} are tied together and to the positive supply through an appropriate supply resistor. The performance characteristics will be similar to those of the negative two-terminal connection. The only advantage of this connection over the standard three-terminal connection is that a lower primary supply can be used, as low as 10.5 volts. This type of operation will require considerable attention to load and primary supply regulation to be sure the AD581 always remains within its regulating range of 1 to 5mA.

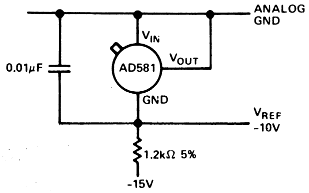


Figure 12. Two-Terminal -10 Volt Reference

10 VOLT REFERENCE WITH MULTIPLYING CMOS D/A OR A/D CONVERTERS

The AD581 is ideal for application with the entire AD7520 series of 10- and 12-bit multiplying CMOS D/A converters, especially for low power applications. It is equally suitable for the AD7574 8-bit A/D converter. In the standard hook-up, as shown in Figure 13, the +10 volt reference is inverted by the amplifier/DAC configuration to produce a 0 to −10 volt range. If an AD308 amplifier is used, total quiescent supply current will typically be 2mA. If a 0 to +10 volt full scale range is desired, the AD581 can be connected to the CMOS DAC in its −10 volt "zener" mode, as shown in Figure 12 (the $-10V_{REF}$ output is connected directly to the $V_{REF\ IN}$ of the CMOS DAC). The AD581 will normally be used in the −10 volt mode with the AD7574 to give a 0 to +10 volt ADC range. This is shown in Figure 14. Bipolar output applications and other operating details can be found in the data sheets for the CMOS products.

PRECISION 12-BIT D/A CONVERTER REFERENCE

The AD562, like most D/A converters, is designed to operate with a +10 volt reference element. In the AD562, this 10 volt reference voltage is converted into a reference current of approximately 0.5mA via the internal 19.95kΩ resistor (in series with the external 100Ω trimmer). The gain temperature coefficient of the AD562 is primarily governed by the temperature tracking of the 19.95kΩ resistor and the 5k/10k span resistors; this gain T.C. is guaranteed to 3ppm/°C. Thus, using the AD581L (at 5ppm/°C) as the 10 volt reference guarantees a maximum full scale temperature coefficient of 8ppm/°C over the commercial range. The 10 volt reference also supplies the normal 1mA bipolar offset current through the 9.95k bipolar offset resistor. The bipolar offset T.C. thus depends only on the T.C. matching of the bipolar offset resistor to the input reference resistor and is guaranteed to 3ppm/°C.

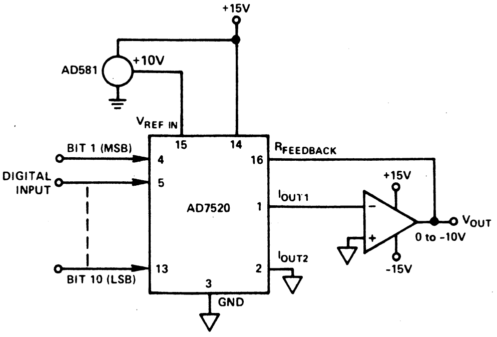
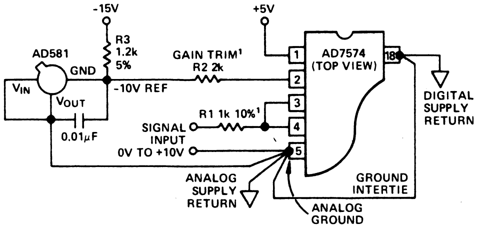


Figure 13. Low Power 10-Bit CMOS DAC Application



NOTE 1: R1 AND R2 CAN BE OMITTED IF GAIN TRIM IS NOT REQUIRED

Figure 14. AD581 as Negative 10-Volt Reference for CMOS ADC

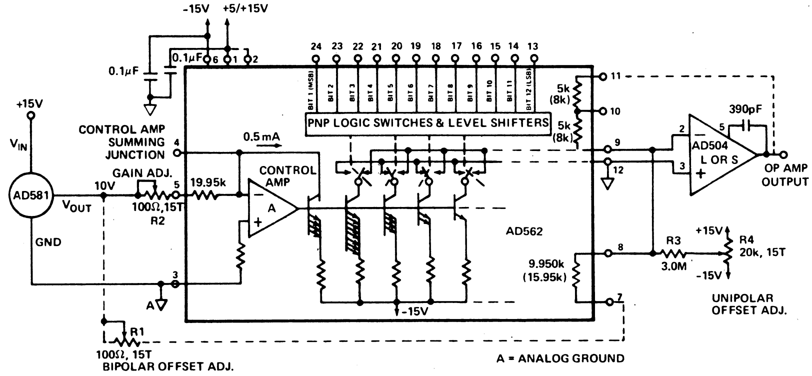


Figure 15. Precision 12-Bit D/A Converter

ANALOG DEVICES

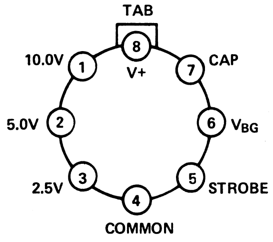
Pin Programmable Precision Voltage Reference

AD584*

FEATURES

Four Programmable Output Voltages:
10.000V, 7.500V, 5.000V, 2.500V
Laser-Trimmed to High Accuracies
No External Components Required
Trimmed Temperature Coefficient:
5ppm/°C max, 0 to +70°C (AD584LH)
15ppm/°C max, -55°C to +125°C (AD584TH)
Zero Output Strobe Terminal Provided
Two Terminal Negative Reference Capability (5V & Above)
Output Sources or Sinks Current
Low Quiescent Current: 1.0mA max
10mA Current Output Capability
Low Cost

AD584 PIN CONFIGURATION



TO-99
TOP VIEW

PRODUCT DESCRIPTION

The AD584 is an eight-terminal precision voltage reference offering pin-programmable selection of four popular output voltages: 10.000V, 7.500V, 5.000V and 2.500V. Other output voltages, above, below or between the four standard outputs, are available by the addition of external resistors. Input voltage may vary between 4.5 and 30 volts.

Laser Wafer Trimming (LWT) is used to adjust the pin-programmable output levels and temperature coefficients, resulting in the most flexible high precision voltage reference available in monolithic form.

In addition to the programmable output voltages, the AD584 offers a unique strobe terminal which permits the device to be turned on or off. When the AD584 is used as a power supply reference, the supply can be switched off with a single, low-power signal. In the "off" state the current drain by the AD584 is reduced to about 100μA. In the "on" state the total supply current is typically 750μA including the output buffer amplifier.

The AD584 is recommended for use as a reference for 8-, 10- or 12-bit D/A converters which require an external precision reference. The device is also ideal for all types of A/D converters of up to 14 bit accuracy, either successive approximation or integrating designs, and in general can offer better performance than that provided by standard self-contained references.

The AD584J, K, and L are specified for operation from 0 to +70°C; the AD584S and T are specified for the -55°C to +125°C range. The AD581S and T grades are also available processed to MIL-STD-883B, Level B. All grades are packaged in a hermetically-sealed eight-terminal TO-99 metal can.

PRODUCT HIGHLIGHTS

1. The flexibility of the AD584 eliminates the need to design-in and inventory several different voltage references. Furthermore one AD584 can serve as several references simultaneously when buffered properly.
2. Laser trimming of both initial accuracy and temperature coefficient results in very low errors over temperature without the use of external components. The AD584LH has a maximum deviation from 10.000 volts of ±7.25mV from 0 to +70°C.
3. The AD584 can be operated in a two-terminal "Zener" mode at 5 volts output and above. By connecting the input and the output, the AD584 can be used in this "Zener" configuration as a negative reference.
4. The output of the AD584 is configured to sink or source currents. This means that small reverse currents can be tolerated in circuits using the AD584 without damage to the reference and without disturbing the output voltage (10V, 7.5V and 5V outputs).

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*Covered by U.S. Patent No. 3,887,863; RE 30,586

SPECIFICATIONS (typical @ V_{IN} = +15V and +25°C unless otherwise noted)

MODEL	AD584JH	AD584KH	AD584LH	AD584SH	AD584TH
ABSOLUTE MAX RATINGS					
Input Voltage V_{IN} to Ground	40V	*	*	*	*
Power Dissipation @ +25°C	600mW	*	*	*	*
Operating Junction Temp. Range	−55°C to +150°C	*	*	*	*
Storage Temperature Range	−65°C to +175°C	*	*	*	*
Lead Temperature Soldering, 10sec)	+300°C	*	*	*	*
Thermal Resistance Junction-to-Ambient	150°C/Watt	*	*	*	*
Operating Temperature Range	0 to +70°C	*	*	−55°C to +125°C	**
OUTPUT VOLTAGE TOLERANCE Maximum Error[1] for Nominal Outputs of:					
10.000V	±30mV	±10mV	±5mV	±30mV	±10mV
7.500V	±22mV	±8mV	±4mV	±22mV	±8mV
5.000V	±15mV	±6mV	±3mV	±15mV	±6mV
2.500V	±7.5mV	±3.5mV	±2.5mV	±7.5mV	±3.5mV
OUTPUT VOLTAGE CHANGE Maximum Deviation from +25°C Value, T_{min} to T_{max}[2]					
10.000, 7.500, 5.000V Outputs	30ppm/°C	15ppm/°C	5ppm/°C	30ppm/°C	15ppm/°C
2.500V Output	30ppm/°C	15ppm/°C	10ppm/°C	30ppm/°C	20ppm/°C
Differential Temperature Coefficients Between Outputs	5ppm/°C typ	3ppm/°C typ	3ppm/°C typ	5ppm/°C typ	3ppm/°C typ
QUIESCENT CURRENT	1.0mA max	*	*	*	*
	750µA typ	*	*	*	*
Temperature Variation	1.5µA/°C typ	*	*	*	*
TURN-ON SETTLING TIME TO 0.1%	200µs	*	*	*	*
NOISE (0.1 to 10Hz)	50µV p-p	*	*	*	*
LONG-TERM STABILITY	25ppm/1000 Hrs. (Non-Cumulative)	*	*	*	*
SHORT CIRCUIT CURRENT	30mA	*	*	*	*
LINE REGULATION (No Load)					
$15V \leq V_{IN} \leq 30V$	0.002%/V	*	*	*	*
$(V_{OUT} + 2.5V) \leq V_{IN} \leq 15V$	0.005%/V	*	*	*	*
LOAD REGULATION					
$0 \leq I_{OUT} \leq 5mA$, All Outputs	50ppm/mA max	*	*	*	*
	(20ppm/mA typ)	*	*	*	*
OUTPUT CURRENT					
$V_{IN} \geq V_{OUT} + 2.5V$					
Source @ +25°C	10mA min	*	*	*	*
Source T_{min} to T_{max}	5mA min	*	*	*	*
Sink T_{min} to T_{max}	5mA min	*	*	200µA min	**
Sink −55°C to +85°C	–	–	–	5mA min	**
PACKAGE STYLE:[3]					
TO-99 Style (H08A)	H	*	*	*	*

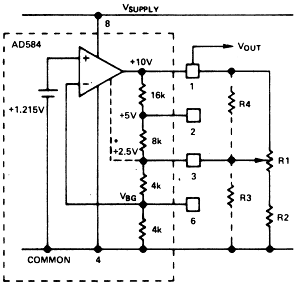
*Specifications same as AD584JH.
**Specifications same as AD584SH.
[1] At Pin 1.
[2] Calculated as average over the operating temperature range.
[3] See Section 20 for package outline information.
Specifications subject to change without notice.

APPLYING THE AD584

With power applied to pins 8 and 4 and all other pins open the AD584 will produce a buffered nominal 10.0V output between pins 1 and 4 (see Figure 1). The stabilized output voltage may be reduced to 7.5V, 5.0V or 2.5V by connecting the programming pins as follows:

OUTPUT VOLTAGE	PIN PROGRAMMING
7.5V	Join the 2.5V and 5.0V pins (2) and (3).
5.0V	Connect the 5.0V pin (2) to the output pin (1).
2.5V	Connect the 2.5V pin (3) to the output pin (1).

The options shown above are available without the use of any additional components. Multiple outputs using only one AD584, are also possible by simply buffering each voltage programming pin with a unity-gain noninverting op amp.



*THE 2.5V TAP IS USED INTERNALLY AS A BIAS POINT AND SHOULD NOT BE CHANGED BY MORE THAN 100mV IN ANY TRIM CONFIGURATION.

Figure 1. Variable Output Options

The AD584 can also be programmed over a wide range of output voltages, including voltages greater than 10V, by the addition of one or more external resistors. Figure 1 illustrates the general adjustment procedure, with approximate values given for the internal resistors of the AD584. The AD584 may be modeled as an op amp with a noninverting feedback connection, driven by a high stability 1.215 volt bandgap reference (see Figure 3 for schematic).

When the feedback ratio is adjusted with external resistors, the output amplifier can be made to multiply the reference voltage by almost any convenient amount, making popular outputs of 10.24V, 5.12V, 2.56V or 6.3V easy to obtain. The most general adjustment (which gives the greatest range and poorest resolution) uses R1 and R2 alone (see Figure 1). As R1 is adjusted to its upper limit the 2.5V pin 3 will be connected to the output, which will reduce to 2.5V. As R1 is adjusted to its lower limit, the output voltage will rise to a value limited by R2. For example, if R2 is about 6kΩ, the upper limit of the output range will be about 20V even for large values of R1. R2 should not be omitted; its value should be chosen to limit the output to a value which can be tolerated by the load circuits. If R2 is zero, adjusting R1 to its lower limit will result in a loss of control over the output voltage. If precision voltages are required to be set at levels other than the standard outputs, the 20% absolute tolerance in the internal resistor ladder must be accounted for.

Alternatively, the output voltage can be raised by loading the 2.5V tap with R3 alone. The output voltage can be lowered by connecting R4 alone. Either of these resistors can be a fixed resistor selected by test or an adjustable resistor. In all cases the resistors should have a low temperature coefficient to match the AD584 internal resistors, which have a negative T.C. less than 60ppm/°C. If both R3 and R4 are used, these resistors should have matched temperature coefficients.

When only small adjustments or trims are required, the circuit of Figure 2 offers better resolution over a limited trim range. The circuit can be programmed to 5.0V, 7.5V or 10V and adjusted by means of R1 over a range of about ±200mV. To trim the 2.5V output option, R2 (Figure 2) can be reconnected to the bandgap reference (pin 6). In this configuration, the adjustment should be limited to ±100mV in order to avoid affecting the performance of the AD584.

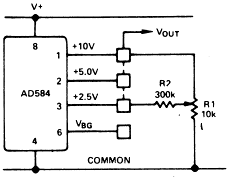


Figure 2. Output Trimming

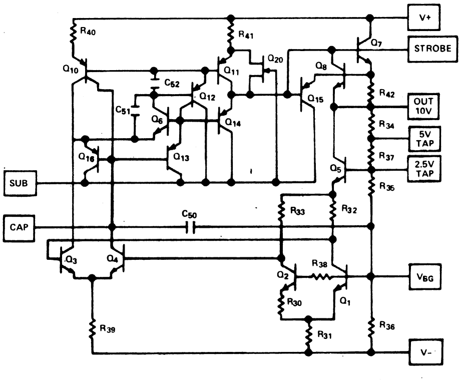


Figure 3. Schematic Diagram

Performance of the AD584

PERFORMANCE OVER TEMPERATURE

Each AD584 is tested at five temperatures over the -55°C to +125°C range to ensure that each device falls within the Maximum Error Band (see Figure 4) specified for a particular grade (i.e., S and T grades); three-point measurement guarantees performance within the error band from 0 to +70°C (i.e., J, K, or L grades). The error band guaranteed for the AD584 is the maximum deviation from the initial value at +25°C. Thus, given the grade of the AD584, the designer can easily determine the maximum total error from initial tolerance plus temperature variation. For example, for the AD584T, the initial tolerance is ±10mV and the error band is ±15mV. Hence, the unit is guaranteed to be 10.000 volts ±25mV from -55°C to +125°C.

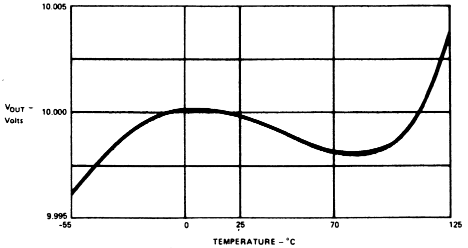


Figure 4. Typical Temperature Characteristic

OUTPUT CURRENT CHARACTERISTICS

The AD584 has the capability to either source or sink current and provide good load regulation in either direction, although it has better characteristics in the source mode (positive current into the load). The circuit is protected for shorts to either positive supply or ground. The output voltage vs. output current characteristics of the device is shown in Figure 5. Source current is displayed as negative current in the figure; sink current is positive. Note that the short circuit current (i.e., zero volts output) is about 28mA; when shorted to +15 volts, the sink current goes to about 20mA.

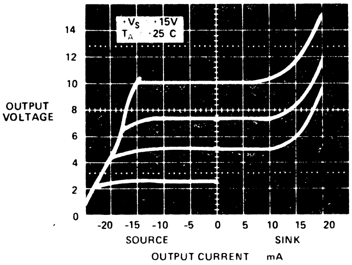


Figure 5. AD584 Output Voltage vs. Sink and Source Current

DYNAMIC PERFORMANCE

Many low power instrument manufacturers are becoming increasingly concerned with the turn-on characteristics of the components being used in their systems. Fast turn-on components often enable the end user to keep power off when not needed, and yet respond quickly when the power is turned on for operation. Figure 6 displays the turn-on characteristic of the AD584. Figure 6a is generated from cold-start operation and represents the true turn-on waveform after an extended period with the supplies off. The figure shows both the coarse and fine transient characteristics of the device; the total settling time to within ±1 millivolt is about 180μs, and there is no long thermal tail appearing after the point.

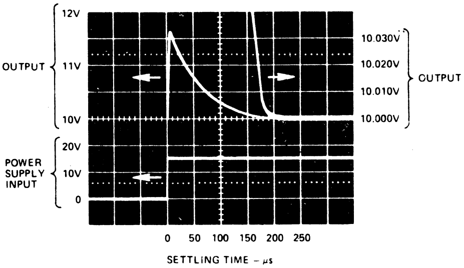
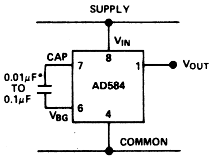


Figure 6. Output Settling Characteristic

NOISE FILTERING

The bandwidth of the output amplifier in the AD584 can be reduced to filter the output noise. A capacitor ranging between 0.01μF and 0.1μF connected between the Cap and V_{BG} terminals will further reduce the wideband and feedthrough noise in the output of the AD584, as shown in Figure 8.



*INCREASES COLD START TURN ON TIME

Figure 7. Additional Noise Filtering with an External Capacitor

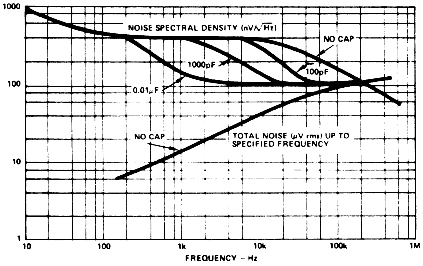


Figure 8. Spectral Noise Density and Total rms Noise vs. Frequency

USING THE STROBE TERMINAL

The AD584 has a strobe input which can be used to zero the output. This unique feature permits a variety of new applications in signal and power conditioning circuits.

Figure 9 illustrates the strobe connection. A simple NPN switch can be used to translate a TTL logic signal into a strobe of the output. The AD584 operates normally when there is no current drawn from pin 5. Bringing this terminal low, to less than 200mV, will allow the output voltage to go to zero. In this mode the AD584 should not be required to source or sink current (unless a 0.7V residual output is permissible). If the AD584 is required to sink a transient current while strobed off, the strobe terminal input current should be limited by a 100Ω resistor as shown in Figure 9.

The strobe terminal will tolerate up to 5μA leakage and its driver should be capable of sinking 500μA continuous. A low leakage open collector gate can be used to drive the strobe terminal directly, provided the gate can withstand the AD584 output voltage plus one volt.

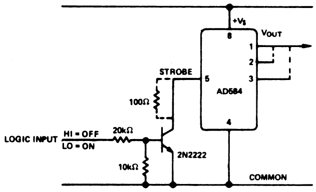


Figure 9. Use of the Strobe Terminal

PRECISION HIGH CURRENT SUPPLY

The AD584 can be easily connected to a power PNP or power Darlington PNP device to provide much greater output current capability. The circuit shown in Figure 10 delivers a precision 10 volt output with up to 4 amperes supplied to the load. The 0.1μF capacitor is required only if the load has a significant capacitive component. If the load is purely resistive, improved high frequency supply rejection results from removing the capacitor.

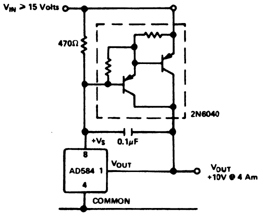


Figure 10. High Current Precision Supply

The AD584 can also use an NPN or Darlington NPN transistor to boost its output current. Simply connect the 10V output terminal of the AD584 to the base of the NPN booster and take the output from the booster emitter as shown in Figure 11. The 5.0V or 2.5V pin must connect to the actual output in this configuration. Variable or adjustable outputs (as shown in Figures 1 and 2) may be combined with +5.0V connection to obtain outputs above +5.0V.

THE AD584 AS A CURRENT LIMITER

The AD584 represents an alternative to current limiter diodes which require factory selection to achieve a desired current. Use of current limiting diodes often results in temperature coefficients of 1%/°C. Use of the AD584 in this mode is not limited to a set current limit; it can be programmed from 0.75 to 5mA with the insertion of a single external resistor (see Figure 12). Of course, the minimum voltage required to drive the connection is 5 volts.

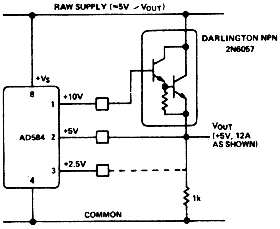


Figure 11. NPN Output Current Booster

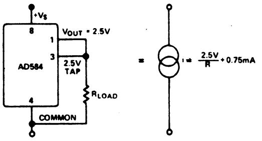


Figure 12. A Two-Component Precision Current Limiter

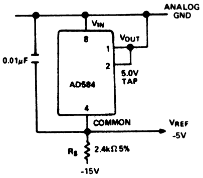


Figure 13. Two-Terminal -5 Volt Reference

NEGATIVE REFERENCE VOLTAGES FROM AN AD584

The AD584 can also be used in a two-terminal "zener" mode to provide a precision -10, -7.5 or -5.0 volt reference. As shown in Figure 13, the V_{IN} and V_{OUT} terminals are connected together to the positive supply (in this case, ground). The AD584 common pin is connected through a resistor to the negative supply. The output is now taken from the common pin instead of V_{OUT}. With 1mA flowing through the AD584 in this mode, a typical unit will show a 2mV increase in output level over that produced in the three-terminal mode. Note also that the effective output impedance in this connection increases from 0.2Ω typical to 2Ω. It is essential to arrange the output load and the supply resistor, R_S, so that the net current through the AD584 is always between 1 and 5mA. The temperature characteristics and long-term stability of the device will be essentially the same as that of a unit used in the standard three-terminal mode. The operating temperature range is limited to -55°C to +85°C.

The AD584 can also be used in a two-terminal mode to develop a positive reference. V_{IN} and V_{OUT} are tied together and to the positive supply through an appropriate supply resistor. The performance characteristics will be similar to those of the negative two-terminal connection. The only advantage of this connection over the standard three-terminal connection is that a lower primary supply can be used, as low as 0.5 volts above the desired output voltage. This type of operation will require considerable attention to load and primary supply regulation to be sure the AD584 always remains within its regulating range of 1 to 5mA.

10 VOLT REFERENCE WITH MULTIPLYING CMOS D/A OR A/D CONVERTERS

The AD584 is ideal for application with the entire AD7520 series of 10- and 12-bit multiplying CMOS D/A converters, especially for low power applications. It is equally suitable for the AD7574 8-bit A/D converter. In the standard hook-up as shown in Figure 14, the standard output voltages are inverted by the amplifier/DAC configuration to produce converted voltage ranges. For example, a +10V reference produces a 0 to -10V range. If an AD308 amplifier is used, total quiescent supply current will typically be 2mA. The AD584 will normally be used in the -10 volt mode with the AD7574 to give a 0 to +10 volt ADC range. This is shown in Figure 16. Bipolar output applications and other operating details can be found in the data sheets for the CMOS products.

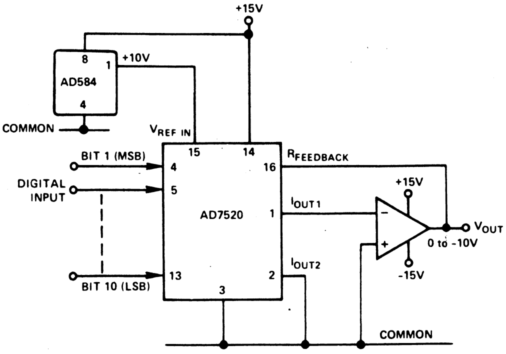
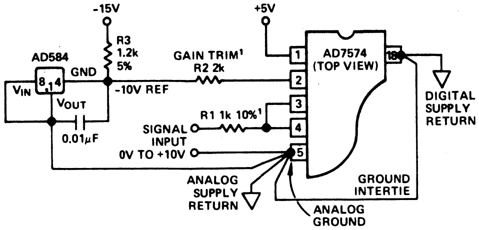


Figure 14. Low Power 10-Bit CMOS DAC Application

PRECISION D/A CONVERTER REFERENCE

The AD562, like many D/A converters, is designed to operate with a +10 volt reference element (Figure 15). In the AD562, this 10 volt reference voltage is converted into a reference current of approximately 0.5mA via the internal 19.95kΩ resistor (in series with the external 100Ω trimmer). The gain temperature coefficient of the AD562 is primarily governed by the temperature tracking of the 19.95kΩ resistor and the 5k/10k span resistors; this gain T.C. is guaranteed to 3ppm/°C. Thus, using the AD584L (at 5ppm/°C) as the 10 volt reference guarantees a maximum full scale temperature coefficient of 8ppm/°C over the commercial range. The 10 volt reference also supplies the normal 1mA bipolar offset current through the 9.95k bipolar offset resistor. The bipolar offset T.C. thus depends only on the T.C. matching of the bipolar offset resistor to the input reference resistor and is guaranteed to 3ppm/°C. Figure 17 demonstrates the flexibility of the AD584 applied to another popular D/A configuration.



NOTE 1: R1 AND R2 CAN BE OMITTED IF GAIN TRIM IS NOT REQUIRED

Figure 16. AD584 as Negative 10 Volt Reference for CMOS ADC

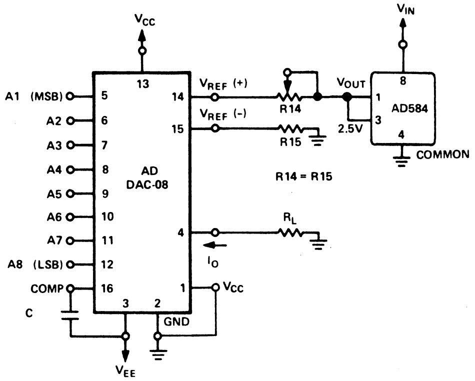


Figure 17. Current Output 8-Bit D/A

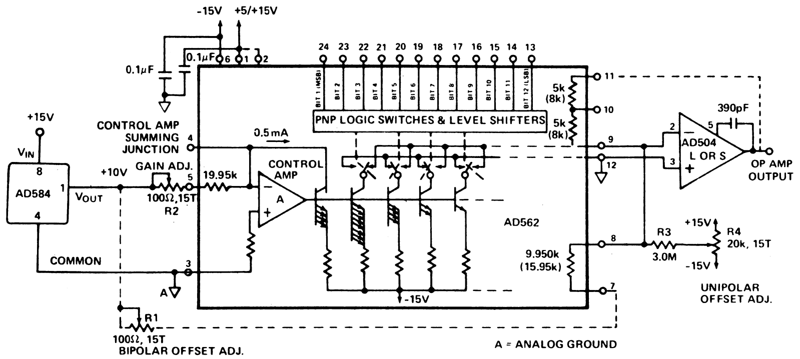


Figure 15. Precision 12-Bit D/A Converter

ANALOG DEVICES

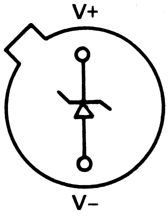
Two-Terminal IC 1.2 Volt Reference

AD589

FEATURES

Superior Replacement for Other 1.2V References
Wide Operating Range: 50μA to 5mA
Low Power: 60μW Total P_D at 50μA
Low Temperature Coefficient:
10ppm/°C max, 0 to +70°C (AD589M)
25ppm/°C max, -55°C to +125°C (AD589U)
Two Terminal "Zener" Operation
Low Output Impedance: 0.6Ω
No Frequency Compensation Required
Low Cost

AD589 FUNCTIONAL BLOCK DIAGRAM



BOTTOM VIEW

PRODUCT DESCRIPTION

The AD589 is a two-terminal, low cost, temperature compensated bandgap voltage reference which provides a fixed 1.23V output voltage for input currents between 50μA and 5.0mA.

The high stability of the AD589 is primarily dependent upon the matching and thermal tracking of the on-chip components. Analog Devices' precision bipolar processing and thin-film technology combine to provide excellent performance at low cost.

Additionally, the active circuit produces an output impedance ten times lower than typical low-TC zener diodes. This feature allows operation with no external components required to maintain full accuracy under changing load conditions.

The AD589 is available in seven versions. The AD589J, K, L and M grades are specified for 0 to +70°C operation, while the S, T and U grades are rated for the full -55°C to +125°C temperature range. Processing to MIL-STD-883B is available on the three military grades.

PRODUCT HIGHLIGHTS

1. The AD589 is a two-terminal device which delivers a a constant reference voltage for a wide range of input current.
2. Output impedance of 0.6Ω and temperature coefficients as low as 10ppm/°C insure stable output voltage over a wide range of operating conditions.
3. The AD589 can be operated as a positive or negative reference. "Floating" operation is also possible.
4. The AD589 will operate with total current as low as 50μA (60μW total power dissipation), ideal for battery powered instrument applications.
5. The AD589S, T, and U grades are available screened to the requirements of MIL-STD-883, Method 5004, Level B.
6. The AD589 is an exact replacement for other 1.2V references, offering superior temperature performance and reduced sensitivity to capacitive loading.

SPECIFICATIONS (typical @ I_{IN} = 500µA and T_A = 25°C unless otherwise noted)

Model	AD589J	AD589K	AD589L	AD589M	AD589S	AD589T	AD589U
ABSOLUTE MAXIMUM RATINGS							
Current	10mA	•	•	•	•	•	•
Reverse Current	10mA	•	•	•	•	•	•
Power Dissipation[1]	125mW	•	•	•	•	•	•
Storage Temperature Range	−65°C to +175°C	•	•	•	•	•	•
Operating Junction Temperature Range	−55°C to +150°C	•	•	•	•	•	•
Lead Temperature (Soldering, 10sec)	300°C	•	•	•	•	•	•
Operating Temperature Range	0 to +70°C	•	•	•	−55°C to +125°C	••	••
OUTPUT VOLTAGE	1.200V min	•	•	•	•	•	•
	1.235V typ	•	•	•	•	•	•
	1.250V max	•	•	•	•	•	•
OUTPUT VOLTAGE CHANGE vs. CURRENT (50µA - 5mA)	5mV max	•	•	•	•	•	•
DYNAMIC OUTPUT IMPEDANCE	0.6Ω typ	•	•	•	•	•	•
	2Ω max	•	•	•	•	•	•
RMS NOISE VOLTAGE 10Hz < f < 10kHz	5µV	•	•	•	•	•	•
TEMPERATURE COEFFICIENT[2] – ppm/°C	100 max	50 max	25 max	10 max	100 max	50 max	25 max
TURN-ON SETTLING TIME TO 0.1%	25µs	•	•	•	•	•	•
OPERATING CURRENT[3]	50µA min	•	•	•	•	•	•
	5mA max	•	•	•	•	•	•
PACKAGE STYLE:[4] H2A	H	•	•	•	•	•	•

NOTES

[1] Absolute maximum power dissipation is limited by maximum current through the device. Maximum rating at elevated temperatures must be computed assuming $T_J \leq 150°C$, and θ_{JA} = 400°C/W.

[2] See following page for explanation of temperature coefficient measurement method.

[3] Optimum performance is obtained at currents below 500µA. Stray shunt capacitances should be minimized. If strays cannot be avoided, a shunt capacitor of at least 1000pF is recommended.

[4] See Section 20 for package outline information.

•Specifications same as AD589J.
••Specifications same as AD589S.
Specifications subject to change without notice.

Understanding the AD589 Specifications

VOLTAGE VARIATION vs. TEMPERATURE

Some confusion exists in the area of defining and specifying reference voltage error over temperature. Historically, references have been characterized using a maximum deviation per degree Centigrade; i.e., 10ppm/°C. However, because of nonlinearities in temperature characteristics, which originated in standard zener references (such as "S" type characteristics) most manufacturers have begun to use a maximum limit error band approach to specify devices. This technique involves measurement of the output at 3, 5 or more different temperatures to guarantee that the output voltage will fall within the given error band. The temperature characteristic of the AD589 consistently follows the curve shown in Figure 1. Three-point measurement guarantees the error band over the specified temperature range. The temperature coefficients specified on page 2 represent the slopes of the diagonals of the error band from +25°C to T_{min} and +25°C to T_{max}.

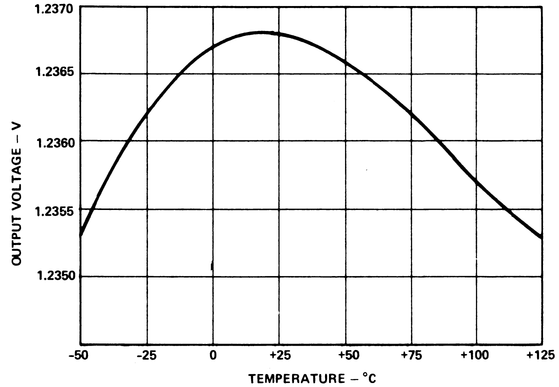


Figure 1. Typical AD589 Temperature Characteristics

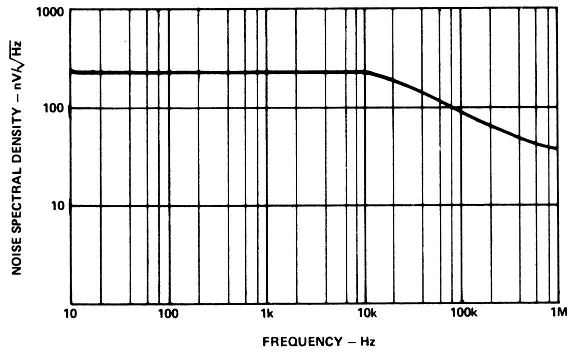


Figure 2. Noise Spectral Density

DYNAMIC PERFORMANCE

Many low power instrument manufacturers are becoming increasingly concerned with the turn-on characteristics of the components being used in their systems. Fast turn-on components often enable the end user to keep power off when not needed, and yet respond quickly when the power is turned on for operation. Figure 3 displays the turn-on characteristic of the AD589. This characteristic is generated from cold-start operation and represents the true turn-on waveform after an extended period with the supplies off. The figure shows both the coarse and fine transient characteristics of the device; the total settling time to within ±1 millivolt is about 25μs, and there is no long thermal tail appearing after that point.

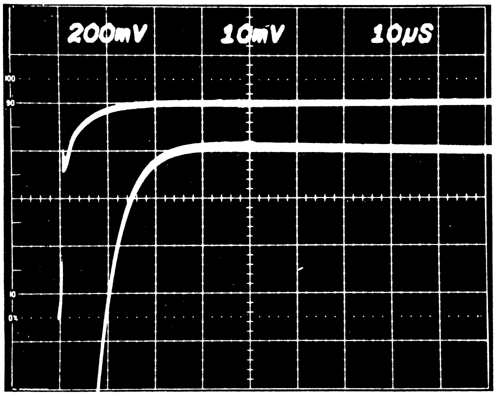


Figure 3. Output Settling Characteristics

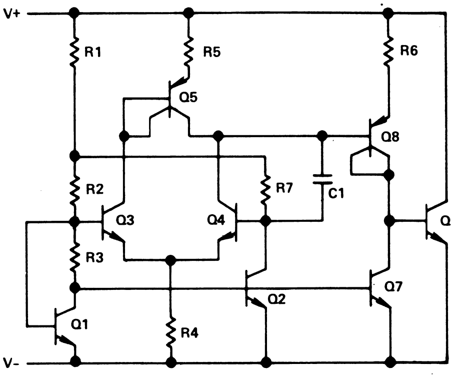


Figure 4. Schematic Diagram

APPLICATION INFORMATION

The AD589 functions as a two-terminal shunt-type regulator. It provides a constant 1.23V output for a wide range of input current from 50μA to 5mA. Figure 5 shows the simplest configuration for an output voltage of 1.2V or less. Note that no frequency compensation is required. If additional filtering is desired for ultra low noise applications, minimum recommended capacitance is 1000pF.

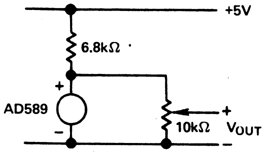


Figure 5. Basic Configuration for 1.2V or Less

The AD589 can also be used as a building block to generate other values of reference voltage. Figure 6 shows a circuit which produces a buffered 10V output. Total supply current for this circuit is approximately 2mA.

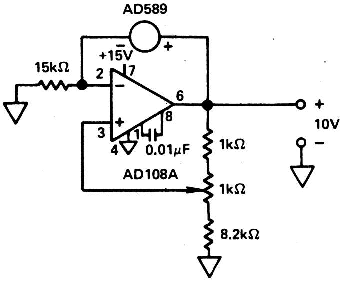
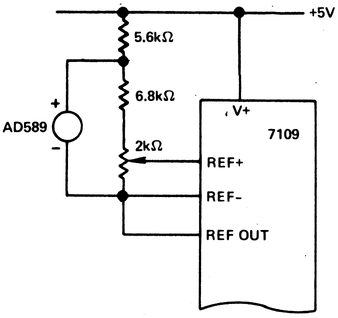
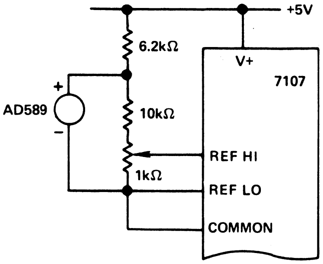


Figure 6. Single-Supply Buffered 10V Reference

The low power operation of the AD589 makes it ideal for use in battery operated portable equipment. It is especially useful as a reference for CMOS analog-to-digital converters. Figure 7 shows the AD589 used in conjunction with two popular integrating type CMOS A/D converters.



a. With 7109 12-Bit Binary A/D



b. With 7107 Panel Meter A/D

Figure 7. AD589 Used as Reference for CMOS A/D Converters

The AD589 also is useful as a reference for CMOS multiplying DACs such as the AD7533. These DACs require a negative reference voltage in order to provide a positive output range. Figure 8 shows the AD589 used to supply an equivalent -1.0V reference to an AD7533.

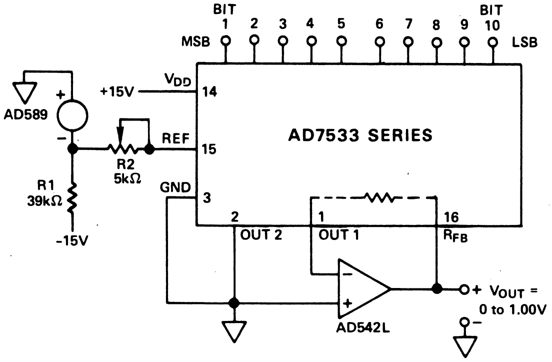


Figure 8. AD589 as Reference for 10-Bit CMOS DAC

ANALOG DEVICES

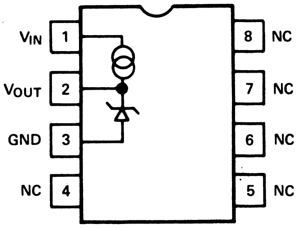
Low Cost, Precision 2.5 Volt IC Reference

AD1403/AD1403A*

FEATURES

- **Improved, Lower Cost, Replacements for Standard 1403, 1403A**
- **3-Terminal Device: Voltage In/Voltage Out**
- **Laser Trimmed to High Accuracy: 2.500V ±10mV (AD1403A)**
- **Excellent Temperature Stability: 25ppm/°C (AD1403A)**
- **Low Quiescent Current: 1.5mA max**
- **Low Cost**
- **Convenient MINI-DIP PACKAGE**

AD1403/AD1403A
FUNCTIONAL BLOCK DIAGRAM



8-PIN MINI-DIP

PRODUCT DESCRIPTION

The AD1403 and AD1403A are improved three-terminal, low cost, temperature compensated, bandgap voltage references that provide a fixed 2.5V output voltage for inputs between 4.5V and 40V. A unique combination of advanced circuit design and laser-wafer-trimmed thin-film resistors provides the AD1403/AD1403A with an initial tolerance of ±10mV and a temperature stability of better than 25ppm/°C. In addition, the low quiescent current drain of 1.5mA (max) offers a clear advantage over classical zener techniques.

The AD1403 or AD1403A is recommended as a stable reference for all 8-, 10- and 12-bit D-to-A converters that require an external reference. In addition, the wide input range of the AD1403/AD1403A allows operation with 5 volt logic supplies, making these devices ideal for digital panel meter applications and when only a single logic supply is available.

The AD1403 and AD1403A are specified for operation over the 0 to +70°C temperature range. The AD580 series of 2.5 volt precision IC references is recommended for applications where operation over the −55°C to +125°C range is required.

PRODUCT HIGHLIGHTS

1. The AD1403A offers improved initial tolerance over the industry-standard 1403A: ±10mV versus ±25mV at a lower cost.
2. The three-terminal voltage in/voltage out operation of the AD1403/AD1403A provides a regulated output voltage without any external components.
3. The AD1403/AD1403A provides a stable 2.5V output voltage for input voltages between 4.5V and 40V making these devices ideal for systems that contain a single logic supply.
4. Thin film resistor technology and tightly controlled bipolar processing provide the AD1403A with temperature stabilities of 25ppm/°C.
5. The low 1.5mA maximum quiescent current drain of the AD1403 and AD1403A makes them ideal for CMOS and other low power applications.

***Covered by Patent Numbers: 3,887,863; RE30,586.**

SPECIFICATIONS (V_{IN} = 15V, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (I_O = 0mA)	V_O				V
AD1403		2.475	2.500	2.525	
AD1403A		2.490	2.500	2.510	
Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$				ppm/°C
AD1403		–	10	40	
AD1403A		–	10	25	
Output Voltage Change, 0 to +70°C	ΔV_O				mV
AD1403		–	–	7.0	
AD1403A		–	–	4.4	
Line Regulation	Reg_{in}				mV
($15V \leqslant V_{IN} \leqslant 40V$)		–	1.2	4.5	
($4.5 \leqslant V_{IN} \leqslant 15V$)		–	0.6	3.0	
Load Regulation ($0mA < I_O < 10mA$)	Reg_{load}	–	–	10	mV
Quiescent Current (I_O = 0mA)	I_I	–	1.2	1.5	mA

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Input Voltage	V_{IN}	40	V
Storage Temperature	T_{STG}	-25 to 100	°C
Junction Temperature	T_J	+175	°C
Operating Ambient Temperature Range	T_A	0 to +70	°C

Specifications subject to change without notice.

ORDERING INFORMATION

Device	Initial Tolerance	Package Style[1]
AD1403N	±25mV	N8A
AD1403AN	±10mV	N8A

[1] See Section 20 for package outline information.

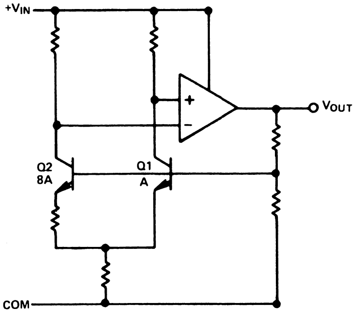


Figure 1. AD1043/AD1403A Functional Diagram

Typical Performance Curves

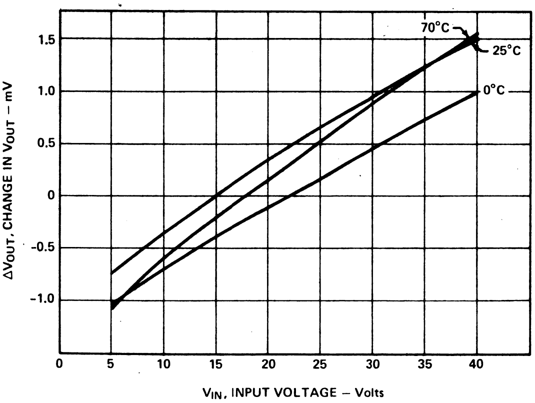


Figure 2. Typical Change in V_{OUT} vs. V_{IN} (Normalized to V_{OUT} @ V_{IN} = 15V @ T_C = 25°C)

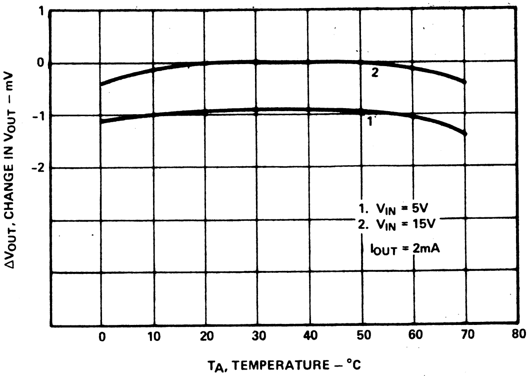


Figure 5. Change in V_{OUT} vs. Temperature (Normalized to V_{OUT} @ V_{IN} = 15V)

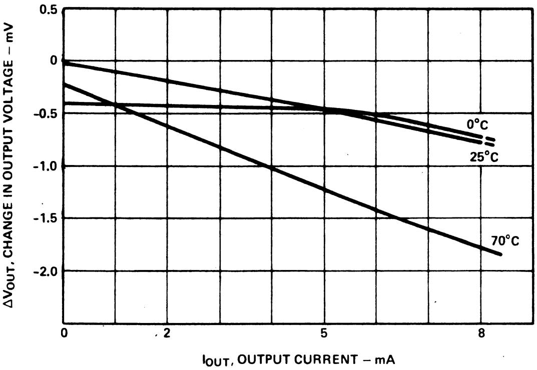


Figure 3. Change in Output Voltage vs. Load Current (Normalized to V_{OUT} @ V_{IN} = 15V, I_{OUT} = 0mA)

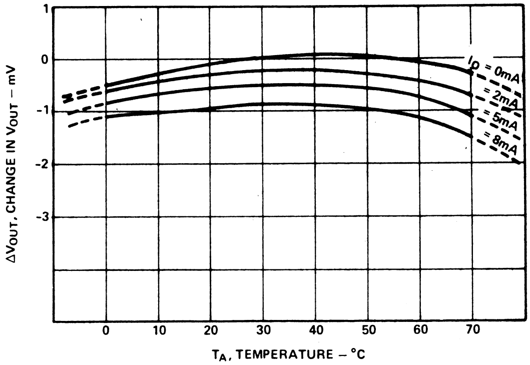


Figure 6. Change in V_{OUT} vs. Temperature (Normalized to V_{OUT} @ V_{IN} = 15V, I_{OUT} = 0mA)

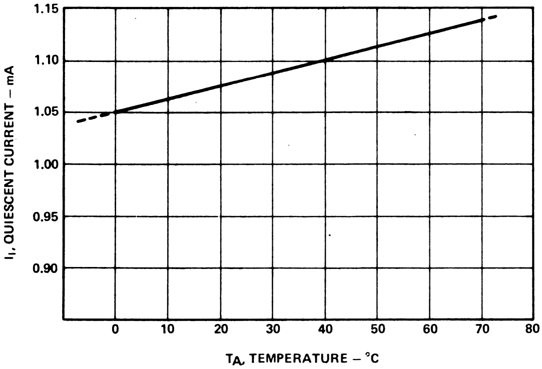


Figure 4. Quiescent Current vs. Temperature (V_{IN} = 15V, I_{OUT} = 0mA)

Applying the AD1403/AD1403A

VOLTAGE VARIATION VS. TEMPERATURE AND LINE

Some confusion exists in the area of defining and specifying reference voltage error over temperature. Historically, references are characterized using a maximum deviation per degree Centigrade; i.e., 10ppm/°C. However, because of the inconsistent nonlinearities in zener references (butterfly or "S" type characteristics), most manufacturers use a maximum limit error band approach to characterize their references. This technique measures the output voltage at 3 to 5 different temperatures and guarantees that the output voltage deviation will fall within the guaranteed error band at these discrete temperatures. This approach, of course, makes no mention or guarantee of performance at any other temperature within the operating temperature range of the device.

The consistent Voltage vs. Temperature performance of a typical AD1403 is shown in Figure 5. Note that the characteristic is quasi-parabolic, not the possible "S" type characteristics of classical zener references. This parabolic characteristic permits a maximum output deviation specification over the device's full operating temperature range, rather than just at 3 to 5 discrete temperatures.

The AD1403 exhibits a worst-case shift of 7.5mV over the entire range of operating input voltage, 4.5 volts to 40 volts. Typically, the shift is less than 1mV as shown in Figure 2.

THE AD1403A AS A LOW POWER, LOW VOLTAGE PRECISION REFERENCE FOR DATA CONVERTERS

The AD1403A has a number of features that make it ideally suited for use with A/D and D/A data converters used in complex microprocessor-based systems. The calibrated 2.500 volt output minimizes user trim requirements and allows operation from a single low voltage supply. Low power consumption (1.5mA quiescent current) is commensurate with that of CMOS-type devices, while the low cost and small package complements the decreasing cost and size of the latest converters.

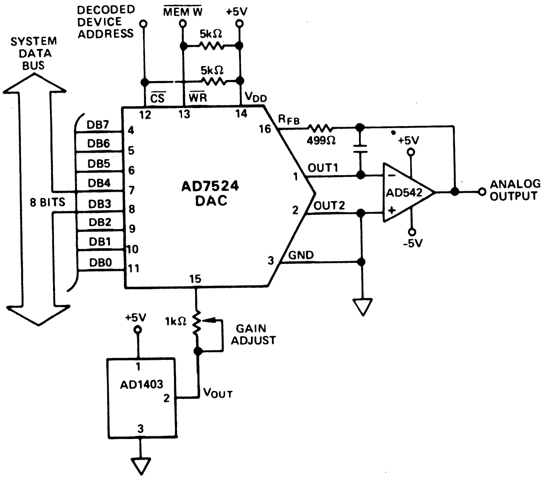


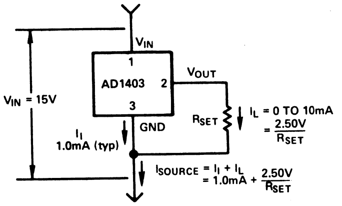
Figure 7. Low Power, Low Voltage Reference for the AD7524 Microprocessor-Compatible 8-Bit DAC

Figure 7 shows the AD1403A used as a reference for the AD7524 low-cost 8-bit CMOS DAC with complete microprocessor interface. The AD1403A and the AD7524 are specified to operate from a single 5 volt supply; this eliminates the need to provide a +15 volt power supply for the sole purpose of operating a reference. The AD7524 includes an 8-bit data register, and address decoding logic; it may thus be interfaced directly to an 8- or 16-bit data bus. Only 300μA of quiescent current from the single +5 volt supply is required to operate the AD7524 which is packaged in a small 16 pin DIP. The AD542 output amplifier is also low power, requiring only 1.5mA quiescent current. Its laser-trimmed offset voltage preserves the ±1/2LSB linearity of the AD7524KN without user trims and it typically settles to ±1/2LSB in less than 5 microseconds. It will provide the 0 volt to -2.5 volt output swing from ±5 volt supplies.

THE AD1403 AS A PRECISION PROGRAMMABLE CURRENT SOURCE

The AD1403 is an excellent building block for precision current sources. Its wide range of operating voltages, 4.5V to 40V, along with excellent line regulation over that range (7.5mV) result in high insensitivity to varying load impedances. The low quiescent current (I_I) of 1.5mA (max) and the maximum specified maximum load current of 10mA allows the user to program current to any value between 1.5mA and 10mA.

Figure 8a shows the AD1403 connected as a current source. Total current is equal to the quiescent current plus the load current. Most of the temperature coefficient comes from the quiescent current term I_I, which has a typical TC of 0.13%/°C (1300ppm/°C). The load voltage (and hence current) TC is much lower at ±40ppm/°C max (AD1403). Therefore, the overall temperature coefficient decreases rapidly as the load current is increased. Figure 8a shows the typical temperature coefficient for currents between 1.5mA and 10mA. Use of an AD1403A will not improve the TC appreciably.



VIN
1
AD1403 2
VOUT
VIN = 15V
3
GND
RSET
$I_L = 0 \text{ TO } 10mA = \frac{2.50V}{R_{SET}}$
I_I
1.0mA (typ)
$I_{SOURCE} = I_I + I_L = 1.0mA + \frac{2.50V}{R_{SET}}$

Figure 8a. The AD1403 as a Precision Programmable Current Source

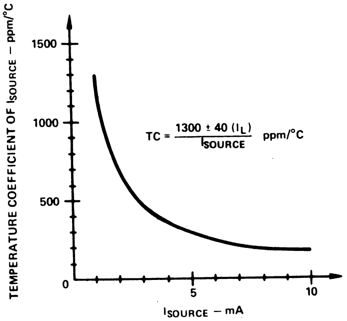


Figure 8b. Typical Temperature Coefficient of Current Source

ANALOG DEVICES

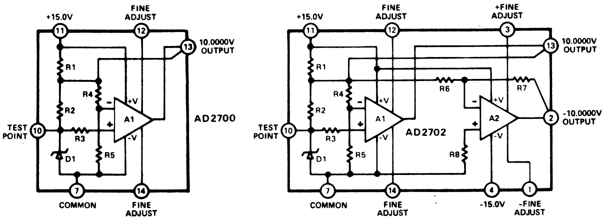
±10 Volt Precision Reference Series

AD2700, AD2701, AD2702

FEATURES

- **Very High Accuracy: 10.000 Volts ±2.5mV (L and U)**
- **Low Temperature Coefficient: 3ppm/°C**
- **Performance Guaranteed -55°C to +125°C**
- **10mA Output Current Capability**
- **Low Noise**
- **Short Circuit Protected**

AD2700 SERIES FUNCTIONAL BLOCK DIAGRAMS



14-PIN DIP

PRODUCT DESCRIPTION

The AD2700 family of precision 10 volt references offer the user excellent accuracy and stability at a moderate price by combining the recognized advantages of thin film technology and active laser trimming. The low temperature drift (3ppm/°C) achieved with these technologies can be matched only by the use of ovens, chip heaters for temperature regulation, or with hand selected components and manual trimming. In addition, temperature-regulated devices are guaranteed only up to +85°C operation, whereas the U- and S-grade devices in the AD2700 family are guaranteed to +125°C. The AD2700U and AD2700S series are also available with screening to MIL-STD-883A, Class B.

The AD2700 is a +10 volt reference which is designed to interface with high accuracy bipolar D/A converters of 10 and 12 bit resolution. The 10mA output drive capability also makes the AD2700 ideal for use as a general positive system reference.

The AD2701 is a negative 10 volt reference especially designed to interface with CMOS D/A and A/D converters, as shown in the applications. For systems requiring a dual tracking reference, the AD2702 offers both positive and negative precision 10 volt outputs in a single package.

All three devices are offered in "J" and "L" grades for operation from -25°C to +85°C and "S" and "U" grades for the -55°C to +125°C temperature range.

Model	Output
AD2700	+10.000V
AD2701	-10.000V
AD2702	±10.000V

SPECIFICATIONS (maximum or minimum @ E_{IN} ±15V @ +25°C, R_L = 2kΩ unless otherwise noted)

MODEL	J	L	S[1]	U[1]
ABSOLUTE MAX RATINGS				
Input Voltage (for applicable supply)	±20V	*	*	*
Power Dissapation @ +25°C – AD2700, 01	300mW	*	*	*
– AD2702	450mW	*	*	*
Operating Temperature Range	-25°C to +85°C	*	-55°C to +125°C	***
Storage Temperature Range	-65°C to +150°C	*	*	*
Lead Temperature (soldering, 10s)	+300°C	*	*	*
Short Circuit Protection (to GND)	Continuous	*	*	*
OUTPUT VOLTAGE				
AD2700	10.000V ±0.005V	±0.0025V	*	**
AD2701	-10.000V ±0.005V	±0.0025V	*	**
AD2702	±10.000V ±0.005V	±0.0025V	*	**
OUTPUT CURRENT – @ +25°C	±10mA	*	*	*
(V_{IN} = ±13 to ±18V) over op. range	±5mA	+5mA, -2mA	**	**
OUTPUT VOLTAGE CHANGE[2] – AD2700, 01	10ppm/°C	3ppm/°C	**	**
	±11.0mV	±4.3mV	±8mV	±5.5mV
T_{min} to T_{max} AD2702	10ppm/°C	5ppm/°C	**	3ppm/°C
	±11.0mV	±5.5mV	±10.0mV	±5.5mV
LINE REGULATION V_{IN} = ±13.5 to ±16.5V	300µV/V	*	*	*
LOAD REGULATION 0 to ±10mA	50µV/mA	*	*	*
OUTPUT RESISTANCE	0.05Ω	*	*	*
INPUT VOLTAGE, OPERATING	±13V to ±18V	*	*	*
QUIESCENT CURRENT – AD2700, 01	±14mA	*	*	*
– AD2702	+17mA, -3mA	*	*	*
NOISE (0.1 to 10Hz)	50µV p-p typ	*	*	*
LONG TERM STABILITY (@ +55°C)	100ppm/1000 Hrs. typ	*	*	*
OFFSET ADJUST RANGE (See Diagrams)	±20mV (min)	*	*	*
OFFSET ADJUST TEMP DRIFT EFFECT	±4µV/°C per mV of Adjust typ	*	*	*
PACKAGE OPTION[3,4]	HY14D	*	*	*

*Same as "J" grade performance.

**Same as "L" grade performance.

***Same as "S" grade performance.

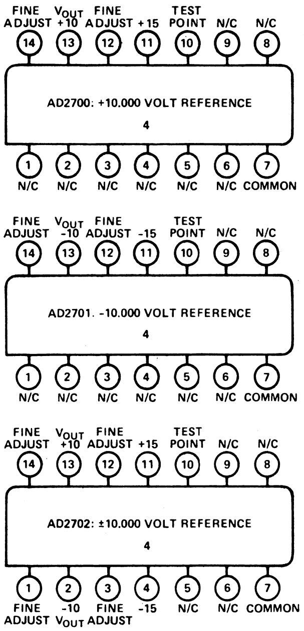
[1] Operational screening ("S or U/883") per MIL-STD-883A Method 5008, Class B; except that constant acceleration is 10kg. (Method 2001, Condition B. Y1 Plane).

[2] Output voltage change as a function of temperature is determined using the box method. Each unit is tested at T_{min}, T_{max} and +25°C. At each temperature V_{OUT} must fall within the rectangular area bounded by the minimum and maximum temperature and whose maximum V_{OUT} value is equal to V_{OUT} nominal plus or minus the maximum +25°C error plus the maximum drift error from +25°C.

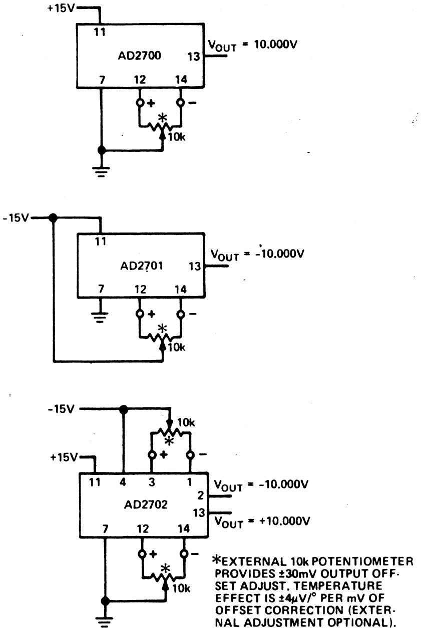
[3] See Section 20 for package outline information.

[4] Analog Devices reserves the right to ship ceramic packages (HY14B) in lieu of metal (HY14D) packages.

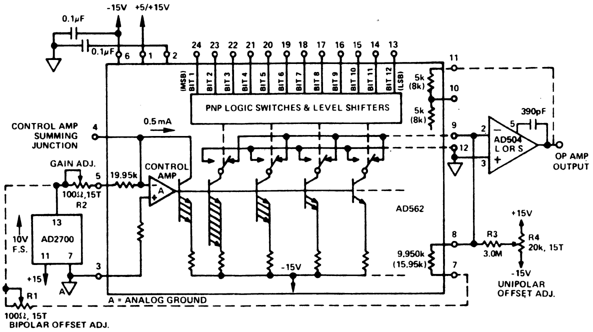
Specifications subject to change without notice.



Pin Designations


+15V
-15V
11
AD2700
13
7
12
14
VOUT = 10.000V
10k
AD2701
VOUT = -10.000V
AD2702
4
3
1
2
VOUT = +10.000V
*EXTERNAL 10k POTENTIOMETER PROVIDES ±30mV OUTPUT OFFSET ADJUST. TEMPERATURE EFFECT IS ±4μV/° PER mV OF OFFSET CORRECTION (EXTERNAL ADJUSTMENT OPTIONAL).

Fine Trim Connections

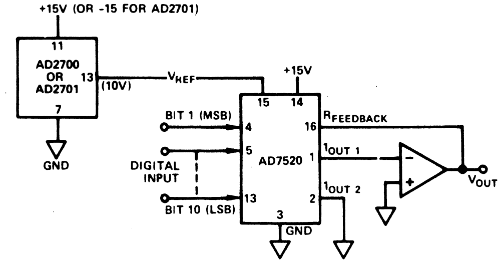


SEE AD562 DATA SHEET FOR ADDITIONAL APPLICATION INFORMATION

Using AD2700 Reference With the AD562 – 12-Bit D/A Converter

USING AD2700 REFERENCE WITH THE AD7520 AND AN IC AMPLIFIER TO BUILD A DAC

The AD2700 series is ideal for use with the AD7520 series of CMOS D/A converters. A CMOS converter in a unipolar application as shown below performs an inversion of the voltage reference input. Thus, use of the +10 volt AD2700 reference will result in a 0 to −10 volt output range. Alternatively, using the −10 volt AD2701 will result in a 0 to +10 volt range. Two operational amplifiers are used to give a bipolar output range of −10 volt to +10 volt, as shown in the lower figure. Either the AD2700 or AD2701 can be used, depending on the transfer code characteristic desired. For more detailed applications information, refer to the AD7520 data sheet.

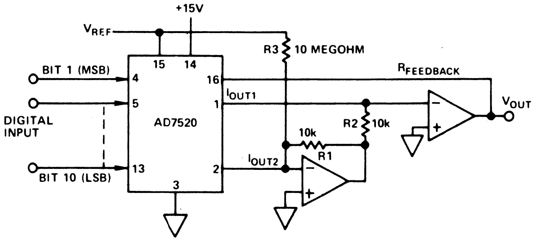


Unipolar Binary Operation

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}\ (1 - 2^{-10})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}\ (1/2 + 2^{-10})$
1 0 0 0 0 0 0 0 0 0	$\frac{-V_{REF}}{2}$
0 1 1 1 1 1 1 1 1 1	$-V_{REF}\ (1/2 - 2^{-10})$
0 0 0 0 0 0 0 0 0 1	$-V_{REF}\ (2^{-10})$
0 0 0 0 0 0 0 0 0 0	0

NOTE: 1 LSB = $2^{-10}\ V_{REF}$

Table 1. Code Table – Unipolar Binary Operation



Bipolar Operation (4-Quadrant Multiplication)

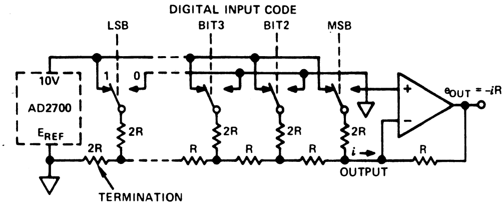
DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}\ (1 - 2^{-9})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}\ (2^{-9})$
1 0 0 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1 1 1	$V_{REF}\ (2^{-9})$
0 0 0 0 0 0 0 0 0 1	$V_{REF}\ (1 - 2^{-9})$
0 0 0 0 0 0 0 0 0 0	V_{REF}

NOTE: 1 LSB = $2^{-9}\ V_{REF}$

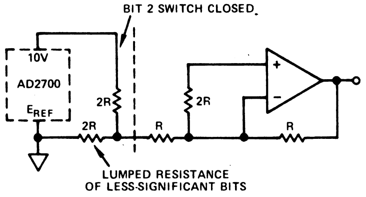
Table 2. Code Table – Bipolar (Offset Binary) Operation

USING THE AD2700 VOLTAGE REFERENCE WITH D/A CONVERTER

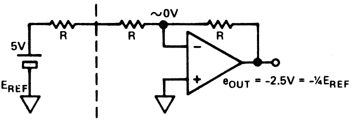
An AD2700 Voltage Reference can be used with an inverting operational amplifier and an R-2R ladder network. If all bits but the MSB are off (i.e., grounded), the output voltage is $(-R/2R)E_{REF}$. If all bits but Bit 2 are off, it can be shown that the output voltage is $½(-R/2R)E_{REF} = ¼E_{REF}$: The lumped resistance of all the less-significant-bit circuitry (to the left of Bit 2) is 2R; the Thevenin equivalent looking back from the MSB towards Bit 2 is the generator, $E_{REF}/2$, and the series resistance 2R; since the grounded MSB series resistance, 2R, has virtually no influence – because the amplifier summing point is at virtual ground – the output voltage is therefore $-E_{REF}/4$. The same line of thinking can be employed to show that the nth bit produces an increment of output equal to $2^{-n}\ E_{REF}$.



a. Basic Circuit



b. Example: Contribution of Bit 2; All Other Bits "0"



c. Simplified Equivalent of Circuit (b.)

ANALOG DEVICES

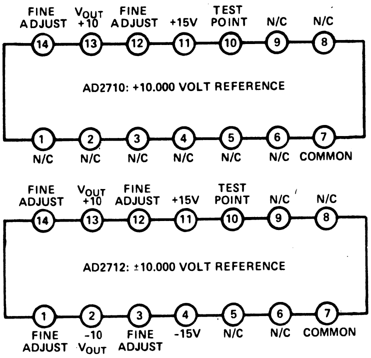
±10.000 Volt Ultra High Precision Reference Series

AD2710, AD2712

FEATURES

Laser Trimmed to High Accuracy: 10.000V ± 1.0mV
Low Temperature Coefficient: 1ppm/°C (L Grade)
Excellent Long Term Stability: 25ppm/1000hrs.
5mA Output Current Capability
Low Noise (30μV p-p)
Short Circuit Protected
No Heater Utilized
Small Size (Standard 14-Pin DIP Package)

AD2710/AD2712 PIN CONFIGURATIONS



14-PIN DUAL IN LINE PACKAGES

PRODUCT DESCRIPTION

The AD2710 and AD2712 are temperature-compensated, hybrid voltage references which provide precise 10.000V output from an unregulated input level from 13.5 to 16.5 volts. Active laser trimming is used to trim both the initial error at +25°C as well as the temperature coefficient, which results in ultra high precision performance previously available only in oven-regulated modules. The 1.0mV maximum initial error and 1ppm/°C guaranteed maximum temperature coefficient of the AD2710L and AD2712L represent the best performance combination available without using ovens or heated substrates for temperature regulation.

The AD2710 series of precision 10.000 volt references offer the user unequalled accuracy and stability with performance guaranteed over the 0 to +70°C temperature range. The devices combine the recognized advantages of thin film technology and active laser trimming with a unique integrated ceramic package design to provide an excellent reference for use in applications requiring high accuracy and stability.

The AD2710 is recommended for use as a reference for 10-, 12- and 14-bit D/A converters which require an external reference. The device is also suitable for many types of high resolution A/D converters, either successive approximation or integrating designs. The 5mA output drive capability of the device also makes the AD2710 ideal for use as a master system reference.

For systems requiring a dual tracking reference, the AD2712 offers both positive and negative outputs in a single package. All units are packaged in an integrated ceramic 14-pin side-brazed package offering superior reliability over other package designs.

PRODUCT HIGHLIGHTS

1. Active laser trimming of both initial accuracy and temperature coefficient results in very high accuracy over the temperature range without the use of external components. AD2710 has a maximum deviation from 10.000 volts of ±1.00mV at 25°C with no external adjustments.
2. The AD2710 and AD2712 are well suited for a broad range of applications requiring an accurate, stable reference source such as data converters, test and measurement systems and calibration standards.
3. The performance of the AD2710 series is achieved by a well-characterized design and close control over the manufacturing process. This eliminates the need for temperature-controlled ovens to provide stability.
4. The advanced multilayer integrated ceramic package results in superior electrical performance as well as inherent high reliability.

SPECIFICATIONS (typical @ V_S ±15V after a 5 minute warm-up at +25°C, no load condition unless otherwise specified)

Model	AD2710KN	AD2710LN	AD2712KN	AD2712LN
ABSOLUTE MAXIMUM RATINGS				
Input Voltage (for applicable supply)	±18V	*	*	*
Power Dissipation @ +25°C	300mW	*	450mW	**
Operating Temperature Range	0 to +70°C	*	*	*
Storage Temperature Range	−55°C to +100°C	*	*	*
Lead Temperature (soldering, 20s)	+260°C	*	*	*
Short Circuit Protection (to GND)	Continuous	*	*	*
OUTPUT VOLTAGE ERROR[1]				
+25°C	±1.0mV max	*	*	*
OUTPUT VOLTAGE TEMPERATURE COEFFICIENT[2]				
+10V Output +25°C to +70°C	±2ppm/°C max	±1ppm/°C max	±2ppm/°C max	±1ppm/°C max
0 to +25°C	±5ppm/°C max	*[3]	*	*[3]
−10V Output[4] +25°C to +70°C	Not Applicable	Not Applicable	±3ppm/°C max	±2ppm/°C max
0 to +25°C	Not Applicable	Not Applicable	±5ppm/°C max	**
LINE REGULATION				
V_S = ±13.5 to ±16.5[5]	125μV/V(200μV/V max)	*	*	*
OUTPUT CURRENT	10mA	*	*	*
LOAD REGULATION				
I_O = 0 to ±5mA	50μV/mA(100μV/mA max)	*	*	*
OUTPUT RESISTANCE	0.05Ω	*	*	*
INPUT VOLTAGE[5]				
Operating Range	±13V to ±18V	*	*	*
Specified Performance	±13.5V to ±16.5V	*	*	*
QUIESCENT SUPPLY CURRENT				
V_S+	9mA(14mA max)	*	12mA (16mA max)	**
V_S−[5]	Not Applicable	Not Applicable	2mA (3mA max)	**
NOISE				
0.1 to 10Hz	30μV p-p	*	*	*
LONG TERM STABILITY				
T_A = +25°C	25ppm/1000 Hours	*	*	*
EXTERNAL TRIM RANGE[6]	±10mV	*	*	*
PACKAGE OPTION[7]	HY14B	*	*	*

NOTES:

*Same as AD2710KN. **Same as AD2712KN performance.

[1] Specifications apply to both outputs of the AD2712.

[2] Refer to next page for definition of temperature-related error specifications.

[3] The AD2710LN and AD2712LN outputs are guaranteed for a maximum ±2ppm/°C temperature coefficient over the +15°C to +25°C temperature range. Refer to Figure 1.

[4] The +10V and −10V outputs of the AD2712 typically track within ±1ppm/°C over the specified temperature range.

[5] Negative power supply not required for AD2710.

[6] Use of the output trim will change the temperature coefficient approximately 0.3ppm/°C for each millivolt of adjustment.

[7] See Section 20 for package outline information.

Specifications subject to change without notice.

UNDERSTANDING THE SPECIFICATIONS

The AD2710 and AD2712 precision references are designed for applications requiring both the lowest possible initial error at room temperature and the lowest possible temperature drift. The specification for initial error is relatively straight-forward, and is the absolute error from exactly 10.000V. The specification for temperature drift, however, must be explained.

Various methods have been used to specify the temperature drift of voltage references, including the "butterfly", "box", and "modified-box" (or total error) methods. The AD2710 and AD2712 are specified with the "butterfly" method.

Using three or more temperatures provides the user with a tighter drift specification, eliminating possible mid-range excursions. The AD2710 and AD2712 have been designed and characterized as having a smooth drift curve with a virtually straight segment from +25°C to +70°C. The typical curve as shown is concave downward and gradually increases slope near 0°C.

As can be seen from Figure 1, the AD2710L and AD2712L +10V outputs will exhibit a maximum temperature coefficient of ±1ppm/°C (±2ppm/°C for "K" grade) from +25°C to +70°C. Over the short range between +15°C and +25°C, the AD2710L and AD2712L +10V outputs have a maximum drift of only ±2ppm/°C and a maximum drift of ±5ppm/°C from 0 to +15°C. The negative output of the AD2712L has a similar temperature coefficient characteristic with a maximum slope of ±2ppm/°C from +25°C to +70°C. This limit continues from +25°C to +15°C and then increases to a ±5ppm/°C maximum slope from +15°C and 0°C. Every unit is 100 percent tested and guaranteed to meet these specifications over the full 0 to +70°C temperature range.

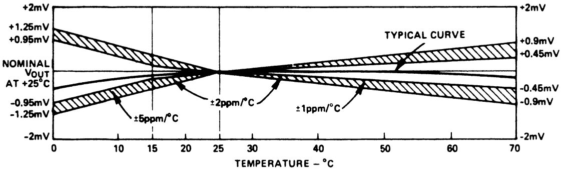


Figure 1. Maximum Change from +10V Output from +25°C Value vs. Temperature

All grades of the AD2710 and AD2712 are tested after a five minute warm-up period. This warm-up allows the entire circuit to attain thermal equilibrium. The warm-up drift is approximately 500 microvolts and is completely settled approximately three minutes after turn-on. Figure 2 shows the typical warm-up characteristics of the AD2710.

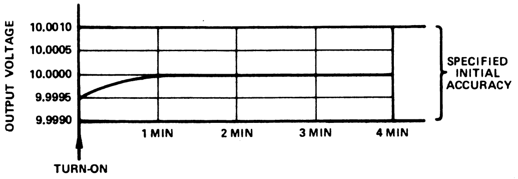


Figure 2. AD2710 Typical Warm-Up Drift

USING THE AD2710 AS A DAC REFERENCE

Digital-to-analog converters require a reference to establish the full scale output range. It is this reference which will ultimately determine the absolute accuracy of the converter. While many converters include internal reference sources, better overall performance can be obtained if a higher precision external reference is used.

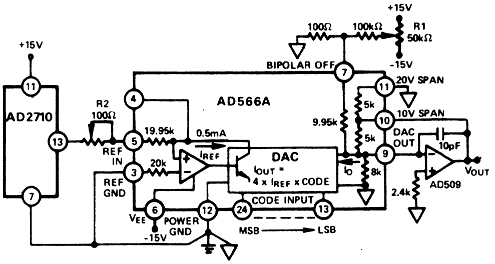


Figure 3. Low Drift 12-Bit D/A Converter

Figure 3 shows the AD2710 used with the AD566A high-speed 12-bit DAC. The AD566AKD is laser trimmed for ±1/4LSB maximum nonlinearity, and exhibits a gain temperature coefficient of 3ppm/°C. Use of the AD2710LN reference will result in a worst case total gain temperature coefficient of 4ppm/°C. After initial calibration of the DAC scale factor at room temperature, 12-bit absolute accuracy can be maintained over the +15°C to +70°C temperature range. The high output current capability of the AD2710 allows it to serve as a reference for up to 10 such converters in a system.

The resolution of the AD566A can be extended as shown in Figure 3 by summing the output of another DAC. In this example, an AD559 is used to provide 4 additional bits. Since the AD559 is driven from the same AD2710 reference as the AD566A which provides the higher-order bits, and uses a similar internal thin-film resistor ladder, it will exhibit first-order temperature tracking. While this circuit provides 16-bits of resolution, it is only as accurate as the AD566A used for the most significant bits. Use of an AD566AKD will typically achieve ±0.003% accuracy (±1/2LSB at 14 bits).

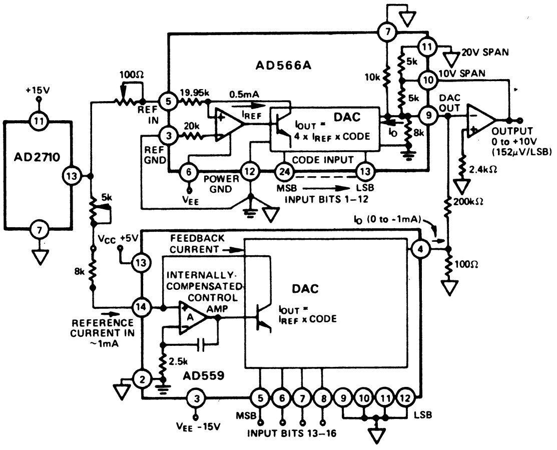
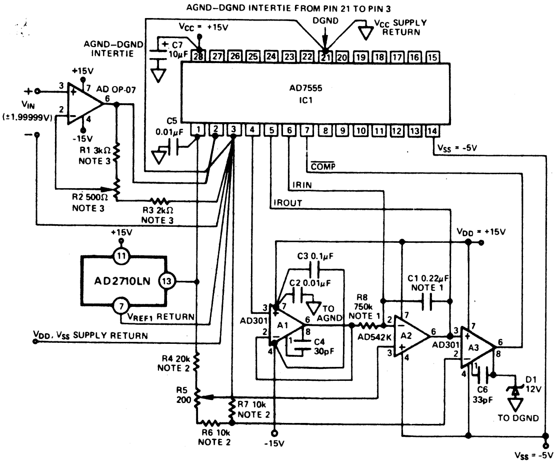


Figure 4. 16-Bit Binary DAC with AD2710 Reference

HIGH RESOLUTION ANALOG-TO-DIGITAL CONVERSION

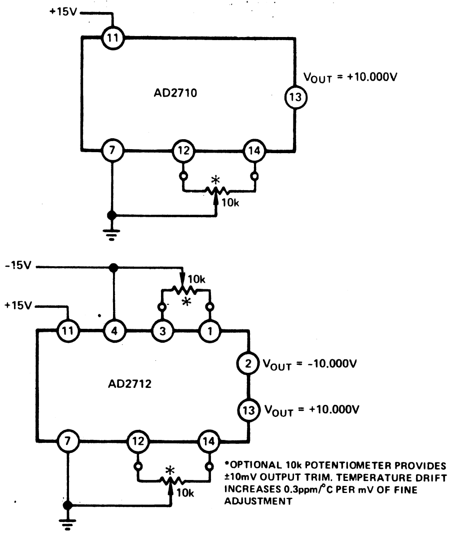
The AD2710 is well-suited to both system and instrument-level analog-to-digital converter reference requirements. The excellent absolute accuracy and low temperature drift allow low-cost measurement systems to offer high levels of performance.

The AD7555 is a 4½/5½ digit ADC subsystem which uses the quad-slope conversion technique to achieve high accuracy at low cost. This patented conversion process performs automatic correction for offsets and other errors in the analog circuitry as a part of each conversion. Total scale factor drift 1.2ppm/°C is possible using the AD2710L reference and medium-precision external amplifiers. This represents a full scale drift of less than ±10 counts in ±200,000 from +15°C to +45°C. Less than 1 count of drift will occur in the 4 1/2 digit mode.



NOTES:
1. R8 C1 VALUES SHOWN ARE FOR 5 1/2 DIGIT MODE. FOR 4 1/2 DIGIT MODE R_8 = 360k, C_1 = 0.22μF. SUITABLE CAPACITORS AVAILABLE FROM COMPONENT RESEARCH CO. INC., 1655 26th STREET, SANTA MONICA, CA. 90404. (STOCK NUMBER FOR 0.22μF CAPACITOR IS D11B224KXW).
2. R4, R6, R7 1% TOLERANCE
3. R1, R3 SHOULD TRACK WITHIN 0.5ppm/°C. EITHER BULK METAL OR WIRE-WOUND RESISTORS (OR A THIN-FILM NETWORK) SHOULD BE USED. R2 SHOULD BE A LOW-TC TYPE POTENTIOMETER OR A SELECTED LOW DRIFT FIXED RESISTOR.

Figure 5. High Accuracy Low Drift A/D Converter



*OPTIONAL 10k POTENTIOMETER PROVIDES ±10mV OUTPUT TRIM. TEMPERATURE DRIFT INCREASES 0.3ppm/°C PER mV OF FINE ADJUSTMENT

Figure 6. Optional Fine Trim Connections

The AD7555 was designed for use with a 4.096V reference, which produces a ±2 volt input range. When the AD2710 is used, the input range is increased to ±4.88281V (24.4μV/count). The new scaling can be handled either by using a precision gain stage before the AD7555 analog input as shown or by using a microprocessor to digitally correct the scale. The actual input signal value can be computed by multiplying the count produced by the AD7555 by V_{REF1} (10 volts in this case), and dividing the result by 409600. Details of the digital circuitry of the AD7555 can be found on the AD7555 data sheet.

It should be noted that when the AD7555 is used with the AD2710 10 volt reference, it is necessary to use a V_{CC} greater than 10 volts. Thus the digital inputs and outputs of the ADC will be compatible with CMOS logic levels.

Transducers

Contents

Page

Selection Guide 9-2

General Information and Definitions of Specifications 9-3

AD590I/J/K/L/M Temperature-to-Current Converter IC 9-5

9

Selection Guide
Transducers

Model	Characteristics	Vol I Page	Vol II Page
AD590I/J/K/L/M	IC, 2-terminal, TO-52 can or miniature flatpack, -55°C to +150°C (218K to 423K) operating range, linear current output, 1μA/K, laser-trimmed for high accuracy; Output current independent of supply voltage.	9–5	9–7
AC2626J/K/L/M	Stainless-steel temperature probe using AD590, same temperature range and electrical characteristics as the AD590, 3/16" outside diameter, 6- or 4-inch standard lengths, includes 3 feet of Teflon-coated lead wire, 2s response in stirred water, sensor electrically isolated from sheath (±200V breakdown—case to leads).	–	9–5

FEATURE SELECTION CHART COMPARED TO TRADITIONAL TEMPERATURE SENSORS FOR -55°C TO +150°C

	AD590/AC2626	RTD	THERMOCOUPLE	THERMISTOR
Linear	●	●		
High Level	●			●
Excitation Insensitive	●		●	
Linearization Required		●	●	●
Remote Sensing Applications	●			
Low Cost	●		●	●

Orientation
Transducers

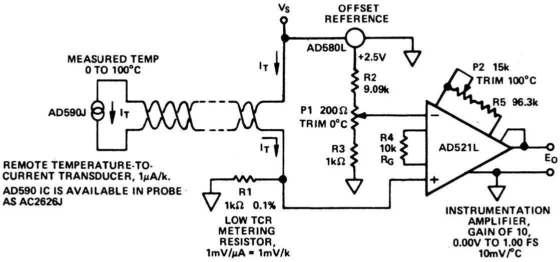
The AD590 is a two-terminal integrated circuit temperature transducer which produces an output current proportional to absolute temperature. The AD590 has a standard 1µA/K output current which is inherently linear, therefore, no linearization is required.

Attention to all the detail is the key to success in most interface criteria. The following application is provided to illustrate the problems involved in designing circuits which measure physical pheonomenon.

In this application, there is a need to measure temperatures from 0 to +100°C, to within 1.0°C, at low cost, at a remote location several hundred feet from the instrumentation. The ambient temperature in the vicinity of the instrumentation is expected to be 25°C ±15°. A number of possible transducers will operate over the specified range, but the requirement for a remote measurement suggests the use of the current-output two-wire AD590 semiconductor temperature sensor, because the current is unaffected by voltage drops and induced voltages.

Consulting the "Accuracies of the AD590"[1] we find that the AD590J, with two external trims, would be suitable; its maximum error over the 0 to 100°C range is 0.3°. This permits an allowance of 0.7° for all other errors. If a tighter tolerance were required, it would be worthwhile to consider using the AD590M with two trims, for an error *below* 0.05°C.

Since AD590 measures absolute temperature (its nominal output is 1µA/K), the output must be offset by 273.2µA in order to read out in degrees Celsius. The output of the AD590 flows through a 1kΩ resistance, developing a voltage of 1mV/K (Figure 1). The output of an AD580 2.5-volt reference is divided down by resistors to provide a 273.2mV offset, which is subtracted from the voltage across the 1kΩ resistor by an AD521 instrumentation amplifier. The AD521 provides a gain of 10.0, so that the output range, corresponding to 0 to 100°C, is 0 to 1.00V (10mV/°C).



VS
OFFSET REFERENCE
AD580L
+2.5V
MEASURED TEMP 0 TO 100°C
IT
R2 9.09k
P2 15k TRIM 100°C
AD590J
IT
R5 96.3k
P1 200Ω TRIM 0°C
IT
R3 1kΩ
R4 10k RG
AD521L
EO
REMOTE TEMPERATURE-TO-CURRENT TRANSDUCER, 1µA/k.
AD590 IC IS AVAILABLE IN PROBE AS AC2626J
R1 1kΩ 0.1%
LOW TCR METERING RESISTOR, 1mV/µA = 1mV/k
INSTRUMENTATION AMPLIFIER, GAIN OF 10, 0.00V TO 1.00 FS 10mV/°C

Figure 1. Thermometer Circuit

The desired system accuracy is to within 1.0°C; as noted, all errors other than that of the AD590 must contribute the equivalent of less than 0.7°. It will be helpful to assemble an error budget for the circuit, assessing the contributions of each of the elements (Table 1). Errors will be expressed in degrees Celsius.

AD590 regulation. If the AD590 is excited by a voltage source of between 5 and 10V, the typical regulation is 0.2µA/V (0.2°C/V). With 1% source regulation, this contribution will be 0.01°C

AD590 linearity error. Total error for AD590J, over the 0 to 100°C range, with two trims, is 0.3°C. Those trims will be the gain and offset trims for the whole circuit, accounting for resistor and ratio errors, AD521L gain, offset and bias-current errors, AD580L voltage error, and the AD590J's calibration error 0.3°C

R1 temperature coefficient. Since R1 is responsible for the conversion of the AD590's current to voltage, high absolute accuracy is important. Consequently, we would expect to use a device having 10ppm/°C or less in this spot. For ±15°C, the maximum error is 373.2µA X 10^{-5}/°C X 15° = 0.06µA 0.06°C

(typical at 25°C and rated supply voltage unless noted otherwise)

Parameter	Condition	Specification
AD580L 2.5V VOLTAGE REFERENCE		
Output voltage	V_S = +15V	2.450V min, 2.550V max
Input voltage, operating		30V max, 7V min
Line regulation	7V≤V_{IN}≤30V	2mV max
Temperature sensitivity	0 to 70°C	4.3mV max, 25ppm/°C, typ
Noise	0.1 to 10Hz	60µV, p-p
Stability (drift with time)	long term	250µV (0.01%)
	per month	25µV (10ppm)
AD590J 1µV/K TEMPERATURE TRANSDUCER		
Output current	Nominal at 25°C (298.2k)	298.2µA
Input voltage, operating		30V max, 4V min
Calibration error	25°C, V_S = 5V	±5°C max
Linearity error	Two trims, 0 to 100°C range	0.3°C max
Repeatability	per month	0.1°C max
Long-term drift		0.1°C max
Noise spectral density		40pA/$\sqrt{Hz}$
Power-supply rejection	+5V≤V_S≤+15V	0.2µA/V
Operating range		-55°C to +150°C
AD521L DIFFERENTIAL INSTRUMENTATION AMPLIFIER		
Gain equation (volts/volt)	Nominal	G = R_S/R_G
Error from equation	Untrimmed	(±0.25 - 0.004G)%
Nonlinearity	±9V output	0.1% max
Gain tempco	0 to 70°C	±(3±0.05G)ppm/°C
Voltage offset	Input	1.0mV max
	Output	100mV max
Voltage offset tempco	Input, 0 to 70°C	2µV/°C max
	Output, 0 to 70°C	75µV/°C max
Voltage offset vs. supply	Input	3µV/%
	Output, untrimmed*	0.5mV/%
Bias current	25°C	40nA max
Bias current tempco	0 to 70°C	500pA/°C
Input impedance	Common-mode	6 X 10^{10}Ω‖3.0pF
Common-mode rejection	G = 10, dc to 60Hz, 1kΩ source unbalance	94dB min
Voltage noise	G = 10, 0.1Hz to 10Hz, p-p, RTO	225µV

*Can be reduced by trimming the output offset.

Table 1. Device Specifications Pertinent to the Analysis in the Text

---

[1] Accuracies of the AD590 Application Note, Analog Devices.

AD580 temperature coefficient. The specified tempco for the AD580L is 25ppm/°C typical (61ppm/°C max over the range 0 to 70°C). Since operation is over a narrow range, the typical value is most useful, unless the AD580 has a critical effect on the overall error. $25 \times 10^{-6}/^\circ C \times 273mV \times 15^\circ = 0.1mV$ 0.10°C

Resistive divider tempco. The absolute values of R2 and R3 are of considerably less importance than their ability to track. 10ppm/°C is a reasonable value for tracking tempco. $10^{-5}/^\circ C \times 273mV \times 15^\circ = 0.04mV$ 0.04°C

Common-mode error. At a gain of 10, the minimum common-mode error of the AD521L amplifier is 94dB, one part in 50,000 of the common-mode voltage (273mV), or 5μV (negligible) 0.0°C

AD521 temperature coefficient. The specified input offset tempco for the AD521L is 2μV/°C max, and the output offset tempco is 75μV/°C max (7.5μV/°C, referred to the input), for a total of 9.5μV/°C R.T.I. $9.5\mu V/^\circ C \times 15^\circ = 143\mu V$ 0.14°C

AD521 bias-current tempco. The maximum bias-current change is $500pA/^\circ C \times 30^\circ$ (range) = 15nA. The equivalent offset-voltage change is $15nA \times 1k\Omega = 15\mu V$ 0.02°C

AD521 gain tempco. The circuit will be calibrated for correct output at 100°C by trimming of the gain of the AD521 at a 25°C ambient temperature. Variation of gain will cause output errors. The specified gain tempco at a gain of 10 for the AD521L is 3.5ppm/°C typical. If max is arbitrarily assumed to be ten times worse, and the resistors contribute 15ppm/°C additional, the maximum error will be $50 \times 10^{-6}/^\circ C \times 100^\circ \times 15^\circ = 0.075^\circ$ 0.075°C

AD521 nonlinearity. The 0.1% nonlinearity specification applies for a ±9V output swing; for a 1V full-scale swing, it may be reasonable to expect a tenfold improvement, or a 1mV linearity error, equivalent to 0.1°C 0.1°C

Total error (worst case) 0.84°C

This means that, once the circuit has been calibrated at 0°C and 100°C (25°C ambient), the maximum error at any combination of measured and ambient temperatures can reasonably be expected to be less than 1°C.

If the summation were root-sum-of-squares, instead of worst-case, the error would come to less than 0.4°. This suggests that the design is quite conservative, since the probability of worst-case error is low; also (with some risk), it suggests that if an AD590M were used in the same design, temperature could be measured to within 0.25°C over the range. Naturally, every precaution should be taken to avoid additional errors attributable to either Murphy's or Natural Law. Aside from errors attributable to ambient temperature variations, this simple interface will require some form of protection from extraneous signals. Shielding and grounding should follow the practice suggested earlier in this book. In addition, capacitance across R1 will help reduce the effects of any ac currents induced in the twisted pair. Power supplies must be chosen to minimize error due to sensitivity of any of the elements to power-supply voltage changes, and bypassed to minimize coupling of interference through the power-supply leads.

ANALOG DEVICES

Two-Terminal IC Temperature Transducer

AD590*

FEATURES

Linear Current Output: 1μA/°K

Wide Range: -55°C to +150°C

Probe Compatible Ceramic Sensor Package

Two-Terminal Device: Voltage In/Current Out

Laser Trimmed to ±0.5°C Calibration Accuracy (AD590M)

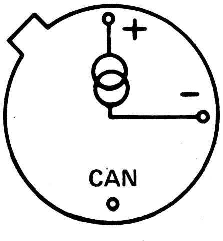
Excellent Linearity: ±0.3°C Over Full Range Range (AD590M)

Wide Power Supply Range: +4V to +30V

Sensor Isolation from Case

Low Cost

AD590 FUNCTIONAL BLOCK DIAGRAM



TO-52
BOTTOM VIEW

PRODUCT DESCRIPTION

The AD590 is a two-terminal integrated circuit temperature transducer which produces an output current proportional to absolute temperature. For supply voltages between +4V and +30V the device acts as a high impedance, constant current regulator passing 1μA/°K. Laser trimming of the chip's thin film resistors is used to calibrate the device to 298.2μA output at 298.2°K (+25°C).

The AD590 should be used in any temperature sensing application below +150°C in which conventional electrical temperature sensors are currently employed. The inherent low cost of a monolithic integrated circuit combined with the elimination of support circuitry makes the AD590 an attractive alternative for many temperature measurement situations. Linearization circuitry, precision voltage amplifiers, resistance measuring circuitry and cold junction compensation are not needed in applying the AD590.

In addition to temperature measurement, applications include temperature compensation or correction of discrete components, biasing proportional to absolute temperature, flow rate measurement, level detection of fluids and anemometry. The AD590 is available in chip form making it suitable for hybrid circuits and fast temperature measurements in protected environments.

The AD590 is particularly useful in remote sensing applications. The device is insensitive to voltage drops over long lines due to its high impedance current output. Any well-insulated twisted pair is sufficient for operation hundreds of feet from the receiving circuitry. The output characteristics also make the AD590 easy to multiplex: the current can be switched by a CMOS multiplexer or the supply voltage can be switched by a logic gate output.

PRODUCT HIGHLIGHTS

1. The AD590 is a calibrated two terminal temperature sensor requiring only a dc voltage supply (+4V to +30V). Costly transmitters, filters, lead wire compensation and linearization circuits are all unnecessary in applying the device.
2. State-of-the-art laser trimming at the wafer level in conjunction with extensive final testing insures that AD590 units are easily interchangeable.
3. Superior interference rejection results from the output being a current rather than a voltage. In addition, power requirements are low (1.5mW's @ 5V @ +25°C). These features make the AD590 easy to apply as a remote sensor.
4. The high output impedance (>10MΩ) provides excellent rejection of supply voltage drift and ripple. For instance, changing the power supply from 5V to 10V results in only a 1μA maximum current change, or 1°C equivalent error.
5. The AD590 is electrically durable: it will withstand a forward voltage up to 44V and a reverse voltage of 20V. Hence, supply irregularities or pin reversal will not damage the device.
6. The device is hermetically sealed in both a ceramic sensor package and in to TO-52 package. MIL-STD-883 processing to level B is available and, for large unit volumes, special accuracy requirements over limited temperature ranges can be satisfied by selections at final test. The device is also available in chip form.

***Covered by Patent No. 4,123,698**

SPECIFICATIONS (typical @ +25°C and V_S = 5V unless otherwise noted)

MODEL	AD590I	AD590J	AD590K	AD590L	AD590M
ABSOLUTE MAXIMUM RATINGS					
Forward Voltage (E+ to E-)	+44V	*	*	*	*
Reverse Voltage (E+ to E-)	-20V	*	*	*	*
Breakdown Voltage (Case to E+ or E-)	±200V	*	*	*	*
Rated Performance Temperature Range[1]	-55°C to +150°C	*	*	*	*
Storage Temperature Range[1]	-65°C to +155°C	*	*	*	*
Lead Temperature (Soldering, 10 sec)	+300°C	*	*	*	*
POWER SUPPLY					
Operating Voltage Range	+4V to +30V	*	*	*	*
OUTPUT					
Nominal Current Output @ +25°C (298.2°K)	298.2μA	*	*	*	*
Nominal Temperature Coefficient	1μA/°K	*	*	*	*
Calibration Error @ +25°C	±10.0°C max	±5.0°C max	±2.5°C max	±1.0°C max	±0.5°C max
Absolute Error[2] (over rated performance temperature range)					
Without External Calibration Adjustment	±20.0°C max	±10.0°C max	±5.5°C max	±3.0°C max	±1.7°C max
With +25°C Calibration Error Set to Zero	±5.8°C max	±3.0°C max	±2.0°C max	±1.6°C max	±1.0°C max
Nonlinearity	±3.0°C max	±1.5°C max	±0.8°C max	±0.4°C max	±0.3°C max
Repeatability[3]	±0.1°C max	*	*	*	*
Long Term Drift[4]	±0.1°C/month max	*	*	*	*
Current Noise	$40pA/\sqrt{Hz}$	*	*	*	*
Power Supply Rejection					
$+4V \leqslant V_S \leqslant +5V$	0.5μA/V	*	*	*	*
$+5V \leqslant V_S \leqslant +15V$	0.2μA/V	*	*	*	*
$+15V \leqslant V_S \leqslant +30V$	0.1μA/V	*	*	*	*
Case Isolation to Either Lead	$10^{10}\Omega$	*	*	*	*
Effective Shunt Capacitance	100pF	*	*	*	*
Electrical Turn-On Time[5]	20μs	*	*	*	*
Reverse Bias Leakage Current[6] (Reverse Voltage = 10V)	10pA	*	*	*	*
PACKAGE OPTION[7]					
"H" Package: TO-52	AD590IH	AD590JH	AD590KH	AD590LH	AD590MH
"F" Package: Flat Pack (F2A)	AD590IF	AD590JF	AD590KF	AD590LF	AD590MF

---

*Specifications same as AD590I

[1] The AD590 has been used at -100°C and +200°C for short periods of measurement with no physical damage to the device. However, the absolute errors specified apply to only the rated performance temperature range.

[2] See section on temperature sensor specifications for explanation of error components. Note that ± 1°C error is the equivalent of ± 1μA error.

[3] Maximum deviation between +25°C readings after temperature cycling between -55°C and +150°C; guaranteed not tested.

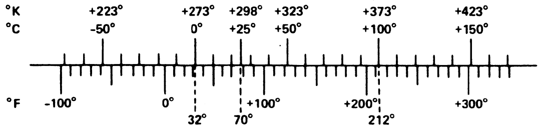
[4] Conditions: constant +5V, constant +125°C; guaranteed, not tested.

[5] Does not include self heating effects.

[6] Leakage current doubles every 10°C.

[7] See Section 20 for package outline information.

Specifications subject to change without notice.



TEMPERATURE SCALE CONVERSION EQUATIONS

$$°C = \frac{5}{9}(°F - 32) \qquad °K = °C + 273.15$$

$$°F = \frac{9}{5}°C + 32 \qquad °R = °F + 459.7$$

CIRCUIT DESCRIPTION[1]

The AD590 uses a fundamental property of the silicon transistors from which it is made to realize its temperature proportional characteristic: if two identical transistors are operated at a constant ratio of collector current densities, r, then the difference in their base-emitter voltages will be (kT/q)(In r). Since both k, Boltzman's constant and q, the charge of an electron, are constant, the resulting voltage is directly proportional to absolute temperature (PTAT).

In the AD590, this PTAT voltage is converted to a PTAT current by low temperature coefficient thin film resistors. The total current of the device is then forced to be a multiple of this PTAT current. Referring to Figure 1, the schematic diagram of the AD590, Q8 and Q11 are the transistors that produce the PTAT voltage. R5 and R6 convert the voltage to current. Q10, whose collector current tracks the collector currents in Q9 and Q11, supplies all the bias and substrate leakage current for the rest of the circuit, forcing the total current to be PTAT. R5 and R6 are laser trimmed on the wafer to calibrate the device at +25°C.

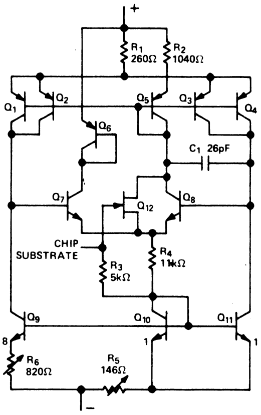


Figure 1. Schematic Diagram

Figure 2 shows the typical V−I characteristic of the circuit at +25°C and the temperature extremes.

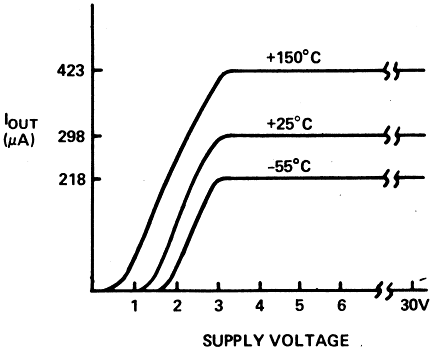


Figure 2. V−I Plot

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[1] For a more detailed circuit description see M.P. Timko, "A Two-Terminal IC Temperature Transducer," IEEE J. Solid State Circuits, Vol. SC-11, p. 784-788, Dec. 1976.

EXPLANATION OF TEMPERATURE SENSOR SPECIFICATIONS

The way in which the AD590 is specified makes it easy to apply in a wide variety of different applications. It is important to understand the meaning of the various specifications and the effects of supply voltage and thermal environment on accuracy.

The AD590 is basically a PTAT (proportional to absolute temperature)[1] current regulator. That is, the output current is equal to a scale factor times the temperature of the sensor in degrees Kelvin. This scale factor is trimmed to 1μA/°K at the factory, by adjusting the indicated temperature (i.e. the output current) to agree with the actual temperature. This is done with 5V across the device at a temperature within a few degrees of 25°C (298.2°K). The device is then packaged and tested for accuracy over temperature.

CALIBRATION ERROR

At final factory test the difference between the indicated temperature and the actual temperature is called the calibration error. Since this is a scale factor error, its contribution to the total error of the device is PTAT. For example, the effect of the 1°C specified maximum error of the AD590L varies from 0.73°C at -55°C to 1.42°C at 150°C. Figure 3 shows how an exaggerated calibration error would vary from the ideal over temperature.

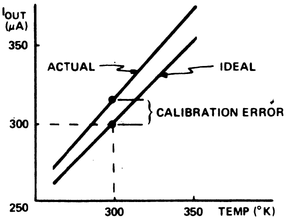

Figure 3. Calibration Error vs. Temperature

The calibration error is a primary contributor to maximum total error in all AD590 grades. However, since it is a scale factor error, it is particularly easy to trim. Figure 4 shows the most elementary way of accomplishing this. To trim this circuit the temperature of the AD590 is measured by a reference temperature sensor and R is trimmed so that V_T = 1mV/°K at that temperature. Note that when this error is trimmed out at one temperature, its effect is zero over the entire temperature range. In most applications there is a current to voltage conversion resistor (or, as with a current input ADC, a reference) that can be trimmed for scale factor adjustment.

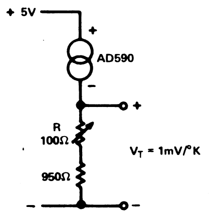

Figure 4. One Temperature Trim

ERROR VERSUS TEMPERATURE: WITH CALIBRATION ERROR TRIMMED OUT

Each AD590 is also tested for error over the temperature range with the calibration error trimmed out. This specification could also be called the "variance from PTAT" since it is the maximum difference between the actual current over temperature and a PTAT multiplication of the actual current at 25°C. This error consists of a slope error and some curvature, mostly at the temperature extremes. Figure 5 shows a typical AD590K temperature curve before and after calibration error trimming.

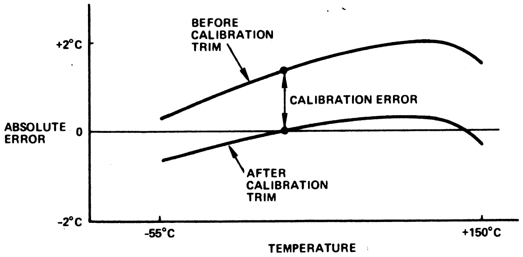

Figure 5. Effect of Scale Factor Trim on Accuracy

ERROR VERSUS TEMPERATURE: NO USER TRIMS

Using the AD590 by simply measuring the current, the total error is the "variance from PTAT" described above plus the effect of the calibration error over temperature. For example the AD590L maximum total error varies from 2.33°C at -55°C to 3.02°C at 150°C. For simplicity, only the larger figure is shown on the specification page.

NONLINEARITY

Nonlinearity as it applies to the AD590 is the maximum deviation of current over temperature from a best-fit straight line. The nonlinearity of the AD590 over the -55°C to +150°C range is superior to all conventional electrical temperature sensors such as thermocouples, RTD's and thermistors. Figure 6 shows the nonlinearity of the typical AD590K from Figure 5.

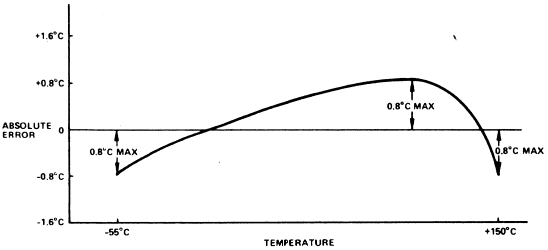

Figure 6. Nonlinearity

Figure 7A shows a circuit in which the nonlinearity is the major contributor to error over temperature. The circuit is trimmed by adjusting R_1 for a 0V output with the AD590 at 0°C. R_2 is then adjusted for 10V out with the sensor at 100°C. Other pairs of temperatures may be used with this procedure as long as they are measured accurately by a reference sensor. Note that for +15V output (150°C) the V+ of the op amp must be greater than 17V. Also note that V- should be at least -4V: if V- is ground there is no voltage applied across the device.

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[1] T(°C) = T(°K) - 273.2; Zero on the Kelvin scale is "absolute zero"; there is no lower temperature.

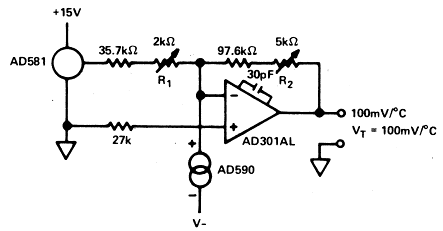


Figure 7A. Two Temperature Trim

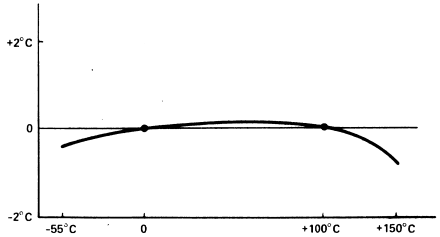


Figure 7B. Typical Two-Trim Accuracy

VOLTAGE AND THERMAL ENVIRONMENT EFFECTS

The power supply rejection specifications show the maximum expected change in output current versus input voltage changes. The insensitivity of the output to input voltage allows the use of unregulated supplies. It also means that hundreds of ohms of resistance (such as a CMOS multiplexer) can be tolerated in series with the device.

It is important to note that using a supply voltage other than 5V does not change the PTAT nature of the AD590. In other words, this change is equivalent to a calibration error and can be removed by the scale factor trim (see previous page).

The AD590 specifications are guaranteed for use in a low thermal resistance environment with 5V across the sensor. Large changes in the thermal resistance of the sensor's environment will change the amount of self-heating and result in changes in the output which are predictable but not necessarily desirable.

The thermal environment in which the AD590 is used determines two important characteristics: the effect of self heating and the response of the sensor with time.

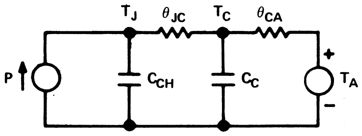


Figure 8. Thermal Circuit Model

Figure 8 is a model of the AD590 which demonstrates these characteristics. As an example, for the TO-52 package, θ_{JC} is the thermal resistance between the chip and the case, about 26°C/watt. θ_{CA} is the thermal resistance between the case and its surroundings and is determined by the characteristics of the thermal connection. Power source P represents the power dissipated on the chip. The rise of the junction temperature, T_J, above the ambient temperature T_A is:

$$T_J - T_A = P\,(\theta_{JC} + \theta_{CA}). \qquad \text{Eq. 1}$$

Table 1 gives the sum of θ_{JC} and θ_{CA} for several common thermal media for both the "H" and "F" packages. The heat-sink used was a common clip-on. Using Equation 1, the temperature rise of an AD590 "H" package in a stirred bath at +25°C, when driven with a 5V supply, will be 0.06°C. However, for the same conditions in still air the temperature rise is 0.72°C. For a given supply voltage, the temperature rise varies with the current and is PTAT. Therefore, if an application circuit is trimmed with the sensor in the same thermal environment in which it will be used, the scale factor trim compensates for this effect over the entire temperature range.

MEDIUM	$\theta_{JC} + \theta_{CA}$ (°C/watt)		τ (sec)(Note 3)	
	H	F	H	F
Aluminum Block	30	10	0.6	0.1
Stirred Oil[1]	42	60	1.4	0.6
Moving Air[2]				
With Heat Sink	45	–	5.0	–
Without Heat Sink	115	190	13.5	10.0
Still Air				
With Heat Sink	191	–	108	–
Without Heat Sink	480	650	60	30

[1] Note: τ is dependent upon velocity of oil; average of several velocities listed above.

[2] Air velocity ≅ 9ft/sec.

[3] The time constant is defined as the time required to reach 63.2% of an instantaneous temperature change.

Table 1. Thermal Resistances

The time response of the AD590 to a step change in temperature is determined by the thermal resistances and the thermal capacities of the chip, C_{CH}, and the case, C_C. C_{CH} is about 0.04 watt-sec/°C for the AD590. C_C varies with the measured medium since it includes anything that is in direct thermal contact with the case. In most cases, the single time constant exponential curve of Figure 9 is sufficient to describe the time response, T (t). Table 1 shows the effective time constant, τ, for several media.

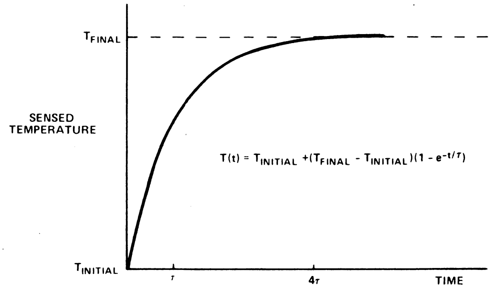


Figure 9. Time Response Curve

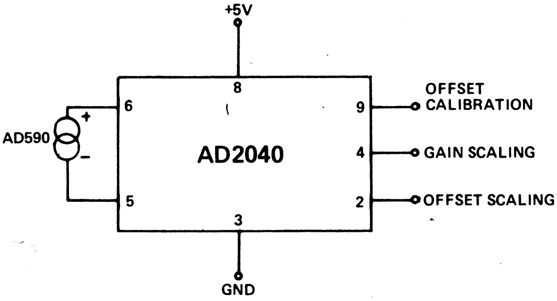


Figure 10. Variable Scale Display

Figure 10 demonstrates the use of a low-cost Digital Panel Meter for the display of temperature on either the Kelvin, Celsius or Fahrenheit scales. For Kelvin temperature Pins 9, 4 and 2 are grounded; and for Fahrenheit temperature Pins 4 and 2 are left open.

The above configuration yields a 3 digit display with 1°C or 1°F resolution, in addition to an absolute accuracy of ±2.0°C over the -55°C to +125°C temperature range if a one-temperature calibration is performed on an AD590K, L, or M.

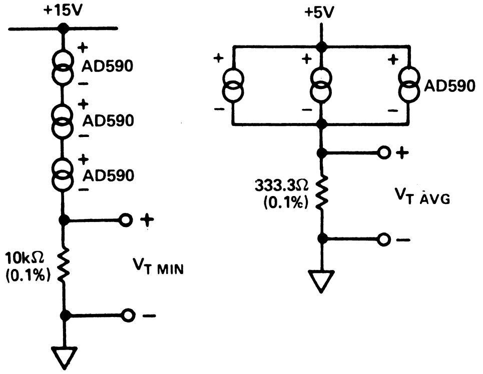


Figure 11. Series & Parallel Connection

Connecting several AD590 units in series as shown in Figure 11 allows the minimum of all the sensed temperatures to be indicated. In contrast, using the sensors in parallel yields the average of the sensed temperatures.

The circuit of Figure 12 demonstrates one method by which differential temperature measurements can be made. R_1 and R_2 can be used to trim the output of the op amp to indicate a desired temperature difference. For example, the inherent offset between the two devices can be trimmed in. If V+ and V- are radically different, then the difference in internal dissipation will cause a differential internal temperature rise. This effect can be used to measure the ambient thermal resistance seen by the sensors in applications such as fluid level detectors or anemometry.

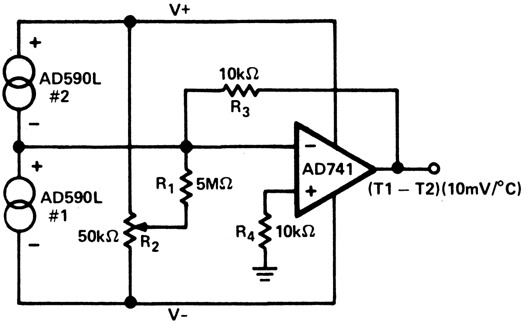


Figure 12. Differential Measurements

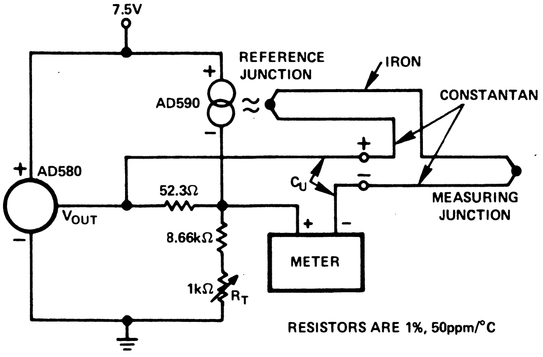


Figure 13. Cold Junction Compensation Circuit for Type J Thermocouple

Figure 13 is an example of a cold junction compensation circuit for a Type J Thermocouple using the AD590 to monitor the reference junction temperature. This circuit replaces an ice-bath as the thermocouple reference for ambient temperatures between +15°C and +35°C. The circuit is calibrated by adjusting R_T for a proper meter reading with the measuring junction at a known reference temperature and the circuit near +25°C. Using components with the T.C.'s as specified in Figure 13, compensation accuracy will be within ±0.5°C for circuit temperatures between +15°C and +35°C. Other thermocouple types can be accommodated with different resistor values. Note that the T.C.'s of the voltage reference and the resistors are the primary contributors to error.

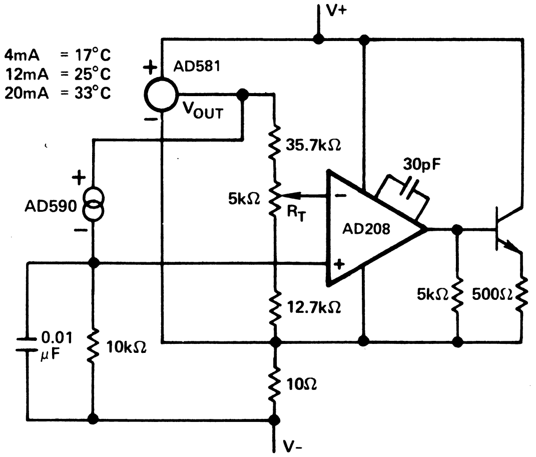


Figure 14. 4 to 20mA Current Transmitter

Figure 14 is an example of a current transmitter designed to be used with 40V, 1kΩ systems; it uses its full current range of 4mA to 20mA for a narrow span of measured temperatures. In this example the 1μA/°K output of the AD590 is amplified to 1mA/°C and offset so that 4mA is equivalent to 17°C and 20mA is equivalent to 33°C. R_T is trimmed for proper reading at an intermediate reference temperature. With a suitable choice of resistors, any temperature range within the operating limits of the AD590 may be chosen.

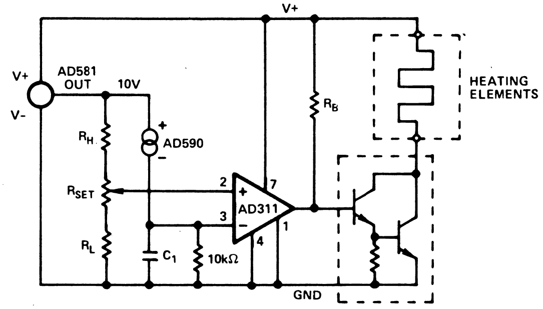


Figure 15. Simple Temperature Control Circuit

Figure 15 is an example of a variable temperature control circuit (thermostat) using the AD590. R_H and R_L are selected to set the high and low limits for R_{SET}. R_{SET} could be a simple pot, a calibrated multi-turn pot or a switched resistive divider. Powering the AD590 from the 10V reference isolates the AD590 from supply variations while maintaining a reasonable voltage (~7V) across it. Capacitor C_1 is often needed to filter extraneous noise from remote sensors. R_B is determined by the β of the power transistor and the current requirements of the load.

Figure 16 shows how the AD590 can be configured with an 8 bit DAC to produce a digitally controlled setpoint. This particular circuit operates from 0 (all inputs high) to +51°C (all inputs low) in 0.2°C steps. The comparator is shown with 1°C hysteresis which is usually necessary to guard-band for extraneous noise; omitting the 5.1MΩ resistor results in no hysteresis.

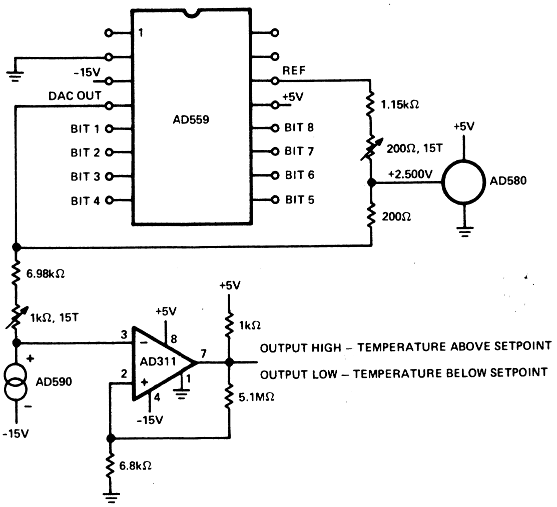


Figure 16. DAC Setpoint

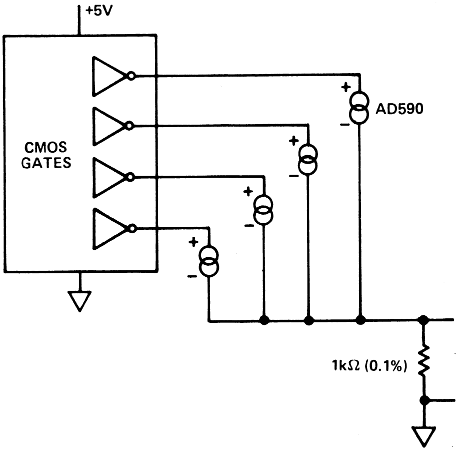


Figure 17. AD590 Driven from CMOS Logic

The voltage compliance and the reverse blocking characteristic of the AD590 allows it to be powered directly from +5V CMOS logic. This permits easy multiplexing, switching or pulsing for minimum internal heat dissipation. In Figure 17 any AD590 connected to a logic high will pass a signal current through the current measuring circuitry while those connected to a logic zero will pass insignificant current. The outputs used to drive the AD590's may be employed for other purposes, but the additional capacitance due to the AD590 should be taken into account.

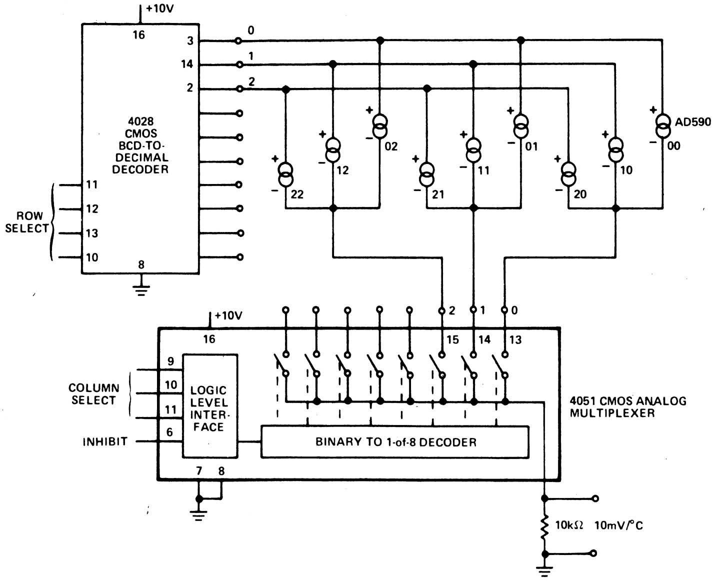


Figure 18. Matrix Multiplexer

CMOS Analog Multiplexers can also be used to switch AD590 current. Due to the AD590's current mode, the resistance of such switches is unimportant as long as 4V is maintained across the transducer. Figure 18 shows a circuit which combines the principal demonstrated in Figure 17 with an 8 channel CMOS Multiplexer. The resulting circuit can select one of eighty sensors over only 18 wires with a 7 bit binary word. The inhibit input on the multiplexer turns all sensors off for minimum dissipation while idling.

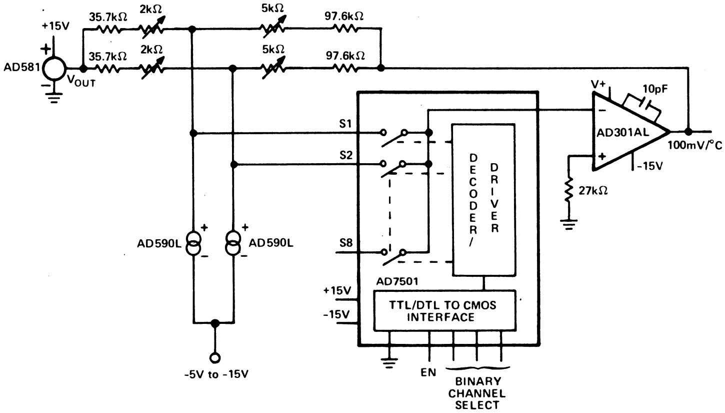


Figure 19. 8-Channel Multiplexer

Figure 19 demonstrates a method of multiplexing the AD590 in the two-trim mode (Figure 7). Additional AD590's and their associated resistors can be added to multiplex up to 8 channels of ±0.5°C absolute accuracy over the temperature range of -55°C to +125°C. The high temperature restriction of +125°C is due to the output range of the op amps; output to +150°C can be achieved by using a +20V supply for the op amp.

Digital-to-Analog Converters

Contents

	Page
Section Guides	10–3
General Information	10–6
Specifications and Terms	10–7
AD370/AD371 Complete Low-Power 12-Bit Hybrid-IC DACs	10–11
●AD390 Quad 12-Bit Microprocessor-Compatible D/A Converter	10–15
AD558 Low-Cost Complete µP-Compatible 8-Bit IC DACs	10–17
AD561 Low-Cost 10-Bit IC Complete Current-Output DACs	10–25
AD562 High-Performance IC 12-Bit Current-Output DACs	10–33
AD563 High-Performance IC 12-Bit Current-Output DACs Including Reference	10–33
AD565 High-Performance Monolithic 12-Bit Current-Output DACs Including Reference	10–39
●AD565A Complete High Speed 12-Bit Monolithic D/A Converter	10–43
AD566 High-Performance Monolithic 12-Bit Current-Output DACs	10–51
●AD566A Low Cost High Speed 12-Bit Monolithic D/A Converter	10–55
●AD567 Microprocessor-Compatible 12-Bit D/A Converter	10–63
AD1408/1508 8-Bit Monolithic Multiplying DACs	10–71
●AD3860 Complete, Voltage Output 12-Bit DAC	10–75
AD7110 CMOS IC Digitally Controlled Audio Attenuator	10–79
●AD7111 CMOS Logarithmic D/A Converter	10–85
●AD7118 CMOS Logarithmic D/A Converter	10–91
AD7520/AD7521 CMOS 10- and 12-Bit Multiplying DACs	10–97
AD7522 CMOS 10-Bit Double-Buffered Multiplying DACs	10–105
AD7523 CMOS 8-Bit Multiplying DACs	10–111
AD7524 CMOS 8-Bit Buffered Multiplying DACs	10–115
AD7525 CMOS 3 1/2-Digit BCD Digitally Controlled Potentiometer	10–121
●AD7527 CMOS 10-Bit Process Control DAC	10–127
●AD7528 CMOS Dual 8-Bit Buffered Multiplying DAC	10–139
AD7530/AD7531 CMOS 10- and 12-Bit Monolithic Multiplying DACs	10–147
AD7533 CMOS Low-Cost 10-Bit Multiplying DACs	10–151
AD7541 CMOS 12-Bit Monolithic Multiplying DACs	10–157
●AD7541A CMOS 12-Bit Monolithic Multiplying DAC	10–163
AD7542 CMOS 12-Bit Microprocessor Compatible DACs	10–165
AD7543 CMOS 12-Bit Serial-Input DACs	10–173
●AD7544 CMOS 12-Bit, 6 Word, FIFO, DAC	10–181
●AD7545 CMOS 12-Bit Buffered Multiplying DAC	10–189
●AD7546 High Resolution 16-Bit D/A Converter	10–197
AD DAC-08 8-Bit Monolithic High-Speed Multiplying DACs	10–205
●AD DAC71/72 High Resolution 16-Bit D/A Converter	10–211
AD DAC80 Low-Cost 12-Bit Hybrid IC DACs	10–215
AD DAC85 High-Performance 12-Bit Hybrid IC DACs	10–223
AD DAC87 Wide-Temperature-Range 12-Bit Hybrid IC DACs	10–231
●AD DAC100 10-Bit Monolithic D/A Converter	10–235
DAC1136/DAC1138 High-Resolution 16- and 18-Bit DAC	10–243
DAC1420/DAC1422 4-to-20mA Output 8- and 10-Bit DAC	10–245

Page

DAC1423 4-20mA Output 10-Bit Isolated DAC (ISO-DAC™) 10–247
•HDD Series Hybrid Video Low Glitch D/A Converter 10–249
•HDD1206 12-Bit Deglitched Voltage Output D/A Converter 10–255
•HDG Series Hybrid Video Digital-to-Analog Converters 10–259
HDH/HDS 8-, 10-, and 12-Bit Video-Speed Hybrid Current-and-Voltage-Output DACs 10–265
•HDS-0810E, HDS-1015E Ultra High-Speed ECL Hybrid D/A Converter 10–269
•HDS-1240E Ultra High-Speed ECL Hybrid D/A Converter 10–271
MDMS Ultra-High-Speed 8-, 10- and 11-Bit Multiplying DACs 10–275

•New product since the *1980 Data-Acquisition Components and Subsystems Catalog.*
ISO-DAC is a trademark of Analog Devices, Inc.

Selection Guide
Digital-to-Analog Converters

GENERAL PURPOSE DACs FEATURE SELECTION CHARTS

		GENERAL PURPOSE					FAST		
		AD1408	AD DAC80-I	AD DAC80-V	AD DAC85-I	AD DAC85-V	AD DAC-08	AD561	AD DAC100
Resolution	8 Bits	●					●		
	10 Bits							●	●
	12 Bits		●	●	●	●			
Accuracy	8 Bits	●					●		
	10 Bits							●	●
	12 Bits		●	●	●	●			
Output Format	Current	●	●		●		●	●	●
	Voltage			●		●			
Internal Reference			●	●	●	●			
Multiplication Capability	2 Quadrant	●					●	●	●
	4 Quadrant								
Logic Compatible with	TTL	●	●	●	●	●	●	●	●
	CMOS	●					●	●	
Input Coding	Binary	●	●	●	●	●	●	●	●
	BCD		●	●	●	●			
Second Source		●	●	●	●	●	●		●
Single Power Supply									
Input Data Latch Structure	Serial								
	Parallel								
Operating Temperature Ranges[1]	C = 0 to +70°C	●	●	●	●	●	●	●	●
	I = -25°C to +85°C				●	●			
	M = -55°C to +125°C	●			●	●	●	●	●
Low Power									
Dice Availability							●	●	
Volume I Page		10-71	10-215	10-215	10-223	10-223	10-205	10-25	10-235

[1] C = Commercial I = Industrial M = Military

		µP BUS COMPATIBLE			MULTIPLYING								SPECIAL PURPOSE	
		AD558	AD7524	AD7522	AD7523	AD7520	AD7530	AD7533	AD7521	AD7531	AD7541	AD7541A	AD7527 SYSTEMS DAC	AD7528 DUAL DAC
Resolution	8 Bits	●	●		●									●
	10 Bits			●		●	●	●					●	
	12 Bits								●	●	●	●		
Accuracy	8 Bits	●	●	●	●	●	●	●	●	●				●
	10 Bits		●	●	●	●	●	●	●	●			●	
	12 Bits										●	●		
Output Format	Current		●	●	●	●	●	●	●	●	●	●	●	●
	Voltage	●												
Internal Reference		●												
Multiplication Capability	2 Quadrant		●	●	●	●	●	●	●	●	●	●	●	●
	4 Quadrant		●	●	●	●	●	●	●	●	●	●	●	●
Logic Compatible with	TTL	●	●	●		●	●	●	●	●	●	●		●
	CMOS	●	●	●	●	●	●	●	●	●	●	●	●	●
Input Coding	Binary	●	●	●	●	●	●	●	●	●	●	●	●	●
	BCD													
Second Source			●	●	●	●	●	●	●	●	●	●		
Single Power Supply		●												
Input Data Latch Structure	Serial			●										
	Parallel	●	●	●									●	●
Operating Temperature Ranges[1]	C = 0 to +70°C	●	●	●	●	●	●	●	●	●	●	●	●	●
	I = -25°C to +85°C		●	●	●	●	●	●	●	●	●	●	●	●
	M = -55°C to +125°C	●	●	●	●	●		●	●		●	●	●	●
Low Power		●	●	●	●	●	●	●	●	●	●	●	●	●
Dice Availability		●	●	●	●	●		●	●		●			
Volume I Page		10-17	10-115	10-105	10-111	10-97	10-147	10-151	10-97	10-147	10-157	10-163	10-127	10-139

[1] C = Commercial I = Industrial M = Military

HIGH PERFORMANCE DACS FEATURE SELECTION CHARTS

HIGH PERFORMANCE

MULTIPLYING

μP COMPATIBLE

FAST

		AD563	AD DAC87	AD370	AD371	AD DAC71/ DAC72	AD7546	DAC1136	DAC1138	AD3860	AD567	AD565	AD565A	DAC1108	AD566	AD566A	MDMS
Resolution	0.375dB Steps to 88.5dB																
	1.5dB Steps to 88.5dB																
	8 Bits																●
	10 Bits																●
	12 Bits	●	●	●	●					●	●	●	●	●	●	●	
	16 Bits					●	●	●									
	18 Bits								●								
Output Format	Current	●	●					●	●		●	●	●	●	●	●	●
	Voltage		●	●	●	●	●	●	●	●							
Internal Reference		●	●	●	●	●		●	●	●	●	●	●	●			
Multiplication Capability	2 Quadrant						●								●	●	●
	4 Quadrant																
Logic Compatible with	TTL	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●
	CMOS	●	●	●	●	●	●										
Input Code	Binary	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●
	BCD	●	●														
Second Source		●	●	●	●	●				●		●	●		●	●	
Single Power Supply																	
Input Data Latch Structure	Serial																
	Parallel						●			●	●						
Operating Temperature Ranges[1]	C = 0 to +70°C	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	I = -25°C to +85°C					●	●										●
	M = -55°C to +125°C	●	●	●	●					●	●	●	●		●	●	
Low Power				●	●		●										
Input/Output Isolation																	
Dice Availability											●		●			●	
Volume I Page		10–33	10–231	10–11	10–11	10–211	10–197	10–243	10–243	10–75	10–63	10–39	10–43	–	10–51	10–55	10–275
Volume II Page		–	–	–	–	–	–	10–15	10–15	–	–	–	–	10–11	–	–	10–37

[1] C = Commercial I = Industrial M = Military

HIGH PERFORMANCE

SPECIAL PURPOSE

MULTIPLYING

μP BUS COMPATIBLE

ATTENUATION

PROCESS CONTROL 4 TO 20mA OUT μP BUS COMPATIBLE

QUAD DAC

		AD562	AD7541	AD7541A	AD7525	AD7542	AD7543	AD7544[1]	AD7545	AD7110	AD7118	AD7111	DAC1420	DAC1422	DAC1423	AD390
Resolution	0.375dB Steps to 88.5dB											●				
	1.5dB Steps to 88.5dB									●	●					
	8 Bits												●			
	10 Bits				●									●	●	
	12 Bits	●	●	●		●	●	●	●							●
	16 Bits															
	18 Bits															
Output Format	Current	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	Voltage															●
Internal Reference													●	●	●	●
Multiplication Capability	2 Quadrant	●	●	●	●	●	●	●	●	●	●	●				●
	4 Quadrant		●	●	●	●	●	●	●							
Logic Compatible with	TTL	●	●	●					●			●	●	●	●	●
	CMOS	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
Input Code	Binary	●	●	●		●	●	●	●	●	●	●				●
	BCD	●			●											
Second Source		●	●	●												
Single Power Supply													●	●	●	
Input Data Latch Structure	Serial						●									
	Parallel					●		●	●			●				●
Operating Temperature Ranges[2]	C = 0 to +70°C	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●
	I = -25°C to +85°C		●	●	●	●	●	●	●		●	●				
	M = -55°C to +125°C	●	●	●	●	●	●	●	●		●	●				●
Low Power			●	●	●	●	●	●	●	●	●	●				
Input/Output Isolation															●	
Dice Availablity			●			●	●									
Volume I Page		10–33	10–157	10–163	10–121	10–165	10–173	10–181	10–189	10–79	10–91	10–85	10–245	10–245	10–247	10–15
Volume II Page		–	–	–	–	–	–	–	–	–	–	–	10–23	10–23	10–27	–

[1] Six-Stage FIFO Input Register [2] C = Commercial I = Industrial M = Military

ULTRA FAST/VIDEO DACS FEATURE SELECTION CHARTS

		CURRENT OUT												
		HDG-0405	HDG-0605	HDG-0805	MDS-0815	MDS-1020	MDS-1240	HDS-0820	HDS-0810E	HDD-0810	HDD-0810C	HDS-1025	HDS-1015E	HDD-1015
Settling Time to Resolution in Bits	<550ns													
	<210ns													
	<75ns											●		
	<21ns				●	●	●	●	●	●	●		●	●
	<8ns	●	●	●										
Resolution	4 Bits	●												
	6 Bits		●											
	8 Bits			●	●			●	●	●	●			
	10 Bits					●						●	●	●
	11 Bits													
	12 Bits						●							
Application	General Purpose				●	●	●	●	●	●		●	●	●
	Lowest Glitch	●	●	●							●			
	Multiplying													
	Composite Video	●	●	●							●			
Output Format	Current	●	●	●	●	●	●	●	●	●	●	●	●	●
	Voltage													
Binary Logic	TTL				●	●	●	●				●		
	ECL	●	●	●					●	●	●		●	●
	Latched	●	●	●						●	●			●
Single Power Supply		●	●	●					●	●	●		●	●
Operating Temperature Ranges	0 to +70°C	●	●	●	●	●	●	●	●	●	●	●	●	●
	-25°C to +85°C									●	●			●
	-55°C to +125°C							●	●			●	●	
Volume I Page		10–259	10–259	10–259	–	–	–	10–265	10–269	10–249	10–249	10–265	10–269	10–249
Volume II Page		–	–	–	10–39	10–39	10–39	–	–	–	–	–	–	–

		CURRENT OUT							VOLTAGE OUT				
		HDD-1015C	HDS-1250	HDS-1240E	DAC1106	MDMS-0801	MDMS-1001	MDMS-1101	HDH-0802	HDH-1003	HDH-1205	MDD-0820	MDD-1020
Settling Time to Resolution in Bits	<550ns										●		
	<210ns					●	●	●	●	●			
	<75ns		●	●	●							●	●
	<21ns	●											
	<8ns												
Resolution	4 Bits												
	6 Bits												
	8 Bits				●	●			●			●	
	10 Bits	●			●		●			●			●
	11 Bits							●					
	12 Bits		●	●							●		
Application	General Purpose		●	●	●				●	●	●		
	Lowest Glitch											●	●
	Multiplying					●	●	●					
	Composite Video	●											
Output Format	Current	●	●	●	●	●	●	●				●	●
	Voltage								●	●	●	●	●
Binary Logic	TTL		●		●	●	●	●	●	●	●	●	●
	ECL	●		●									
	Latched	●											
Single Power Supply		●											
Operating Temperature Ranges	0 to +70°C	●	●	●	●	●	●	●	●	●	●	●	●
	-25°C to +85°C	●											
	-55°C to +125°C		●	●[1]					●	●	●		
Volume I Page		10–249	10–265	10–271	–	10–275	10–275	10–275	10–265	10–265	10–265	–	–
Volume II Page		–	–	–	10–11	10–37	10–37	10–37	–	–	–	10–33	10–33

[1] -55°C to +100°C

Orientation

Digital-to-Analog Converters

FACTORS IN CHOOSING A D/A CONVERTER

In the current issue of this two-volume catalog, there are listed some 56 different families of digital-to-analog converters (DACs). If one were to consider all the variations, there would be more than 224 types to choose among. The reason for so many different types is the number of degrees of freedom in selection—technological, functional, and performance. Complete information on converters may be found in the 250-page book, ANALOG-DIGITAL CONVERSION NOTES, published by Analog Devices and available for $5.95 from P.O. Box 796, Norwood MA 02062.

FUNCTIONAL CHARACTERISTICS

The basic structure of all conventional D/A converters involves a network of precision resistors, a set of switches, and some form of level-shifting to adapt the switch drives to the specified logic levels. In addition, the device may contain output-conditioning circuitry, an output amplifier, a reference amplifier, an on-board reference, on-board buffer-registers (single- or dual-rank), configuration conditioning, and even high-voltage isolation.

Basic DAC

This form, which supplies a current, and consequently a small voltage across its internal impedance or an external low-impedance load, is used principally for high speed, for example, the 10ns HDS-0810E. Basic current-output DACs, such as AD566, are inherently fast, but additional elements (such as an output op amp), furnished by the user to meet overall system specs, slow down the conversion. Some popular CMOS IC devices, such as the AD7523 and the AD7533, are quite simple (and correspondingly low in cost), but they usually require a buffering op amp.

While the basic DAC function is almost always linear, there are exceptions. For example, the AD7110 audio attenuator, which has linear two-quadrant analog response, has a digitally controlled exponential gain function, i.e., 1.5dB per bit; thus, its gain at the input code, 001000 (binary 8), is -12dB (8 × 1.5), and the analog output swing for 10V p-p input is 2.512V p-p (10 exp (10) (-12/20)).

Output Conditioning

The analog quantity that is the "output" of a DAC, representing the input digital data, may be a "gain" (multiplying DAC), a current, and/or a voltage. In order to obtain a substantial voltage output at low impedance, an op amp is required. It is generally provided on-board in modular and hybrid DACs (and in the monolithic AD558), but there are many ICs and other types that permit the user to choose an external op amp that will meet the particular needs of the application in stability, speed, and cost.

Almost all types of DACs provide one or more feedback resistors; they are matched to, and thermally track, resistances in the network, so that an external op amp, if used, will not require an external feedback resistor that might introduce tracking errors. If more than one feedback resistor is provided, a choice of analog output voltage ranges becomes available, e.g., 0–5V full-scale or 0–10V full-scale. If bipolar output-voltage ranges are specified, a bipolar-offset resistor is provided to subtract a half-scale value from the current flowing through the op amp summing point; it is usually derived from the DAC's reference (or analog) input to avoid additional tracking error. Multiplying DACs use an internal or external op amp for bipolar offset.

In order to avoid difficulties, the user must pay especial attention to the specified output polarity, its relationship to the reference (if external) and to the input digital code. This can be especially tricky if the output is bipolar and the input requires a complementary (negative-true) digital coding. Another such case is where a current-output DAC, specified for a particular output-voltage polarity when used with an inverting op amp, is used in a mode that develops an output voltage passively (without the op amp) across an external resistive load. In addition to polarity, in this case, the user should be aware of the output-compliance constraint and the specified resistive component of output impedance.

Reference Input

The reference may be specified as external or internal, fixed or variable, single-polarity or bipolar. If internal, it may be permanently connected (as in the AD561) or optionally connectible (as in the AD565). If the DAC is a 4-quadrant multiplying type, the reference (or "analog input") is external, variable, and bipolar (e.g., AD7533, 7541, etc.) The user should check a converter's specifications to determine whether the full-scale accuracy specifications are overall or subdivided into a converter-gain spec and a reference spec.

Digital Data

There are a number of ways in which converters differ in regard to the input data: First, the *coding* must be appropriate (binary, offset-binary, two's-complement, BCD, arbitrary, etc.), and its sense should be understood (positive-true, negative-true). The *resolution* (number of bits) must be sufficient; in addition, the specifications must be checked to ascertain that the 2^n distinct binary input codes will not only be accepted, but that also they will (if necessary) correspond to 2^n output values in a monotonic progression at any temperature in the operating range, with sufficient accuracy. The *data levels* accepted by the converter must be checked (TTL, ECL, low-voltage CMOS, high-voltage CMOS), as must the input loading imposed by the converter, and the supply conditions under which the converter will respond to the data. Check the data notation (is the MSB Bit 1 or Bit (n-1)?)—misinterpretation can lead to connecting the data bits in backward order.

If *buffer registers* are desired, the converter should have an appropriate buffer configuration (for example, the AD558 has a set of TTL buffers, the AD567, AD7542 and AD7543 have two ranks of buffering).

Controls

If the DAC has external digital controls—for example, register strobes— their drive levels, digital sense (true or false), loading, and timing must be considered. The function and use of configuration controls (where present), such as serial/parallel, short-cycle, or chip-select decoding should be understood, and the appropriate ways of disabling them when not needed should be employed.

Power Supplies
Appropriate power supplies should be made available, considering the logic levels and analog output signals to be employed in the system. The appropriate degree of power-supply stability to meet the accuracy specs should be employed. Any recommended external protection circuitry (e.g., Schottky diodes, to ensure that V_{CC} is never more than 0.4V above V_{DD} in the AD7522) should be planned for. In many cases separate analog and digital grounds are required; ground wiring should follow best practice to minimize digital interference with high-accuracy analog signals, while ensuring that a connection between the grounds can always exist at one point, even if the "mecca" point is inadvertently unplugged from the system.

SPECIFICATIONS AND TERMS

Definitions of the performance specifications, and related information, are provided on the next few pages, in alphabetical order.

Accuracy, Absolute
Error of a D/A converter is the difference between the actual analog output and the output that is expected when a given digital code is applied to the converter. Sources of error include gain (calibration) error, zero error, linearity errors, and noise. Error is usually commensurate with resolution, i.e., less than $2^{-(n+1)}$, or "½ LSB" of full scale. However, accuracy may be much better than resolution in some applications; for example, a 4-bit reference supply having only 16 discrete digitally chosen levels would have a resolution of 1/16, but it might have an accuracy to within 0.01% of each ideal value.

Absolute-accuracy measurements should be made under a set of standard conditions with sources and meters traceable to an internationally accepted standard.

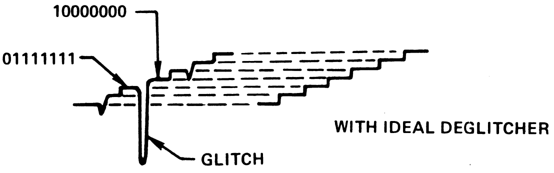
Accuracy, Relative
Relative accuracy error, expressed in %, ppm, or fractions of 1 LSB, is the deviation of the analog value at any code (relative to the full analog range of the device transfer characteristics) from its theoretical value (relative to the same range), after the full-scale range (FSR) has been calibrated. Since the discrete analog output values corresponding to the digital input values ideally lie on a straight line, the relative-accuracy error of a linear DAC can be interpreted as a measure of nonlinearity (see *Linearity*).

Compliance-Voltage Range
For a current-output DAC, the maximum range of (output) terminal voltage for which the device will provide the specified current-output characteristics.

Common-Mode Rejection (CMR)
The ability of an amplifier to reject the effect of voltage applied to both input terminals simultaneously. Usually a logarithmic expression representing a "common-mode rejection ratio" e.g., 1,000,000:1 (CMRR) or 120dB (CMR). A CMRR of 10^6:1 means that a 1V common-mode voltage passes through the device as though it were a differential input signal of 1 microvolt.

Common-Mode Voltage
An undesirable signal picked up in a circuit by both wires making up the circuit, with reference to an arbitrary "ground." Amplifiers differ in their ability to amplify a desired signal accurately in the presence of a common-mode voltage.

Deglitcher
As the input code to a DAC is increased or decreased by small changes, it passes through what is known as major and minor transitions. The most major transition is at half-scale, when the DAC switches around the MSB, and all switches change state, i.e., 01111111 to 10000000. If, at major transitions, the switches are faster (or slower) to switch off than on, this means that, for a short time, the D/A will give a zero (or full-scale) output, and then return to the required 1 LSB above the previous reading. Such large transient spikes which differ widely in amplitude and are extremely difficult to filter out, are commonly known as "glitches", hence, a deglitcher is a device which removes these glitches or reduces them to a set of small, uniform pulses. It normally consists of a fast sample-hold circuit, which holds the output constant until the switches reach equilibrium. Glitch energy is smallest in fast-switching DACs driven by fast logic gates that have little time-skew between 0-1 and 1-0 transitions.



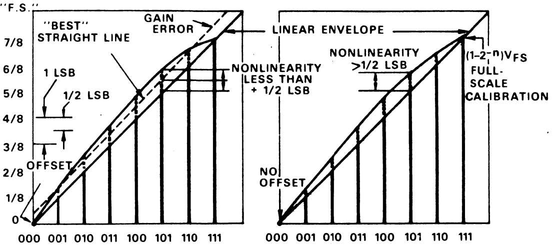
Feedthrough
Undesirable signal coupling around switches or other devices that are supposed to be turned off or provide isolation, e,g,. *feedthrough error* in a multiplying DAC. It is variously specified in %, ppm, fractions of 1 LSB, or fractions of 1 volt, with a given set of inputs, at a specified frequency.

Four-Quadrant
In a multiplying DAC, "four quadrant" refers to the fact that both the reference signal and the number represented by the digital input may be of either positive or negative polarity. A four-quadrant multiplier is expected to obey the rules of multiplication for algebraic sign.

Gain
The "gain" of a converter is that analog scale-factor setting that provides the nominal conversion relationship, e.g., 10V span for a full-scale code change, in a fixed-reference converter. For fixed-reference converters where the use of the internal reference is optional, the converter gain and the reference may be specified separately. Gain- and zero-adjustment are discussed under *Zero.*

Least-Significant Bit (LSB)
In a system in which a numerical magnitude is represented by a series of binary (i.e., two-valued) digits, the LSB is that bit that carries the smallest value, or weight. For example, in the natural-binary number 1101 (decimal 13, or $2^3 + 2^2 + 0 + 2^0$), the rightmost digit is the LSB. Its analog weight, relative to full scale, is 2^{-n}, where n is the number of binary digits. It represents the smallest analog change that can be resolved by an n-bit converter.

Linearity
Linearity error of a converter (also, *integral nonlinearity*, see *Linearity, Differential*), expressed in % or ppm of full-scale range, or (sub)multiples of 1 LSB, is a deviation of the analog values, in a plot of the measured conversion relationship, from a straight line. The straight line can be either a "best straight line", determined empirically by manipulation of the gain and/or offset to equalize maximum positive and negative deviations of the actual transfer characteristics from this straight line; or it can be a straight line passing through the end points of the transfer characteristic after they have been calibrated (sometimes referred to as "end-point" linearity). End-point linearity error is similar to *relative-accuracy* error.



a. ½LSB Nonlinearity Achieved By Arbitrary Location of "Best Straight Line".

b. Nonlinearity Reference is Straight Line Through End Points. Nonlinearity >½LSB for Curve of a.

Comparison of Linearity Criteria for 3-Bit D/A Converter. Straight Line Through End Points is Easier to Measure, Gives More-Conservative Specification.

For multiplying D/A converters, the *analog* linearity error, at a specified digital code, is defined in the same way as for multipliers, i.e., by deviation from a "best straight line" through the plot of the analog output-input response.

Linearity, Differential
Any two adjacent digital codes should result in measured output values that are exactly 1 LSB apart (2^{-n} of full scale for an n-bit converter). Any deviation of the measured "step" from the ideal difference is called *differential nonlinearity*, expressed in (sub)multiples of 1 LSB. It is an important specification, because a differential linearity error greater than 1 LSB can lead to non-monotonic response in a D/A converter and missed codes in an A/D converter (see *Differential Linearity* in the A/D converter section for an illustration).

Monotonic
A DAC is said to be monotonic if the output either increases or remains constant as the digital input increases, with the result that the output will always be a single-valued function of the input. The specification "monotonic" (over a given temperature range) is sometimes substituted for a *differential nonlinearity* specification, since differential nonlinearity less than 1 LSB is a sufficient condition for monotonic behavior.

Most-Significant Bit (MSB)
In a system in which a numerical magnitude is represented by a series of binary (i.e., two-valued) digits, the MSB is that digit (or bit) that carries the largest value of weight. For example, in the natural-binary number 1101 (decimal 13, or $2^3 + 2^2 + 0 + 2^0$), the leftmost "1" is the MSB, with a weight of 2^{n-1}, or 8 LSBs. Its analog weight, relative to a DAC's full-scale span, is ½. In bipolar DACs, the MSB indicates the polarity of the number represented by the rest of the bits.

Multiplying DAC
A multiplying DAC differs from a fixed-reference DAC in being designed to operate with varying (or ac) reference signals. The output signal of such a DAC is proportional to the product of the "reference" (i.e., analog input) voltage and the fractional equivalent of the digital input number (see also *four-quadrant*).

Noise, Peak and rms
Internally generated random noise is not a major factor in D/A converters, except at extreme resolutions (e.g., DAC1138) and dynamic ranges (AD7110). Random noise is characterized by rms specifications for a given bandwidth, or as a spectral density (current or voltage per root hertz); if the distribution is Gaussian, the probability of peak-to-peak values exceeding 7x the rms value is less than 0.1%.

Of much greater importance in DACs is interference in the form of high-amplitude low-energy (hence low-rms) spikes appearing at the DAC's output, caused by coupling of digital signals in a surprising variety of ways; they include coupling via stray capacitance, via power supplies, via inadequate ground systems, via feedthrough, and by glitch-generation. Their presence underscores the necessity for maximum application of the designer's art, including layout, shielding, guarding, grounding, bypassing, and deglitching.

Offset
For almost all bipolar converters (e.g., ±10-volt output), instead of actually generating negative currents to correspond to negative numbers, a unipolar DAC is used, and the output is offset by half full scale (1 MSB). For best results, this offset voltage or current is derived from the same reference supply that determines the gain of the converter.

This makes the zero point of the converter independent of thermal drift of the reference, because the ½ scale offset cancels the weight of the MSB at zero, independently of the amplitude of both.

Power-Supply Sensitivity
The sensitivity of a converter to changes in the power-supply voltages is normally expressed in terms of percent-of-full-scale change in analog output value (or fractions of 1 LSB) for a 1% dc change in the power supply, e.g., $0.05\%/\%\Delta V_S$). Power supply sensitivity may also be expressed in relation to a specified dc shift of supply voltage. A converter may be considered "good" if the change in reading at full scale does not exceed ±½ LSB for a 3% change in power supply. Even better specs are necessary for converters designed for battery operation.

Quantizing Uncertainty (or "Error")
The analog continuum is partitioned into 2^n discrete ranges for n-bit processing. All analog values within a given range of output (of a DAC) are represented by the same digital code, usually assigned to the nominal midrange value. For applications in which an analog continuum is to be restored, there is an inherent quantization uncertainty of ±½ LSB, due to limited resolution, in addition to the actual conversion errors. For applications in which discrete output levels are desired (e.g., digitally controlled power supplies or digitally controlled gains), this consideration is not relevant.

Resolution
An n-bit binary converter should be able to provide 2^n distinct and different analog output values corresponding to the set of n-bit binary words. A converter that satisfies this criterion is said to have a *resolution* of n bits. The smallest output change that can be resolved by a linear DAC is 2^{-n} of the full-scale span. However, a nonlinear device, such as the AD7110 audio attenuator has a logarithmic gain resolution of 1.5/88.5dB = 1:59dB, which corresponds to a gain increment of 18.9%/step, or 26,600:1.

Settling Time
The time required, following a prescribed data change, for the output of a DAC to reach and remain within a given fraction (usually ±½ LSB) of the final value. Typical prescribed changes are full-scale, 1 MSB, and 1 LSB at a major carry. Settling time of current-output DACs is quite fast. The major share of settling time of a voltage-output DAC is usually contributed by the settling time of the output op-amp circuit.

Slew Rate (or Slewing Rate)
Slew rate of a device or circuit is a limitation in the rate of change of output voltage, usually imposed by some basic circuit consideration, such as limited current to charge a capacitor. Amplifiers with slew rate of a few V/μs are common, and moderate in cost. Slew rates greater than about 75 volts/μs are usually seen only in more sophisticated (and expensive) devices. The output slewing speed of a voltage-output D/A converter is usually limited by the slew rate of the amplifier used at its output (if one is used).

Stability
Stability of a converter usually applies to the insensitivity of its characteristics to time, temperature, etc. All measurements of stability are difficult and time consuming, but stability vs. temperature is sufficiently critical in most applications to warrant universal inclusion of temperature coefficients in tables of specifications (see "Temperature Coefficient").

Staircase
A voltage or current, increasing in equal increments as a function of time and having the appearance of a staircase (in a time plot), generated by applying a pulse train to a counter, and the output of the counter to the input of a DAC.

A very simple A/D converter can be built by comparing a staircase from a DAC with the unknown analog input. When the DAC output exceeds the analog input by a fraction of 1 LSB, the count is stopped, and the code corresponding to the count is the digital output.

Switching Time
In a DAC, the switching time is the time it takes for the switch to change from one state to the other ("delay time" plus "rise time" from 10%-90%), but does not include settling time, e.g. to <½ LSB.

Temperature Coefficients
In general, temperature instabilities are expressed as %/°C, ppm/°C, as fractions of 1 LSB/°C, or as a change in a parameter over a specified temperature range. Measurements are usually made at room temperature and at the extremes of the specified range, and the temperature coefficient (tempco, T.C.) is defined as the change in the parameter, divided by the corresponding temperature change. Parameters of interest include *gain, linearity, offset* (bipolar), and *zero*.

Gain Tempco: Two factors principally affect converter gain stability with temperature.

a) In fixed-reference converters the reference source will vary with temperature. For example, the tempco of an AD581L is generally less than 5ppm/°C

b) The reference circuitry and switches may add another 3ppm/°C in good 12-bit converters (e.g. AD566K/T). High-resolution converters require much better tempcos for accuracy commensurate with the resolution.

Linearity Tempco: Sensitivity of linearity ("integral" and/or differential linearity) to temperature (in % FSR/°C or ppm FSR/°C) over the specified range. Monotonic behavior is achieved if the differential nonlinearity is less than 1 LSB at any temperature in the range of interest. The *differential nonlinearity temperature coefficient* may be expressed as a ratio, as a maximum change over a temperature range, and/or implied by a statement that the device is monotonic over the specified temperature range.

Offset Tempco: The temperature coefficient of the all-DAC-switches-off (minus full scale) point of a bipolar converter (in % FSR/°C or ppm FSR/°C) depends on three major factors:

a) The tempco of the reference source
b) The voltage zero-stability of the output amplifier
c) The tracking capability of the bipolar-offset resistors and the gain resistors

Unipolar Zero Tempco (in % FSR/°C or ppm FSR/°C): The temperature stability of a unipolar fixed-reference DAC is principally affected by current leakage (current-output DAC), and offset voltage and bias current of the output op-amp (voltage-output DAC).

Zero- and Gain-Adjustment Principles

The output of a unipolar DAC is set to zero volts in the all-bits-off condition. The gain is set for F.S. $(1 - 2^{-n})$ with all bits on. The "zero" of an offset-binary bipolar DAC is set to -F.S. with all bits off, and the gain is set for +F.S. $(1 - 2^{-(n-1)})$ with all bits on. The data sheet instructions should be followed.

ANALOG DEVICES

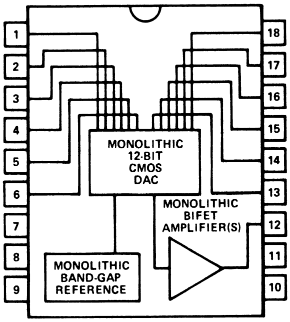
Complete, Low Power 12-Bit D/A Converter

AD370/AD371

FEATURES

- Bipolar Voltage Output: AD370
- Unipolar Voltage Output: AD371
- Low Power: 150mW max
- Linearity: ±1/2LSB, -55°C to +125°C (S Version)
- TTL/CMOS Compatible
- Compatible with Standard 18-Pin DAC Configurations
- Hermetic 18-Pin DIP ("D" Package)
- Factory Trimmed Gain and Offset: No External Adjustments Required
- Monotonicity Guaranteed Over Specified Temperature Range

AD370/AD371 FUNCTIONAL BLOCK DIAGRAM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MONOLITHIC 12-BIT CMOS DAC
MONOLITHIC BIFET AMPLIFIER(S)
MONOLITHIC BAND-GAP REFERENCE

18-PIN DIP

PRODUCT DESCRIPTION

The AD370/AD371 is a complete 12-bit digital-to-analog converter fabricated with the most advanced monolithic and hybrid technologies. The design incorporates a low power monolithic CMOS DAC, precision high speed FET-input operational amplifiers and a low drift reference available in a hermetically sealed package. This innovative design results in significant performance advantages over conventional designs. The integral package-substrate combined with a lower chip count improves reliability over the standard low power hybrids of this type.

The converters come in two versions: AD370 with a bipolar output voltage range (-10V to +10V) and AD371 with a unipolar output voltage range (0 to +10V). Each device is internally laser trimmed for gain and offset to provide adjustment-free operation with only ±0.05% absolute error. The FET input operational amplifiers optimize the speed vs. power trade-off by settling to 1/2LSB from a full scale transition in 35μs with maximum total power dissipation of only 150mW. The low power monolithic CMOS DAC employs a current-switched silicon-chromium R-2R ladder to ensure that monotonicity is maintained over the full temperature range.

The AD370/AD371 "K" and "S" features ±1/2LSB maximum linearity error. Its rated temperature ranges are 0 to +70°C for the "J" and "K" versions and -55°C to +125°C for the "S" version.

PRODUCT HIGHLIGHTS

1. The AD370/AD371 replaces other devices of this type with significant increases in performance.
2. Reduced power consumption requirements (150mW max) result in improved stability and shorter warm-up time.
3. The precision output amplifiers and CMOS DAC have been optimized to settle within 1/2LSB for a full scale transition in 35μs.
4. Reduced chip count and integral package-subsrate improve reliability.
5. System performance upgrading is possible without redesign.
6. Internally laser trimmed—no gain or offset adjustments are required for specified accuracy.
7. The device is available in a hermetically-sealed ceramic 18 lead dual-in-line package. Processing to MIL-STD-883 Class B is available.
8. The AD370/AD371 is a second-source for 18-pin 12-bit DACs of the same configuration.

SPECIFICATIONS (typical at T_A = +25°C, V_S = ±15 Volts unless otherwise noted)

Model	AD370J	AD370K	AD371J	AD371K	AD370S[1]	AD371S[1]	Units
RANGE	-10 to +10	*	0 to +10	**	*	**	Volts
CODE	OCBI	*	CBI	**	*	**	
LINEARITY ERROR							
+25°C	±1	±1/2	±1	±1/2	±1/2	±1/2	LSB[2] max
T_{min} - T_{max}	±1	±1/2	±1	±1/2	±1/2	±1/2	LSB[2] max
ABSOLUTE ACCURACY							
+25°C	±0.05	*	*	*	*	*	% of FSR[3] max
T_{min} - T_{max}	±0.2	*	*	*	±0.3	±0.3	% of FSR[3] max
OFFSET ERROR							
+25°C	±5	*	±1	**	*	**	mV max
FULL SCALE SETTLING TIME TO ±1/2LSB	25(35 max)	*	*	*	*	*	μs
INTERNAL REFERENCE	+10.0	*	*	*	*	*	Volts
DIGITAL INPUTS							
V_{INH}	2.0	*	*	*	*	*	Volts min
V_{INL}	0.8	*	*	*	*	*	Volts max
INPUT LEAKAGE CURRENT	±1.0	*	*	*	*	*	μA
INPUT CAPACITANCE	8	*	*	*	*	*	pF
POWER SUPPLY REJECTION RATIO							
+15V Supply	0.01	*	*	*	*	*	% FSR[3]/% V_S max
-15V Supply	0.01	*	*	*	*	*	% FSR[3]/% V_S max
POWER SUPPLY CURRENTS							
+15V Supply	3.5(5 max)	*	*	*	*	*	mA max
-15V Supply	2.5(4 max)	*	*	*	*	*	mA max
POWER DISSIPATION	105(150 max)	*	*	*	*	*	mW
TEMPERATURE RANGE	0 to +70	*	*	*	-55 to +125	***	°C

NOTES

[1] Also available to MIL-STD-883, Level B.

[2] LSB: Least Significant Bit

[3] FSR: Full Scale Range

*Specifications same as AD370J.

**Specifications same as AD371J.

***Specifications same as AD370S.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

V_{DD} (to GND) . . . . +17V
V_{EE} (to GND) . . . . –17V
Digital Input Voltage Range . . . . V_{DD} to GND
Storage Temperature . . . . –65°C to +150°C

CAUTION – ELECTROSTATIC SENSITIVE DEVICES

The digital control inputs are zener protected; however permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

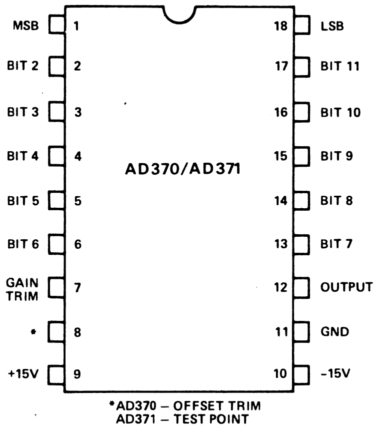


Figure 1. Pin Designations

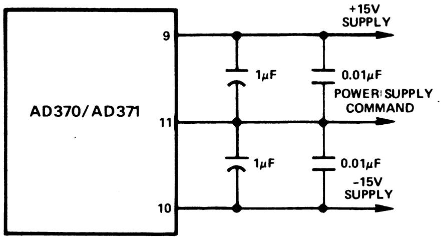


Figure 2. Power Supply Decoupling

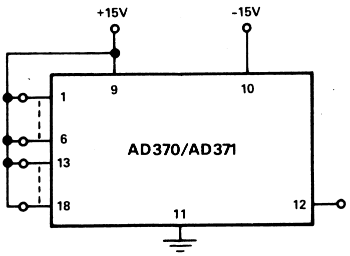


Figure 3. Burn-In Circuit

DIGITAL INPUT	NOMINAL ANALOG OUTPUT
111111111111	0
100000000000	4.9975 Volts
011111111111	5.0000 Volts
000000000000	9.9975 Volts

Table 1. Code Table for the AD371 (CBI)

DIGITAL INPUT	NOMINAL ANALOG OUTPUT
111111111111	-10.000 Volts
100000000001	-0.0097 Volt
100000000000	-0.0048 Volt
011111111111	0
000000000000	9.9952 Volts

Table 2. Code Table for the AD370 (OCBI)

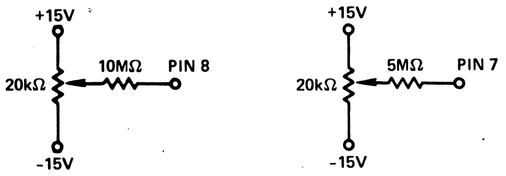
ACCURACY

Accuracy error of a D/A converter is defined as the difference between the analog output that is expected when a given digital code is applied and the output that is actually measured with that code applied to the converter. Accuracy error can be caused by gain error, zero error or linearity error. The initial accuracy of the AD370/AD371 is trimmed to within 0.05% of full scale by laser trimming the gain and zero errors. Of the error specifications, the linearity error specification is the most important since it cannot be corrected by the user. The linearity error of the AD370/AD371 is specified over its entire temperature range. This means that the analog output will not vary by more than ±1/2LSB maximum from an ideal straight line drawn between the end points (inputs all "1s" and all "0s") over the specified operating temperature range of 0 to +70°C for the "K" version and -55°C to +125°C for the "S" version.

The absolute accuracy of the AD370/AD371 has been guaranteed to ±0.05% of full scale by internal factory trim of the gain and offset. External gain and offset adjustment terminals have been made available to allow fine adjustment to the ±0.012% accuracy level. The measurement system used to calibrate the output should be capable of stable resolution of 1/4LSB in the regions of zero and full scale. The adjustment procedure, described below, should be carefully followed to assure optimum converter performance.

The proper connections for the offset and gain adjustments are shown in Figure 4. For the AD371 full-scale calibration apply a digital input of all "1s" and adjust the gain potentiometer to +9.9975 volts (see Table 1).

The offset adjustment of the AD370 is made at the half-scale code. Adjust the offset potentiometer until 0.000V is obtained on the output. The full-scale adjustment is made at the negative endpoint or a code of all "1s". Adjust the gain potentiometer until -10.000 volts is obtained on the output.



OFFSET TRIM
(AD370 ONLY)

GAIN TRIM

Figure 4. Optional External Trims

SETTLING TIME

Settling time for the AD370/AD371 is the total time required for the output to settle within ±1/2LSB band around its final value after a change in input (including slew time). The settling time specification is given for a full scale step which is 20V for the AD370 and 10V for the AD371.

IMPROVED SECOND SOURCE

The substrate design of the AD370/AD371 provides for complete pin-for-pin compatibility with other 18-pin DACs,; Hybrid Systems Corp. DAC340, DAC350 series and Micro Networks Corp. MN360, MN370, MN3200 series 18-pin 12-bit digital-to-analog converters all share the same pin configuration except for pin 7 and pin 8 (see Table 3). The AD370/AD371 is a superior direct replacement for these devices where the function of pins 7 and 8 allow. The versatility designed into the AD370/AD371 allows the function of pin 7 and pin 8 to be configured to exactly second source each of the other units. Information on other second source devices with 4 quadrant multiplying capability is available from Analog Devices.

Analog Devices	Hybrid Systems			Micro Networks		
AD370KD	DAC346C-12BPG			MN360	MN370	MN3211
AD371KD	DAC346C-12UP			MN362	MN371	MN3210
AD370SD	DAC347LPC-12G	DAC356C-12	DAC356LPC-12	MN360H	MN370H	
AD370SD/883B	DAC347LPS-12G	DAC356B-12	DAC356LPB-12			
AD371SD	DAC347LPC-12U			MN362H	MN371H	
AD371SD/883B	DAC347LPB-12U					

Table 3. Cross Reference

AD370/AD371 ORDERING GUIDE

Model	Package	Package Style[1]	Linearity	Output Voltage Range	Operating Temperature Range
AD370JN	Polymer Seal	HY18A	1LSB	-10V to +10V	0 to +70°C
AD370JD	Hermetic	HY18A	1LSB	-10V to +10V	0 to +70°C
AD371JN	Polymer Seal	HY18A	1LSB	0 to +10V	0 to +70°C
AD371JD	Hermetic	HY18A	1LSB	0 to +10V	0 to +70°C
AD370KN	Polymer Seal	HY18A	1/2LSB	-10V to +10V	0 to +70°C
AD370KD	Hermetic	HY18A	1/2LSB	-10V to +10V	0 to +70°C
AD371KN	Polymer Seal	HY18A	1/2LSB	0 to +10V	0 to +70°C
AD371KD	Hermetic	HY18A	1/2LSB	0 to +10V	0 to +70°C
AD370SD	Hermetic	HY18A	1/2LSB	-10V to +10V	-55°C to +125°C
AD370SD/883B	Hermetic	HY18A	1/2LSB	-10V to +10V	-55°C to +125°C
AD371SD	Hermetic	HY18A	1/2LSB	0 to +10V	-55°C to +125°C
AD371SD/883B	Hermetic	HY18A	1/2LSB	0 to +10V	-55°C to +125°C

[1] See Section 20 for package outline information.

ANALOG DEVICES

Quad 12-Bit Microprocessor-Compatible D/A Converter

AD390

ADVANCE TECHNICAL INFORMATION

FEATURES

Four Complete 12-Bit DACs in One IC Package
Voltage Output
Guaranteed Monotonic Over Full Temperature Range
Double-Buffered Data Inputs
Includes Data Latches and Reference
Fast Settling: 8µs max
Low Cost

PRODUCT DESCRIPTION

The AD390 contains four 12-bit high speed voltage-output digital-to-analog converters in a compact 28-pin hybrid package. The design is based on a proprietary latched 12-bit DAC chip which reduces chip count and provide high realiability. The AD390 is ideal for systems requiring digital control of many analog voltages. Such applications include automatic test equipment, process controllers, and vector-scan displays.

The AD390 is laser-trimmed to ±¼LSB max nonlinearity (AD390KD) and absolute accuracy of ±0.05 percent of full scale. The high initial accuracy is made possible by the use of thin-film scaling resistors on the monolithic DAC chips. The internal buried zener voltage reference provides excellent temperature drift characteristics (30ppm/°C) and an initial tolerance of ±0.025% maximum. The AD390 can also be used with an external reference in large system applications.

The individual DACs are accessed by the $\overline{CS1}$ through $\overline{CS4}$ control inputs and the $\overline{A0}$ and $\overline{A1}$ lines. These control signals permit the registers of the four DACs to be loaded independently and the outputs to be simultaneously updated at a later time.

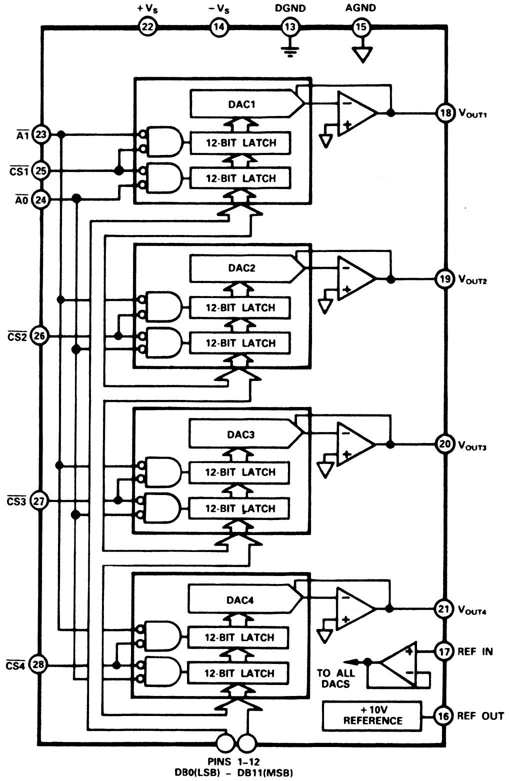
The AD390 outputs are calibrated for a ±10V range. A 0 to +10V version is available on special order.

The AD390 is packaged in a 28-lead ceramic package and is specified for operation over the 0 to +70°C and −55°C to +125°C temperature range.

PRODUCT HIGHLIGHTS

1. The AD390 offers a dramatic reduction in printed circuit board space requirements in systems using multiple DACs.
2. Each DAC is independently addressable, providing a versatile control architecture for simple interface to microprocessors. All latch enable signals are level-triggered.
3. The output voltage is trimmed to a full scale accuracy of ±0.05%. Settling time to ±½LSB is 8 microseconds maximum.
4. An internal 10 volt reference is available or an external reference can be used. With an external reference, the AD390 gain TC is ±5ppm/°C maximum.
5. The proprietary monolithic DAC chips provide excellent linearity and guaranteed monotonicity over the full operating temperature range.

AD390 FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS1}$	$\overline{CS2}$	$\overline{CS3}$	$\overline{CS4}$	A0	A1	Operation
1	1	1	1	x	x	No Operation
0	1	1	1	0	1	Enable 1st rank of DAC 1
1	0	1	1	0	1	Enable 1st rank of DAC 2
1	1	0	1	0	1	Enable 1st rank of DAC 3
1	1	1	0	0	1	Enable 1st rank of DAC 4
1	1	1	1	1	0	Loads 2nd rank from each 1st rank
0	0	0	0	0	0	All latches transparent

SPECIFICATIONS (T_A = +25°C, V_S = ±15V unless otherwise specified)

	AD390JD/SD			AD390KD/TD			
Model	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
DATA INPUTS (Pins 1-12 and 23-28)							
TTL or 5 Volts CMOS							
Input Voltage							
Bit ON (Logic "1")	+2.0		+5.5	+2.0		+5.5	V
Bit OFF (Logic "0")			+0.8			+0.8	V
Input Current							
Bit ON (Logic "1")		500	1200		500	1200	μA
Bit OFF (Logic "0")		150	400		150	400	μA
RESOLUTION			12			12	Bits
OUTPUT							
Voltage Range[1]			± 10			± 10	V
Current			5			5	mA
Settling Time (to ± ½LSB)		4	8		4	8	μs
ACCURACY							
Gain Error		2	4		2	2	LSB
Offset		1	2		½	1	LSB
Linearity Error		± ¼	± ½		± ⅛	± ¼	LSB
Differential Linearity Error		± ½	± ¾		± ¼	± ½	LSB
TEMPERATURE DRIFT							
Gain (internal reference)			± 16			± 8	ppm/°C
(external reference)			± 8			± 4	ppm/°C
Offset			± 4			± 2	ppm/°C
Linearity Error 0 to + 70°C		± ½	± ¾		± ¼	± ½	LSB
Differential Linearity	MONOTONICITY GUARANTEED OVER FULL TEMPERATURE RANGE						
REFERENCE							
Voltage	9.9975	10.000	10.0025	9.9975	10.0000	10.0025	V
Current (available extended use)	2.5	3.5		2.5	3.5		mA
Ref In Input Resistance		10^{10}			10^{10}		Ω
POWER REQUIREMENTS							
Voltage	± 13.5	± 15	± 16.5	± 13.5	± 15	± 16.5	V
Current							
$+V_S$		12	20		12	20	mA
$-V_S$		− 75	− 90		− 75	− 90	mA
POWER SUPPLY GAIN SENSITIVITY							
$+V_S$		0.002	0.006		0.002	0.006	%FS/%
$-V_S$		0.0025	0.006		0.0025	0.006	%FS/%
TEMPERATURE RANGE							
Operating (Full Specifications) J, K	0		+ 70	0		+ 70	°C
S, T	− 55		+ 125	− 55		+ 125	°C
Storage	− 65		+ 150	− 65		+ 150	°C
PACKAGE STYLE[2]		HY28A			HY28A		

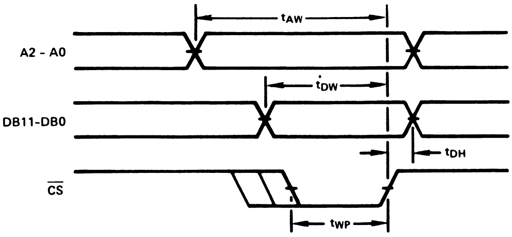
[1] 0 to + 10V range is standard. A 0 to 10V version is available on special order. Consult the factory.

[2] See Section 20 for package outline information.

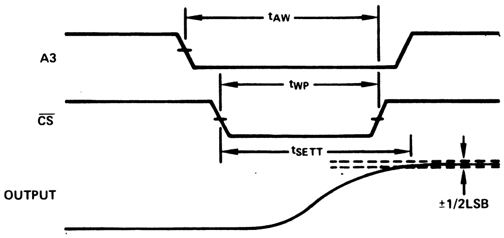
Specifications subject to change without notice.

TIMING DIAGRAMS

WRITE CYCLE #1
(Load First Rank from Data Bus; A3 = 1)



WRITE CYCLE #2
(Load Second Rank from First Rank; A2–A0 = 1)



Symbol	Parameter	Min	Typ	Max	ns
t_{DW}	Data Valid to End of $\overline{CS}$	50			ns
t_{AW}	Address Valid to End of $\overline{CS}$	100			ns
t_{WP}	Control Pulse Width	100			ns
t_{DH}	Data Hold Time	0			ns
t_{SETT}	Output Current Settling Time		400	500	ns

ANALOG DEVICES

DACPORT™ Low Cost Complete µP-Compatible 8-Bit DAC

AD558*

FEATURES

- Complete 8-Bit DAC
- Voltage Output – 2 Calibrated Ranges
- Internal Precision Band-Gap Reference
- Single-Supply Operation: +5V to +15V
- Full Microprocessor Interface
- Fast: 1µs Voltage Settling to ±1/2LSB
- Low Power: 75mW
- No User Trims
- Guaranteed Monotonic Over Temperature
- All Errors Specified T_{min} to T_{max}
- Small 16-Pin DIP Package
- Single Laser-Wafer-Trimmed Chip for Hybrids
- Low Cost

PRODUCT DESCRIPTION

The AD558 DACPORT is a complete voltage-output 8-bit digital-to-analog converter, including output amplifier, full microprocessor interface and precision voltage reference on a single monolithic chip. No external components or trims are required to interface, with full accuracy, an 8-bit data bus to an analog system.

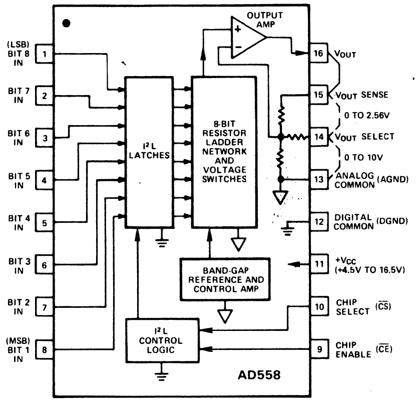
The performance and versatility of the DACPORT is a result of several recently-developed monolithic bipolar technologies. The complete microprocessor interface and control logic is implemented with integrated injection logic (I^2L), an extremely dense and low-power logic structure that is process-compatible with linear bipolar fabrication. The internal precision voltage reference is the patented low-voltage band-gap circuit which permits full-accuracy performance on a single +5V to +15V power supply. Thin-film silicon-chromium resistors provide the stability required for guaranteed monotonic operation over the entire operating temperature range (all grades), while recent advances in laser-wafer-trimming of these thin-film resistors permit absolute calibration at the factory to within ±1LSB; thus no user-trims for gain or offset are required. A new circuit design provides voltage settling to ±1/2LSB for a full-scale step in 800ns.

The AD558 is available in four performance grades. The AD558J and K are specified for use over the 0 to +70°C temperature range, while the AD558S and T grades are specified for −55°C to +125°C operation. The hermetically-sealed ceramic package is standard. Processing to MIL-STD-883, Class B is optional on S and T grades.

PRODUCT HIGHLIGHTS

1. The 8-bit I^2L input register and fully microprocessor-compatible control logic allow the AD558 to be directly connected to 8- or 16-bit data buses and operated with standard control signals. The latch may be disabled for direct DAC interfacing.

AD558 FUNCTIONAL BLOCK DIAGRAM



TO-116

2. The laser-trimmed on-chip SiCr thin-film resistors are calibrated for absolute accuracy and linearity at the factory. Therefore, no user trims are necessary for full rated accuracy over the operating temperature range.
3. The inclusion of a precision low-voltage band-gap reference eliminates the need to specify and apply a separate reference source.
4. The voltage-switching structure of the AD558 DAC section along with a high-speed output amplifier and laser-trimmed resistors give the user a choice of 0V to +2.56V or 0V to +10V output ranges, selectable by pin-strapping. Circuitry is internally compensated for minimum settling time on both ranges; typically settling to ±1/2LSB for a full-scale 2.55 volt step in 800ns.
5. The AD558 is designed and specified to operate from a single +4.5V to +16.5V power supply.
6. Low digital input currents, 100µA max, minimize bus loading. Input thresholds are TTL/low voltage CMOS compatible over the entire operating V_{CC} range.
7. The single-chip, low power I^2L design of the AD558 is inherently more reliable than hybrid multi-chip or conventional single-chip bipolar designs. The AD558S and T grades, which are specified over the −55°C to +125°C temperature range, are available processed to MIL-STD-883, Class B.
8. All AD558 grades are available in chip form with guaranteed specifications from +25°C to T_{max}. MIL-STD-883, Class B visual inspection is standard on Analog Devices bipolar chips. Contact the factory for additional chip information.

***Covered by U.S. Patent Nos. 3,887,863; 3,685,045; Patents Pending.**
DACPORT is a trademark of Analog Devices, Inc.

SPECIFICATIONS (typical @ T_A = +25°C, V_{CC} = +5V to +15V unless otherwise specified)

MODEL	AD558J	AD558K	AD558S[1]	AD558T[1]
RESOLUTION	8 Bits	*	*	*
RELATIVE ACCURACY[2]				
0 to +70°C	±1/2LSB max	±1/4LSB max	*	**
-55°C to +125°C	–	–	±3/4LSB max	±3/8LSB max
OUTPUT				
Ranges	0V to +2.56V	*	*	*
	0V to +10V [3]	*	*	*
Current, Source	+5mA	*	+5mA min	***
Sink	Internal Passive Pull-Down to Ground[4]	*	*	*
OUTPUT SETTLING TIME[5]				
0 to 2.56 volt range	0.8μs (1.5μs max)	*	*	*
0 to 10 volt range[3]	2.0μs (3.0μs max)	*	*	*
FULL SCALE ACCURACY				
@ 25°C	±1.5LSB (±0.6%) max	±0.5LSB (±0.2%) max	*	**
T_{min} to T_{max}	±2.5LSB (±1.0%) max	±1LSB (±0.4%) max	*	**
ZERO ERROR				
@ 25°C	±1LSB max	±1/2LSB max	*	**
T_{min} to T_{max}	±2LSB max	±1LSB max	*	**
MONOTONICITY[6]				
T_{min} to T_{max}	Guaranteed	*	*	*
DIGITAL INPUTS				
T_{min} to T_{max}				
Input Current	±100μA max	*	*	*
Data Inputs, Voltage				
Bit On – Logic "1"	2.0V min	*	*	*
Bit Off – Logic "0"	0.8V max	*	*	*
Control Inputs, Voltage				
On – Logic "1"	2.0V min	*	*	*
Off – Logic "0"	0.8V max	*	*	*
Input Capacitance	4pF	*	*	*
TIMING[7]				
T_{min} to T_{max}				
t_W (Strobe Pulse Width)	100ns min	*	*	*
t_{DH} (Data Hold Time)	10ns min	*	*	*
t_{DS} (Data Set-Up Time)	100ns min	*	*	*
POWER SUPPLY				
Operating Voltage Range (V_{CC})				
2.56 Volt Range	+4.5V to +16.5V	*	*	*
10 Volt Range	+11.4V to +16.5V	*	*	*
Current (I_{CC})	15mA typ, 25mA max	*	*	*
Rejection Ratio	0.03%/% max	*	*	*
POWER DISSIPATION, V_{CC} = 5V	75mW (125mW max)	*	*	*
V_{CC} = 15V	225mW (375mW max)	*	*	*
OPERATING TEMPERATURE RANGE				
T_{min}	0°C	*	-55°C	***
T_{max}	+70°C	*	+125°C	***

NOTES

[1] The AD558S and AD558T are available processed and screened to the requirements of MIL-STD-883, Class B. Order AD558SD/883B or AD558TD/883B.

[2] Relative Accuracy is defined as the deviation of the code transition points from the ideal transfer point on a straight line from the zero to the full scale of the device.

[3] Operation of the 0 to 10 volt output range requires a minimum supply voltage of +11.4 volts.

[4] Passive pull-down resistance is 2kΩ for 2.56 volt range, 10kΩ for 10 volt range.

[5] Settling time is specified for a positive-going full-scale step to ±1/2LSB. Negative-going steps to zero are slower, but can be improved with an external pull-down.

[6] A monotonic converter has a maximum differential linearity error of ±1LSB.

[7] See Figure 7.

*Specifications same as AD558J.
**Specifications same as AD558K.
***Specifications same as AD558S.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

V_{CC} to Ground	0V to +18V
Digital Inputs (Pins 1-10)	0 to +7.0V
V_{OUT}	Indefinite Short to Ground Momentary Short to V_{CC}
Power Dissipation	450mW
Storage Temperature Range	
D (ceramic) Package	-55°C to +150°C
Lead Temperature (soldering, 10 second)	300°C
Thermal Resistance	
Junction to Ambient/Junction to Case	
D (ceramic) Package	100/30°C/W

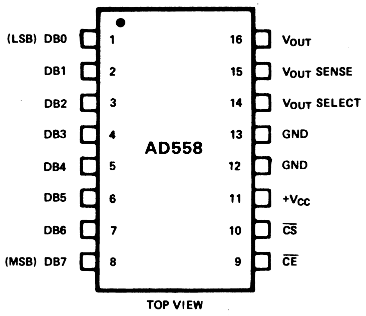


Figure 1. AD558 Pin Configuration

AD558 ORDERING GUIDE

Model	Package	Temperature	Relative Accuracy Error Max T_{min} to T_{max}	Full-Scale Error, Max T_{min} to T_{max}	Package Style[1]
AD558JN	Plastic	0 to +70°C	±1/2LSB	±2.5LSB	N16A[2]
AD558KN	Plastic	0 to +70°C	±1/4LSB	±1LSB	N16A[2]
AD558JD	Ceramic	0 to +70°C	±1/2LSB	±2.5LSB	D16A
AD558KD	Ceramic	0 to +70°C	±1/4LSB	±1LSB	D16A
AD558SD	Ceramic	-55°C to +125°C	±3/4LSB	±2.5LSB	D16A
AD558SD/883B	Ceramic	-55°C to +125°C	±3/4LSB	±2.5LSB	D16A
AD558TD	Ceramic	-55°C to +125°C	±3/8LSB	±1LSB	D16A
AD558TD/883B	Ceramic	-55°C to +125°C	±3/8LSB	±1LSB	D16A

[1] See Section 20 for package outline information.

[2] To be available June, 1982.

CIRCUIT DESCRIPTION

The AD558 consists of four major functional blocks, fabricated on a single monolithic chip (see Figure 2). The main D to A converter section uses eight equally-weighted laser-trimmed current sources switched into a silicon-chromium thin-film R/2R resistor ladder network to give a direct but unbuffered 0mV to 400mV output range. The transistors that form the DAC switches are PNPs; this allows direct positive-voltage logic interface and a zero-based output range.

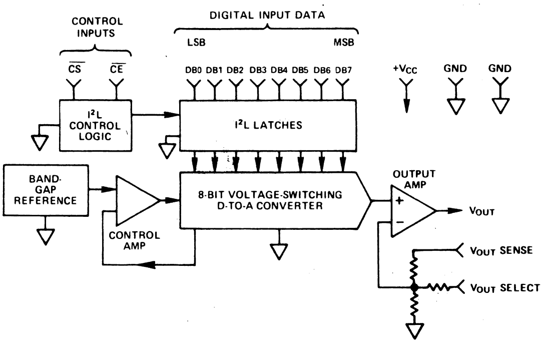


Figure 2. AD558 Functional Block Diagram

The high-speed output buffer amplifier is operated in the non-inverting mode with gain determined by the user-connections at the output range select pin. The gain-setting application resistors are thin-film laser-trimmed to match and track the DAC resistors and to assure precise initial calibration of the two output ranges, 0V to 2.56V and 0V to 10V. The amplifier output stage is an NPN transistor with passive pull-down for zero-based output capability with a single power supply.

The internal precision voltage reference is of the patented band-gap type. This design produces a reference voltage of 1.2 volts and thus, unlike 6.3 volt temperature-compensated zeners, may be operated from a single, low-voltage logic power supply.

The microprocessor interface logic consists of an 8-bit data latch and control circuitry. Low-power, small geometry and high-speed are advantages of the I^2L design as applied to this section. I^2L is bipolar process compatible so that the performance of the analog sections need not be compromised to provide on-chip logic capabilities. The control logic allows the latches to be operated from a decoded microprocessor address and write signal. If the application does not involve a μP or data bus, wiring $\overline{CS}$ and $\overline{CE}$ to ground renders the latches "transparent" for direct DAC access.

CONNECTING THE AD558

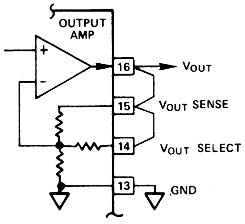
The AD558 has been configured for ease of application. All reference, output amplifier and logic connections are made internally. In addition, all calibration trims are performed at the factory assuring specified accuracy without user trims. The only connection decision that must be made by the user is a single jumper to select output voltage range. Clean circuit-board layout is facilitated by isolating all digital bit inputs on one side of the package; analog outputs are on the opposite side.

Figure 3 shows the two alternative output range connections. The 0V to 2.56V range may be selected for use with any power supply between +4.5V and +16.5V. The 0V to 10V range requires a power supply of +11.4V to +16.5V.

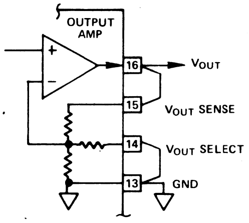
Because of its precise factory calibration, the AD558 is intended to be operated without user trims for gain and offset; therefore no provisions have been made for such user-trims. If a small increase in scale is required, however, it may be accomplished by slightly altering the effective gain of the output buffer. A resistor in series with V_{OUT} SENSE will increase the output range.

For example if a 0V to 10.24V output range is desired (40mV = 1LSB), a nominal resistance of 850Ω is required. It must be remembered that, although the internal resistors all ratio-match and track, the *absolute* tolerance of these resistors is typically ±20% and the *absolute* TC is typically -50ppm/°C (0 to -100ppm/°C). That must be considered when re-scaling is performed. Figure 4 shows the recommended circuitry for a full-scale output range of 10.24 volts. Internal resistance values shown are nominal.

NOTE: Decreasing the scale by putting a resistor in series with GND will not work properly due to the code-dependent currents in GND. Adjusting offset by injecting dc at GND is not recommended for the same reason.



a. 0V to 2.56V Output Range



b. 0V to 10V Output Range

Figure 3. Connection Diagrams

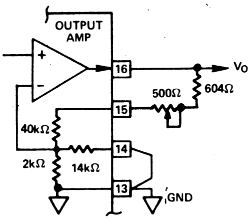


Figure 4. 10.24V Full-Scale Connection

GROUNDING AND BYPASSING*

All precision converter products require careful application of good grounding practices to maintain full rated performance. Because the AD558 is intended for application in microcomputer systems where digital noise is prevalent, special care must be taken to assure that its inherent precision is realized.

The AD558 has two ground (common) pins; this minimizes ground drops and noise in the analog signal path. Figure 5 shows how the ground connections should be made.

It is often advisable to maintain separate analog and digital grounds throughout a complete system, tying them common in one place only. If the common tie-point is remote and accidental disconnection of that one common tie-point occurs due to card removal with power on, a large differential voltage between the two commons could develop. To protect devices that interface to both digital and analog parts of the system, such as the AD558, it is recommended that common ground tie-points should be provided at *each* such device. If only one system ground can be connected directly to the AD558, it is recommended that analog common be selected.

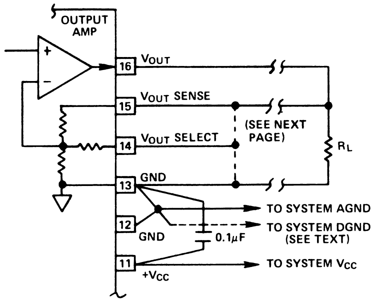


Figure 5. Recommended Grounding and Bypassing

POWER SUPPLY CONSIDERATIONS

The AD558 is designed to operate from a single positive power supply voltage. Specified performance is achieved for any supply voltage between +4.5V and +16.5V. This makes the AD558 ideal for battery-operated, portable, automotive or digital main-frame applications.

The only consideration in selecting a supply voltage is that, in order to be able to use the 0V to 10V output range, the power supply voltage must be between +11.4V and +16.5V. If, however, the 0V to 2.56V range is to be used, power consumption will be minimized by utilizing the lowest available supply voltage (above +4.5V).

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*For additional insight, "An IC Amplifier Users' Guide to Decoupling, Grounding and Making Things Go Right For A Change", is available at no charge from any Analog Devices Sales Office.

TIMING AND CONTROL

The AD558 has data input latches that simplify interface to 8- and 16-bit data buses. These latches are controlled by Chip Enable ($\overline{CE}$) and Chip Select ($\overline{CS}$) inputs, pins 9 and 10 respectively. $\overline{CE}$ and $\overline{CS}$ are internally "NORed" so that the latches transmit input data to the DAC section when both $\overline{CE}$ and $\overline{CS}$ are at Logic "0". If the application does not involve a data bus, a "00" condition allows for direct operation of the DAC. When either $\overline{CE}$ or $\overline{CS}$ go to Logic "1", the input data is latched into the registers and held until both $\overline{CE}$ and $\overline{CS}$ return to "0". (Unused $\overline{CE}$ or $\overline{CS}$ inputs should be tied to ground.) The truth table is given in Table I. The logic function is also shown in Figure 6.

Input Data	$\overline{CE}$	$\overline{CS}$	DAC Data	Latch Condition
0	0	0	0	"transparent"
1	0	0	1	"transparent"
0	ʃ	0	0	latching
1	ʃ	0	1	latching
0	0	ʃ	0	latching
1	0	ʃ	1	latching
X	1	X	previous data	latched
X	X	1	previous data	latched

Notes: X = Does not matter
ʃ = Logic Threshold at Positive-Going Transition

Table I. AD558 Control Logic Truth Table

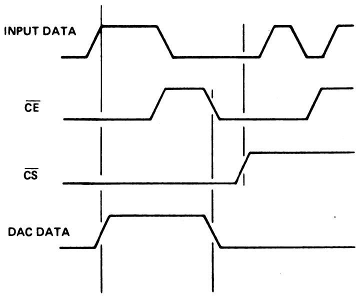
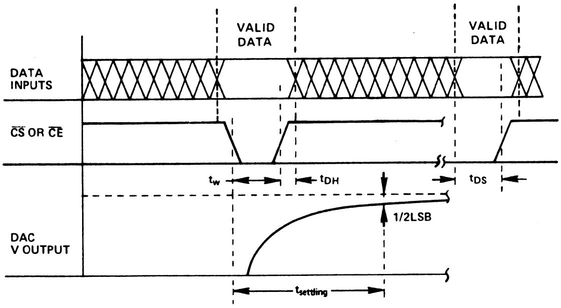


Figure 6. AD558 Control Logic Function

Figure 7 shows the timing for the data and control signals; $\overline{CE}$ and $\overline{CS}$ are identical in timing as well as in function.

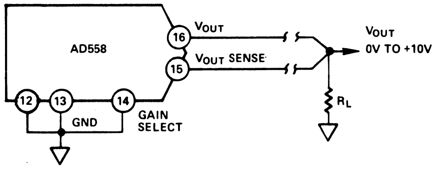


t_w = Strobe pulse width
t_{DH} = Data hold time
t_{DS} = Data setup time
$t_{settling}$ = DAC output settling time to ±1/2LSB

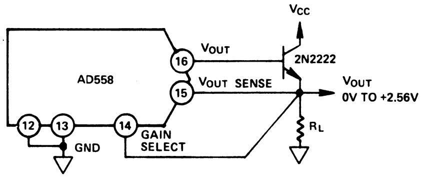
Figure 7. AD558 Timing

USE OF V_{OUT} SENSE

Separate access to the feedback resistor of the output amplifier allows additional application versatility. Figure 8a shows how I X R drops in long lines to remote loads may be cancelled by putting the drops "inside the loop". Figure 8b shows how the separate sense may be used to provide a higher output current by feeding back around a simple current booster.



a. Compensation for I x R Drops in Output Lines



b. Output Current Booster

Figure 8. Use of V_{OUT} Sense

OPTIMIZING SETTLING TIME

In order to provide single-supply operation and zero-based output voltage ranges, the AD558 output stage has a passive "pull-down" to ground. As a result, settling time for negative-going output steps may be longer than for positive-going output steps. The relative difference depends on load resistance and capacitance. If a negative power supply is available, the negative-going settling time may be improved by adding a pull-down resistor from the output to the negative supply as shown in Figure 9. The value of the resistor should be such that, at zero voltage out, current through that resistor is 0.5mA max.

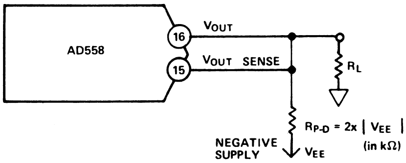
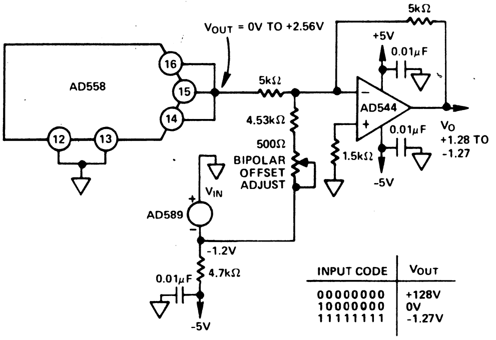


Figure 9. Improved Settling Time

BIPOLAR OUTPUT RANGES

The AD558 was designed for operation from a single power supply and is thus capable of providing only unipolar (0V to +2.56 and 0V to 10V) output ranges. If a negative supply is available, bipolar output ranges may be achieved by suitable output offsetting and scaling. Figure 10 shows how a ±1.28 volt output range may be achieved when a -5 volt power supply is available. The offset is provided by the AD589 precision 1.2 volt reference which will operate from a +5 volt supply. The AD544 output amplifier can provide the necessary ±1.28 volt output swing from ±5 volt supplies. Coding is complementary offset binary.

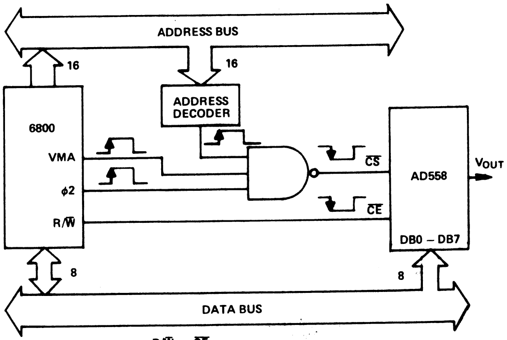


INPUT CODE	VOUT
00000000	+128V
10000000	0V
11111111	-1.27V

Figure 10. Bipolar Operation of AD558 from ±5V Supplies

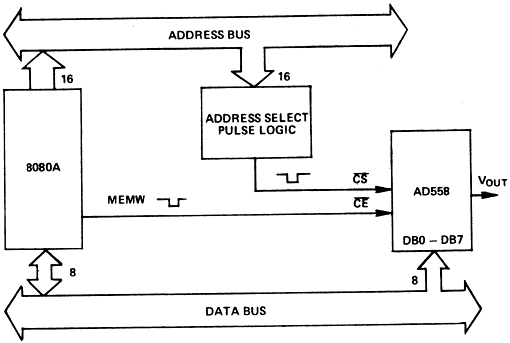
INTERFACING THE AD558 TO MICROPROCESSOR DATA BUSES*

The AD558 is configured to act like a "write only" location in memory that may be made to coincide with a read only memory location or with a RAM location. The latter case allows data previously written into the DAC to be read back later via the RAM. Address decoding is partially complete for either ROM or RAM. Figure 11 shows interfaces for three popular microprocessor systems.



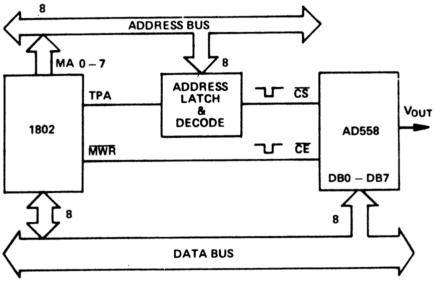
R/$\overline{W}$ → $\overline{CE}$
GATED DECODED ADDRESS → $\overline{CS}$

a. 6800/AD558 Interface



$\overline{MEMW}$ → $\overline{CE}$
DECODED ADDRESS SELECT PULSE → $\overline{CS}$

b. 8080A/AD558 Interface



CDP 1802: MWR → $\overline{CE}$
DECODED ADDRESS SELECT PULSE → $\overline{CS}$

c. 1802/AD558 Interface

Figure 11. Interfacing the AD558 to Microprocessors

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*The microprocessor-interface capabilities of the AD558 are extensive. A comprehensive application note, "Interfacing the AD558 DACPORT™ to Microprocessors" is available from any Analog Devices Sales Office upon request, free of charge.

AD558 Performance (typical @ +25°C, V_{CC} = +5V to +15V unless otherwise noted)

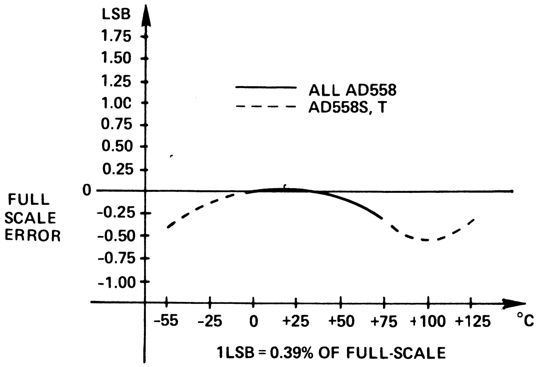


Figure 12. Full Scale Accuracy vs. Temperature Performance of AD558

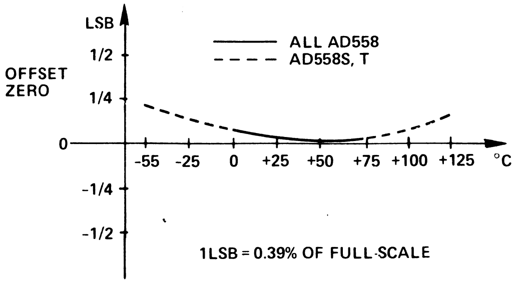


Figure 13. Zero Drift vs. Temperature Performance of AD558

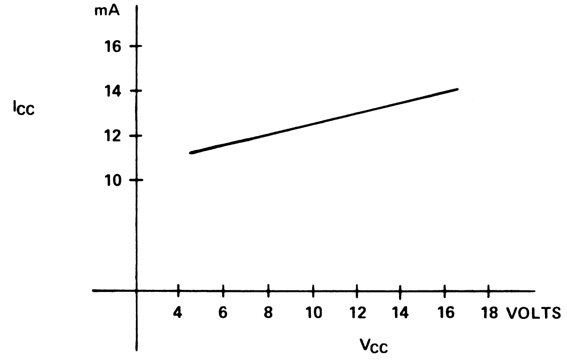


Figure 14. Quiescent Current vs. Power Supply Voltage for AD558

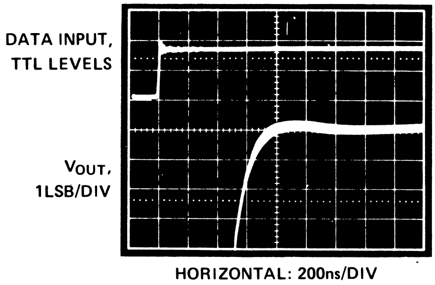


Figure 15. AD558 Settling Characteristic Detail 0V to 2.56V Output Range Full-Scale Step

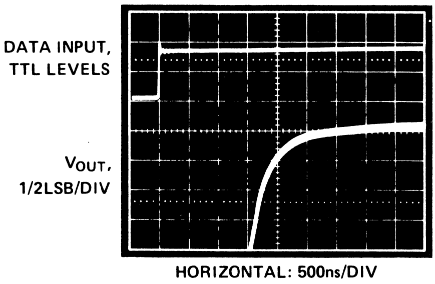


Figure 16. AD558 Settling Chracteristic Detail 0V to 10V Output Range Full-Scale Step

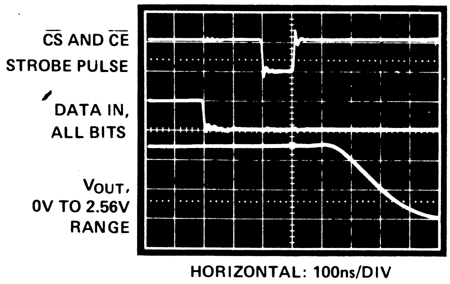


Figure 17. AD558 Logic Timing

ANALOG DEVICES

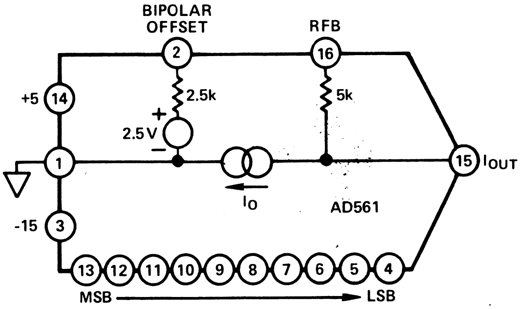
Low Cost 10-Bit Monolithic D/A Converter

AD561*

FEATURES

Low Cost
Complete Current Output Converter
High Stability Buried Zener Reference
Laser Trimmed to High Accuracy (1/4LSB Max Error, AD561K, T)
Trimmed Output Application Resistors for 0 to +10, ±5 Volt Ranges
Fast Settling – 250ns to 1/2LSB
Guaranteed Monotonicity Over Full Operating Temperature Range
TTL/DTL and CMOS Compatible (Positive True Logic)
Single Chip Monolithic Construction

AD561 FUNCTIONAL BLOCK DIAGRAM



TO-116

PRODUCT DESCRIPTION

The AD561 is an integrated circuit 10-bit digital-to-analog converter combined with a high stability voltage reference fabricated on a single monolithic chip. Using 10 precision high-speed current-steering switches, a control amplifier, voltage reference, and laser-trimmed thin-film SiCr resistor network, the device produces a fast, accurate analog output current. Laser trimmed output application resistors are also included to facilitate accurate, stable current-to-voltage conversion; they are trimmed to 0.1% accuracy, thus eliminating external trimmers in many situations.

Several important technologies combine to make the AD561 the most accurate and most stable 10-bit DAC available. The low temperature coefficient, high stability thin-film network is trimmed at the wafer level by a fine resolution laser system to 0.01% typical linearity. This results in an accuracy specification of ±1/4LSB max for the K and T versions, and 1/2LSB max for the J and S versions.

The AD561 also incorporates a low noise, high stability subsurface zener diode to produce a reference voltage with excellent long term stability and temperature cycle characteristics which challenge the best discrete zener references. A temperature compensation circuit is laser-trimmed to allow custom correction of the temperature coefficient of each device. This results in a typical full-scale temperature coefficient of 15ppm/°C; the T.C. is tested and guaranteed to 30ppm/°C max for the K and T versions, 60ppm/°C max for the S, and 80ppm/°C for the J.

The AD561J and K versions are specified for operation over the 0 to +70°C temperature range, the AD561S and T for operation over the full military temperature range from -55°C to +125°C.

PRODUCT HIGHLIGHTS

1. Advanced monolithic processing and laser trimming at the wafer level have made the AD561 the most accurate 10-bit converter available while keeping costs consistent with large volume integrated circuit production. The AD561K and T have 1/4LSB max relative accuracy and 1/2LSB max differential nonlinearity. The low T.C. R-2R ladder guarantees that all AD561 units will be monotonic over the entire operating temperature range.
2. Digital system interfacing is simplified by the use of a positive true straight binary code. The digital input voltage threshold is a function of the positive supply level; connecting V_{CC} to the digital logic supply automatically sets the threshold to the proper level for the logic family being used. Logic sink current requirement is only 25μA.
3. The high speed current steering switches are designed to settle in less than 250ns for the worst case digital code transition. This allows construction of successive-approximation A/D converters in the 3 to 5μs range.
4. The AD561 has an output voltage compliance range from -2 to +10 volts, thus allowing direct current-to-voltage conversion with just an output resistor, omitting the op amp. The 40MΩ open collector output impedance results in negligible errors due to output leakage currents.

***Covered by Patent Nos.: 3,940,760; 3,747,088; RE 28,633; 3,803,590; RE 29,619; 3,961,326; 4,141,004; 4,213,806; 4,136,349.**

SPECIFICATIONS (T_A = +25°C, V_{cc} = +5V, V_{ee} = -15V, unless otherwise specified)

MODEL	AD561J MIN	AD561J TYP	AD561J MAX	AD561K MIN	AD561K TYP	AD561K MAX	UNITS
RESOLUTION		10 Bits			10 Bits		
ACCURACY (Error Relative to Full Scale)		±1/4 (0.025)	±1/2 (0.05)		±1/8 (0.012)	±1/4 (0.025)	LSB % of F.S.
DIFFERENTIAL NONLINEARITY		±1/2			±1/4	±1/2	LSB
DATA INPUTS							
TTL, V_{CC} = +5V							
Bit ON Logic "1"	+2.0			*			V
Bit OFF Logic "0"			+0.8			*	V
CMOS, 10V ≤ V_{CC} ≤ 16.5V (See Figure 1)							
Bit ON Logic "1"	70% V_{CC}			*			V
Bit OFF Logic "0"			30% V_{CC}			*	V
Logic Current (Each Bit) (T_{min} to T_{max})							
Bit ON Logic "1"		+5	+100		*	*	nA
Bit OFF Logic "0"		-5	-25		*	*	μA
OUTPUT							
Current							
Unipolar	1.5	2.0	2.4	*	*	*	mA
Bipolar	±0.75	±1.0	±1.2	*	*	*	mA
Resistance (Exclusive of Application Resistors)		40M			*		Ω
Unipolar Zero (All Bits OFF)		0.01	0.05		*	*	% of F.S.
Capacitance		25			*		pF
Compliance Voltage	-2	-3	+10	*	*	*	V
SETTLING TIME TO 1/2LSB							
All Bits ON-to-OFF or OFF-to-ON		250			*		ns
POWER REQUIREMENTS							
V_{CC}, +4.5V dc to +16.5V dc		8	10		*	*	mA
V_{EE}, −10.8V dc to −16.5V dc		12	16		*	*	mA
POWER SUPPLY GAIN SENSITIVITY							
V_{CC}, +4.5V dc to +16.5V dc		2	10		*	*	ppm of F.S./%
V_{EE}, −10.8V dc to −16.5V dc		4	25		*	*	ppm of F.S./%
TEMPERATURE RANGE							
Operating		0 to +70			*	*	°C
Storage		-65 to +150			*	*	°C
TEMPERATURE COEFFICIENTS							
With Internal Reference							
Unipolar Zero		1	10		1	5	ppm of F.S./°C
Bipolar Zero		2	20		2	10	ppm of F.S./°C
Full Scale		15	80		15	30	ppm of F.S./°C
Differential Nonlinearity		2.5			2.5		ppm of F.S./°C
MONOTONICITY		Guaranteed over full operating temp. range			Guaranteed over full operating temp. range		
PROGRAMMABLE OUTPUT RANGES (See Figures 3, 4)		0 to +10 -5 to +5			* *		V V
CALIBRATION ACCURACY							
Full Scale Error with Fixed 25Ω Resistor		±0.1			*		% of F.S.
Bipolar Zero Error with Fixed 10Ω Resistor		±0.1			*		% of F.S.
CALIBRATION ADJUSTMENT RANGE							
Full Scale (With 50Ω Trimmer)		±0.5			*		% of F.S.
Bipolar Zero (With 50Ω Trimmer)		±0.5			*		% of F.S.

***Specifications same as AD561J specs.**
Specifications subject to change without notice.

		AD561S			AD561T		
MODEL	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
RESOLUTION		10 Bits			10 Bits		
ACCURACY (Error Relative to Full Scale)		±1/4 (0.025)	±1/2 (0.05)		±1/8 (0.012)	±1/4 (0.025)	LSB % of F.S.
DIFFERENTIAL NONLINEARITY		±1/2			±1/4	±1/2	LSB
DATA INPUTS							
TTL, V_{CC} = +5V							
Bit ON Logic "1"	+2.0			**			V
Bit OFF Logic "0"			+0.8			**	V
CMOS, 10V $\leqslant V_{CC} \leqslant$ 16.5V (See Figure 1)							
Bit ON Logic "1"	70% V_{CC}			**			V
Bit OFF Logic "0"			30% V_{CC}			**	V
Logic Current (Each Bit) (T_{min} to T_{max})							
Bit ON Logic "1"		+20	+100		**	**	nA
Bit OFF Logic "0"		-25	-100		**	**	µA
OUTPUT							
Current							
Unipolar	1.5	2.0	2.4	**	**	**	mA
Bipolar	±0.75	±1.0	±1.2	**	**	**	mA
Resistance (Exclusive of Application Resistors)		40M			**		Ω
Unipolar Zero (All Bits OFF)		0.01	0.05		**	**	% of F.S.
Capacitance		25			**		pF
Compliance Voltage	-2	-3	+10	**	**	**	V
SETTLING TIME TO 1/2LSB							
All Bits ON-to-OFF or OFF-to-ON		250			**		ns
POWER REQUIREMENTS							
V_{CC}, +4.5V dc to +16.5V dc		6	10		**	**	mA
V_{EE}, -10.8V dc to -16.5V dc		11	16		**	**	mA
POWER SUPPLY GAIN SENSITIVITY							
V_{CC}, +4.5V dc to +16.5V dc		2	10		**	**	ppm of F.S./%
V_{EE}, -10.8V dc to -16.5V dc		4	25		**	**	ppm of F.S./%
TEMPERATURE RANGE							
Operating		-55 to +125			**	**	°C
Storage		-65 to +150			**	**	°C
TEMPERATURE COEFFICIENTS							
With Internal Reference							
Unipolar Zero		1	10		1	5	ppm of F.S./°C
Bipolar Zero		2	20		2	10	ppm of F.S./°C
Full Scale		15	60		15	30	ppm of F.S./°C
Differential Nonlinearity		2.5			2.5		ppm of F.S./°C
MONOTONICITY		Guaranteed over full operating temp. range			Guaranteed over full operating temp. range		
PROGRAMMABLE OUTPUT RANGES (See Figures 3, 4)		0 to +10 -5 to +5			** **		V V
CALIBRATION ACCURACY							
Full Scale Error with Fixed 25Ω Resistor		±0.1			**		% of F.S.
Bipolar Zero Error with Fixed 10Ω Resistor		±0.1			**		% of F.S.
CALIBRATION ADJUSTMENT RANGE							
Full Scale (With 50Ω Trimmer)		±0.5			**		% of F.S.
Bipolar Zero (With 50Ω Trimmer)		±0.5			**		% of F.S.

****Specifications same as AD561S specs.**
Specifications subject to change without notice.

DIGITAL LOGIC INTERFACE

All standard positive supply logic families interface easily with the AD561. The digital code is positive true binary (all bits high, Logic "1", gives positive full scale output). The logic input load factor (100nA max at Logic "1", -25μA max at Logic "0", 3pF capacitance), is less than one equivalent digital load for all logic families, including unbuffered CMOS. The digital threshold is set internally as a function of the positive supply, as shown in Figure 1. For most applications, connecting V_{CC} to the positive logic supply will set the threshold at the proper level for maximum noise immunity. For nonstandard applications, refer to Figure 1 for threshold levels. Uncommitted bit input lines will assume a "1" state (similar to TTL), but they are high impedance and subject to noise pickup. Unused digital inputs should be connected directly to ground or V_{CC}, as desired.

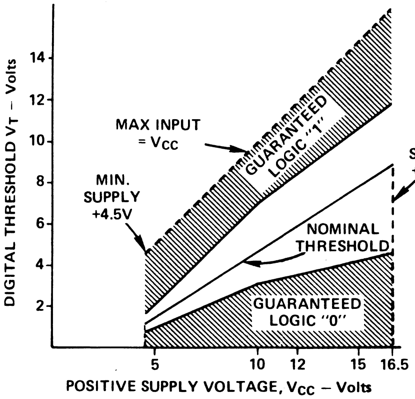


Figure 1. Digital Threshold Vs. Positive Supply

THE AD561 OFFERS TRUE 10-BIT RESOLUTION OVER FULL TEMPERATURE RANGE

ACCURACY: Analog Devices defines accuracy as the maximum deviation of the actual, adjusted DAC output (see next page) from the ideal analog output (a straight line drawn from 0 to F.S. – 1LSB) for any bit combination. The AD561 is laser trimmed to 1/4LSB (0.025% of F.S.) maximum error at +25°C for the K and T versions – 1/2LSB for the J and S.

MONOTONICITY: A DAC is said to be monotonic if the output either increases or remains constant for increasing digital inputs such that the output will always be a single-valued function of the input. All versions of the AD561 are monotonic over their full operating temperature range.

DIFFERENTIAL NONLINEARITY: Monotonic behavior requires that the differential nonlinearity error be less than 1LSB both at +25°C and over the temperature range of interest. Differential nonlinearity is the measure of the variation in analog value, normalized to full scale, associated with a 1LSB change in digital input code. For example, for a 10 volt full scale output, a change of 1LSB in digital input code should result in a 9.8mV change in the analog output (1LSB = 10V x 1/1024 = 9.8mV). If in actual use, however, a 1LSB change in the input code results in a change of only 2.45mV (1/4LSB) in analog output, the differential nonlinearity error would be 7.35mV, or 3/4LSB. The AD561K and T have a max differential linearity error of 1/2LSB.

The differential nonlinearity temperature coefficient must also be considered if the device is to remain monotonic over its full operating temperature range. A differential nonlinearity temperature coefficient of 2.5ppm/°C could under worst case conditions for a temperature change of +25°C to +125°C add 0.025% (100 x 2.5ppm/°C of error). The resulting error could then be as much as 0.025% + 0.025% = 0.05% of F.S. (1/2LSB represents 0.05% of F.S.). To be sure of accurate performance all versions of the AD561 are therefore 100% tested to be monotonic over the full operating temperature range.

AD561 ORDERING GUIDE

MODEL	TEMP RANGE	ACCURACY @ +25°C	GAIN T.C. (of F.S./°C)	PACKAGE OPTIONS[1]
AD561JD	0 to +70°C	±½LSB max	80ppm max	D16A
AD561JN	0 to +70°C	±½LSB max	80ppm max	N16A[2]
AD561KD	0 to +70°C	±¼LSB max	30ppm max	D16A
AD561KN	0 to +70°C	±¼LSB max	30ppm max	N16A[2]
AD561SD	-55 to +125°C	±½LSB max	60ppm max	D16A
AD561SD/883B*	-55 to +125°C	±½LSB max	60ppm max	D16A
AD561TD	-55 to +125°C	±¼LSB max	30ppm max	D16A
AD561TD/883B*	-55 to +125°C	±¼LSB max	30ppm max	D16A

*The AD561SD/883B and AD561TD/883B are fully processed to MIL-STD-883, Method 5004, Class B.

[1] See Section 20 for package outline information.

[2] To be available June, 1982.

CONNECTING THE AD561 FOR BUFFERED VOLTAGE OUTPUT

The standard current-to-voltage conversion connections using an operational amplifier are shown here with the preferred trimming techniques. If a low offset operational amplifier (AD510, AD741L, AD301AL) is used, excellent performance can be obtained in many situations without trimming. (A 5mV op amp offset is equivalent to 1/2LSB on a 10 volt scale). If a 25Ω fixed resistor is substituted for the 50Ω trimmer, unipolar zero will typically be within ±1/10LSB (plus op amp offset), and full scale accuracy will be within ±1LSB. Substituting a 10Ω resistor for the 50Ω bipolar offset trimmer will give a bipolar zero error typically within ±1LSB.

The AD509 is recommended for buffered voltage-output applications which require a settling time to ±1/2LSB of one microsecond. The feedback capacitor is shown with the optimum value for each application; this capacitor is required to compensate for the 25picofarad DAC output capacitance.

FIGURE 3. UNIPOLAR CONFIGURATION

This configuration will provide a unipolar 0 to +10 volt output range.

STEP I . . . ZERO ADJUST

Turn all bits OFF and adjust op amp trimmer, R_1, until the output reads 0.000 volts (1LSB = 9.76mV).

STEP II . . . GAIN ADJUST

Turn all bits ON and adjust 50Ω gain trimmer, R_2, until the output is 9.990 volts. (Full scale is adjusted to 1LSB less than nominal full scale of 10.000 volts.) If a 10.23V full scale is desired (exactly 10mV/bit), insert a 120Ω resistor in series with R_2.

FIGURE 4. BIPOLAR CONFIGURATION

This configuration will provide a bipolar output voltage from -5.000 to +4.990 volts, with positive full scale occurring with all bits ON (all 1's).

STEP I . . . ZERO ADJUST

Turn ON MSB only, turn OFF all other bits. Adjust 50Ω trimmer R_3, to give 0.000 output volts.

STEP II . . . GAIN ADJUST

Turn OFF all bits, adjust 50Ω gain trimmer to give a reading of -5.000 volts.

Please note that it is not necessary to trim the op amp to obtain full accuracy at room temperature. In most bipolar situations, the op amp trimmer is unnecessary unless the untrimmed offset drift of the op amp is excessive.

FIGURE 5. ±10 VOLT BUFFERED BIPOLAR OUTPUT

The AD561 can also be connected for a ±10 volt bipolar range with an additional external resistor as shown in Figure 5. A larger value trimmer is required to compensate for tolerance in the thin film resistors (which are trimmed to match the full scale current). For best full scale temperature coefficient performance, the external resistors should have a T.C. of -50ppm/°C. For applications requiring optimum performance, a ±10 volt bonding option is available on special order.

PIN CONFIGURATION
TOP VIEW

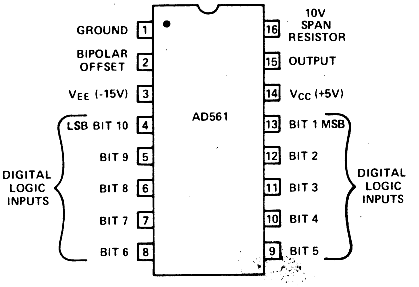


Figure 2.

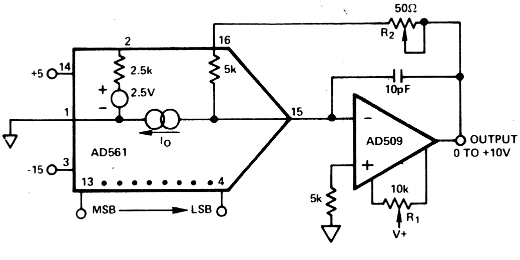


Figure 3. 0 to +10V Unipolar Voltage Output

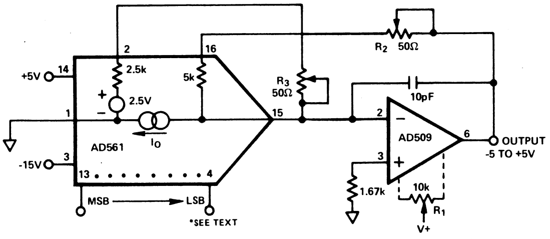


Figure 4. ±5V Buffered Bipolar Voltage Output

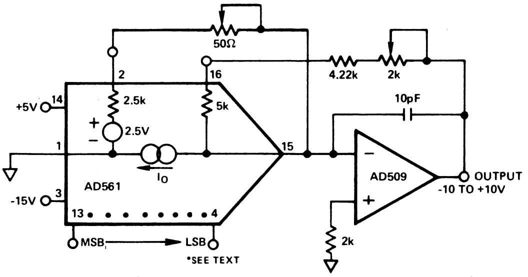


Figure 5. ±10V Buffered Voltage Output

CIRCUIT DESCRIPTION

A simplified schematic with the essential circuit features of the AD561 is shown in Figure 6. The voltage reference, CR1, is a buried zener (or subsurface breakdown diode). This device exhibits far better all-around performance than the NPN base-emitter reverse-breakdown diode (surface zener), which is in nearly universal use in integrated circuits as a voltage reference. Greatly improved long term stability and lower noise are the major benefits the buried zener derives from isolating the breakdown point from surface stress and mobile oxide charge effects. The nominal 7.5 volt device (including temperature compensation circuitry) is driven by a current source to the negative supply so that the positive supply can be allowed to go as low as 4.5 volts. The temperature coefficient of each diode is determined individually; this data is then used to laser trim a compensating circuit to balance the overall T.C. to zero. The typical resulting T.C. is 0 to ±15ppm/°C.

The negative reference level is inverted and scaled by A_1 to give a +2.5 volt reference (which can be driven by the low positive supply). The AD561, packaged in the 16-pin DIP, has the +2.5 volt reference (REF OUT) connected directly to the input of the control amplifier (REF IN). The buffered reference is not directly available externally except through the 2.5kΩ bipolar offset resistor; it can still be used as a voltage reference as shown below in Figure 9.

The 2.5kΩ scaling resistor and control amplifier A_2 then force a 1mA reference current to flow through reference transistor Q1, which has a relative emitter area of 8A. This is accomplished by forcing the bottom of the ladder to the proper voltage. Since Q_1 and Q_2 have equal emitter areas and have equal 5kΩ emitter resistors, Q_2 also carries 1mA. The ladder voltage drop constrains Q_7 (with area 4A) to carry only 0.5mA; Q_8 carries 0.25mA, etc.

The first four significant bit cells are scaled exactly in emitter area to match Q_1 for optimum V_{BE} and V_{BE} drift match, as well as for beta match. These effects are insignificant for the lower order bits, which account for a total of only 1/16 of full scale. However, the 18mV V_{BE} difference between two matched transistors carrying emitter currents in a ratio of 2:1 must be corrected. This is done by forcing 120μA through the 150Ω interbase resistors. These resistors and the R-2R ladder resistors are actively laser-trimmed at the wafer level to bring total device accuracy to better than 1/4LSB. Sufficient ratio accuracy in the last two bits is obtained by simple emitter area ratio such that it is unnecessary to use additional area for ladder resistors. The current in Q_{16} is added to the ladder to balance it properly but is not switched to the output; thus full scale is 1023/1024 x 2mA.

The switching cell of Q_3, Q_4, Q_5 and Q_6 serves to steer the cell current either to ground (BIT 1 low) or to the DAC output (BIT 1 high). The entire switching cell carries the same current whether the bit is on or off, thus minimizing thermal transients and ground current errors. The logic threshold, which is generated from the positive supply (see Digital Logic Interface) is applied to one side of each cell.

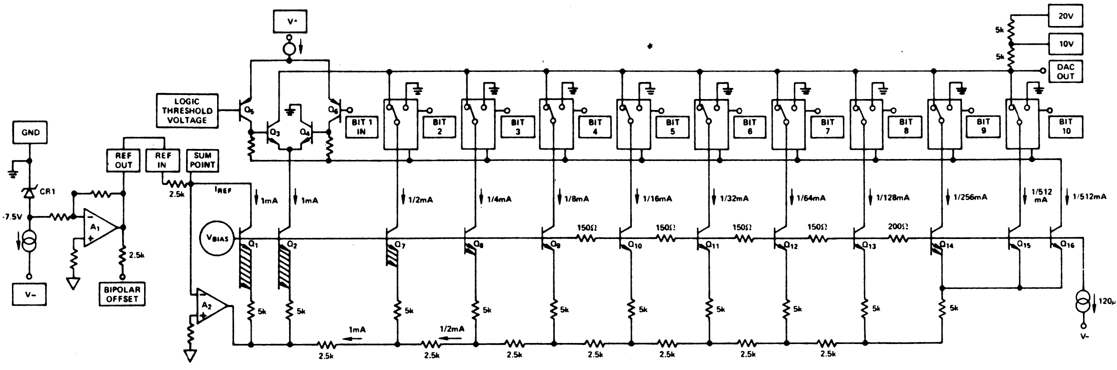


Figure 6. Circuit Diagram Showing Reference, Control Amplifier, Switching Cell, R-2R Ladder, and Bit Arrangement of AD561

PRECISION LOW-NOISE REFERENCE

The precision reference of the AD561 can be brought out separately from the DAC to serve as a master system reference. Since the reference is connected through the 2.5kΩ bipolar offset resistor, it must be buffered externally, as shown here in Figure 7. The DAC section can still be operated independently in a unipolar mode, but internal thermal and ground loop effects will create crosstalk of about 0.01% with an ideal ground. The long term stability of this reference will be especially good, typically ±0.01% per year or better. If the filter capacitor, C is not used, wideband output noise will be about 120ppm p-p (1.2mV p-p for 10 volts). If C is 4.7μF, wideband noise will be about 25μV p-p (10 volts out) and 15μV p-p from 0.1 to 10Hz.

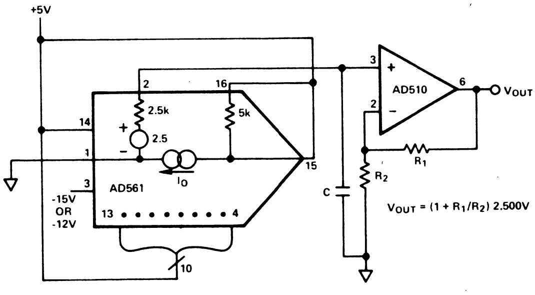


Figure 7. Precision Ultra Low Noise Reference

SETTLING TIME

The high speed NPN current steering switching cell and internally compensated reference amplifier of the AD561 are specifically designed for fast settling operation. The typical settling time to ±0.05% (1/2LSB) for the worst case transition (major carry, 0111111111 to 1000000000) is less than 250ns; the lower order bits all settle in less than 200ns. (Worst case settling occurs when all bits are switched, especially the MSB.) But full realization of this high speed performance requires strict attention to detail by the user in all areas of application and testing.

The settling time for the AD561 is specified in terms of the current output, an inherently high speed DAC operating mode. However, most DAC applications require a current-to-voltage conversion at some point in the signal path, although an unbuffered voltage level (not using an op amp) is suitable for use in a successive-approximation A/D converter (see next page), or in many display applications. This form of conversion can give very fast operation if proper design and layout is done. The fastest voltage conversion is achieved by connecting a low value resistor directly to the output, as shown in Figure 9. In this case, the settling time is primarily determined by the cell switching time and by the RC time constant of the AD561 output capacitance of 25 picofarads (plus stray capacitance) combined with the output resistor value. Settling to 0.05% of full scale (for a full scale transition) requires 7.6 time constants. This effect is important for $R > 1k\Omega$.

If an op amp must be used to provide a low impedance output signal, some loss in settling time will be seen due to op amp dynamics. The normal current-to-voltage converter op amp circuits are shown in the applications circuits using the fast settling AD509. The circuits shown settle to ±1/2LSB in 600ns unipolar and 1.1μs bipolar. The DAC output capacitance, which acts as a stray capacitance at the op amp inverting input, must be compensated by a feedback capacitor, as shown. The value should be chosen carefully for each application and each op amp type.

Fastest operation will be obtained by minimizing lead lengths, stray capacitance and impedance levels. Both supplies should be bypassed near the devices; 0.1μF will be sufficient since the AD561 runs at constant supply current regardless of input code.

POWER SUPPLY SELECTION

The AD561 will operate over a wide range of power supply voltages, with a total supply from 15.3 to 33 volts. Symmetrical supplies are not required, and in many applications not recommended.

The positive supply level determines the digital threshold level, as explained previously and shown in Figure 1. It is therefore recommended that V_{CC} be connected directly to the digital supply for best threshold match.

Positive output voltage compliance range is unaffected by the positive supply level because of the open collector output stage design; thus the full +10 volt compliance is available even with a +5 volt V_{CC} level. Power supply rejection is excellent, so that digital supply noise will not be reflected to the output. but use of a 0.1μF bypass capacitor near the AD561 is recommended for decoupling.

The nominal negative supply level is -15 volts, with an allowable range of −10.8 to −16.5 volts. The negative supply level affects the negative compliance range, as shown in Figure 8.

OUTPUT VOLTAGE COMPLIANCE

The AD561 has a typical output compliance range from -3 to +10 volts. The output current is unaffected by changes in the output terminal voltage over that range. This results from the use of open collector output switching stages in a cascode configuration, and gives an output impedance of 40MΩ. Positive compliance range is limited only by collector breakdown (and is independent of positive supply level), but the negative range is limited by the required bias levels and resistor ladder voltage. Negative compliance varies with negative supply, as shown in Figure 8. The compliance range is guaranteed to be -2 to +10 volts with V_{EE} = -15 volts.

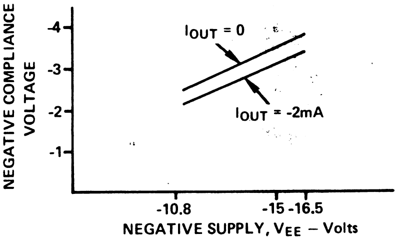


Figure 8. Typical Negative Compliance Range Vs. Negative Supply

DIRECT UNBUFFERED VOLTAGE OUTPUT

The wide compliance range allows direct current-to-voltage conversion with just an output resistor. Figure 1 shows a connection using the gain and bipolar output resistors to give a ±1.66 volt bipolar swing. In this situation, the digital code is complementary binary. Other combinations of internal and external output resistors (R_X) can be used to scale to alternate voltage ranges, simply by appropriately scaling the 0 to -2mA unipolar output current and using the 2.5 volt reference voltage for bipolar offset. For example, setting R_X = 2.5kΩ gives a ±1 volt range with a 1kΩ equivalent output impedance. A 0 to +10 volt output can be obtained by connecting the 5kΩ gain resistor to 9.99 volts; again the digital code is complementary binary.

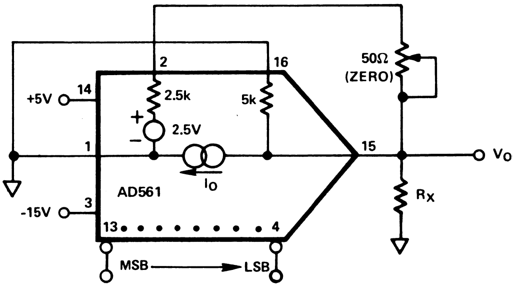


Figure 9. Unbuffered Bipolar Voltage Output

HIGH SPEED 10-BIT A/D CONVERTERS

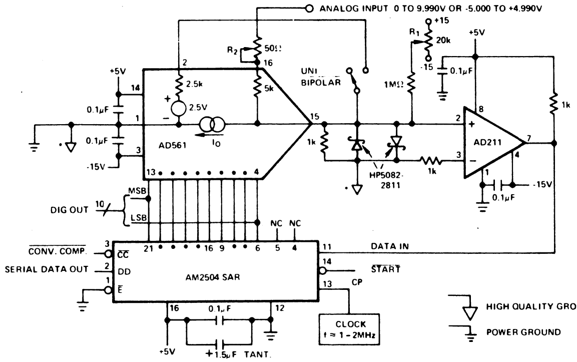
The fast settling characteristics of the AD561 make it ideal for high speed successive approximation A/D converters. The internal reference and trimmed application resistors allow a 10-bit converter system to be constructed with a minimum parts count. Shown here is a configuration using standard components; this system completes a full 10-bit conversion in 5.5μs unipolar or 12μs bipolar. This converter will be accurate to ±1/2LSB of 10 bits and have a typical gain T.C. of 10ppm/°C.

In the unipolar mode, the system range is 0 to 9.99 volts, with each bit having a value of 9.76mV. For true conversion accuracy, an A/D converter should be trimmed so that a given bit code output results from input levels from 1/2LSB below to 1/2LSB above the exact voltage which that code represents. Therefore, the converter zero point should be trimmed with an input voltage of +4.9mV; trim R_1 until the LSB just begins to appear in the output code (all other bits "0"). For full scale, use an input voltage of +9.9985 volts (10 volts – 1LSB – 1/2LSB); then trim R_2 again until the LSB just begins to appear (all other bits "1").

The bipolar signal range is -5.0 to +4.99 volts. Bipolar offset trimming is done by applying a +4.9mV input signal and trimming R_1 for the LSB transition (MSB "1", all other bits "0"). Full scale is set by applying -4.995 volts and trimming R_2 for the LSB transition (all other bits "0"). In many applications, the pretrimmed application resistors are sufficiently accurate that external trimmers will be unnecessary, especially in situations requiring less than full 10-bit ±1/2LSB accuracy.

For fastest operation, the impedance at the comparator summing node must be minimized, as mentioned in the section on settling time. However, lowering the impedance will reduce the voltage signal to the comparator (at an equivalent impedance of 1kΩ, 1LSB = 2mV) to the point that comparator performance will be sacrificed. A 1kΩ resistor is the optimum value for this application for 10-bit accuracy. The chart shown in the figure gives the speed of the ADC for ±1/2LSB accuracy (and no missing codes) for 6, 8 and 10-bit resolution.

A much faster converter can be constructed by using higher performance external components. Each individual high-order bit settles in less than 250ns; the low-order bits less than 200ns. Because of this, a staged clock which speeds up for lower bits will improve the speed. Also, a faster comparator and Schottky TTL or ECL logic would be necessary. 10-bit converters in the 3 to 5μs range could be built around the AD561 with these techniques.



CONVERSION TIME (μs)

	UNIPOLAR	BIPOLAR
6 BITS	1.4	2.1
8 BITS	2.7	4.0
10 BITS	5.5	12

Figure 10. Fast Precision Analog to Digital Converter

DIGITAL 4 TO 20mA OR 1 TO 5 VOLT CONVERTER

A direct digital 4 to 20mA or 1 to 5 volt line driver can be built with the AD561 as shown in Figure 11. The 2.5 volt reference is divided to provide 1 volt at the op amp non-inverting input – thus a zero input code results in a 1 volt output at the Darlington emitter (V_{OUT}). The 2k feedback resistance converts the nominal 2mA (±20%) full scale output from the AD561 to 4 volts, for a total output of 5 volts F.S. The voltage at the emitter forces a proportional current through the 250Ω (which appears at the collector as I_{OUT}). The AD561 current is added to the 4–20mA line; thus 5 volts full scale gives 22mA in the current loop. For exactly 20mA, trim the 1k pot for 4.5V F.S. (A single op amp circuit will not produce both 1 to 5 volt and 4 to 20mA outputs simultaneously.)

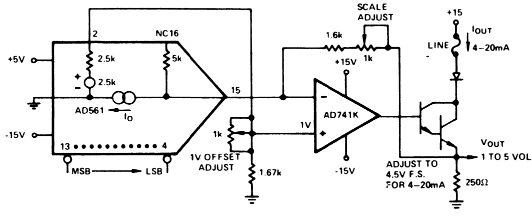


Figure 11. Digital 4 to 20mA or 1 to 5 Volt Line Driver

DIGITALLY PROGRAMMABLE SET-POINT COMPARATOR

Figure 12 demonstrates a high accuracy systems-oriented set-point comparator. The 2.5 volt reference is buffered and amplified by the AD741K to produce an exact 10.000 volt reference which could be used as a primary system reference for several such circuits. The +10 volt compliance of the AD561 then allows it to generate a zero to +10 volt output swing through the 5kΩ application resistor without an additional op amp. The digital code for this system will be complementary binary (all 1's give 0.00 volts out).

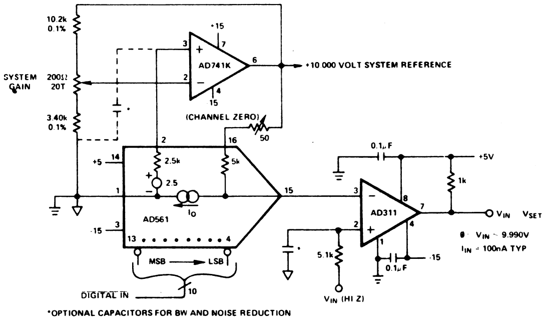


Figure 12. Digitally Programmable Set-Point Comparator

ANALOG DEVICES

IC 12-Bit D/A Converter

AD562/AD563*

FEATURES

Low Cost
True 12-Bit Accuracy
Guaranteed Monotonicity Over Full Temperature Range
Hermetic 24-Pin DIP
TTL/DTL and CMOS Compatibility
Positive True Logic

PRODUCT DESCRIPTION

The AD562/AD563 are monolithic 12-bit digital-to-analog converters consisting of especially designed precision bipolar switches and control amplifiers and compatible high stability silicon chromium thin film resistors. The AD563 also includes its own internal voltage reference.

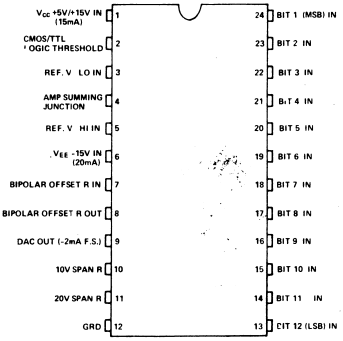
A unique combination of advanced circuit design, high stability SiCr thin film resistor processing and laser trimming technology provide the AD562/AD563 with true 12-bit accuracy. The maximum error at +25°C is limited to ±½LSB on all versions and monotonicity is guaranteed over the full operating temperature range.

The AD562 and AD563 are recommended for high accuracy 12-bit D/A converter applications where true 12-bit performance is required, but low cost and small size are considerations. Both devices are also ideal for use in constructing A/D conversion systems and as building blocks for higher resolution D/A systems. J and K versions are specified for operation over the 0 to +70°C temperature range, the S and T for operation over the military temperature range, -55°C to +125°C.

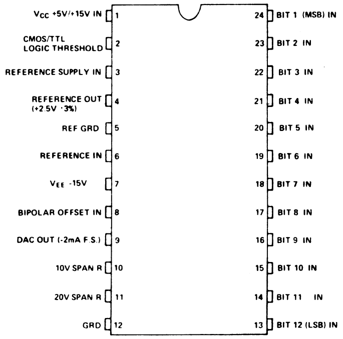
PRODUCT HIGHLIGHTS

1. The AD562 multiplies in two quadrants when a varying reference voltage is applied. When multiplication is not required, the AD563 is recommended with its internal low drift voltage reference.
2. True 12-bit resolution is achieved with guaranteed monotonicity over the full operating temperature range. Voltage outputs are easily implemented by using an external operational amplifier and the AD562/AD563s internally provided feedback resistors.
3. The devices incorporate a newly developed and fully differential, non-saturating precision current switching cell structure which provides increased immunity to supply voltage variation and also reduces nonlinearities due to thermal transients as the various bits are switched; nearly all critical components operate at constant power dissipation.

AD562, AD563 PIN CONFIGURATIONS



AD562



AD563

4. The thin film resistor network contains gain, range, and bipolar offset resistors so that various output voltage ranges can be programmed by changing connections to the device terminal leads. Thin film resistors are laser trimmed while the device is powered to accurately calibrate all scale factors. The scale factors are dependent upon the tracking coefficient (<±2ppm/°C) of these resistors, rather than upon their absolute temperature coefficients.
5. TTL or CMOS input can be accommodated for supply voltages from +5V to +15V.
6. Positive true logic eliminates the need for additional inverter components.

***Covered by Patent Nos. 3,961,326; 4,141,004; 3,747,088; RE 28,633; 3,803,590; 4,020,486; the AD563 is also covered by 4,213,806; 4,136,349.**

SPECIFICATIONS (T_A = +25°C, unless otherwise specified)

MODEL	AD562KD/BIN AD562KD/BCD	AD562AD/BIN AD562AD/BCD	AD562SD/BIN AD562SD/BCD
DATA INPUTS (positive True, Binary (BCD) and Offset Binary (BCD))			
TTL, V_{CC} = +5V, Pin 2			
Open Circuit			
Bit ON Logic "1"	+2.0V	*	*
Bit OFF Logic "0"	+0.8V max	*	*
CMOS, $4.75 \leq V_{CC} \leq 15.8$, Pin 2 Tied to Pin 1			
Bit ON Logic "1"	70%V_{CC} min	*	*
Bit OFF Logic "0"	30%V_{CC} max	*	*
Logic Current (Each Bit)			
Bit ON Logic "1"	+20nA typ, +100nA max	*	*
Bit OFF Logic "0"	-50µA typ, -100µA max	*	*
OUTPUT			
Current			
Unipolar	-1.6mA min, -2.0mA typ, -2.4mA max	*	*
Bipolar	±0.8mA min, ±1.0mA typ, ±1.2mA max	*	*
Resistance (Exclusive of Span Resistors)	5.3kΩ min, 6.6kΩ typ, 7.9kΩ max	*	*
Unipolar Zero (All Bits OFF)	0.01% of F.S. typ, 0.05% of F.S. max	*	*
Capacitance	33pF typ	*	*
Compliance Voltage	-1.5V to +10V typ	*	*
RESOLUTION			
Binary	12 Bits	*	*
BCD	3 Digits	*	*
ACCURACY (Error Relative to Full Scale)			
Binary	±1/2LSB max	*	±1/4LSB max
BCD	±1/2LSB max	*	±1/10LSB max
DIFFERENTIAL NONLINEARITY	±1/2LSB max	*	*
SETTLING TIME TO 1/2LSB			
All Bits ON-to-OFF or OFF-to-ON	1.5µs typ	*	*
POWER REQUIREMENTS			
V_{CC}, +4.75 to +15.8V dc	15mA typ, 18mA max	*	*
V_{EE}, -15V dc ±5%	20mA typ, 25mA max	*	*
POWER SUPPLY GAIN SENSITIVITY			
V_{CC} @ +5V dc	2ppm of F.S./% max	*	*
V_{CC} @ +15V dc	2ppm of F.S./% max	*	*
V_{EE} @ -15V dc	6ppm of F.S./% max	*	*
TEMPERATURE RANGE			
Operating	0 to +70°C typ	-25°C to +85°C	-55°C to +125°C
Storage	-65°C to +150°C typ	*	*
TEMPERATURE COEFFICIENT			
Unipolar Zero	2ppm of F.S./°C max	*	2ppm of F.S./°C max
Bipolar Zero	4ppm of F.S./°C max	*	*
Gain	5ppm of F.S./°C max	*	*
Differential Nonlinearity	2ppm of F.S./°C	*	1ppm of F.S./°C
MONOTONICITY	Guaranteed Over Full Operating Temperature Range	*	*
EXTERNAL ADJUSTMENTS[1]			
Gain Error with Fixed 50Ω Resistor	±0.2% of F.S. typ	*	*
Bipolar Zero Error with Fixed 50Ω Resistor	±0.1% of F.S. typ	*	*
Gain Adjustment Range	±0.25% of F.S. typ	*	*
Binary Bipolar Zero Adjustments Range	±0.25% of F.S. typ	*	*
BCD Bipolar Offset Adjustment Range	±0.17% of F.S. typ	*	*
PROGRAMMABLE OUTPUT RANGES	0 to +5V typ	*	*
	-2.5V to +2.5V typ	*	*
	0V to +10V typ	*	*
	-5V to +5V typ	*	*
	-10V to +10V typ	*	*
REFERENCE INPUT			
Input Impedance	20kΩ typ	*	*

*Specifications same as AD562KD. **Specifications same as AD563KD. ***Specifications same as AD563JD. [1] Device calibrated with internal reference.
Specifications subject to change without notice.

AD563JD/BIN AD563JD/BCD	AD563KD/BIN AD563KD/BCD	AD563SD/BIN AD563SD/BCD	AD563TD/BIN AD563TD/BCD
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
•	±1/4LSB	••	••
•	±1/4LSB	••	••
•	•	•	•
•	•	•	•
15mA typ, 20mA max	•••	•••	•••
•	•	•	•
3ppm of F.S./% typ, 10ppm of F.S./% max	•••	•••	•••
3ppm of F.S./% typ, 10ppm of F.S./% max	•••	•••	•••
14ppm of F.S./% typ, 25ppm of F.S./% max	•••	•••	•••
•	•	-55°C to +125°C	-55°C to +125°C
•	•	•	•
With Internal Reference			
1ppm of F.S./°C typ, 2ppm of F.S./°C max	•••	•••	•••
10ppm of F.S./°C max	•••	•••	•••
50ppm of F.S./°C max	20ppm of F.S./°C max	30ppm of F.S./°C max	10ppm of F.S./°C max
•	•	•	•
•	•	•	•
With Fixed 10Ω Resistor			
±0.2% of F.S. typ	•••	•••	•••
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
5kΩ typ	•••	•••	•••

THE AD562/AD563 OFFERS TRUE 12-BIT RESOLUTION OVER FULL TEMPERATURE RANGE

Accuracy: Analog Devices defines accuracy as the maximum deviation of the actual DAC output from the ideal analog output (a straight line drawn from 0 to F.S. − 1LSB) *for any bit combination.* The AD563, for example, is laser trimmed to ¼LSB (0.006% of F.S.) maximum error at +25°C for K, S and T versions . . . ½LSB for the J version.

Monotonicity: A DAC is said to be monotonic if the output either increases or remains constant for increasing digital inputs such that the output will always be a single-valued function of the input. All versions of the AD562/AD563 are monotonic over their full operating temperature range.

Differential Nonlinearity: Monotonic behavior requires that the differential nonlinearity error be <1LSB both at 25°C and over the temperature range of interest. Differential nonlinearity is the measure of the variation in analog value, normalized to full scale, associated with a one LSB change in digital input code. For example, for a 10V full-scale output, a change of one LSB in the digital input code should result in a 2.4mV change in the analog output (10V x 1/4096 = 2.4mV). If in actual use, however, a one LSB change in the input code results in a change of 1.3mV in analog output, the differential nonlinearity would be 1.1mV, or 0.011% of F.S. The differential nonlinearity temperature coefficient must also be considered if the device is to remain monotonic over its full operating temperature range. A differential nonlinearity temperature coefficient of 1ppm/°C could, under worst case conditions for a temperature change of +25°C to +125°C, add 0.01% (100°C x 1ppm/°C) of error. The resulting error could then be as much as 0.006% + 0.01% = 0.016% of F.S. (1LSB represents 0.024% of F.S.). All versions of the AD563 are 100% tested to be monotonic over the full operating temperature range.

UNIPOLAR DAC's

STEP I . . . OUTPUT RANGE

Determine the output range required. For +10V F.S., connect the external operational amplifier output to Pin 10 and leave Pin 11 unconnected. For +5V F.S., connect the external op amp output to Pin 10 and short Pin 11 to Pin 9.

STEP II . . . ZERO ADJUST

Turn all bits OFF and adjust R_1 until op amp output is 0 volts.

STEP III . . . GAIN ADJUST

Turn all bits ON for binary DAC's (bits 1, 4, 5, 8, 9 and 12 ON for BCD DAC's). Adjust R_2 until op amp output is:

BINARY	BCD
4.9988V for +5V Range	4.9950 for +5V Range
9.9976 for +10V Range	9.9900 for +10V Range

BIPOLAR DAC's

Figure 1b is a typical connection scheme for the AD563 used in bipolar operation.

STEP I . . . OUTPUT RANGE

Determine the output range required. For ±10V F.S., connect the external op amp output to Pin 11 and leave Pin 10 unconnected. For ±5V F.S., connect the external op amp output to Pin 10 and leave Pin 11 unconnected. For ±2.5V F.S., connect the external op amp output to Pin 10 and short Pin 11 to Pin 9.

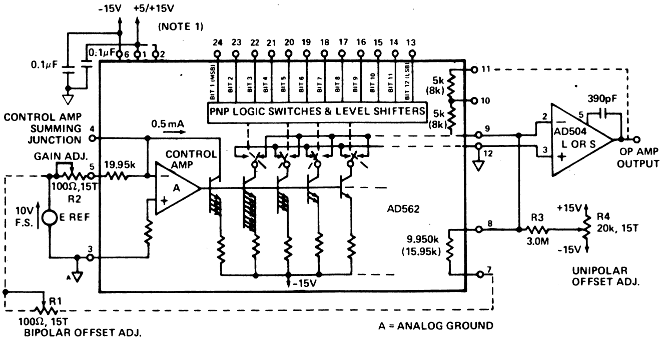
STEP II . . . OFFSET ADJUST

Turn all bits OFF and adjust R_3 until op amp output is:

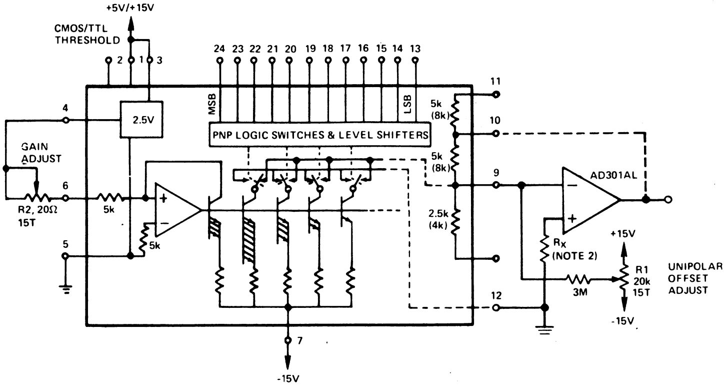
-2.5000V for ±2.5V Range
-5.0000V for ±5V Range
-10.0000V for ±10V Range

STEP III . . . GAIN ADJUST (Bipolar Zero)

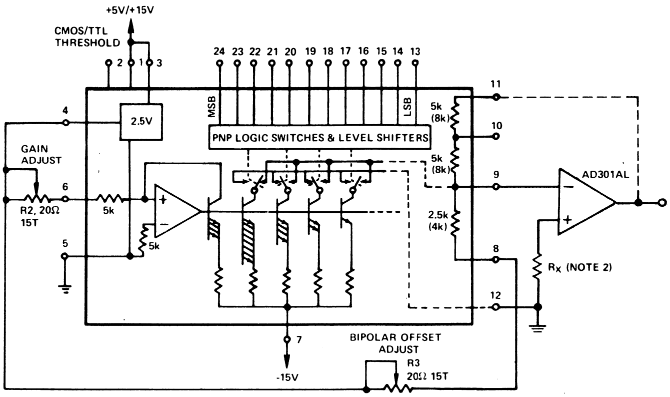
Turn bit 1 ON for Binary DAC's (bits 2 and 4 ON for BCD DAC's). Adjust R_2 until op amp output is 0 volts.



AD562 in Typical Unipolar and Bipolar Connection Scheme



AD563 in Typical Unipolar Connection Scheme



NOTE 1.

A. FOR TTL AND DTL COMPATIBILITY, CONNECT +5 VOLTS TO PIN 1 AND LEAVE PIN 2 OPEN.

B. FOR LOW VOLTAGE CMOS COMPATIBILITY, CONNECT +5 VOLTS TO PIN 1 AND SHORT PIN 2 TO PIN 1.

C. FOR HIGH VOLTAGE CMOS COMPATIBILITY, CONNECT +15 VOLTS TO PIN 1 AND SHORT PIN 2 TO PIN 1.

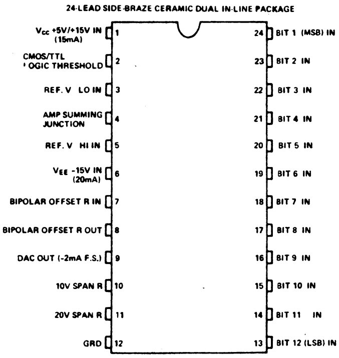
NOTE 2. IN UNIPOLAR OPERATION, R_X SHOULD BE MADE EQUAL TO THE PARALLEL COMBINATION OF THE INTERNAL FEEDBACK RESISTOR AND 6.6k. IN BIPOLAR, R_X EQUALS THE FEEDBACK RESISTOR IN PARALLEL WITH 1.8k.

NOTE 3. RESISTOR VALUES IN PARENTHESES ARE FOR BCD MODEL.

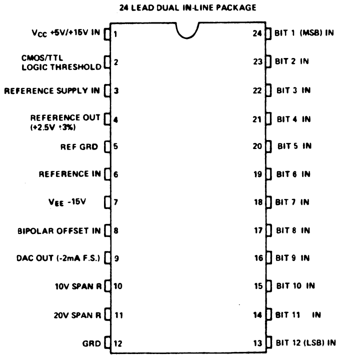
NOTE 4. SUPPLIES MAY BE BYPASSED WITH 0.1μF CAPACITORS.

AD563 in Typical Bipolar Connection Scheme

PIN CONFIGURATIONS
TOP VIEW



AD562



AD563

ORDERING GUIDE

MODEL	INPUT CODE	TEMP. RANGE	ACCURACY @ +25°C	GAIN T.C. (of F.S./°C)	PACKAGE[1] OPTIONS
AD562KD/BIN	Binary	0 to +70°C	±1/2LSB max	3ppm max	D24A
AD562KN/BIN	Binary	0 to +70°C	±1/2LSB max	3ppm max	N24A[2]
AD562KD/BCD	Binary Coded Decimal	0 to +70°C	±1/2LSB max	3ppm max	D24A
AD562KN/BCD	Binary Coded Decimal	0 to +70°C	±1/2LSB max	3ppm max	N24A[2]
AD562AD/BIN	Binary	-25°C to +85°C	±1/2LSBmax	3ppm max	D24A
AD562AD/BCD	Binary Coded Decimal	-25°C to +85°C	±1/2LSB max	3ppm max	D24A
AD562SD/BIN	Binary	-55°C to +125°C	±1/4LSB max	3ppm max	D24A
AD562SD/BCD	Binary Coded Decimal	-55°C to +125°C	±1/10LSB max	3ppm max	D24A
AD563JD/BIN	Binary	0 to +70°C	±1/2LSB max	50ppm max	D24A
AD563JN/BIN	Binary	0 to +70°C	±1/2LSB max	50ppm max	N24A[2]
AD563JD/BCD	Binary Coded Decimal	0 to +70°C	±1/2LSB max	50ppm max	D24A
AD563JN/BCD	Binary Coded Decimal	0 to +70°C	±1/2LSB max	50ppm max	N24A[2]
AD563KD/BIN	Binary	0 to +70°C	±1/4LSB max	20ppm max	D24A
AD563KN/BIN	Binary	0 to +70°C	±1/4LSB max	20ppm max	N24A[2]
AD563KD/BCD	Binary Coded Decimal	0 to +70°C	±1/4LSB max	20ppm max	D24A
AD563KN/BCD	Binary Coded Decimal	0 to +70°C	±1/4LSB max	20ppm max	N24A[2]
AD563SD/BIN	Binary	-55°C to +125°C	±1/4LSB max	30ppm max	D24A
AD563SD/BCD	Binary Coded Decimal	-55°C to +125°C	±1/4LSB max	30ppm max	D24A
AD563TD/BIN	Binary	-55°C to +125°C	±1/4LSB max	10ppm max	D24A
AD563TD/BCD	Binary Coded Decimal	-55°C to +125°C	±1/4LSB max	10ppm max	D24A

[1] See Section 20 for package outline information.
[2] To be available June 1982.

ANALOG DEVICES

Complete High Speed 12-Bit Monolithic D/A Converter

AD565*

FEATURES

Single Chip Construction
Very High Speed: Settles to 1/2LSB in 200ns
Full Scale Switching Time: 30ns
High Stability Buried Zener Reference on Chip
Monotonicity Guaranteed Over Temperature
Linearity Guaranteed Over Temperature: 1/2LSB max (AD565K, T)
Low Power: 225mW Including Reference
Pin-Out Compatible with AD563
Low Cost

PRODUCT DESCRIPTION

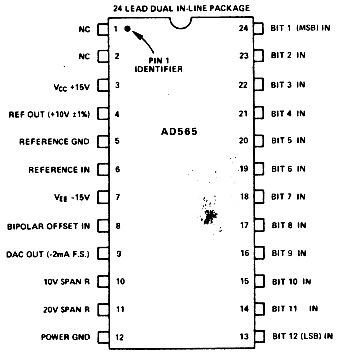
The AD565 is a fast 12-bit digital-to-analog converter combined with a high stability voltage reference on a single monolithic chip. The AD565 chip uses 12 precision, high speed bipolar current steering switches, control amplifier, laser-trimmed thin film resistor network, and buried Zener voltage reference to produce a very fast, high accuracy analog output current.

The combination of performance and flexibility in the AD565 has resulted from major innovations in circuit design, an important new high-speed bipolar process, and continuing advances in laser-wafer-trimming techniques (LWT). The AD565 has a 10 – 90% full scale transition time under 35 nanoseconds and settles to within ±1/2LSB in 200 nanoseconds. AD565 chips are laser-trimmed at the wafer level to ±1/8LSB typical linearity and are specified to ±1/4LSB max error (K and T grades) at +25°C. This high speed and accuracy make the AD565 the ideal choice for high speed display drivers as well as fast analog-to-digital converters.

The subsurface (buried) Zener diode on the chip provides a low-noise voltage reference which has long-term stability and temperature drift characteristics comparable to the best discrete reference diodes. The laser trimming process which provides the excellent linearity is also used to trim both the absolute value of the reference as well as its temperature coefficient. The AD565 is thus well suited for wide temperature range performance with maximum linearity error ±1/2LSB and guaranteed monotonicity over the full temperature range. Typical full scale gain T.C. is 10ppm/°C.

The AD565 is available in four performance grades and two package types. The AD565J and K are specified for use over the 0 to 70°C temperature range and are both available in either a 24-pin, hermetically-sealed, side-brazed ceramic DIP or a 24 pin plastic DIP. The AD565S and T grades are specified for the -55°C to +125°C range and are available in the ceramic package.

AD565 PIN CONFIGURATION



PRODUCT HIGHLIGHTS

1. The AD565 is a self-contained current output DAC and voltage reference fabricated on a single IC chip.
2. The device incorporates a newly developed* fully differential, non-saturating precision current switching cell structure which combines the dc accuracy and stability first developed in the AD562 with very fast switching times and an optimally-damped settling characteristic.
3. The internal buried zener reference is laser-trimmed to 10.00 volts with a ±1% maximum error. The reference voltage is available externally and can supply up to 1.5mA beyond that required for the reference and bipolar offset resistors.
4. The chip also contains SiCr thin film application resistors which can be used either with an external op amp to provide a precision voltage output or as input resistors for a successive approximation A/D converter. The resistors are matched to the internal ladder network to guarantee a low gain temperature coefficient and are laser-trimmed for minimum full scale and bipolar offset errors.
5. The pin-out of the AD565 is compatible with the industry-standard AD563 so that a system can easily be upgraded to higher speed performance without board changes.
6. The single-chip construction makes the AD565 inherently more reliable than hybrid multi-chip designs. The AD565S and T grades with guaranteed linearity and monotonicity over the -55°C to +125°C range are especially recommended for high reliability needs in harsh environments. These units are available processed to MIL-STD-883, Level B.

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*Covered by Patent Nos. 3,803,590; 3,747,088; 4,020,486; RE 28,633; 4,213,806; 4,136,349.

SPECIFICATIONS (T_A = +25°C, V_{CC} = +15V, V_{EE} = -15V, unless otherwise specified)

		AD565J			AD565K		
MODEL	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
DATA INPUTS (Pins 13 to 24)							
TTL or 5 Volt CMOS (T_{min} to T_{max})							
Input Voltage							
Bit ON Logic "1"	+2.0		+5.5	+2.0		+5.5	V
Bit OFF Logic "0"			+0.8			+0.8	V
Logic Current (each bit)							
Bit ON Logic "1"		+120	+300		+120	+300	μA
Bit OFF Logic "0"		+35	+100		+35	+100	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current							
Unipolar (all bits on)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar (all bits on or off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (exclusive of span resistors)	6k	8k	10k	6k	8k	10k	Ω
Offset							
Unipolar		0.01	0.05		0.01	0.05	% of F.S.
Bipolar (50Ω fixed)		0.05	0.15		0.05	0.1	% of F.S.
Capacitance		25			25		pF
Compliance Voltage							
T_{min} to T_{max}	-1.5		+10	-1.5		+10	V
ACCURACY (error relative to full scale) +25°C		±1/4	±1/2		±1/8	±1/4	LSB
		(0.006)	(0.012)		(0.003)	(0.006)	% of F.S.
T_{min} to T_{max}		±1/2	±3/4		±1/4	±1/2	LSB
		(0.012)	(0.018)		(0.006)	(0.012)	% of F.S.
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_{min} to T_{max}		MONOTONICITY GUARANTEED			MONOTONICITY GUARANTEED		
TEMPERATURE COEFFICIENTS							
With Internal Reference							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		15	30		10	20	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2LSB							
All Bits ON-to-OFF or OFF-to-ON		200	400		200	400	ns
FULL SCALE TRANSITION							
10% to 90% Delay plus Rise Time		15	30		15	30	ns
90% to 10% Delay plus Fall Time		30	50		30	50	ns
TEMPERATURE RANGE							
Operating	0		+70	0		+70	°C
Storage (D Package)	-65		+150	-65		+150	°C
Storage (N Package)	-25		+100	-25		+100	°C
POWER REQUIREMENTS							
V_{CC}, +13.5 to +16.5V dc		3	5		3	5	mA
V_{EE}, -13.5 to -16.5V dc		-12	-18		-12	-18	mA
POWER SUPPLY GAIN SENSITIVITY							
V_{CC} = +15V, ±10%		3	10		3	10	ppm of F.S./%
V_{EE} = -15V, ±10%		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT RANGE		0 to +5			0 to +5		V
		-2.5 to +2.5			-2.5 to +2.5		V
		0 to +10			0 to +10		V
		-5 to +5			-5 to +5		V
		-10 to +10			-10 to +10		V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor		±0.1	±0.25		±0.1	±0.25	% of F.S.
Bipolar Zero Error with Fixed 50Ω Resistor		±0.05	±0.15		±0.05	±0.1	% of F.S.
Gain Adjustment Range	±0.25			±0.25			% of F.S.
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S.
REFERENCE INPUT							
Input Impedance	15k	20k	25k	15k	20k	25k	Ω
REFERENCE OUTPUT							
Voltage	9.90	10.00	10.10	9.90	10.00	10.10	V
Current (available for external loads)	1.5	2.5		1.5	2.5		mA
POWER DISSIPATION		225	345		225	345	mW

Specifications subject to change without notice.

	AD565S			AD565T			
MODEL	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
DATA INPUTS (Pins 13 to 24)							
TTL or 5 Volt CMOS (T_{min} to T_{max})							
Input Voltage							
Bit ON Logic "1"	+2.0		+5.5	+2.0		+5.5	V
Bit OFF Logic "0"			+0.8			+0.8	V
Logic Current (each bit)							
Bit ON Logic "1"		+120	+300		+120	+300	μA
Bit OFF Logic "0"		+35	+100		+35	+100	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current							
Unipolar (all bits on)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar (all bits on or off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (exclusive of span resistors)	6k	8k	10k	6k	8k	10k	Ω
Offset							
Unipolar		0.01	0.05		0.01	0.05	% of F.S.
Bipolar (50Ω fixed)		0.05	0.15		0.05	0.1	% of F.S.
Capacitance		25			25		pF
Compliance Voltage							
T_{min} to T_{max}	-1.5		+10	-1.5		+10	V
ACCURACY (error relative to full scale) +25°C		±1/4	±1/2		±1/8	±1/4	LSB
		(0.006)	(0.012)		(0.003)	(0.006)	% of F.S.
T_{min} to T_{max}		±1/2	±3/4		±1/4	±1/2	LSB
		(0.012)	(0.018)		(0.006)	(0.012)	% of F.S.
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_{min} to T_{max}	MONOTONICITY GUARANTEED			MONOTONICITY GUARANTEED			
TEMPERATURE COEFFICIENTS							
With Internal Reference							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		15	30		10	15	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2LSB							
All Bits ON-to-OFF or OFF-to-ON		200	400		200	400	ns
FULL SCALE TRANSITION							
10% to 90% Delay plus Rise Time		15	30		15	30	ns
90% to 10% Delay plus Fall Time		30	50		30	50	ns
TEMPERATURE RANGE							
Operating	-55		+125	-55		+125	°C
Storage (D Package)	-65		+150	-65		+150	°C
POWER REQUIREMENTS							
V_{CC}, +13.5 to +16.5V dc		3	5		3	5	mA
V_{EE}, -13.5 to -16.5V dc		-12	-18		-12	-18	mA
POWER SUPPLY GAIN SENSITIVITY							
V_{CC} = +15V, ±10%		3	10		3	10	ppm of F.S./%
V_{EE} = -15V, ±10%		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT RANGE		0 to +5			0 to +5		V
		-2.5 to +2.5			-2.5 to +2.5		V
		0 to +10			0 to +10		V
		-5 to +5			-5 to +5		V
		-10 to +10			-10 to +10		V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor		±0.1	±0.25		±0.1	±0.25	% of F.S.
Bipolar Zero Error with Fixed 50Ω Resistor		±0.05	±0.15		±0.05	±0.1	% of F.S.
Gain Adjustment Range	±0.25			±0.25			% of F.S.
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S.
REFERENCE INPUT							
Input Impedance	15k	20k	25k	15k	20k	25k	Ω
REFERENCE OUTPUT							
Voltage	9.90	10.00	10.10	9.90	10.00	10.10	V
Current (available for external loads)	1.5	2.5		1.5	2.5		mA
POWER DISSIPATION		225	345		225	345	mW

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

V_{CC} to Power Ground	0V to +18V
V_{EE} to Power Ground	0V to -18V
Voltage on DAC Output (Pin 9)	-3V to +12V
Digital Inputs (Pins 13 to 24) to Power Ground	-1.0V to +7.0V
Ref In to Reference Ground	±12V
Bipolar Offset to Reference Ground	±12V
10V Span R to Reference Ground	±12V
20V Span R to Reference Ground	±24V
Ref Out	Indefinite short to power ground Momentary Short to V_{CC}
Power Dissipation	1000mW

THE AD565 OFFERS TRUE 12-BIT PERFORMANCE OVER THE FULL TEMPERATURE RANGE

ACCURACY: Analog Devices defines accuracy as the maximum deviation of the actual, adjusted DAC output from the ideal analog output (a straight line drawn from 0 to F.S.–1LSB) for any bit combination. The AD565 is laser trimmed to 1/4LSB (0.006% of F.S.) maximum error at +25°C for the K and T Versions–1/2LSB for the J and S.

MONOTONICITY: A DAC is said to be monotonic if the output either increases or remains constant for increasing digital inputs such that the output will always be a non-decreasing function of the input. All versions of the AD565 are monotonic over their full operating temperature range.

DIFFERENTIAL NONLINEARITY: Monotonic behavior requires that the differential linearity error be less than 1LSB both at +25°C and over the temperature range of interest. Differential nonlinearity is the measure of the variation in analog value, normalized to full scale, associated with a 1LSB change in digital input code. For example, for a 10 volt full scale output, a change of 1LSB in digital input code should result in a 2.44mV change in the analog output (1LSB = 10V x 1/4096 = 2.44mV). If in actual use, however, a 1LSB change in the input code results in a change of only 0.61mV (1/4LSB) in analog output, the differential linearity error would be 1.83mV, or 3/4LSB. The AD565K and T have a max differential linearity error of 1/2LSB, which is a tighter specification than to simply guarantee monotonicity.

The differential nonlinearity temperature coefficient must also be considered if the device is to remain monotonic over its full operating temperature range. A differential nonlinearity temperature coefficient of 1.0ppm/°C could under worst case conditions for a temperature change of +25°C to +125°C add 0.01% (100 x 1.0ppm/°C of error). The resulting error could then be as much as 0.01% + 0.006% = 0.016% of F.S. (1/2LSB represents 0.012% of F.S.). To be sure of accurate performance all versions of the AD565 are therefore 100% tested for monotonicity over the full operating temperature range.

AD565 ORDERING GUIDE

MODEL	PACKAGE	TEMP RANGE	LINEARITY ERROR MAX @ 25°C	MAX GAIN T.C. (ppm of F.S./°C)	PACKAGE STYLE[1]
AD565JD/BIN	Ceramic	0 to +70°C	±1/2LSB	30	D24A
AD565KD/BIN	Ceramic	0 to +70°C	±1/4LSB	20	D24A
AD565SD/BIN	Ceramic	-55°C to +125°C	±1/2LSB	30	D24A
AD565SD/BIN/883B	Ceramic	-55°C to +125°C	±1/2LSB	30	D24A
AD565TD/BIN	Ceramic	-55°C to +125°C	±1/4LSB	15	D24A
AD565TD/BIN/883B	Ceramic	-55°C to +125°C	±1/4LSB	15	D24A

[1] See Section 20 for package outline information.

ANALOG DEVICES

Complete High Speed 12-Bit Monolithic D/A Converter

AD565A*

FEATURES

Single Chip Construction
Very High Speed: Settles to 1/2LSB in 250ns max
Full Scale Switching Time: 30ns
High Stability Buried Zener Reference on Chip
Monotonicity Guaranteed Over Temperature
Linearity Guaranteed Over Temperature: 1/2LSB max (AD565AK, T)
Guaranteed for Operation with ±12V Supplies
Low Power: 225mW Including Reference
Pin-Out Compatible with AD563, AD565
Low Cost

PRODUCT DESCRIPTION

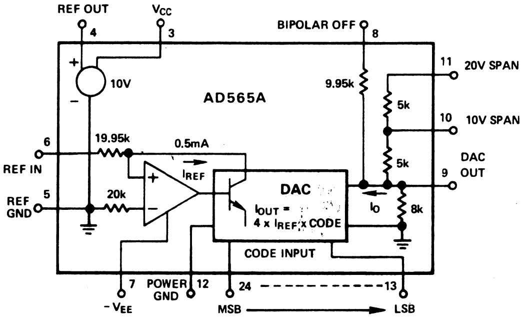
The AD565A is a fast 12-bit digital-to-analog converter combined with a high stability voltage reference on a single monolithic chip. The AD565A chip uses 12 precision, high speed bipolar current steering switches, control amplifier, laser-trimmed thin film resistor network, and buried Zener voltage reference to produce a very fast, high accuracy analog output current.

The combination of performance and flexibility in the AD565A has resulted from major innovations in circuit design, an important new high-speed bipolar process, and continuing advances in laser-wafer-trimming (LWT) techniques. The AD565A has a 10 – 90% full scale transition time under 35 nanoseconds and settles to within ±1/2LSB in 250 nanoseconds max. The AD565A chips are laser-trimmed at the wafer level to ±1/8LSB typical linearity and are specified to ±1/4LSB max error (K and T grades) at +25°C. This high speed and accuracy make the AD565A the ideal choice for high speed display drivers as well as fast analog-to-digital converters.

The subsurface (buried) Zener diode on the chip provides a low-noise voltage reference which has long-term stability and temperature drift characteristics comparable to the best discrete reference diodes. The laser trimming process which provides the excellent linearity is also used to trim both the absolute value of the reference as well as its temperature coefficient. The AD565A is thus well suited for wide temperature range performance with maximum linearity error ±1/2LSB and guaranteed monotonicity over the full temperature range. Typical full scale gain T.C. is 10ppm/°C.

The AD565A is available in four performance grades. The AD565AJ and K are specified for use over 0 to +70°C temperature range and are available in a 24-pin hermetically-sealed, side-brazed ceramic DIP. The AD565AS and T grades are specified for the -55°C to +125°C range and are available in the ceramic package.

AD565A FUNCTIONAL BLOCK DIAGRAM



24-PIN DUAL IN LINE PACKAGE

PRODUCT HIGHLIGHTS

1. The AD565A is a self-contained current output DAC and voltage reference fabricated on a single IC chip.
2. The device incorporates a newly developed, fully differential, non-saturating precision current switching cell structure which combines the dc accuracy and stability first developed in the AD562 with very fast switching times and an optimally-damped settling characteristic.
3. The internal buried zener reference is laser-trimmed to 10.00 volts with a ±1% maximum error. The reference voltage is available externally and can supply up to 1.5mA beyond that required for the reference and bipolar offset resistors.
4. The chip also contains SiCr thin film application resistors which can be used either with an external op amp to provide a precision voltage output or as input resistors for a successive approximation A/D converter. The resistors are matched to the internal ladder network to guarantee a low gain temperature coefficient and are laser-trimmed for minimum full scale and bipolar offset errors.
5. The pin-out of the AD565A is compatible with the industry-standard AD563, AD565 so that a system can easily be upgraded to higher speed performance without board changes.
6. The single-chip construction makes the AD565A inherently more reliable than hybrid multi-chip designs. The AD565AS and T grades with guaranteed linearity and monotonicity over the -55°C to +125°C range are especially recommended for high reliability needs in harsh environments. These units are available processed to MIL-STD-883, Level B.

***Covered by Patent Nos.: 3,803,590; RE 28,633; 4,213,806; 4,136,349.**

SPECIFICATIONS (T_A = +25°C, V_{CC} = +15V, V_{EE} = -15V, unless otherwise specified)

		AD565AJ			AD565AK		
MODEL	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
DATA INPUTS[1] (Pins 13 to 24)							
TTL or 5 Volt CMOS							
Input Voltage							
Bit ON Logic "1"	+2.0		+5.5	+2.0		+5.5	V
Bit OFF Logic "0"			+0.8			+0.8	V
Logic Current (each bit)							
Bit ON Logic "1"		+120	+300		+120	+300	µA
Bit OFF Logic "0"		+35	+100		+35	+100	µA
RESOLUTION			12			12	Bits
OUTPUT							
Current							
Unipolar (all bits on)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar (all bits on or off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (exclusive of span resistors)	6k	8k	10k	6k	8k	10k	Ω
Offset							
Unipolar		0.01	0.05		0.01	0.05	% of F.S.
Bipolar (Figure 3, R_2 = 50Ω fixed)		0.05	0.15		0.05	0.1	% of F.S.
Capacitance		25			25		pF
Compliance Voltage							
T_{min} to T_{max}	-1.5		+10	-1.5		+10	V
ACCURACY (error relative to full scale) +25°C		±1/4	±1/2		±1/8	±1/4	LSB
		(0.006)	(0.012)		(0.003)	(0.006)	% of F.S.
T_{min} to T_{max}		±1/2	±3/4		±1/4	±1/2	LSB
		(0.012)	(0.018)		(0.006)	(0.012)	% of F.S.
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_{min} to T_{max}	MONOTONICITY GUARANTEED			MONOTONICITY GUARANTEED			
TEMPERATURE COEFFICIENTS							
With Internal Reference							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		15	50		10	20	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2LSB							
All Bits ON-to-OFF or OFF-to-ON		150	250		150	250	ns
FULL SCALE TRANSITION							
10% to 90% Delay plus Rise Time		15	30		15	30	ns
90% to 10% Delay plus Fall Time		30	50		30	50	ns
TEMPERATURE RANGE							
Operating	0		+70	0		+70	°C
Storage	-65		+150	-65		+150	°C
POWER REQUIREMENTS							
V_{CC}, +11.4 to +16.5V dc		3	5		3	5	mA
V_{EE}, -11.4 to -16.5V dc		-12	-18		-12	-18	mA
POWER SUPPLY GAIN SENSITIVITY[2]							
V_{CC} = +11.4 to +16.5V dc		3	10		3	10	ppm of F.S./%
V_{EE} = -11.4 to -16.5V dc		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT RANGE (see Figures 2, 3, 4)		0 to +5			0 to +5		V
		-2.5 to +2.5			-2.5 to +2.5		V
		0 to +10			0 to +10		V
		-5 to +5			-5 to +5		V
		-10 to +10			-10 to +10		V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor for R2 (Figure 2)		±0.1	±0.25		±0.1	±0.25	% of F.S.
Bipolar Zero Error with Fixed 50Ω Resistor for R1 (Figure 3)		±0.05	±0.15		±0.05	±0.1	% of F.S.
Gain Adjustment Range (Figure 2)	±0.25			±0.25			% of F.S.
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S.
REFERENCE INPUT							
Input Impedance	15k	20k	25k	15k	20k	25k	Ω
REFERENCE OUTPUT							
Voltage	9.90	10.00	10.10	9.90	10.00	10.10	V
Current (available for external loads)[3]	1.5	2.5		1.5	2.5		mA
POWER DISSIPATION		225	345		225	345	mW

NOTES

[1] The digital inputs are guaranteed but not tested over the operating temperature range.

[2] The power supply gain sensitivity is tested in reference to a V_{CC}, V_{EE} of ±15V dc.

[3] For operation at elevated temperatures the reference cannot supply current for external loads. It, therefore, should be buffered if additional loads are to be supplied.

Specifications subject to change without notice.

	AD565AS			AD565AT			
MODEL	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
DATA INPUTS[1] (Pins 13 to 24)							
TTL or 5 Volt CMOS							
Input Voltage							
Bit ON Logic "1"	+2.0		+5.5	+2.0		+5.5	V
Bit OFF Logic "0"			+0.8			+0.8	V
Logic Current (each bit)							
Bit ON Logic "1"		+120	+300		+120	+300	μA
Bit OFF Logic "0"		+35	+100		+35	+100	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current							
Unipolar (all bits on)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar (all bits on or off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (exclusive of span resistors)	6k	8k	10k	6k	8k	10k	Ω
Offset							
Unipolar		0.01	0.05		0.01	0.05	% of F.S.
Bipolar (Figure 3, R_2 = 50Ω fixed)		0.05	0.15		0.05	0.1	% of F.S.
Capacitance		25			25		pF
Compliance Voltage							
T_{min} to T_{max}	-1.5		+10	-1.5		+10	V
ACCURACY (error relative to full scale) +25°C		±1/4	±1/2		±1/8	±1/4	LSB
		(0.006)	(0.012)		(0.003)	(0.006)	% of F.S.
T_{min} to T_{max}		±1/2	±3/4		±1/4	±1/2	LSB
		(0.012)	(0.018)		(0.006)	(0.012)	% of F.S.
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_{min} to T_{max}	MONOTONICITY GUARANTEED			MONOTONICITY GUARANTEED			
TEMPERATURE COEFFICIENTS							
With Internal Reference							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		15	30		10	15	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2LSB							
All Bits ON-to-OFF or OFF-to-ON		150	250		150	250	ns
FULL SCALE TRANSITION							
10% to 90% Delay plus Rise Time		15	30		15	30	ns
90% to 10% Delay plus Fall Time		30	50		30	50	ns
TEMPERATURE RANGE							
Operating	-55		+125	-55		+125	°C
Storage	-65		+150	-65		+150	°C
POWER REQUIREMENTS							
V_{CC}, +11.4 to +16.5V dc		3	5		3	5	mA
V_{EE}, -11.4 to -16.5V dc		-12	-18		-12	-18	mA
POWER SUPPLY GAIN SENSITIVITY[2]							
V_{CC} = +11.4 to +16.5V dc		3	10		3	10	ppm of F.S./%
V_{EE} = -11.4 to -16.5V dc		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT RANGES (see Figures 2, 3, 4)		0 to +5			0 to +5		V
		-2.5 to +2.5			-2.5 to +2.5		V
		0 to +10			0 to +10		V
		-5 to +5			-5 to +5		V
		-10 to +10			-10 to +10		V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor for R2 (Figure 2)		±0.1	±0.25		±0.1	±0.25	% of F.S.
Bipolar Zero Error with Fixed 50Ω Resistor for R1 (Figure 3)		±0.05	±0.15		±0.05	±0.1	% of F.S.
Gain Adjustment Range (Figure 2)	±0.25			±0.25			% of F.S.
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S.
REFERENCE INPUT							
Input Impedance	15k	20k	25k	15k	20k	25k	Ω
REFERENCE OUTPUT							
Voltage	9.90	10.00	10.10	9.90	10.00	10.10	V
Current (available for external loads)[3]	1.5	2.5		1.5	2.5		mA
POWER DISSIPATION		225	345		225	345	mW

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

V_{CC} to Power Ground	0V to +18V
V_{EE} to Power Ground	0V to -18V
Voltage on DAC Output (Pin 9)	-3V to +12V
Digital Inputs (Pins 13 to 24) to Power Ground	-1.0V to +7.0V
Ref In to Reference Ground	±12V
Bipolar Offset to Reference Ground	±12V
10V Span R to Reference Ground	±12V
20V Span R to Reference Ground	±24V
Ref Out	Indefinite short to power ground Momentary Short to V_{CC}
Power Dissipation	1000mW

THE AD565A OFFERS TRUE 12-BIT PERFORMANCE OVER THE FULL TEMPERATURE RANGE

ACCURACY: Analog Devices defines accuracy as the maximum deviation of the actual, adjusted DAC output (see next page) from the ideal analog output (a straight line drawn from 0 to F.S. – 1LSB) for any bit combination. The AD565A is laser trimmed to 1/4LSB (0.006% of F.S.) maximum error at +25°C for the K and T Versions—1/2LSB for the J and S.

MONOTONICITY: A DAC is said to be monotonic if the output either increases or remains constant for increasing digital inputs such that the output will always be a non-decreasing function of the input. All versions of the AD565A are monotonic over their full operating temperature range.

DIFFERENTIAL NONLINEARITY: Monotonic behavior requires that the differential linearity error be less than 1LSB both at +25°C and over the temperature range of interest. Differential nonlinearity is the measure of the variation in analog value, normalized to full scale, associated with a 1LSB change in digital input code. For example, for a 10 volt full scale output, a change of 1LSB in digital input code should result in a 2.44mV change in the analog output (1LSB = 10V x 1/4096 = 2.44mV). If in actual use, however, a 1LSB change in the input code results in a change of only 0.61mV (1/4LSB) in analog output, the differential linearity error would be 1.83mV, or 3/4LSB. The AD565AK and T have a max differential linearity error of 1/2LSB, which is a tighter specification than to simply guarantee monotonicity.

The differential nonlinearity temperature coefficient must also be considered if the device is to remain monotonic over its full operating temperature range. A differential nonlinearity temperature coefficient of 1.0ppm/°C could under worst case conditions for a temperature change of +25°C to +125°C add 0.01% (100 x 1.0ppm/°C of error). The resulting error could then be as much as 0.01% + 0.006% = 0.016% of F.S. (1/2LSB represents 0.012% of F.S.). To be sure of accurate performance all versions of the AD565A are therefore 100% tested for monotonicity over the full operating temperature range.

AD565A ORDERING GUIDE

MODEL	PACKAGE	TEMP RANGE	LINEARITY ERROR MAX @ 25°C	MAX GAIN T.C. (ppm of F.S./°C)	Package Style[1]
AD565AJN/BIN	Plastic	0 to +70°C	±1/2LSB	50	N24A
AD565AJD/BIN	Ceramic	0 to +70°C	±1/2LSB	50	D24A
AD565AKN/BIN	Plastic	0 to +70°C	±1/4LSB	20	N24A
AD565AKD/BIN	Ceramic	0 to +70°C	±1/4LSB	20	D24A
AD565ASD/BIN	Ceramic	-55°C to +125°C	±1/2LSB	30	D24A
AD565ASD/BIN/883B	Ceramic	-55°C to +125°C	±1/2LSB	30	D24A
AD565ATD/BIN	Ceramic	-55°C to +125°C	±1/4LSB	15	D24A
AD565ATD/BIN/883B	Ceramic	-55°C to +125°C	±1/4LSB	15	D24A

[1] See Section 20 for package outline information.

CONNECTING THE AD565A FOR BUFFERED VOLTAGE OUTPUT

The standard current-to-voltage conversion connections using an operational amplifier are shown here with the preferred trimming techniques. If a low offset operational amplifier (AD510L, AD517L, AD741L, AD301AL, AD OP-07) is used, excellent performance can be obtained in many situations without trimming (an op amp with less than 0.5mV max offset voltage should be used to keep offset errors below 1/2LSB). If a 50Ω fixed resistor is substituted for the 100Ω trimmer, unipolar zero will typically be within ±1/2LSB (plus op amp offset), and full scale accuracy will be within 0.1% (0.25% max). Substituting a 50Ω resistor for the 100Ω bipolar offset trimmer will give a bipolar zero error typically within ±2LSB (0.05%).

The AD509 is recommended for buffered voltage-output applications which require a settling time to ±1/2LSB of one microsecond. The feedback capacitor is shown with the optimum value for each application; this capacitor is required to compensate for the 25 picofarad DAC output capacitance.

FIGURE 2. UNIPOLAR CONFIGURATION

This configuration will provide a unipolar 0 to +10 volt output range. In this mode, the bipolar terminal, pin 8, should be grounded if not used for trimming.

STEP I . . . ZERO ADJUST

Turn all bits OFF and adjust zero trimmer R1, until the output reads 0.000 volts (1LSB = 2.44mV). In most cases this trim is not needed, but pin 8 should then be connected to pin 12.

STEP II . . . GAIN ADJUST

Turn all bits ON and adjust 100Ω gain trimmer R2, until the output is 9.9976 volts. (Full scale is adjusted to 1LSB less than nominal full scale of 10.000 volts.) If a 10.2375V full scale is desired (exactly 2.5mV/bit), insert a 120Ω resistor in series with the gain resistor at pin 10 to the op amp output.

FIGURE 3. BIPOLAR CONFIGURATION

This configuration will provide a bipolar output voltage from -5.000 to +4.9976 volts, with positive full scale occurring with all bits ON (all 1's).

STEP I . . . OFFSET ADJUST

Turn OFF all bits. Adjust 100Ω trimmer R1 to give -5.000 volts output.

STEP II . . . GAIN ADJUST

Turn ON All bits. Adjust 100Ω gain trimmer R2 to give a reading of +4.9976 volts.

Please note that it is not necessary to trim the op amp to obtain full accuracy at room temperature. In most bipolar situations, an op amp trim is unnecessary unless the untrimmed offset drift of the op amp is excessive.

FIGURE 4. OTHER VOLTAGE RANGES

The AD565A can also be easily configured for a unipolar 0 to +5 volt range or ±2.5 volt and ±10 volt bipolar ranges by using the additional 5k application resistor provided at the 20 volt span R terminal, pin 11. For a 5 volt span (0 to +5 or ±2.5), the two 5k resistors are used in parallel by shorting pin 11 to pin 9 and connecting pin 10 to the op amp output and the bipolar offset either to ground for unipolar or to REF OUT for the bipolar range. For the ±10 volt range (20 volt span) use the 5k resistors in series by connecting only pin 11 to the op amp output and the bipolar offset connected as shown. The ±10 volt option is shown in Figure 4.

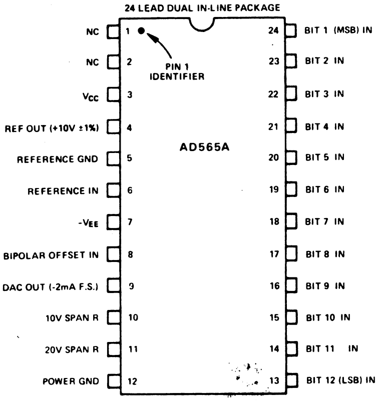


Figure 1.

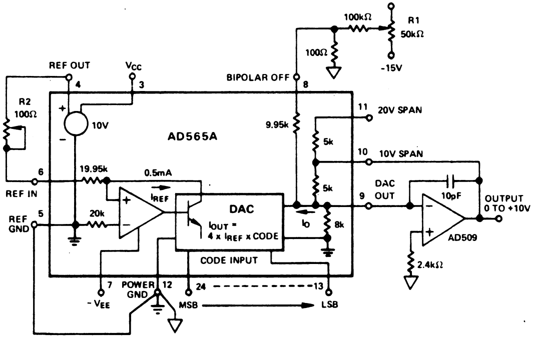


Figure 2. 0 to +10V Unipolar Voltage Output

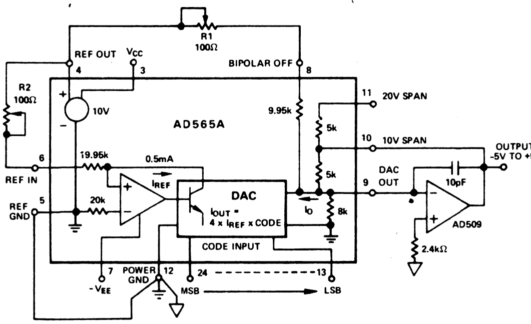


Figure 3. ±5V Bipolar Voltage Output

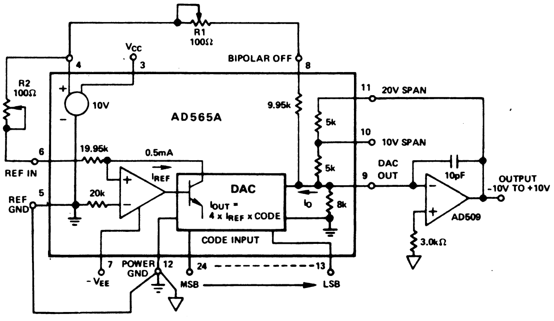


Figure 4. ±10V Voltage Output

INTERNAL/EXTERNAL REFERENCE USE

The AD565A has an internal low-noise buried zener diode reference which is trimmed for absolute accuracy and temperature coefficient. This reference is buffered and optimized for use in a high speed DAC and will give long-term stability equal or superior to the best discrete zener reference diodes. The performance of the AD565A is specified with the internal reference driving the DAC since all trimming and testing (especially for full scale and bipolar) is done in this configuration.

The AD565A can be used with an external reference, but may not have sufficient trim range to accommodate a reference which does not match the internal reference. For external reference applications, the AD566A series is recommended.

The internal reference has sufficient buffering to drive external circuitry in addition to the reference currents required for the DAC (typically 0.5mA to Ref In and 1.0mA to Bipolar Offset, if used). A minimum of 1.5mA is available for driving external circuits. For use over the extended temperature range, however, a buffer should be used to preserve the accuracy. The reference is typically trimmed to ±0.2%, then tested and guaranteed to ±1.0% max error. The temperature coefficient is comparable to that of the full scale TC for a particular grade.

DIGITAL INPUT CONSIDERATIONS

The AD565A uses a standard positive true straight binary code for unipolar outputs (all 1's give full scale output), and an offset binary code for bipolar output ranges. In the bipolar mode, with all 0's on the inputs, the output will go to negative full scale; with 100. . . 00 (only the MSB on), the output will be 0.00 volts; with all 1's, the output will go to positive full scale.

The threshold of the digital input circuitry is set at 1.4 volts and does not vary with supply voltage. The input lines can interface with any type of 5 volt logic, TTL/DTL or CMOS, and have sufficiently low input currents to interface easily with unbuffered CMOS logic. The configuration of the input circuit is shown in Figure 5. The input line can be modeled as a 30kΩ resistance connected to a –0.7V rail.

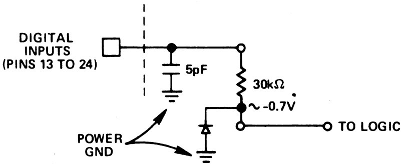


Figure 5. Equivalent Digital Input Circuit

GROUNDING RULES

The AD565A brings out separate reference and power grounds to allow optimum connections for low noise and high speed performance. These grounds should be tied together at one point, usually the device power ground. The separate ground returns are provided to minimize current flow in low-level signal paths. In this way, logic return currents are not summed into the same return path with analog signals.

The reference ground at pin 5 is the ground point for the internal reference and is thus the "high quality" ground for the AD565A; it should be connected directly to the analog reference point of the system. The power ground at pin 12 can be connected to the most convenient ground point; analog power return is preferred. If power ground contains high frequency noise beyond 200mV, this noise may feed through the converter, thus some caution will be required in applying these grounds.

OUTPUT VOLTAGE COMPLIANCE

The AD565A has a typical output compliance range from –2 to +10 volts. The current-steering output stages will be unaffected by changes in the output terminal voltage over that range. However, there is an equivalent output impedance of 8k in parallel with 25pF at the output terminal which produces an equivalent error current if the voltage deviates from analog common. This is a linear effect which does not change with input code. Operation beyond the compliance limits may cause either output stage saturation or breakdown which results in nonlinear performance. Compliance limits are not affected by the positive power supply, but are a function of output current and negative supply, as shown in Figure 6.

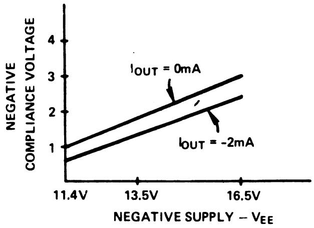


Figure 6. Typical Negative Compliance Range vs. Negative Supply

SETTLING TIME

The high speed NPN current steering switching cell and internally compensated reference amplifier of the AD565A are specifically designed for fast settling operation. The typical settling time to ±0.01% (1/2LSB) for the worst case transition (major carry or full scale step) is about 200ns; the lower order bits all settle in less than 200ns. (Worst case settling occurs when all bits are switched, especially the MSB).

The excellent high speed performance of the AD565A is demonstrated in these oscilloscope photographs. The measurements are made with the AD565A driving directly into an equivalent 50Ω load, and amplified with a low capacitance MOS-input, UHF amplifier. Both figures show the worst case situation, which is full scale transition from switching all bits ON to OFF.

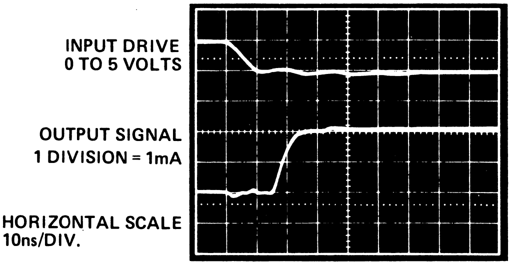


Figure 7. Full Scale Transition

The full transition characteristic is shown in Figure 7. There is about a 6-8ns delay, followed by a 10ns rise time and minimal overshoot. The transition in the other direction shows approximately a 20ns delay prior to a 10ns rise time. The slewing characteristics for smaller transitions show a similar characteristic.

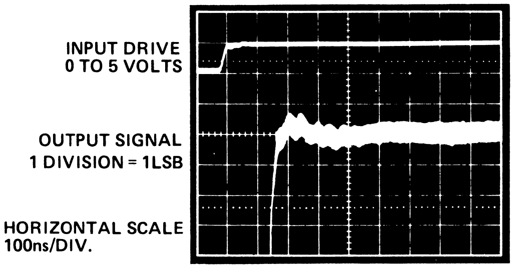


Figure 8. Settling Characteristic Detail

The fine detail of the full scale settling characteristic is shown in Figure 8. The equipment and circuitry used to make the measurements adds about 50ns to the actual device performance. The final portion of the signal slews to within 10LSB's in less than 150ns, reaches and stays within 1/2LSB in about 200ns, and shows less than 1/2LSB overshoot. The characteristic is completely settled out in less than 250ns.

HIGH SPEED SYSTEM DESIGN

Full realization of this high speed performance requires strict attention to detail by the user in all areas of application and testing.

The settling time for the AD565A is specified in terms of the current output, an inherently high speed DAC operating mode. However, most DAC applications require a current-to-voltage conversion at some point in the signal path, although an unbuffered voltage level (not using an op amp) is suitable for use in a successive-approximation A/D converter (see the next page), or in many display applications. This form of current-to-voltage conversion can give very fast operation if proper design and layout is done. The fastest voltage conversion is achieved by connecting a low value resistor directly to the output, as shown in Figure 9. In this case, the settling time is primarily determined by the cell switching time and by the RC time constant of the AD565A output capacitance of 25 picofarads (plus stray capacitance) combined with the output resistor value. Settling to 0.01% of full scale (for a full scale transition) requires 9 time constants. This effect is important for an equivalent resistance over 1kΩ.

If an op amp must be used to provide a low impedance output signal, some loss in settling time will be seen due to op amp dynamics. The normal current-to-voltage converter op amp circuits are shown in the applications circuits using the fast settling AD509. The circuits shown settle to ±1/2LSB in 1μs unipolar or bipolar. The DAC output capacitance, which acts as a stray capacitance at the op amp inverting input, must be compensated by a feedback capacitor, as shown. The value should be chosen carefully for each application and each op amp type.

Fastest operation will be obtained by minimizing lead lengths, stray capacitance and impedance levels. Both supplies should be bypassed near the devices: 0.1μF will be sufficient since the AD565A runs at constant supply current regardless of input code.

DIRECT UNBUFFERED VOLTAGE OUTPUT FOR CABLE DRIVING

The wide compliance range allows direct current-to-voltage conversion with just an output resistor. Figure 9 shows a connection using the gain and bipolar output resistors to give a ±1.60 volt bipolar swing. In this situation, the digital code is complementary binary. Other combinations of internal and external output resistors (R_X) can be used to scale to alternate voltage ranges, simply by appropriately scaling the 0 to -2mA unipolar output current and using the 10.0 volt reference voltage for bipolar offset. For example, setting R_X = 2.67kΩ gives a ±1 volt range with a 1kΩ equivalent output impedance.

This connection is especially useful for directly driving a long cable at high speed. Using a 50Ω resistor for R_X would allow interface to a 50Ω cable with a ±50mV full scale swing. Settling time would be very fast, as discussed in the section above.

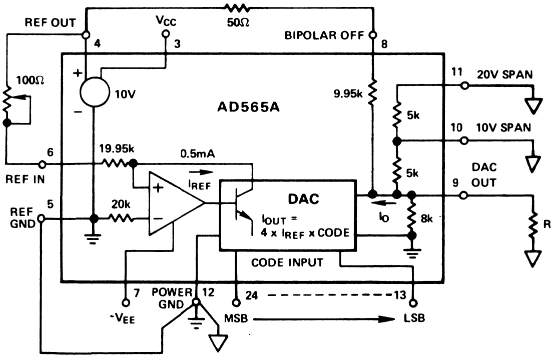


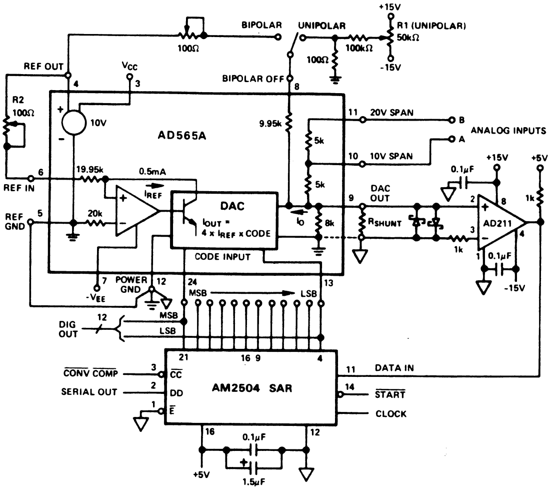
Figure 9. Unbuffered Bipolar Voltage Output

HIGH SPEED 12-BIT A/D CONVERTERS

The fast settling characteristics of the AD565A make it ideal for high speed successive approximation A/D converters. The internal reference and trimmed application resistors allow a 12-bit converter system to be constructed with a minimum parts count. Shown in Figure 10 is a configuration using standard components; this system completes a full 12-bit conversion in 10µs unipolar or bipolar. This converter will be accurate to ±1/2LSB of 12 bits and have a typical gain T.C. of 10ppm/°C.

In the unipolar mode, the system range is 0 to 9.9976 volts, with each bit having a value of 2.44mV. For true conversion accuracy, an A/D converter should be trimmed so that a given bit code output results from input levels from 1/2LSB below to 1/2LSB above the exact voltage which that code represents. Therefore, the converter zero point should be trimmed with an input voltage of +1.22mV; trim R1 until the LSB just begins to appear in the output code (all other bits "0"). For full scale, use an input voltage of +9.9963 volts (10 volts – 1LSB – 1/2LSB); then trim R2 until the LSB just begins to appear (all other bits "1").

The bipolar signal range is -5.0 to +4.9976 volts. Bipolar offset trimming is done by applying a -4.9988V input signal and trimming R1 for the LSB transition (all other bits "0").



INPUT RANGES

Unipolar	Bipolar	Connect	Equiv DAC Z_{OUT}
0 TO +10	±5	INPUT TO A	2.35kΩ
0 TO +5	±2.5	INPUT TO A	1.90kΩ
0 TO +20	±10	INPUT TO B B TO DAC OUT	3.08kΩ

Figure 10. Fast Precision Analog to Digital Converter

Full scale is set by applying +4.9963 volts and trimming R2 for the LSB transition (all other bits "1"). In many applications, the pretrimmed application resistors are sufficiently accurate that external trimmers will be unnecessary, especially in situations requiring less than full 12-bit ±1/2LSB accuracy.

For fastest operation, the impedance at the comparator summing node must be minimized, as mentioned in the section on settling time. However, lowering the impedance will reduce the voltage signal to the comparator (at an equivalent impedance at the summing node of 1kΩ, 1LSB = 0.5mV), to the point that comparator performance will be sacrificed. The contribution to this impedance from the DAC will vary with the input configuration, as shown in the input range table.

To prevent dynamic errors, the input signal should have a low dynamic source impedance, such as that of the AD509 high speed op amp.

HIGH-RESOLUTION CIRCUITS

Sixteen-bit resolution digital-to-analog converters can be built by cascading an AD565A 12-bit DAC with an AD559 or AD1408 8-bit DAC. This technique can be used either to provide a 16-bit binary DAC or a 4-digit BCD DAC. By using an AD565AK with ±1/8LSB typical linearity to 12 bits, the total circuit will typically achieve ±1/2LSB accuracy for 14 binary bits, and ±1/2 least significant digit to 4 digits BCD. The binary configuration is shown in Figure 11. The AD559, with its thin film ladder netowrk similar to the AD565A, is prefered for good performance over temperature.

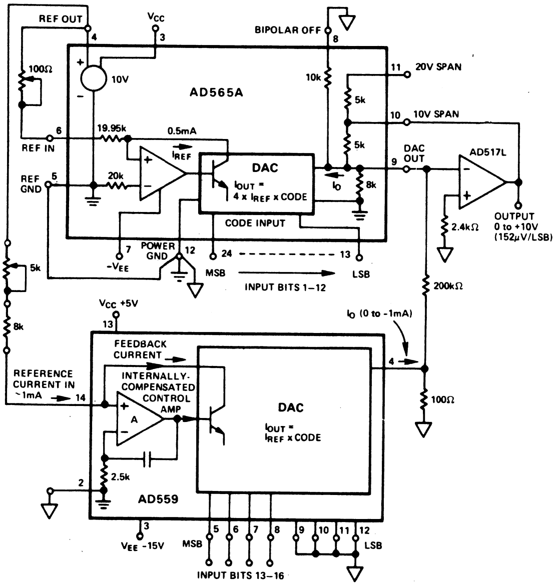


Figure 11. 16-Bit Binary DAC

COMPLEMENTARY BINARY CODE CIRCUITS

The AD565A can be used in circuits where only a complementary binary code is available. This is done by connecting the 10 volt span resistor to the 10 volt reference and connecting the DAC output to a noninverting amplifier as shown in Figure 12. The 8kΩ DAC output impedance and the 5kΩ span resistor will form a divider which will give a full scale output voltage (with all bits off) to the amplifier of about 6.15 volts. To obtain a 10 volt full scale, the amplifier is shown with a gain network back to the inverting input.

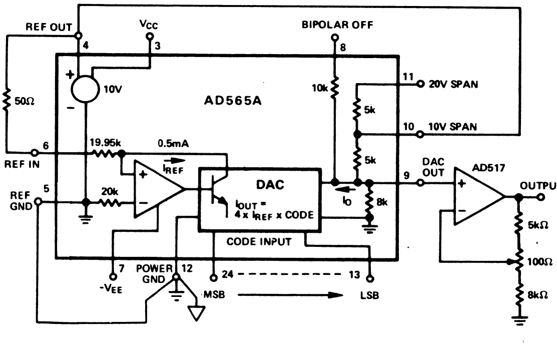


Figure 12. Complementary Output DAC

ANALOG DEVICES

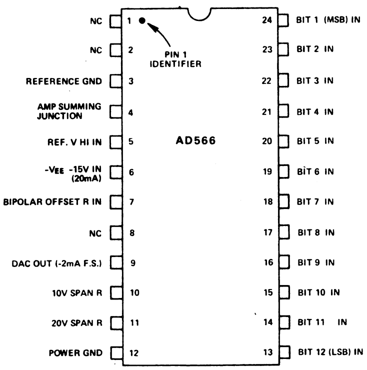
Low Cost High Speed 12-Bit Monolithic D/A Converter

AD566*

FEATURES

Single Chip Construction
Very High Speed: Settles to 1/2LSB in 200ns
Full Scale Switching Time: 30ns
Single Supply Operation
Monotonicity Guaranteed Over Temperature
Linearity Guaranteed Over Temperature: 1/2LSB max (AD566K, T)
Low Power: 180mW
Pin-Out Compatible with AD562
Low Cost

AD566 PIN CONFIGURATION



24-PIN DUAL IN LINE PACKAGE

PRODUCT DESCRIPTION

The AD566 is a fast 12-bit digital-to-analog converter which incorporates the latest advances in analog circuit design into a low power monolithic chip.

The AD566 chip uses 12 precision, high speed bipolar current steering switches, control amplifier and a laser-trimmed thin film resistor network to produce a very fast, high accuracy analog output current.

The combination of performance and flexibility in the AD566 has resulted from major innovations in circuit design, an important new high-speed bipolar process, and continuing advances in laser-wafer-trimming techniques (LWT). The AD566 has a 10–90% full scale transition time less than 35 nanoseconds and settles to within ±1/2LSB in 200 nanoseconds. AD566 chips are laser-trimmed at the wafer level to ±1/8LSB typical linearity and are specified to ±1/4LSB max error (K and T grades) at +25°C. High speed and accuracy make the AD566 the ideal choice for high speed display drivers as well as fast analog-to-digital converters.

The AD566 is available in four performance grades and two package types. The AD566J and K are specified for use over the 0 to +70°C temperature range and are available in either a 24-pin, hermetically-sealed, side-brazed ceramic DIP, or a 24-pin plastic DIP. The AD566S and T grades are specified for the -55°C to +125°C range and are available in the ceramic package.

PRODUCT HIGHLIGHTS

1. The combination of single supply operation with wide output compliance range is idealy suited for fast, low noise, accurate voltage output configurations without an output amplifier.
2. The device incorporates a newly developed, full differential, nonsaturating precision current switching cell structure which combines the dc accuracy and stability first developed in the AD562 with very fast switching times and an optimally-damped settling characteristic.
3. The chip also contains SiCr thin film application resistors which can be used with an external op amp to provide a precision voltage output or as input resistors for a successive approximation A/D converter. The resistors are matched to the internal ladder network to guarantee a low gain temperature coefficient and are laser-trimmed for minimum full scale and bipolar offset errors.
4. The pin-out of the AD566 is compatible with the industry-standard AD562 so that a system can easily be upgraded to provide higher speed performance.
5. The single-chip construction makes the AD566 inherently more reliable than hybrid multi-chip designs. The AD566S and T grades, with guaranteed linearity and monotonicity over the -55°C to +125°C range, are especially recommended for high reliability needs in harsh environments. These units are available processed to MIL-STD-883, Level B.

***Covered by patent numbers: 3,803,590; 4,020,486; 3,747,088; RE28,633.**

SPECIFICATIONS (T_A = +25°C, V_{EE} = -15V, unless otherwise specified)

	AD566J			AD566K			
MODEL	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
DATA INPUTS (Pins 13 to 24)							
TTL or 5 Volt CMOS (T_{min} to T_{max})							
Input Voltage							
Bit ON Logic "1"	+2.0		+5.5	+2.0		+5.5	V
Bit OFF Logic "0"	0		+0.8	0		+0.8	V
Logic Current (each bit)							
Bit ON Logic "1"		+120	+300		+120	+300	μA
Bit OFF Logic "0"		+35	+100		+35	+100	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current							
Unipolar (all bits on)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar (all bits on or off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (exclusive of span resistors)	6k	8k	10k	6k	8k	10k	Ω
Offset							
Unipolar (adjustable to zero)[1]		0.01	0.05		0.01	0.05	% of F.S.
Bipolar (R_1 and R_2 = 50Ω fixed)[1]		0.05	0.15		0.05	0.1	% of F.S.
Capacitance		25			25		pF
Compliance Voltage							
T_{min} to T_{max}	-1.5		+10	-1.5		+10	V
ACCURACY (error relative to full scale) +25°C		±1/4	±1/2		±1/8	±1/4	LSB
		(0.006)	(0.012)		(0.003)	(0.006)	% of F.S.
T_{min} to T_{max}		±1/2	±3/4		±1/4	±1/2	LSB
		(0.012)	(0.018)		(0.006)	(0.012)	% of F.S.
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_{min} to T_{max}	MONOTONICITY GUARANTEED			MONOTONICITY GUARANTEED			
TEMPERATURE COEFFICIENTS							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		7	10		2	3	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2LSB							
All Bits ON-to-OFF or OFF-to-ON		200	400		200	400	ns
FULL SCALE TRANSITION							
10% to 90% Delay plus Rise Time		15	30		15	30	ns
90% to 10% Delay plus Fall Time		30	50		30	50	ns
POWER REQUIREMENTS							
V_{EE}, -13.5 to -16.5V dc		-12	-20		-12	-20	mA
POWER SUPPLY GAIN SENSITIVITY							
V_{EE} = -15V, ±10%		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT RANGE[1]		0 to +5			0 to +5		V
		-2.5 to +2.5			-2.5 to +2.5		V
		0 to +10			0 to +10		V
		-5 to +5			-5 to +5		V
		-10 to +10			-10 to +10		V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor for R2[1]		±0.1	±0.25		±0.1	±0.25	% of F.S.
Bipolar Zero Error with Fixed 50Ω Resistor for R1[1]		±0.05	±0.15		±0.05	±0.1	% of F.S.
Gain Adjustment Range[1]	±0.25			±0.25			% of F.S.
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S.
REFERENCE INPUT							
Input Impedance	15k	20k	25k	15k	20k	25k	Ω
POWER DISSIPATION		180	300		180	300	mW
MULTIPLYING MODE PERFORMANCE (All Models)							
Quadrants		Two (2): Bipolar Operation at Digital Input Only					
Reference Voltage		+1V to +10V, Unipolar					
Accuracy		10 Bits (±0.05% of Reduced F.S.) for 1V dc Reference Voltage					
Reference Feedthrough (unipolar mode, all bits OFF, and 1V to +10V [p-p] sinewave frequency for 1/2LSB [p-p] feedthrough)		40kHz typ					
Output Slew Rate 10%-90%		5mA/μs					
90%-10%		1mA/μs					
Output Settling Time (all bits on and a 0–10V step change in reference voltage)		1.5μs to 0.01% F.S.					
CONTROL AMPLIFIER							
Full Power Bandwidth		300kHz					
Small-Signal Closed-Loop Bandwidth		1.8MHz					

Specifications subject to change without notice.

[1] See AD566A data sheet for complete information.

		AD566S			AD566T		
MODEL	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
DATA INPUTS (Pins 13 to 24)							
TTL or 5 Volt CMOS (T_{min} to T_{max})							
Input Voltage							
Bit ON Logic "1"	+2.0		+5.5	+2.0		+5.5	V
Bit OFF Logic "0"	0		+0.8	0		+0.8	V
Logic Current (each bit)							
Bit ON Logic "1"		+120	+300		+120	+300	μA
Bit OFF Logic "0"		+35	+100		+35	+100	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current							
Unipolar (all bits on)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar (all bits on or off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (exclusive of span resistors)	6k	8k	10k	6k	8k	10k	Ω
Offset							
Unipolar (adjustable to zero)[1]		0.01	0.05		0.01	0.05	% of F.S.
Bipolar (R_1 and R_2 = 50Ω fixed)[1]		0.05	0.15		0.05	0.1	% of F.S.
Capacitance		25			25		pF
Compliance Voltage							
T_{min} to T_{max}	-1.5		+10	-1.5		+10	V
ACCURACY (error relative to full scale) +25°C		±1/4	±1/2		±1/8	±1/4	LSB
		(0.006)	(0.012)		(0.003)	(0.006)	% of F.S.
T_{min} to T_{max}		±1/2	±3/4		±1/4	±1/2	LSB
		(0.012)	(0.018)		(0.006)	(0.012)	% of F.S.
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_{min} to T_{max}	MONOTONICITY GUARANTEED			MONOTONICITY GUARANTEED			
TEMPERATURE COEFFICIENTS							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		7	10		2	3	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2LSB							
All Bits ON-to-OFF or OFF-to-ON		200	400		200	400	ns
FULL SCALE TRANSITION							
10% to 90% Delay plus Rise Time		15	30		15	30	ns
90% to 10% Delay plus Fall Time		30	50		30	50	ns
POWER REQUIREMENTS							
V_{EE}, -13.5 to -16.5V dc		-12	-20		-12	-20	mA
POWER SUPPLY GAIN SENSITIVITY							
V_{EE} = -15V, ±10%		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT RANGE[1]		0 to +5			0 to +5		V
		-2.5 to +2.5			-2.5 to +2.5		V
		0 to +10			0 to +10		V
		-5 to +5			-5 to +5		V
		-10 to +10			-10 to +10		V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor for R2[1]		±0.1	±0.25		±0.1	±0.25	% of F.S.
Bipolar Zero Error with Fixed 50Ω Resistor for R1[1]		±0.05	±0.15		±0.05	±0.1	% of F.S.
Gain Adjustment Range[1]	±0.25			±0.25			% of F.S.
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S.
REFERENCE INPUT							
Input Impedance	15k	20k	25k	15k	20k	25k	Ω
POWER DISSIPATION		180	300		180	300	mW
MULTIPLYING MODE PERFORMANCE (All Models)							
Quadrants		Two (2): Bipolar Operation at Digital Input Only					
Reference Voltage		+1V to +10V, Unipolar					
Accuracy		10 Bits (±0.05% of Reduced F.S.) for 1V dc Reference Voltage					
Reference Feedthrough (unipolar mode, all bits OFF, and 1V to +10V [p-p] sinewave frequency for 1/2LSB [p-p] feedthrough)		40kHz typ					
Output Slew Rate 10%-90%		5mA/μs					
90%-10%		1mA/μs					
Output Settling Time (all bits on and a 0–10V step change in reference voltage)		1.5μs to 0.01% F.S.					
CONTROL AMPLIFIER							
Full Power Bandwidth		300kHz					
Small-Signal Closed-Loop Bandwidth		1.8MHz					

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

V_{EE} to Power Ground . . . . 0V to −18V
Voltage on DAC Output (Pin 9) . . . . −3V to +12V
Digital Inputs (Pins 13 to 24) to Power Ground . . . . −1.0V to +7.0V
Ref In to Reference Ground . . . . ±12V
Bipolar Offset to Reference Ground . . . . ±12V
10V Span R to Reference Ground . . . . ±12V
20V Span R to Reference Ground . . . . ±24V
Power Dissipation 1000mW

AD566 ORDERING GUIDE

MODEL	PACKAGE	TEMP RANGE	LINEARITY ERROR MAX @ 25°C	MAX GAIN T.C. (ppm of F.S./°C)	PACKAGE STYLE[1]
AD566JD/BIN	Ceramic	0 to +70°C	±1/2LSB	10	D24A
AD566KD/BIN	Ceramic	0 to +70°C	±1/4LSB	3	D24A
AD566SD/BIN	Ceramic	-55°C to +125°C	±1/2LSB	10	D24A
AD566SD/BIN/883B	Ceramic	-55°C to +125°C	±1/2LSB	10	D24A
AD566TD/BIN	Ceramic	-55°C to +125°C	±1/4LSB	3	D24A
AD566TD/BIN/883B	Ceramic	-55°C to +125°C	±1/4LSB	3	D24A

[1] See Section 20 for package outline information.

ANALOG DEVICES

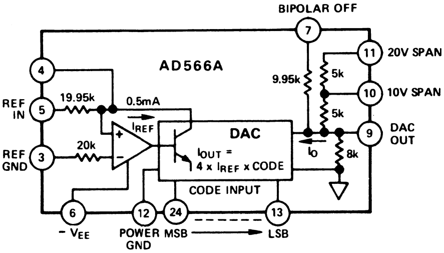
Low Cost High Speed 12-Bit Monolithic D/A Converter

AD566A*

FEATURES

Single Chip Construction
Very High Speed: Settles to 1/2LSB in 350ns max
Full Scale Switching Time: 30ns
Guaranteed for Operation with -12V Supply
Monotonicity Guaranteed Over Temperature
Linearity Guaranteed Over Temperature: 1/2LSB max (AD566AK, T)
Low Power: 180mW
Pin-Out Compatible with AD562, AD566
Low Cost

AD566A FUNCTIONAL BLOCK DIAGRAM



24-PIN DUAL IN LINE PACKAGE

PRODUCT DESCRIPTION

The AD566A is a fast 12-bit digital-to-analog converter which incorporates the latest advances in analog circuit design into a low power monolithic chip.

The AD566A chip uses 12 precision, high speed bipolar current steering switches, control amplifier and a laser-trimmed thin film resistor network to produce a very fast, high accuracy analog output current.

The combination of performance and flexibility in the AD566A has resulted from major innovations in circuit design, an important new high-speed bipolar process, and continuing advances in laser-wafer-trimming techniques (LWT). The AD566A has a 10–90% full scale transition time less than 35 nanoseconds and settles to within ±1/2LSB in 350 nanoseconds max. AD566A chips are laser-trimmed at the wafer level to ±1/8LSB typical linearity and are specified to ±1/4LSB max error (K and T grades) at +25°C. High speed and accuracy make the AD566A the ideal choice for high speed display drivers as well as fast analog-to-digital converters.

The AD566A is available in four performance grades. The AD566AJ and K are specified for use over the 0 to +70°C temperature range and the AD566AS and AT grades are specified for the -55°C to +125°C range. All are packaged in a 24-pin hermetic ceramic dual in line package.

PRODUCT HIGHLIGHTS

1. The wide output compliance range is ideally suited for fast, low noise, accurate voltage output configurations without an output amplifier.
2. The device incorporates a newly developed, fully differential, nonsaturating precision current switching fell structure which combines the dc accuracy and stability first developed in the AD562 with very fast switching times and an optimally-damped settling characteristic.
3. The chip also contains SiCr thin film application resistors which can be used with an external op amp to provide a precision voltage output or as input resistors for a successive approximation A/D converter. The resistors are matched to the internal ladder network to guarantee a low gain temperature coefficient and are laser-trimmed for minimum full scale and bipolar offset errors.
4. The pin-out of the AD566A is compatible with the industry-standard AD562 so that a system can easily be upgraded to provide higher speed performance.
5. The single-chip construction makes the AD566A inherently more reliable than hybrid multi-chip designs. The AD566AS and T grades, with guaranteed linearity and monotonicity over the -55°C to +125°C range, are especially recommended for high reliability needs in harsh environments. These units are available processed to MIL-STD-883, Level B.

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*Covered by patent numbers: 3,803,590; RE 28,633; 4,020,486; 3,747,088.

SPECIFICATIONS (T_A = +25°C, V_{EE} = −15V, unless otherwise specified)

MODEL	AD566AJ MIN	AD566AJ TYP	AD566AJ MAX	AD566AK MIN	AD566AK TYP	AD566AK MAX	UNITS
DATA INPUTS[1] (Pins 13 to 24)							
TTL or 5 Volt CMOS							
Input Voltage							
Bit ON Logic "1"	+2.0		+5.5	+2.0		+5.5	V
Bit OFF Logic "0"	0		+0.8	0		+0.8	V
Logic Current (each bit)							
Bit ON Logic "1"		+120	+300		+120	+300	μA
Bit OFF Logic "0"		+35	+100		+35	+100	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current							
Unipolar (all bits on)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar (all bits on or off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (exclusive of span resistors)	6k	8k	10k	6k	8k	10k	Ω
Offset							
Unipolar (adjustable to zero per Figure 3)		0.01	0.05		0.01	0.05	% of F.S.
Bipolar (Figure 4 R_1 and R_2 = 50Ω fixed)		0.05	0.15		0.05	0.1	% of F.S.
Capacitance		25			25		pF
Compliance Voltage							
T_{min} to T_{max}	-1.5		+10	-1.5		+10	V
ACCURACY (error relative to full scale) +25°C		±1/4	±1/2		±1/8	±1/4	LSB
		(0.006)	(0.012)		(0.003)	(0.006)	% of F.S.
T_{min} to T_{max}		±1/2	±3/4		±1/4	±1/2	LSB
		(0.012)	(0.018)		(0.006)	(0.012)	% of F.S.
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_{min} to T_{max}		MONOTONICITY GUARANTEED			MONOTONICITY GUARANTEED		
TEMPERATURE COEFFICIENTS							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		7	10		2	3	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2LSB							
All Bits ON-to-OFF or OFF-to-ON (Figure 8)		250	350		250	350	ns
FULL SCALE TRANSITION							
10% to 90% Delay plus Rise Time		15	30		15	30	ns
90% to 10% Delay plus Fall Time		30	50		30	50	ns
POWER REQUIREMENTS							
V_{EE}, -11.4 to -16.5V dc		-12	-18		-12	-18	mA
POWER SUPPLY GAIN SENSITIVITY[2]							
V_{EE} = -11.4 to -16.5V dc		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT RANGE (see Figures 3, 4, 5)		0 to +5			0 to +5		V
		-2.5 to +2.5			-2.5 to +2.5		V
		0 to +10			0 to +10		V
		-5 to +5			-5 to +5		V
		-10 to +10			-10 to +10		V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor for R2 (Figure 3)		±0.1	±0.25		±0.1	±0.25	% of F.S.
Bipolar Zero Error with Fixed 50Ω Resistor for R1 (Figure 4)		±0.05	±0.15		±0.05	±0.1	% of F.S.
Gain Adjustment Range (Figure 3)	±0.25			±0.25			% of F.S.
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S.
REFERENCE INPUT							
Input Impedance	15k	20k	25k	15k	20k	25k	Ω
POWER DISSIPATION		180	300		180	300	mW
MULTIPLYING MODE PERFORMANCE (All Models)							
Quadrants		Two (2): Bipolar Operation at Digital Input Only					
Reference Voltage		+1V to +10V, Unipolar					
Accuracy		10 Bits (±0.05% of Reduced F.S.) for 1V dc Reference Voltage					
Reference Feedthrough (unipolar mode, all bits OFF, and 1 to +10V [p-p], sinewave frequency for 1/2LSB [p-p] feedthrough)		40kHz typ					
Output Slew Rate 10%-90%		5mA/μs					
90%-10%		1mA/μs					
Output Settling Time (all bits on and a 0–10V step change in reference voltage)		1.5μs to 0.01% F.S.					
CONTROL AMPLIFIER							
Full Power Bandwidth		300kHz					
Small-Signal Closed-Loop Bandwidth		1.8MHz					

NOTES

[1] The digital input levels are guaranteed but not tested over the temperature range.

[2] The power supply gain sensitivity is tested in reference to a V_{EE} of -15V dc.

Specifications subject to change without notice.

MODEL	AD566AS MIN	AD566AS TYP	AD566AS MAX	AD566AT MIN	AD566AT TYP	AD566AT MAX	UNITS
DATA INPUTS[1] (Pins 13 to 24)							
TTL or 5 Volt CMOS							
Input Voltage							
Bit ON Logic "1"	+2.0		+5.5	+2.0		+5.5	V
Bit OFF Logic "0"	0		+0.8	0		+0.8	V
Logic Current (each bit)							
Bit ON Logic "1"		+120	+300		+120	+300	μA
Bit OFF Logic "0"		+35	+100		+35	+100	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current							
Unipolar (all bits on)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar (all bits on or off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (exclusive of span resistors)	6k	8k	10k	6k	8k	10k	Ω
Offset							
Unipolar (adjustable to zero per Figure 3)		0.01	0.05		0.01	0.05	% of F.S.
Bipolar (Figure 4 R_1 and R_2 = 50Ω fixed)		0.05	0.15		0.05	0.1	% of F.S.
Capacitance		25			25		pF
Compliance Voltage							
T_{min} to T_{max}	-1.5		+10	-1.5		+10	V
ACCURACY (error relative to full scale) +25°C		±1/4	±1/2		±1/8	±1/4	LSB
		(0.006)	(0.012)		(0.003)	(0.006)	% of F.S.
T_{min} to T_{max}		±1/2	±3/4		±1/4	±1/2	LSB
		(0.012)	(0.018)		(0.006)	(0.012)	% of F.S.
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_{min} to T_{max}	MONOTONICITY GUARANTEED			MONOTONICITY GUARANTEED			
TEMPERATURE COEFFICIENTS							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		7	10		2	3	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2LSB							
All Bits On-to-OFF or OFF-to-ON (Figure 8)		250	350		250	350	ns
FULL SCALE TRANSITION							
10% to 90% Delay plus Rise Time		15	30		15	30	ns
90% to 10% Delay plus Fall Time		30	50		30	50	ns
POWER REQUIREMENTS							
V_{EE}, -11.4 to -16.5V dc		-12	-18		-12	-18	mA
POWER SUPPLY GAIN SENSITIVITY[2]							
V_{EE} = -11.4 to -16.5V dc		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT RANGE (see Figures 3, 4, 5)		0 to +5			0 to +5		V
		-2.5 to +2.5			-2.5 to +2.5		V
		0 to +10			0 to +10		V
		-5 to +5			-5 to +5		V
		-10 to +10			-10 to +10		V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor R2 (Figure 3)		±0.1	±0.25		±0.1	±0.25	% of F.S.
Bipolar Zero Error with Fixed 50Ω Resistor for R1 (Figure 4)		±0.05	±0.15		±0.05	±0.1	% of F.S.
Gain Adjustment Range (Figure 3)	±0.25			±0.25			% of F.S.
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S.
REFERENCE INPUT							
Input Impedance	15k	20k	25k	15k	20k	25k	Ω
POWER DISSIPATION		180	300		180	300	mW

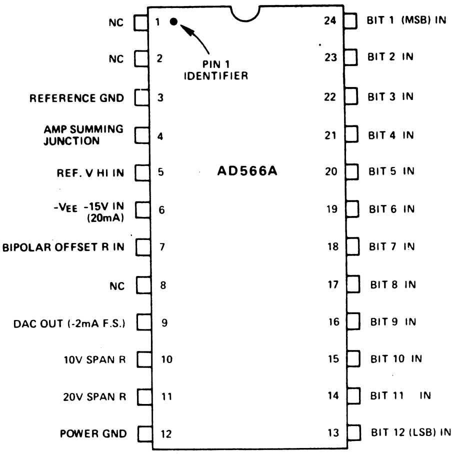
MULTIPLYING MODE PERFORMANCE (All Models)	
Quadrants	Two (2): Bipolar Operation at Digital Input Only
Reference Voltage	+1V to +10V, Unipolar
Accuracy	10 Bits (±0.05% of Reduced F.S.) for 1V dc Reference Voltage
Reference Feedthrough (unipolar mode, all bits OFF, and 1 to +10V [p-p], sinewave frequency for 1/2LSB [p-p] feedthrough)	40kHz typ
Output Slew Rate 10%-90%	5mA/μs
90%-10%	1mA/μs
Output Settling Time (all bits on and a 0–10V step change in reference voltage)	1.5μs to 0.01% F.S.
CONTROL AMPLIFIER	
Full Power Bandwidth	300kHz
Small-Signal Closed-Loop Bandwidth	1.8MHz

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

V_{EE} to Power Ground	0V to –18V
Voltage on DAC Output (Pin 9)	–3V to +12V
Digital Inputs (Pins 13 to 24) to Power Ground	–1.0V to +7.0V
Ref In to Reference Ground	±12V
Bipolar Offset to Reference Ground	±12V
10V Span R to Reference Ground	±12V
20V Span R to Reference Ground	±24V
Power Dissipation	1000mW

PIN CONFIGURATION
TOP VIEW



AD566A ORDERING GUIDE

MODEL	PACKAGE	TEMP RANGE	LINEARITY ERROR MAX @+25°C	MAX GAIN T.C. (ppm of F.S./°C)	PACKAGE OPTION[1]
AD566AJN/BIN	Plastic	0 to +70°C	±1/2LSB	10	N24A
AD566AJD/BIN	Ceramic	0 to +70°C	±1/2LSB	10	D24A
AD566AKN/BIN	Plastic	0 to +70°C	±1/4LSB	3	N24A
AD566AKD/BIN	Ceramic	0 to +70°C	±1/4LSB	3	D24A
AD566ASD/BIN	Ceramic	-55°C to +125°C	±1/2LSB	10	D24A
AD566ASD/BIN/883B	Ceramic	-55°C to +125°C	±1/2LSB	10	D24A
AD566ATD/BIN	Ceramic	-55°C to +125°C	±1/4LSB	3	D24A
AD566ATD/BIN/883B	Ceramic	-55°C to +125°C	±1/4LSB	3	D24A

[1] See Section 20 for package outline information.

THE AD566A OFFERS TRUE 12-BIT PERFORMANCE

ACCURACY: Analog Devices defines accuracy as the maxideviation of the actual, adjusted DAC output (see the next page) from the ideal analog output (a straight line drawn from 0 to F.S. – 1LSB) for any bit combination. The AD566A is laser trimmed to 1/4LSB (0.025% of F.S.) maximum error at +25°C for the K and T version and to 1/2LSB for the J and S versions.

MONOTONICITY: A DAC is said to be monotonic if the output either increases or remains constant for increasing digital inputs such that the output will always be a non-decreasing function of the input. All versions of the AD566A are monotonic over their entire operating temperature range.

DIFFERENTIAL NONLINEARITY: Monotonic behavior requires that the differential nonlinearity error be less than 1LSB both at +25°C and over the temperature range of interest. Differential nonlinearity is the measure of the variation in analog value, normalized to full scale, associated with a 1LSB change in digital input code. For example, if a 1LSB change in the input code results in a change of only 0.61mV (1/4LSB) in analog output, the differential nonlinearity error would be 1.83mV, or 3/4LSB. The AD566AK and T have a max differential linearity error of 1/2LSB, which is a tighter specification than simply guaranteed monotonicity.

ANALYZING DEVICE ACCURACY OVER THE TEMPERATURE RANGE

For the purposes of temperature drift analysis, the major device components are shown in Figure 1.

The input reference current to the DAC, I_{REF}, is developed from the external reference and will show the same drift rate as the reference voltage. The DAC output current, I_{DAC} which is a function of the digital input code, is designed to track I_{REF}; if there is a slight mismatch in these currents over temperature, it will contribute to the gain T.C. The bipolar offset resistor, R_{BP}, and gain setting resistor, R_{GAIN}, also have temperature coefficients which contribute to system drift errors.

There are three types of drift errors over temperature: offset, gain, and linearity. Offset drift causes a vertical translation of the entire transfer curve; gain drift is a change in the slope of the curve; and linearity drift represents a change in the shape of the curve. The combination of these three drifts results in the complete specification for total error over temperature.

Total error is defined as the deviation from a true straight line transfer characteristic from exactly zero at a digital input which calls for zero output to a point which is defined as full scale. A specification for total error over temperature assumes that both the zero and full scale points have been trimmed for zero error at +25°C. Total error is normally expressed a percentage of the full scale range. In the bipolar situation, this means the total range from $-V_{FS}$ to $+V_{FS}$.

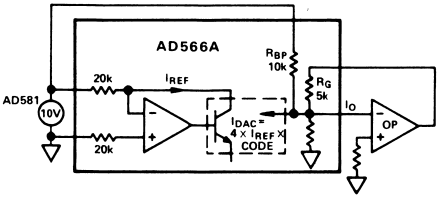


Figure 1. Bipolar Configuration

MONOTONICITY AND LINEARITY

The initial linearity error of ±1/2LSB max and the differential linearity error of ±3/4LSB max guarantee monotonic performance over the range of –55°C to +125°C. It can, therefore, be assumed that linearity errors are insignificant in computation of total temperature errors.

UNIPOLAR ERRORS

Temperature error analysis in the unipolar mode is straightforward: there is an offset drift and a gain drift. The offset drift of 2ppm/°C max (which comes from leakage currents) causes a linear shift in the transfer curve as shown in Figure 2. The gain drift causes a change in the slope of the curve which results from reference drift and the device gain drift. The device gain drift is the DAC drift and drift in R_{GAIN} relative to the DAC resistors for a total of 3ppm/°C max (AD566AK, T). Total absolute error due to all of these effects is guaranteed to be less than ±0.05% of full scale from –55°C to +125°C.

BIPOLAR RANGE ERRORS

The analysis is slightly more complex in the bipolar mode. In this mode R_{BP} is connected to V_{REF} (see Figure 1) to generate a current which exactly balances the current of the MSB so that the output voltage is zero with the MSB on.

Note that if the DAC and application resistors track perfectly, the bipolar offset drift will be zero even if the reference drifts. A change in the reference voltage, which causes a shift in the bipolar offset, will also cause an equivalent change in I_{REF} and thus I_{DAC}, so that I_{DAC} will always be exactly balanced by I_{BP} with the MSB turned on. This effect is shown in Figure 2. The net effect of the reference drift then is simply to cause a rotation in the transfer around bipolar zero. However, consideration of second order effects (which are often overlooked) reveals the errors in the bipolar mode. The unipolar offset drifts discussed before will have the same effect on the bipolar offset. A mismatch of R_{BP} to the DAC resistors is usually the largest component of bipolar drift, but in the AD566A this error is held to 10ppm max. The total of all these errors is held to ±0.15% of full scale from –55°C to +125°C (AD566AT). Note that, in the bipolar ranges, full scale is defined as the total range from $-V_{FS}$ to $+V_{FS}$.

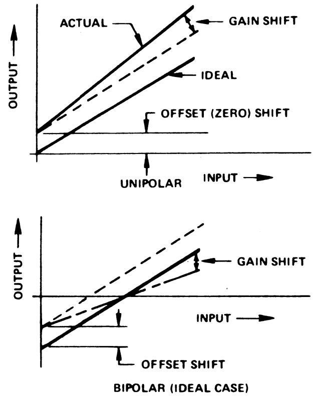


Figure 2. Unipolar and Bipolar Drifts

CONNECTING THE AD566A FOR BUFFERED VOLTAGE OUTPUT

The standard current-to-voltage conversion connections using an operational amplifier are shown here with the preferred trimming techniques. If a low offset operational amplifier (AD510L, AD517L, AD741L, AD301AL, AD OP-07) is used, excellent performance can be obtained in many situations without trimming (an op amp with less than 0.5mV max offset voltage should be used to keep offset errors below 1/2LSB). If a 50Ω fixed resistor is substituted for the 100Ω trimmer, unipolar zero will typically be within ±1/2LSB (plus op amp offset), and full scale accuracy will be within 0.1% (0.25% max). Substituting a 50Ω resistor for the 100Ω bipolar offset trimmer will give a bipolar zero error typically within ±2LSB (0.05%).

The AD509 is recommended for buffered voltage-output applications which require a settling time to ±1/2LSB of one microsecond. The feedback capacitor is shown with the optimum value for each application; this capacitor is required to compensate for the 25 picofarad DAC output capacitance.

FIGURE 3 UNIPOLAR CONFIGURATION

This configuration will provide a unipolar 0 to +10 volt output range. In this mode, the bipolar terminal, pin 7, should be grounded if not used for trimming.

STEP I . . . ZERO ADJUST

Turn all bits OFF and adjust zero trimmer, R1, until the output reads 0.000 volts (1LSB = 2.44mV). In most cases this trim is not needed, but pin 7 should then be connected to pin 12.

STEP II . . . GAIN ADJUST

Turn all bits ON and adjust 100Ω gain trimmer, R2, until the output is 9.9976 volts. (Full scale is adjusted to 1LSB less than nominal full scale of 10.000 volts.) If a 10.2375V full scale is desired (exactly 2.5mV/bit), insert a 120Ω resistor in series with the gain resistor at pin 10 to the op amp output.

FIGURE 4. BIPOLAR CONFIGURATION

This configuration will provide a bipolar output voltage from -5.000 to +4.9976 volts, with positive full scale occurring with all bits ON (all 1's).

STEP I . . . OFFSET ADJUST

Turn OFF all bits. Adjust 100Ω trimmer R1 to give -5.000 output volts.

STEP II . . . GAIN ADJUST

Turn ON all bits. Adjust 100Ω gain trimmer R2 to give a reading of +4.9976 volts.

Please note that it is not necessary to trim the op amp to obtain full accuracy at room temperature. In most bipolar situations, an op amp trim is unnecessary unless the untrimmed offset drift of the op amp is excessive.

FIGURE 5. OTHER VOLTAGE RANGES

The AD566A can also be easily configured for a unipolar 0 to +5 volt range or ±2.5 volt and ±10 volt bipolar ranges by using the additional 5k application resistor provided at the 20 volt span R terminal, pin 11. For a 5 volt span (0 to +5V or ±2.5V), the two 5k resistors are used in parallel by shorting pin 11 to pin 9 and connecting pin 10 to the op amp output and the bipolar offset resistor either to ground for unipolar or to V_{REF} for the bipolar range. For the ±10 volt range (20 volt span) use the 5k resistors in series by connecting only pin 11 to the op amp output and the bipolar offset connected as shown. The ±10 volt option is shown in Figure 5.

DIGITAL INPUT		ANALOG OUTPUT		
MSB	LSB	Straight Binary	Offset Binary	Two's Compl.*
000000000000		Zero	-Full Scale	Zero
011111111111		Mid Scale -1LSB	Zero -1LSB	+FS -1LSB
100000000000		+1/2 FS	Zero	-FS
111111111111		+FS -1LSB	+ Full Scale -1LSB	Zero -1LSB

*Invert the MSB of the offset binary code with an external inverter to obtain two's complement.

Table 1. Digital Input Codes

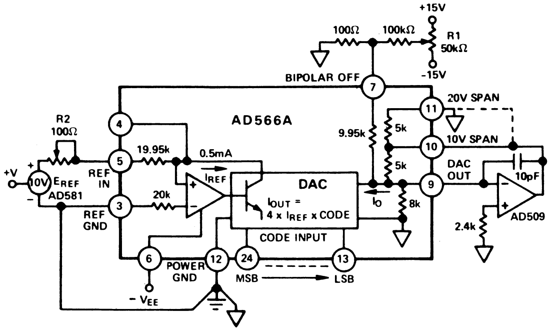


Figure 3. 0 to +10V Unipolar Voltage Output

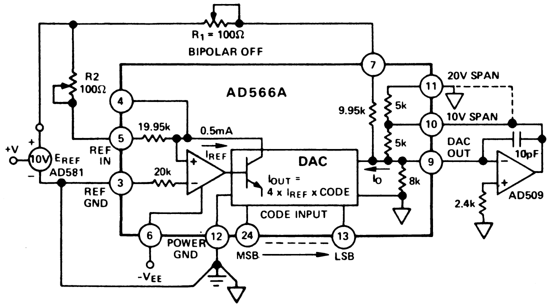
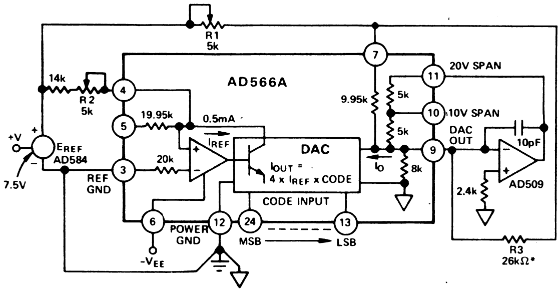


Figure 4. ±5V Bipolar Voltage Output



*THE PARALLEL COMBINATION OF THE BIPOLAR OFFSET RESISTOR AND R3 ESTABLISH A CURRENT TO BALANCE THE MSB CURRENT. THE EFFECT OF TEMPERATURE COEFFICIENT MISMATCH BETWEEN THE BIPOLAR RESISTOR COMBINATION AND DAC RESISTORS IS EXPLAINED ON PREVIOUS PAGE.

Figure 5. ±10V Voltage Output

DIGITAL INPUT CONSIDERATIONS

The threshold of the digital input circuitry is set at 2.0 volts and does not vary with supply voltage. The input lines can interface with any type of 5 volt logic, TTL/DTL or CMOS, and have sufficiently low input currents to interface easily with unbuffered CMOS logic. The configuration of the input circuit is shown in Figure 6. The input line can be modelled as a 30kΩ resistance connected to a -0.7V rail.

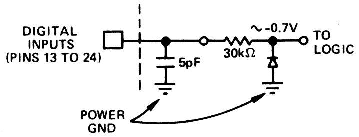


Figure 6. Equivalent Digital Input Circuit

GROUNDING RULES

The AD566A brings out separate reference and power grounds to allow optimum connections for low noise and high speed performance. These grounds must be tied together at one point, usually the device power ground. The separate ground returns are provided to minimize the current flow in low-level signal paths. In this way, logic gate return currents are not summed into the same return path with analog signals.

The reference ground at pin 3 is the ground point for the internal reference and is thus the "high quality" ground for the AD566A; it should be connected directly to the analog reference point of the system. The power ground at pin 12 can be connected to the most convenient ground point; analog power return is preferred. If the power ground contains high frequency noise in excess of 200mV, this noise may feed through to the output of the converter; thus some caution is required in applying these grounds.

OUTPUT VOLTAGE COMPLIANCE

The AD566A has a typical output compliance range of -2 to +10 volts. The current-steering output stages will be unaffected by changes in the output terminal voltage over that range. However, there is an equivalent output impedance of 8kΩ in parallel with 25pF at the output terminal which produces an equivalent error current if the voltage deviates from analog common. This is a linear effect which does not change with input code. Operation beyond the compliance limits may cause either output stage saturation or breakdown which results in nonlinear performance. Compliance limits are a function of output current and negative supply, as shown in Figure 7.

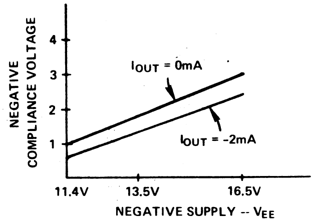


Figure 7. Typical Neg. Compliance Range vs. Neg. Supply

HIGH SPEED SYSTEM DESIGN

Full realization of the AD566A high speed capabilities requires strict attention to detail by the user in all areas of application and testing.

The settling time for the AD566A is specified for the current output, an inherently high speed DAC operating mode. However, most DAC applications require a current-to-voltage conversion at some point in the signal path, although an unbuffered voltage level (not using an op amp) is suitable for use in a successive-approximation A/D converter or in many display applications (see next page). With proper design this form of current-to-voltage conversion can give very fast operation. The fastest voltage conversion is achieved by connecting a low value resistor directly to the output, as shown in Figure 8. In this case, the settling time is primarily determined by the cell switching time and by the RC time constant of the AD566A output capacitance of 25 picofarads (plus stray capacitance) combined with the output resistor value. Settling to 0.01% of full scale (for a full scale transition) requires 9 time constants. This effect is important for an equivalent resistance over 1kΩ.

If an op amp is used to provide a low impedance output signal, some loss in settling time will be seen due to op amp dynamics. The normal current-to-voltage converter op amp circuits, based on the fast settling AD509, are shown in the applications circuit. The unipolar or bipolar circuits shown settle to ±1/2LSB in 1μs. The DAC output capacitance, which acts as a stray capacitance at the op amp inverting input, must be compensated by a feedback capacitor as shown. The value should be chosen carefully for each application and each op amp type.

Fastest operation will be obtained by minimizing lead lengths, stray capacitance and impedance levels. The supply should be bypassed near the device; 0.1μF will be sufficient since the AD566A runs at constant supply current regardless of input code. Output capacitance effects can be minimized by grounding pin 11 in 10V span applications.

DIRECT UNBUFFERED VOLTAGE OUTPUT FOR CABLE DRIVING

The wide compliance range allows direct current-to-voltage conversion with just an output resistor. Figure 8 shows a connection using the gain and bipolar output resistors to give a ±1.60 volt bipolar swing. In this situation, the digital code is complementary binary. Other combinations of internal and external output resistors (R_X) can be used to scale to alternate voltage ranges, simply by appropriately scaling the 0 to -2mA unipolar output current and using the 10.0 volt reference voltage for bipolar offset. For example, setting R_X = 2.67kΩ gives a ±1 volt range with a 1kΩ equivalent output impedance.

This connection is especially useful for directly driving a long cable at high speed. A 50Ω R_X resistor drives a 50Ω cable with a ±50mV full scale swing; settling time is very fast as discussed in the section above.

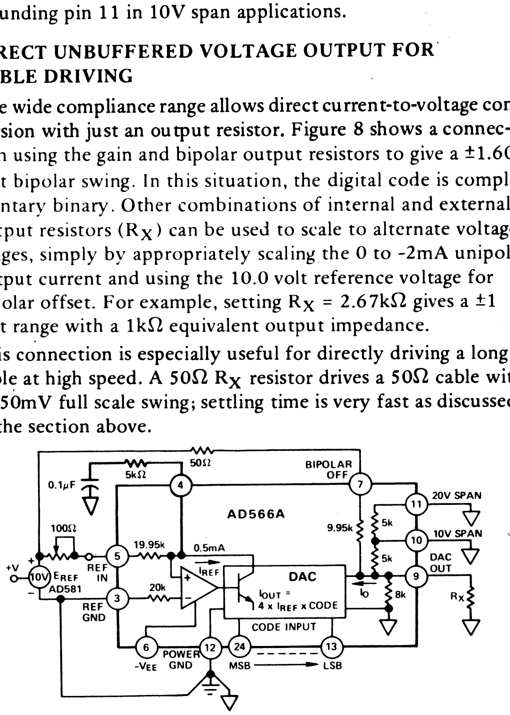


Figure 8. Unbuffered Bipolar Voltage Output

MICROPROCESSOR CONTROL FOR A 12-BIT DAC

A common I/O interface is the Digital-to-Analog Converter output, which provides a voltage corresponding to a data word from a microprocessor.

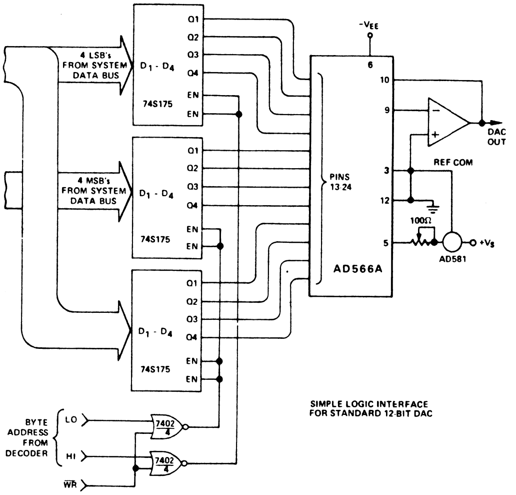

4 LSB's FROM SYSTEM DATA BUS
4 MSB's FROM SYSTEM DATA BUS
Q1
Q2
Q3
Q4
D1 - D4
EN
EN
74S175
-VEE
6
10
9
DAC OUT
REF COM
PINS 13-24
3
12
100Ω
5
+Vs
AD581
AD566A
SIMPLE LOGIC INTERFACE FOR STANDARD 12-BIT DAC
BYTE ADDRESS FROM DECODER
LO
HI
WR
7402 1/4

Figure 9.

Interfacing is more complex when the DAC needs more bits of resolution than the system data bus can carry in 1 byte. For example, applications using an 8-bit microprocessor to drive a 12-bit DAC are common. Several hardware formats are possible; the most convenient one depends on the desired data format. If the least significant 8 bits are in one byte of memory, they can be transferred into an 8-bit latch in one memory-or I/O-write cycle. An adjacent cycle can be used to transfer the 4 least-significant bits of another data word into a latch controlling the 4 most-significant bits of the DAC. The least-significant bits of the data bus drive two 4-bit latches which are controlled by two separate addresses. The Hi Byte address allows the microprocessor to write in the 4 most significant data bits and the Lo Byte address allows the microprocessor to write in the 8 remaining bits. When all 12 bits are latched, the DAC output will assume its proper new value. An intermediate value will be momentarily present at the DAC terminals between Hi and Lo Byte write cycles. For applications such as CRT displays where this intermediate value cannot be tolerated, double buffering can be effectively employed. This could be implemented with a separately-controlled 12-bit latch at the DAC inputs or a sample and hold amplifier on the output.

D/A CONVERTER DISPLAYS

In Figure 10, a counter-driven AD566A is shown as a sawtooth sweep generator. When used for displays, this scheme provides a highly-repeatable, controllable linear sweep.

Raster displays are usually generated by a fast horizontal scan and a slower vertical scan which is derived from the horizontal scan. Intensity modulation during each horizontal scan provides the pictorial information. The picture resolution is expressed in terms of the number of discernible data points per line multiplied by the number of lines. The minimum frame period is the time allowed for the horizontal scan-plus-retrace multiplied by the number of lines, plus vertical retrace time.

A family of monolithic D/A converters is available from Analog Devices that are suitable for vertical sweeps. The line-spacing uniformity depends on linearity while maximum number of lines depends on DAC resolution. A display of 1024 lines would require 10 bits of resolution and 12 bits of linearity (0.012% of linearity provides less than 12% of spacing error). Switching transients created within the vertical sweep DAC are blanked because they occur during the horizontal retrace interval.

For horizontal sweeps, the DAC requirements are more severe. For example, to resolve 500 points per line, at 500 lines per frame, at a 30Hz frame rate, requires that each digital horizontal step settle within 100ns (typical full scale settling time is 200ns), and that there be no "glitches". Even if the display is blanked between horizontal steps, large glitches at major carries can cause deflection-amplifier transients, which distort the pattern.

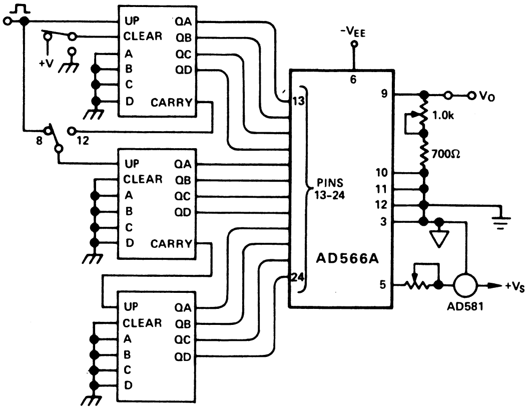


Figure 10.

The excellent high speed performance of the AD566A is demonstrated in the oscilloscope photograph of Figure 11. This measurement is made with the AD566A driving directly into an equivalent 50Ω load, amplified with a low capacitance MOS-input, UHF amplifier. The figure shows the worst case situation, which is full scale transition from switching all bits OFF to ON. The equipment and circuitry used to make the measurements adds about 50ns to the actual device performance.

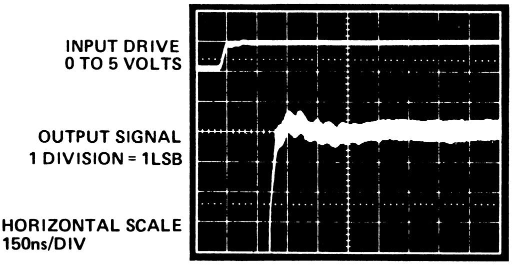


Figure 11. Settling Characteristic Detail

ANALOG DEVICES

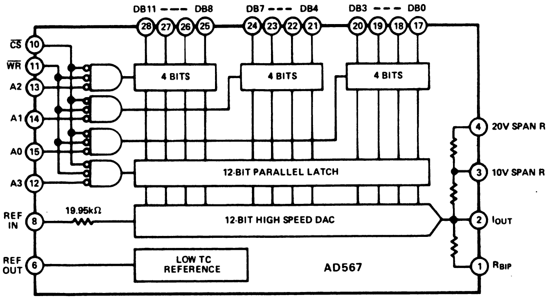
Microprocessor-Compatible 12-Bit D/A Converter

AD567*

FEATURES

- Single Chip Construction
- Double-Buffered Latch for 8-Bit μP-Compatibility
- Fast Settling Time: 500ns max to ±1/2LSB
- High Stability Buried Zener Reference on Chip
- Monotonicity Guaranteed Over Temperature
- Linearity Guaranteed Over Temperature: 1/2LSB max (AD567K, T)
- Guaranteed for Operation with ±12V or ±15V Supplies
- Low Power: 300mW Including Reference
- TTL/5V CMOS Compatible Logic Inputs
- Low Cost

AD567 FUNCTIONAL BLOCK DIAGRAM



28-PIN DIP

PRODUCT DESCRIPTION

The AD567 is a complete high speed 12-bit digital-to-analog converter including a high stability buried zener voltage reference and double-buffered input latch on a single chip. The converter uses 12 precision high speed bipolar current steering switches and a laser trimmed thin film resistor network to provide fast settling time and high accuracy.

Microprocessor compatibility is achieved by the on-chip double-buffered latch. The design of the input latch allows direct interface to 4-, 8-, 12-, or 16-bit buses. The 12 bits of data from the first rank of latches can then be transferred to the second rank, avoiding generation of spurious analog output values. The latch responds to strobe pulses as short as 100ns, allowing use with the fastest available microprocessors.

The functional completeness and high performance in the AD567 results from a combination of advanced switch design, high speed bipolar manufacturing process, and the proven laser wafer-trimming (LWT) technology. The AD567 is trimmed at the wafer level and is specified to ±1/4LSB maximum linearity error (K and T grades) at 25°C and ±1/2LSB over the full operating temperature range.

The subsurface (buried) Zener diode on the chip provides a low-noise voltage reference which has long-term stability and temperature drift characteristics comparable to the best discrete reference diodes. The laser trimming process which provides the excellent linearity is also used to trim both the absolute value of the reference as well as its temperature coefficient. The AD567 is thus well suited for wide temperature range performance with ±1/2LSB maximum linearity error and guaranteed monotonicity over the full temperature range. Typical full scale gain T.C. is 10ppm/°C.

The AD567 is available in four performance grades. The AD567J and K are specified for use over the 0 to +70°C temperature range and are available in either a 28-pin hermetically-sealed, ceramic DIP or a 28-pin molded plastic DIP (N package). The AD567S and T grades are specified for the −55°C to +125°C range and are available in the ceramic package.

PRODUCT HIGHLIGHTS

1. The AD567 is a complete current output DAC with voltage reference and digital latches on a single IC chip.
2. The double-buffered latch structure permits direct interface to 4-, 8-, 12-, or 16-bit data buses. All logic inputs are TTL or 5 volt CMOS compatible.
3. The internal buried zener reference is laser-trimmed to 10.00 volts with a ±1% maximum error. The reference voltage is also available for external application.
4. The chip also contains SiCr thin film application resistors which can be used either with an external op amp to provide a precision voltage output or as input resistors for an A/D converter. The resistors are matched to the internal ladder network to guarantee a low gain temperature coefficient and are laser-trimmed for minimum full scale and bipolar offset errors.
5. The precision high speed current switch design* provides high dc accuracy and an optimally-damped settling characteristic. Output current settling time is 500 nanoseconds maximum to ±1/2LSB.
6. The single-chip construction makes the AD567 inherently more reliable than multichip hybrid designs. The AD567S and T grades with guaranteed linearity and monotonicity over the −55°C to +125°C range are especially recommended for high reliability needs in harsh environments. These units are available processed to MIL-STD-883, Level B.

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*Covered by patent numbers: 3,803,590; 3,890,611; 3,932,863; 3,978,473; 4,020,486; and other patents pending.

SPECIFICATIONS (T_A = +25°C, V_{CC} = +12V or +15V, V_{EE} = -12V or -15V, unless otherwise specified)

	AD567J			AD567K			
MODEL	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
DATA INPUTS[1] (Pins 10-15 and 17-28)							
TTL or 5 Volt CMOS							
Input Voltage							
Bit ON Logic "1"	+2.0		+5.5	+2.0		+5.5	V
Bit OFF Logic "0"			+0.8			+0.8	V
Logic Current (each bit)							
Bit ON Logic "1"		+120	+300		+120	+300	μA
Bit OFF Logic "0"		+35	+100		+35	+100	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current							
Unipolar (all bits on)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar (all bits on or off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (exclusive of span resistors)	6k	8k	10k	6k	8k	10k	Ω
Offset							
Unipolar		0.01	0.05		0.01	0.05	% of F.S.
Bipolar (Figure 3, R_2 = 50Ω fixed)		0.05	0.15		0.05	0.1	% of F.S.
Capacitance		25			25		pF
Compliance Voltage							
T_{min} to T_{max}	-1.5		+10	-1.5		+10	V
ACCURACY (error relative to full scale) +25°C		±1/4	±1/2		±1/8	±1/4	LSB
		(0.006)	(0.012)		(0.003)	(0.006)	% of F.S.
T_{min} to T_{max}		±1/2	±3/4		±1/4	±1/2	LSB
		(0.012)	(0.018)		(0.006)	(0.012)	% of F.S.
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_{min} to T_{max}		MONOTONICITY GUARANTEED			MONOTONICITY GUARANTEED		
TEMPERATURE COEFFICIENTS							
With Internal Reference							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		15	50		10	20	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
TEMPERATURE RANGE							
Operating	0		+70	0		+70	°C
Storage	-65		+150	-65		+150	°C
POWER REQUIREMENTS							
V_{CC}, +11.4 to +16.5V dc		3	5		3	5	mA
V_{EE}, -11.4 to -16.5V dc		-17	-25		-17	-25	mA
POWER SUPPLY GAIN SENSITIVITY[2]							
V_{CC} = +11.4 to +16.5V dc		3	10		3	10	ppm of F.S./%
V_{EE} = -11.4 to -16.5V dc		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT RANGE (see Figures 1, 2, 3)		0 to +5			0 to +5		V
		-2.5 to +2.5			-2.5 to +2.5		V
		0 to +10			0 to +10		V
		-5 to +5			-5 to +5		V
		-10 to +10			-10 to +10		V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor for R2 (Figure 2)		±0.1	±0.25		±0.1	±0.25	% of F.S.
Bipolar Zero Error with Fixed 50Ω Resistor for R1 (Figure 3)		±0.05	±0.15		±0.05	±0.1	% of F.S.
Gain Adjustment Range (Figure 2)	±0.25			±0.25			% of F.S.
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S.
REFERENCE INPUT							
Input Impedance	15k	20k	25k	15k	20k	25k	Ω
REFERENCE OUTPUT							
Voltage	9.90	10.00	10.10	9.90	10.00	10.10	V
Current (available for external loads)	0.1	1.0		0.1	1.0		mA
POWER DISSIPATION		300	495		300	495	mW
PACKAGE OPTION[3]							
Ceramic DIP (D28A)		AD567JD			AD567KD		
Plastic DIP (N28A)		AD567JN[4]			AD567KN[4]		

NOTES

[1] The digital input specifications are guaranteed but not tested over the operating temperature range.

[2] The power supply gain sensitivity is tested in reference to a V_{CC}, V_{EE} of ±15V dc ±10%.

[3] See Section 20 for package outline information.

[4] The AD567JN, KN, SD and TD will be available in June 1982.

Specifications subject to change without notice.

		AD567S			AD567T		
MODEL	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
DATA INPUTS[1] (Pins 10-15 and 17-28)							
TTL or 5 Volt CMOS							
Input Voltage							
Bit ON Logic "1"	+2.0		+5.5	+2.0		+5.5	V
Bit OFF Logic "0"			+0.8			+0.8	V
Logic Current (each bit)							
Bit ON Logic "1"		+120	+300		+120	+300	μA
Bit OFF Logic "0"		+35	+100		+35	+100	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current							
Unipolar (all bits on)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar (all bits on or off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (exclusive of span resistors)	6k	8k	10k	6k	8k	10k	Ω
Offset							
Unipolar		0.01	0.05		0.01	0.05	% of F.S.
Bipolar (Figure 3, R_2 = 50Ω fixed)		0.05	0.15		0.05	0.1	% of F.S.
Capacitance		25			25		pF
Compliance Voltage							
T_{min} to T_{max}	-1.5		+10	-1.5		+10	V
ACCURACY (error relative to full scale) +25°C		±1/4	±1/2		±1/8	±1/4	LSB
		(0.006)	(0.012)		(0.003)	(0.006)	% of F.S.
T_{min} to T_{max}		±1/2	±3/4		±1/4	±1/2	LSB
		(0.012)	(0.018)		(0.006)	(0.012)	% of F.S.
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_{min} to T_{max}		MONOTONICITY GUARANTEED			MONOTONICITY GUARANTEED		
TEMPERATURE COEFFICIENTS							
With Internal Reference							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		15	30		10	20	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
TEMPERATURE RANGE							
Operating	-55		+125	-55		+125	°C
Storage	-65		+150	-65		+150	°C
POWER REQUIREMENTS							
V_{CC}, +11.4 to +16.5V dc		3	5		3	5	mA
V_{EE}, -11.4 to -16.5V dc		-17	-25		-17	-25	mA
POWER SUPPLY GAIN SENSITIVITY[2]							
V_{CC} = +11.4 to +16.5V dc		3	10		3	10	ppm of F.S./%
V_{EE} = -11.4 to -16.5V dc		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT RANGES (see Figures 1, 2, 3)		0 to +5			0 to +5		V
		-2.5 to +2.5			-2.5 to +2.5		V
		0 to +10			0 to +10		V
		-5 to +5			-5 to +5		V
		-10 to +10			-10 to +10		V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor for R2 (Figure 2)		±0.1	±0.25		±0.1	±0.25	% of F.S.
Bipolar Zero Error with Fixed 50Ω Resistor for R1 (Figure 3)		±0.05	±0.15		±0.05	±0.1	% of F.S.
Gain Adjustment Range (Figure 2)	±0.25			±0.25			% of F.S.
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S.
REFERENCE INPUT							
Input Impedance	15k	20k	25k	15k	20k	25k	Ω
REFERENCE OUTPUT							
Voltage	9.90	10.00	10.10	9.90	10.00	10.10	V
Current (available for external loads)	0.1	1.0		0.1	1.0		mA
POWER DISSIPATION		300	495		300	495	mW
PACKAGE OPTION[3]		AD567SD[4]			AD567TD[4]		

Specifications subject to change without notice.

TIMING SPECIFICATIONS

(All Models, T_A = 25°C, V_{CC} = +12V or +15V, V_{EE} = -12V or -15V)

Symbol	Parameter	Min	Typ	Max	
t_{DW}	Data Valid to End of $\overline{WR}$	50	–	–	ns
t_{CW}	$\overline{CS}$ Valid to End of $\overline{WR}$	100	–	–	
t_{AW}	Address Valid to End of $\overline{WR}$	100	–	–	ns
t_{WP}	Write Pulse Width	100	–	–	ns
t_{DH}	Data Hold Time	0	–	–	ns
t_{SETT}	Output Current Settling Time	–	400	500	ns

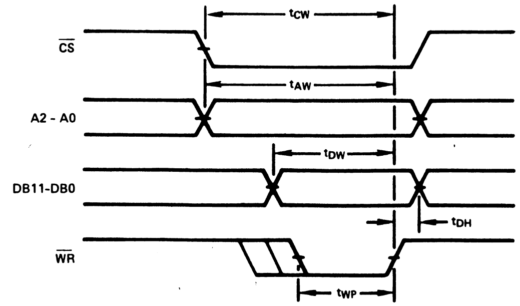
ABSOLUTE MAXIMUM RATINGS

V_{CC} to Power Ground . . . . .0V to +18V
V_{EE} to Power Ground . . . . .0V to -18V
Voltage on DAC Output (Pin 2). . . . .-3V to +12V
Digital Inputs (Pins 10–15, 17–28)
to Power Ground. . . . . -1.0V to +7.0V
Ref In to Reference Ground . . . .±12V
Bipolar Offset to Reference Ground . . . .±12V
10V Span R to Reference Ground . . . .±12V
20V Span R to Reference Ground . . . .±24V
Ref Out. . . . . .Indefinite short to power ground
Momentary Short to V_{CC}
Power Dissipation 1000mW

TIMING DIAGRAMS

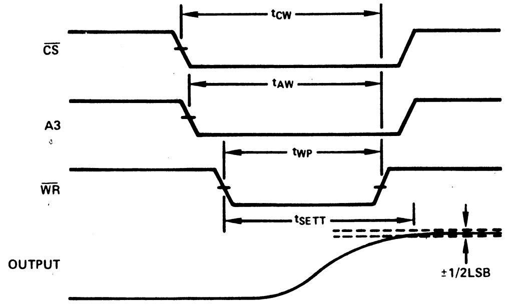
WRITE CYCLE #1

(Load First Rank from Data Bus; A3 = 1)



WRITE CYCLE #2

(Load Second Rank from First Rank; A_2, A_1, A_0 = 1)

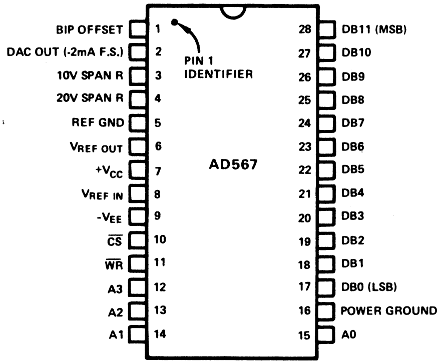


AD567 ORDERING GUIDE

MODEL	PACKAGE	TEMP RANGE	LINEARITY ERROR MAX @ 25°C	GAIN T.C. MAX
AD567JN*	Plastic	Com	±1/2LSB	50ppm/°C
AD567KN*	Plastic	Com	±1/4LSB	20ppm/°C
AD567JD	Ceramic	Com	±1/2LSB	50ppm/°C
AD567KD	Ceramic	Com	±1/4LSB	20ppm/°C
AD567SD*	Ceramic	Mil	±1/2LSB	30ppm/°C
AD567SD/883B*	Ceramic	Mil	±1/2LSB	30ppm/°C
AD567TD*	Ceramic	Mil	±1/4LSB	20ppm/°C
AD567TD/883B*	Ceramic	Mil	±1/4LSB	20ppm/°C

*To be available June 1982.

PIN CONNECTIONS TOP VIEW



THE AD567 OFFERS TRUE 12-BIT PERFORMANCE OVER THE FULL TEMPERATURE RANGE

RELATIVE ACCURACY: Analog Devices defines relative accuracy as the maximum deviation of the actual, adjusted DAC output from the ideal analog output (a straight line drawn from 0 to F.S. – 1LSB) for any bit combination. The AD567 is laser trimmed to 1/4LSB (0.006% of F.S.) maximum error at +25°C for the K and T versions and 1/2LSB for the J and S.

MONOTONICITY: A DAC is said to be monotonic if the output either increases or remains constant for increasing digital inputs such that the output will always be a non-decreasing function of input. All versions of the AD567 are monotonic over their full operating temperature range.

DIFFERENTIAL NONLINEARITY: Monotonic behavior requires that the differential linearity error be less than 1LSB both at +25°C and over the temperature range of interest. Differential nonlinearity is the measure of the variation in analog value, normalized to full scale, associated with a 1LSB change in digital input code. For example, for a 10 volt full scale output, a change of 1LSB in digital input code should result in a 2.44mV change in the analog output (1LSB = 10V x 1/4096 = 2.44mV). If in actual use, however, a 1LSB change in the input code results in a change of only 0.61mV (1/4LSB) in analog output, the differential linearity error would be 1.83mV, or 3/4LSB. The AD567K and T have a max differential linearity error of 1/2LSB, which specifies that every step will be at least 1/2LSB and at most 1 1/2 LSB.

The differential nonlinearity temperature coefficient must also be considered if the device is to remain monotonic over its full operating temperature range. A differential nonlinearity temperature coefficient of 1.0ppm/°C could, under worst case conditions for a temperature change of +25°C to +125°C, add 0.01% (100°C x 1.0ppm/°C) of error. The resulting error could then be as much as 0.01% + 0.006% (initial error, 1/4LSB) = 0.016% of F.S. (1/2LSB represents 0.012% of F.S.). To be sure of accurate performance all versions of the AD567 are 100% tested for monotonicity over the full operating temperature range.

ANALOG CIRCUIT CONNECTIONS

The standard current-to-voltage conversion connections using an operational amplifier are shown here with the preferred trimming techniques. If a low offset operational amplifier (AD510L; AD517L; AD741L; AD301AL; AD OP-07) is used, excellent performance can be obtained in many situations without trimming (an op amp with less than 0.5mV max offset voltage should be used to keep offset errors below 1/2LSB). Unipolar zero will typically be within ±1/2LSB (plus op amp offset), and full scale accuracy will be within 0.1% (0.25% max). Substituting a 50Ω resistor for the 100Ω bipolar offset trimmer will give a bipolar zero error typically within ±2LSB (0.05%).

The AD544 is recommended for buffered voltage-output applications which require fast settling time to ±1/2LSB. The feedback capacitor is shown with the optimum value for each application; this capacitor is required to compensate for the 25 picofarad DAC output capacitance.

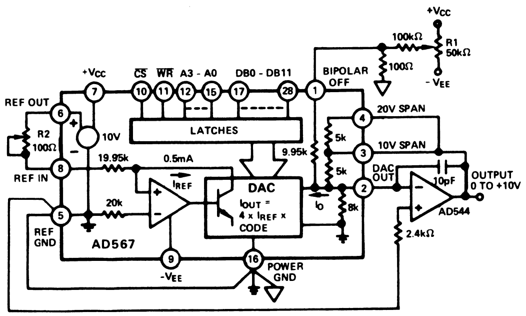


Figure 1. 0 to +10V Unipolar Voltage Output

FIGURE 1. UNIPOLAR CONFIGURATION

This configuration will provide a unipolar 0 to +10 volt output range. In this mode, the bipolar terminal, pin 1, should be grounded if not used for trimming.

STEP I . . . ZERO ADJUST

Turn all bits OFF and adjust zero trimmer R1, until the output reads 0.000 volts (1LSB = 2.44mV). In most cases this trim is not needed, and pin 1 should be connected to pin 5.

STEP II . . . GAIN ADJUST

Turn all bits ON and adjust 100Ω gain trimmer R2, until the output is 9.9976 volts. (Full scale is adjusted to 1LSB less than nominal full scale of 10.000 volts.) If a 10.2375V full scale is desired (exactly 2.5mV/bit), insert a 120Ω resistor in series with the gain resistor at pin 3 to the op amp output.

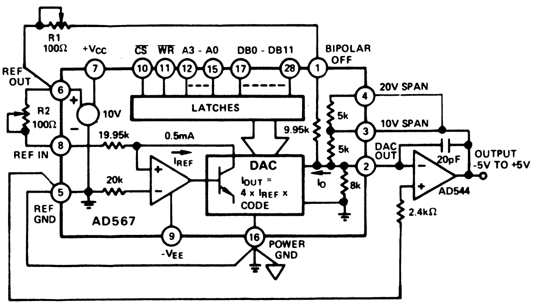


Figure 2. ±5V Bipolar Voltage Output

FIGURE 2. BIPOLAR CONFIGURATION

This configuration will provide a bipolar output voltage from -5.000 to +4.9976 volts, with positive full scale occurring with all bits ON (all 1's).

STEP I . . . OFFSET ADJUST

Turn OFF all bits. Adjust 100Ω trimmer R1 to give -5.000 volts output.

STEP II . . . GAIN ADJUST

Turn ON All bits. Adjust 100Ω gain trimmer R2 to give a reading of +4.9976 volts.

Please note that it is not necessary to trim the op amp to obtain full accuracy at room temperature. In most bipolar situations, an op amp trim is unnecessary unless the untrimmed offset drift of the op amp is excessive.

FIGURE 3 OTHER VOLTAGE RANGES

The AD567 can also be easily configured for a unipolar 0 to +5 volt range or ±2.5 volt and ±10 volt bipolar ranges by using the additional 5k application resistor provided at the 20 volt span R terminal, pin 4. For a 5 volt span (0 to +5 or ±2.5), the two 5k resistors are used in parallel by shorting pin 4 to pin 2 and connecting pin 3 to the op amp output and the bipolar offset either to ground for unipolar or to REF OUT for the bipolar range. For the ±10 volt range (20 volt span) use the 5k resistors in series by connecting only pin 4 to the op amp output and the bipolar offset connected as shown. The ±10 volt option is shown in Figure 3.

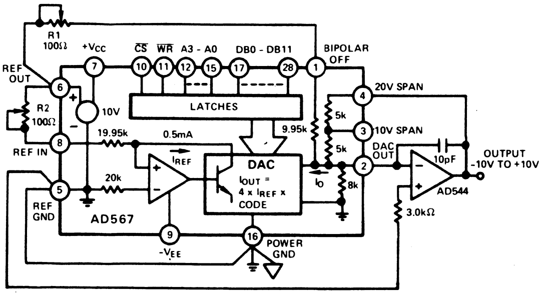


Figure 3. ±10V Voltage Output

The internal resistor values shown in Figures 1, 2, and 3 are nominal values only, as is the output current. These values are subject to an absolute tolerance of approximately ±20%. Furthermore, the resistors in the AD567 exhibit a temperature coefficient of approximately –50ppm/°C. While these absolute tolerances may appear excessively wide, the ratios of the resistor values and tracking TC are extremely well-controlled. In applications where the internal feedback resistor determines the output voltage range it is the ratios which determine the accuracy. However, in applications where the desired full scale range requires use of an external resistor, sufficient trim range must be provided to compensate for the tolerance of the internal resistance.

INTERNAL/EXTERNAL REFERENCE USE

The AD567 has an internal low-noise buried zener diode reference which is trimmed for absolute accuracy and temperature coefficient. This reference is buffered and optimized for use in a high speed DAC and will give long-term stability equal or superior to the best discrete zener reference diodes. The performance of the AD567 is specified with the internal reference driving the DAC since all trimming and testing (especially for full scale error and bipolar offset) is done in this configuration.

The AD567 can be used with an external reference, but may not have sufficient trim range to accommodate a reference which does not match the internal reference.

The internal reference has sufficient buffering to drive external circuitry in addition to the reference currents required for the DAC (typically 0.5mA to Ref In and 1.0mA to Bipolar Offset). A minimum of 0.1mA is available for driving external loads. The AD567 reference output should be buffered with an external op amp if it is required to supply additional output current. The reference is typically trimmed to ±0.2%, then tested and guaranteed to ±1.0% max error. The temperature coefficient is comparable to that of the full scale TC for a particular grade.

OUTPUT VOLTAGE COMPLIANCE

The AD567 has a typical output compliance range from –1.5 to +10 volts. The current-steering output stages will be unaffected by changes in the output terminal voltage over that range. However, there is an equivalent output impedance of 8k in parallel with 25pF at the output terminal which produces an equivalent error current if the voltage deviates from analog common. This is a linear effect which does not change with input code. Operation beyond the compliance limits may cause either output stage saturation or breakdown which results in nonlinear performance. Compliance limits are not affected by the positive power supply, but are a function of output current and negative supply, as shown in Figure 4.

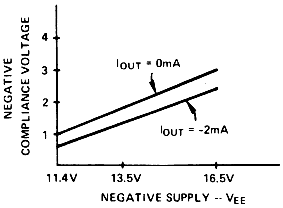


Figure 4. Typical Negative Compliance Range vs. Negative Supply

GROUNDING RULES

The AD567 brings out separate reference and power grounds to allow optimum connections for low noise and high speed performance. These grounds should be tied together at one point, usually the device power ground. The separate ground returns are provided to minimize current flow in low-level signal paths. In this way, logic return currents are not summed into the same return path with analog signals.

The reference ground at pin 5 is the ground point for the internal reference and is thus the "high quality" ground for the AD567; it should be connected directly to the analog reference point of the system. The power ground at pin 16 can be connected to the most convenient ground point; analog power return is preferred. If power ground contains high frequency noise beyond 200mV, this noise may feed through the converter, thus some caution will be required in applying these grounds.

It is also important to properly apply decoupling capacitors on the power supplies for the AD567 and the output amplifier. The correct method for decoupling is to connect a capacitor from each power supply pin of both the AD567 and the amplifier directly to the reference ground pin of the AD567. Any load driven by the output amplifier should also be referred to the reference ground pin.

Output Range	Connect Pin 3 to:	Connect Pin 4 to:	Connect Pin 1 to:
0 to +5V	Amplifier Output	Pin 2	Pin 5
0 to +10V	Amplifier Output	Amplifier Output	Pin 5
-2.5V to +2.5V	Amplifier Output	Pin 2	Pin 6 (through 50Ω)
-5V to +5V	Amplifier Output	Amplifier Output	Pin 6 (through 50Ω)
-10V to +10V	–	Amplifier Output	Pin 6 (through 50Ω)

Table 1. Connections for Various Output Ranges

DIGITAL CIRCUIT DETAILS

The bus interface logic of the AD567 consists of four independently addressable registers in two ranks. The first rank consists of three four-bit registers which can be loaded directly from a 4-, 8-, 12-, or 16-bit microprocessor bus. Once the complete 12-bit data word has been assembled in the first rank, it can be loaded into the 12-bit register of the second rank. This double-buffered organization avoids the generation of spurious analog output values. Figure 5 shows the block diagram of the AD567 logic section.

The latches are controlled by the address inputs, A0–A3, and the $\overline{CS}$ and $\overline{WR}$ inputs. All control inputs are active low, consistent with general practice in microprocessor systems. The $\overline{CS}$ and $\overline{WR}$ inputs must both be low for any operation to occur. The four address lines each enable one of the four latches, as indicated in Table 2 below.

All latches in the AD567 are level-triggered. This means that data present during the time when the control signals are valid will enter the latch. When any one of the control signals returns high, the data is latched.

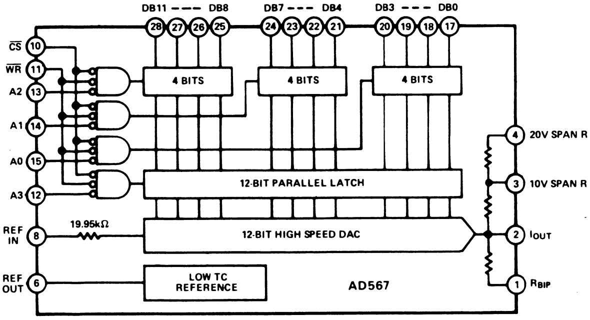


Figure 5. AD567 Block Diagram

$\overline{CS}$	$\overline{WR}$	A3	A2	A1	A0	Operation
1	X	X	X	X	X	No Operation
X	1	X	X	X	X	No Operation
0	0	1	1	1	0	Enable 4 LSBs of First Rank
0	0	1	1	0	1	Enable 4 Middle Bits of First Rank
0	0	1	0	1	1	Enable 4 MSBs of First Rank
0	0	0	1	1	1	Loads Second Rank from First Rank
0	0	0	0	0	0	All Latches Transparent

"X" = Don't Care

Table 2. AD567 Truth Table

MICROPROCESSOR BUS INTERFACING

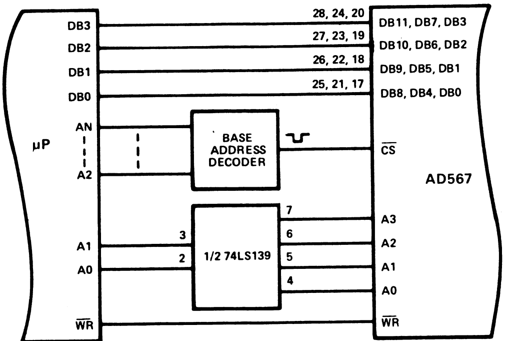
The AD567 interface logic is configured with enough flexibility to allow relatively simple interface to the various microprocessor bus structures. The required control signals, $\overline{CS}$ and $\overline{WR}$, are easily derived in most systems. Usually a base address is decoded, and this active-low signal is used for $\overline{CS}$ (Chip Select). Either I/O Write or Memory Write can be used for $\overline{WR}$, depending on the system design. The relative timing of these signals is not important and they are interchangeable.

The address lines determine which of the latches are being enabled. It is permissible to enable two or more latches simultaneously, as in the examples of 8-, 12-, and 16-bit interfaces.

The double-buffered latch permits data to be loaded into the first rank latches of several AD567s and subsequently strobed into the second rank registers of all the DACs. All analog outputs will then update simultaneously.

4-BIT PROCESSOR INTERFACE

Many industrial control applications use four-bit microprocessors but require 12-bit accurate analog control voltages. The AD567 is well suited to these applications, due to its flexible control structure.



ADDRESS	OPERATION
X00	LOAD 4LSBs
X01	LOAD 4 MIDDLE BITS
X10	LOAD 4 MSBs
X11	UPDATE OUTPUT

Figure 6. Addressing for 4-Bit Microprocessor Interface

Each AD567 occupies four locations in a 4-bit microprocessor system. A single 74LS139 2-to-4 decoder is used to provide sequential addresses for the four AD567 registers. $\overline{CS}$ is derived from an address decoder driven from the high order address bits. The system $\overline{WR}$ is used for the $\overline{WR}$ input of the AD567.

8-BIT MICROPROCESSOR INTERFACE

The AD567 interfaces easily to 8-bit microprocessor systems of all types. The control logic makes possible the use of right- or left-justified data formats.

Whenever a 12-bit DAC is loaded from an 8-bit bus, two bytes are required. If the program considers the data to be a 12-bit binary fraction (between 0 and 4095/4096), the data is left-justified, with the eight most significant bits in one byte and the remaining bits in the upper half of another byte. Right-justified data calls for the eight least significant bits to occupy one byte, with the 4 most significant bits residing in the lower half of another byte, simplifying integer arithmetic.

DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4

DB3	DB2	DB1	DB0	X	X	X	X

a. Left Justified

X	X	X	X	DB11	DB10	DB9	DB8

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

b. Right Justified

Figure 7. 12-Bit Data Formats for 8-Bit Systems

Figure 8 shows an addressing scheme for use with an AD567 set up for left-justified data in an 8-bit system. The base address is decoded from the high-order address bits and the resultant active-low signal is applied to $\overline{CS}$. The two LSBs of the address bus are connected as shown to the AD567 address inputs. The latches now reside in two consecutive locations, with location X01 loading the four LSBs and location X10 loading the eight MSBs and updating the output.

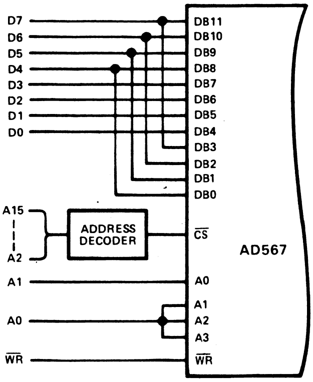


Figure 8. Left-Justified 8-Bit Bus Interface

Right-justified data can be similarly accommodated. The overlapping of data lines is reversed, and the address connections are slightly different. The AD567 still occupies two adjacent locations in the processor's memory map.

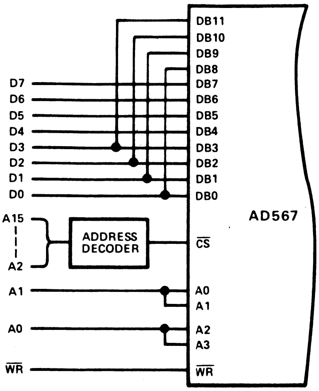
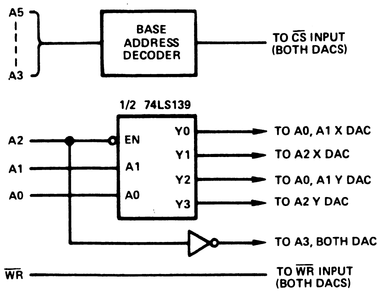


Figure 9. Right-Justified 8-Bit Bus Interface

USING MULTIPLE AD567 DACS IN 8-BIT SYSTEMS

Many applications use multiple digital-to-analog converters driven from the same data bus. For example, automatic test equipment systems often require all analog outputs to be produced simultaneously. Vector-scan graphic systems require that the X and Y coordinates of the stroke endpoints be updated simultaneously. The AD567 can be used with a very simple address decoder to perform this function, as shown in Figure 10. The 74LS139 two-line to four-line decoder and one inverter provide a set of distinct address pulses which assign the registers of the two DACs to a block of consecutive memory locations. In this circuit, write operations to addresses X000 and X001 load the first rank registers of one DAC in a right-justified data format. Addresses X010 and X011 load the first tank of another DAC, also in a right-justified format. A write to any address from X100 to X111 will load the second rank registers of both DACs simultaneously from their respective first rank registers.



A2	A1	A0	OPERATION
0	0	0	LOAD 8LSB – X DAC
0	0	1	LOAD 4MSB – X DAC
0	1	0	LOAD 8LSB – Y DAC
0	1	1	LOAD 4MSB – Y DAC
1	X	X	UPDATE BOTH DACS

Figure 10. Addressing for Two DACs (Right-Justified) on 8-Bit Bus

USING THE AD567 WITH 12- AND 16-BIT BUSES

The AD567 is easily interfaced to 12- and 16-bit data buses. In this operation, all four address lines (A0 through A3) are tied to low, and the latch is enabled by $\overline{CS}$ and $\overline{WR}$ going low. The AD567 thus occupies a single memory location.

This configuration renders the second rank register transparent, using the first rank of registers as the data latch. The $\overline{CS}$ input can be driven from an active-low decoded address, and $\overline{WR}$ can be the system $\overline{WR}$ signal. It should be noted that any data bus activity during the period when $\overline{CS}$ and $\overline{WR}$ are both active will cause activity at the AD567 output. If data is not guaranteed stable during this period, the second rank register can be used to provide double buffering.

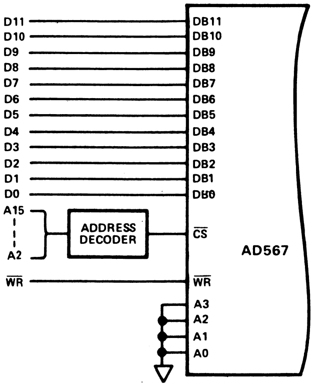


Figure 11. Connections for 12- and 16-Bit Bus Interface

DIGITAL INPUT CONSIDERATIONS

The threshold of the digital input circuitry is set at 1.4 volts and does not vary with supply voltage. The input lines can thus interface with any type of 5 volt logic. The configuration of the input circuit is shown in Figure 12. The input line can be modeled as a 30kΩ resistance connected to a –0.7V rail, in parallel with a 5pF capacitance to ground.

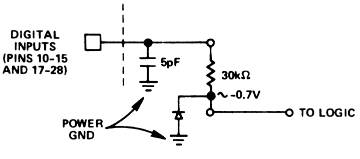


Figure 12. Equivalent Digital Input Circuit

ANALOG
DEVICES

8-Bit Monolithic Multipling D/A Converter

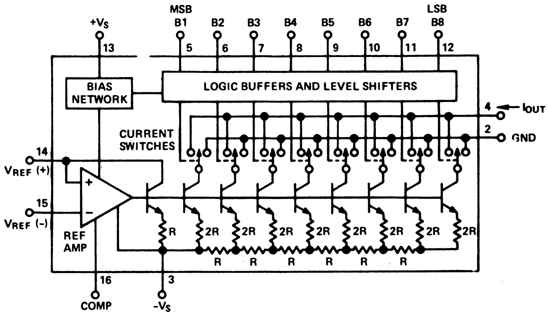
AD1408/AD1508*

PRELIMINARY TECHNICAL DATA

FEATURES

Improved Replacement for Industry Standard 1408/1508
Improved Settling Time: 250ns typ
Improved Linearity: ±0.1% Accuracy Guaranteed Over Temperature Range (-9 Grade)
High Output Voltage Compliance: +0.5V to -5.0V
Low Power Consumption: 157mW typ
High Speed 2-Quadrant Multiplying Input: 4.0mA/µs Slew Rate
Single Chip Monolithic Construction
Hermetic 16-Pin Ceramic DIP
Low Cost

AD1408/AD1508 FUNCTIONAL BLOCK DIAGRAM



TO-116

PRODUCT DESCRIPTION

The AD1408 and AD1508 are low cost monolithic integrated circuit 8-bit multiplying digital-to-analog converters, consisting of matched bipolar switches, a precision resistor network and a control amplifier. The single chip is mounted in a hermetically sealed ceramic 16 lead dual-in-line package.

Advanced circuit design and precision processing techniques result in significant performance advantages over older industry standard 1408/1508 devices. The maximum linearity error over the specified operating temperature range is guaranteed to be less than ±¼LSB (-9 grade) while settling time to ±½LSB is reduced to 250ns typ. The temperature coefficient of gain is typically 20ppm/°C and monotonicity is guaranteed over the entire operating temperature range.

The AD1408/AD1508 is recommended for all low-cost 8-bit DAC requirements; it is also suitable for upgrading overall performance where older, less accurate and slower 1408/1508 devices have been designed in. The AD1408 series is specified for operation over the 0 to +75°C temperature range, the AD1508 series for operation over the entire military temperature range of -55°C to +125°C.

PRODUCT HIGHLIGHTS

1. Monolithic IC construction makes the AD1408/AD1508 an optimum choice for applications where low cost is a major consideration.
2. The AD1408/AD1508 directly replaces other devices of this type.
3. Versatile design configuration allows voltage or current outputs, variable or fixed reference inputs, CMOS or TTL logic compatibility and a wide choice of accuracy and temperature range specifications.
4. Accuracies within ±¼LSB allow performance improvement of older applications without redesign.
5. Faster settling time (250ns typ) permits use in higher speed applications.
6. Low power consumption improves stability and reduces warm-up time.
7. The AD1408/AD1508 multiplies in two quadrants when a varying reference voltage is applied. When multiplication is not required, a fixed reference is used.
8. The device is packaged in a hermetically-sealed ceramic 16 lead dual-in-line package. Processing to MIL-STD-883 level B is available.

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*Covered by Patent Numbers 3,961,326; 4,141,004.

SPECIFICATIONS (typical @ +25°C and V_{CC} = +5.0V dc, V_{EE} = -15V dc unless otherwise noted)

MAXIMUM RATINGS

RATING	SYMBOL	VALUE	UNIT
POWER SUPPLY VOLTAGE	V_{CC}	+5.5	V dc
	V_{EE}	-16.5	V dc
DIGITAL INPUT VOLTAGE	V_5 thru V_{12}	+5.5, 0	V dc
APPLIED OUTPUT VOLTAGE	V_0	+0.5, -5.2	V dc
REFERENCE CURRENT	I_{14}	5.0	mA
REFERENCE AMPLIFIER INPUTS	V_{14}, V_{15}	V_{CC}, V_{EE}	V dc
POWER DISSIPATION			
(Package Limitation)		1000	mW
Derate above T_A = +25°C	P_D	6.7	mW/°C
OPERATING TEMPERATURE RANGE			
AD1408 Series	T_A	0 to +75	°C
AD1508 Series	T_A	-55 to +125	°C
STORAGE TEMPERATURE RANGE	T_{STG}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5.0V dc, V_{EE} = -15V dc, $\frac{V_{REF}}{R14}$ = 2.0mA, **AD1508 Series:** T_A = -55°C to +125°C **AD1408 Series:** T_A = 0 to +75°C unless otherwise noted. All digital inputs at high logic level.)

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
RELATIVE ACCURACY					
(Error Relative to Full Scale I_O)					
AD1508-9, AD1408-9	E_r	–	–	±0.10	%
AD1508-8, AD1408-8	E_r	–	–	±0.19	%
AD1408-7	E_r	–	–	±0.39	%
SETTLING TIME					
to Within 1/2LSB [Includes t_{PLH}]					
(T_A = +25°C)	t_S	–	250	–	ns
PROPAGATION DELAY TIME					
T_A = +25°C	t_{PLH}, t_{PHL}	–	30	100	ns
OUTPUT FULL SCALE CURRENT DRIFT	TCI_O	–	-20	–	ppm/°C
DIGITAL INPUT LOGIC LEVELS (MSB)					
High Level, Logic "1"	V_{IH}	2.0	–	–	V dc
Low Level, Logic "0"	V_{IL}	–	–	0.8	V dc
DIGITAL INPUT CURRENT (MSB)					
High Level, V_{IN} = 5.0V	I_{IH}	–	0	0.04	mA
Low Level, V_{IL} = 0.8V	I_{IL}	–	-0.4	-0.8	mA
REFERENCE INPUT BIAS CURRENT					
(Pin 15)	I_{15}	–	-1.0	-3.0	µA
OUTPUT CURRENT RANGE					
V_{EE} = -5.0V	I_{OR}	0	2.0	2.1	mA
V_{EE} = -6.0V to -15V	I_{OR}	0	2.0	4.2	mA
OUTPUT CURRENT					
V_{REF} = 2.000V, R14 = 1000Ω	I_O	1.9	1.99	2.1	mA
OUTPUT CURRENT					
(All Bits Low)	I_O (min)	–	0	4.0	µA
OUTPUT VOLTAGE COMPLIANCE					
($E_r \leq 0.19\%$ at T_A = +25°C)					
V_{EE} = -5V	V_O	–	–	-0.6, +0.5	V dc
V_{EE} below -10V	V_O	–	–	-5.0, +0.5	V dc
REFERENCE CURRENT SLEW RATE	SRI_{REF}	–	4.0	–	mA/µs
OUTPUT CURRENT POWER SUPPLY SENSITIVITY	$PSSI_O$	–	0.5	2.7	µA/V
POWER SUPPLY CURRENT					
(All Bits Low)	I_{CC}	–	+9	+14	mA
	I_{EE}	–	-7.5	-13	mA
POWER SUPPLY VOLTAGE RANGE					
(T_A = +25°C)	V_{CCR}	+4.5	+5.0	+5.5	V dc
	V_{EER}	-4.5	-15	-16.5	V dc
POWER DISSIPATION					
All Bits Low					
V_{EE} = -5.0V dc	P_D	–	82	135	mW
V_{EE} = -15V dc	P_D	–	157	265	mW
All Bits High					
V_{EE} = -5.0V dc	P_D	–	70	–	mW
V_{EE} = -15V dc	P_D	–	132	–	mW

Specifications subject to change without notice.

APPLYING THE AD1408/1508

Reference Amplifier Drive and Compensation

Figures 2a and 2b are the connection diagrams for using the AD1408/AD1508 in basic voltage output modes. In Figure 2a, a positive reference voltage, V_{REF}, is converted to a current by resistor R14. This reference current determines the scale factor for the output current such that the full scale output is 1LSB (1/256) less than the reference current. R15 provides bias current compensation to the reference control amplifier to minimize temperature drift; it is nominally equal to R14 although it needn't be a stable precision resistor. This configuration develops a negative output voltage across R_L and requires a positive V_{REF}.

If a negative V_{REF} is to be used, connections to the reference control amplifier must be reversed as shown in Figure 2b. This circuit also delivers a negative output voltage, but presents a high impedance to the reference source. The negative V_{REF} must be at least 4 volts above the V_{EE} supply.

Two quadrant multiplication may be performed by applying a bipolar ac signal as the reference as long as pin 14 is positive relative to pin 15 (reference current must flow into pin 14). If the ac reference is applied to pin 14 through R14, a negative voltage equal to the negative peak of the ac reference must be applied through R15 to pin 15; if the ac reference is applied to pin 15 through R15, a positive voltage equal to the positive peak of the ac reference must be applied through R14 to pin 14.

When a dc reference is used, capacitive bypass from reference to ground will improve noise rejection.

The compensation capacitor, C, provides proper phase margin for the reference control amplifier. As R14 is increased, the closed-loop gain of the amplifier is decreased, therefore C must be increased. For R14 = 1.0kΩ, 2.5kΩ and 5.0kΩ, minimum values of capacitance are 15pF, 37pF and 75pF respectively. C may be tied to either V_{EE} or ground, but tying it to V_{EE} increases negative supply noise rejection. If the reference is driven by a high-impedance current source, heavy compensation of the amplifier is required; this causes a reduction in overall bandwidth.

Output Current Range

The nominal value for output current range is 0 to 1.992mA as determined by a 2mA reference current. If V_{EE} is more negative than -7.0 volts, this range may be increased to a maximum of 0 to 4.2mA. An increase in speed may be realized at increased output current levels, but power consumption will increase, possibly causing small shifts in linearity.

Pin 1, range control, may be grounded or unconnected. Although other older devices of this type require different terminations for various applications, the AD1408/AD1508 compensates automatically. This pin is not connected internally, therefore any previously installed connections will be tolerated.

Output Voltage Range

The voltage on pin 4 is restricted to a +0.5 to -0.6 volt range when V_{EE} = -5V. When V_{EE} is more negative than -10 volts, this range is extended to +0.5 to -5.0 volts. If the current into pin 14 is 2mA (full-scale output current = 1.992mA), a 2.5kΩ resistor between the output, pin 4, and ground will provide a 0 to -4.980 volt full-scale. If R_L exceeds 500Ω however, the settling time of the device is increased.

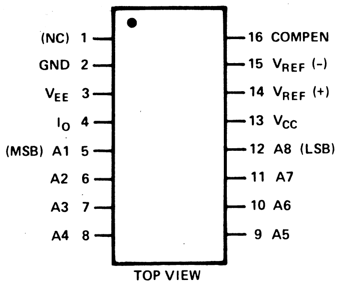
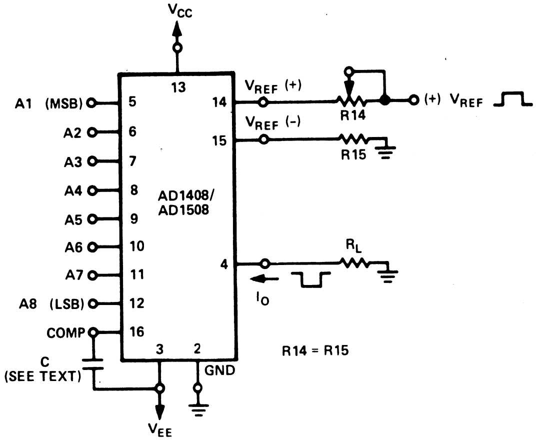
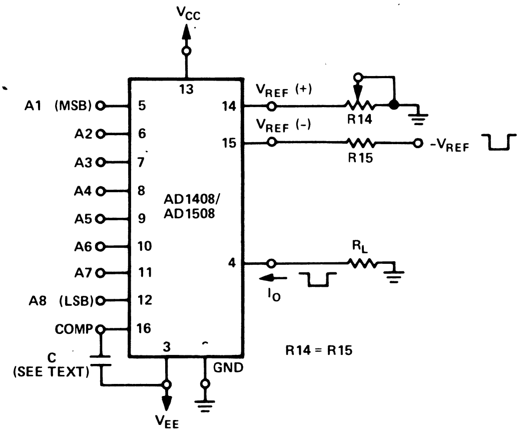


Figure 1. Pin Connections



a. Connections for Use with Positive Reference



b. Connections for Use with Negative Reference

Figure 2. Basic Connections

Voltage Output

A low impedance voltage output may be derived from the output current of the AD1408/AD1508 by using an output amplifier as shown in Figure 3. The output current I_O flows in R_O to create a positive-going voltage range at the output of amplifier A1. R_O may be chosen for the desired range of output voltage; the complete circuit transfer function is given in Figure 3.

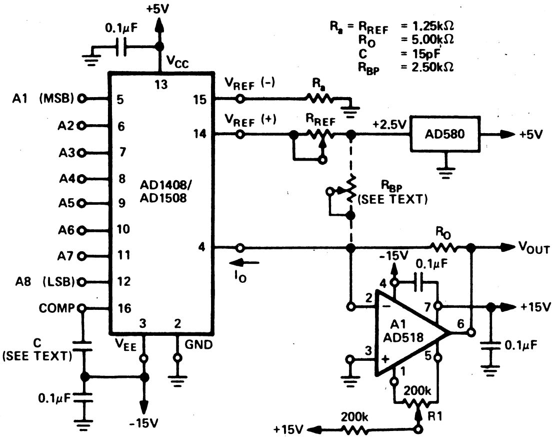
If a bipolar output voltage range is desired, R_{BP}, shown dotted, must be installed. Its purpose is to provide an offset equal to one-half of full-scale at the output of A1. The procedure for calibrating the circuit of Figure 3 is as follows:

Calibration for Unipolar Outputs (No R_{BP})

1. With all bits "OFF", adjust the A1 null-pot, R1, for V_{OUT} = 0.00V.
2. With all bits "ON", adjust R_{REF} for V_{OUT} = (Nominal Full Scale) − 1LSB = +9.961 volts

Calibration for Bipolar Outputs (R_{BP} installed, R1 not required)

1. With all bits "OFF", adjust R_{BP} for V_{OUT} = -F.S. = -5.000 volts
2. With Bit 1 (MSB) "ON", and all other Bits "OFF", adjust R_{REF} for V_{OUT} = 0.000V.
3. With all bits "ON", verify that E_{OUT} = +5.000V− 1LSB = 4.961V.



$$V_{OUT} = \frac{V_{REF}}{R_{REF}}(R_O)\left[\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256}\right]$$

ADJUST V_{REF}, R_{REF} OR R_O SO THAT WITH ALL DIGITAL INPUTS AT LOGIC "1", V_{OUT} = 9.961 VOLTS:

$$V_{OUT} = \frac{2.5}{1.25k\Omega}(5k\Omega)\left[\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64} + \frac{1}{128} + \frac{1}{256}\right] = 9.961 \text{ VOLTS}$$

Figure 3. Typical Connection Diagram, AD1408/AD1508, Voltage Output, Fixed Reference

AD1408/AD1508 ORDERING GUIDE

MODEL	ACCURACY (±% F.S.)	TEMP. RANGE (°C)	PACKAGE STYLE[1]
AD1408-7D	0.39	0 to +75	Q16A
AD1408-8D	0.19	0 to +75	Q16A
AD1408-9D	0.10	0 to +75	Q16A
AD1508-8D	0.19	-55 to +125	Q16A
AD1508-9D	0.10	-55 to +125	Q16A
AD1508-8D/ 883B	0.19	-55 to +125	Q16A
AD1508-9D/ 883B	0.10	-55 to +125	Q16A

[1] SEE SECTION 20 FOR PACKAGE OUTLINE INFORMATION

ANALOG DEVICES

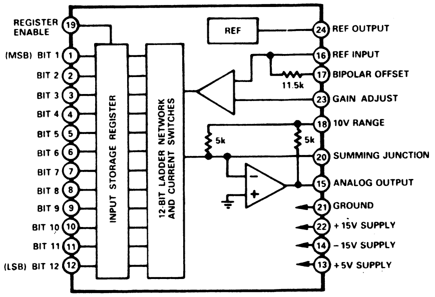
Complete, Voltage Output 12-Bit DAC

AD3860

FEATURES

Resolution: 12 Bits
Nonlinearity: ±1/2LSB T_{min} to T_{max}
Microprocessor Compatible
Small Size: 24 pin DIP
Fast Settling: 5μs
Internal Reference
Internal Output Amplifier

AD3860 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD3860 is a precision 12-bit D/A converter designed for direct interface to 4- or 8-bit microprocessors.

The functional diagram shows that the AD3860 consists of a 12-bit input storage register, a 12-bit DAC, internal reference, and a fast output amplifier. It is TTL compatible and the input register's enable input facilitates deglitching and microprocessor interfacing. The 6.3 volt voltage reference can be used internally or externally. All units are laser trimmed to operate from this reference. The output amplifier gives the user a voltage output and combines with the other features of this circuit to produce a functionally complete digital to analog converter.

The AD3860 is laser trimmed to achieve ±¼LSB linearity typical and ±½LSB maximum over the full operating temperature range. The AD3860 is well suited for wide temperature range performance as monotonicity is guaranteed over the full temperature range. Typical full scale gain T.C. is 10ppm/°C.

The AD3860 is available in three versions. The AD3860K is specified for use over 0 to +70°C temperature range. The AD3860S is specified for the −55°C to +125°C temperature range and is especially recommended for high reliability needs in harsh environments. The S version is available proccessed to MIL-STD-883, Level B. All units are in small 24 pin, hermetically-sealed ceramic DIPs.

PRODUCT HIGHLIGHTS

1. The AD3860 is a functionally complete voltage output DAC with voltage reference, digital latches, and output amplifier in a single hybrid package.
2. The input buffer latches permit interface to microprocessor data busses. All logic inputs are TTL or 5 volt CMOS compatible.
3. Laser trimming the thin-film resistors assures superior linearity and accuracy stability over temperature. Both commerical temperature range and military temperature range models have ±½LSB linearity maximum guaranteed over the full operating temperature range.
4. Monotonicity is also guaranteed over the full operating temperature range. The typical full scale temperature coefficient is 10ppm/°C.
5. The internal 6.3 volt reference is accurate to within ±2%. All units are actively laser trimmed to operate from this reference.
6. The fast output amplifier provides a voltage output with a 5μs settling time. The AD3860 is designed for military, industrial, and OEM applications where high speed D/A conversion is required.

SPECIFICATIONS (T_A = +25°C, rated power supplies unless otherwise noted)

Model	AD3860K	AD3860S
DIGITAL INPUTS		
Resolution	12 Bits	*
Logic Coding: Unipolar Ranges	Complementary Straight Binary	*
Bipolar Ranges	Complementary Offset Binary	*
Logic Levels (TTL Compatible): Logic "1"	+2.0V dc min, +5.5V dc max	*
Logic "0"	0V dc min, 0.7V dc max	*
Input Currents		
Data Inputs: Logic "1"	30μA max	*
Logic "0"	−0.6mA max	*
Register Enable: Logic "1"	60μA max	*
Logic "0"	−1.2mA max	*
ANALOG OUTPUTS		
Output Impedance	0.5Ω typ	*
Output Current	±10mA typ, ±5mA min	*
ACCURACY		
Linearity Error	±¼LSB[1] typ, ±½LSB max	±½LSB max
Differential Linearity Error	±½LSB typ, ±1LSB max	±1LSB max
Monotonicity	Guaranteed Over Temperature	*
Full Scale Absolute Accuracy Error[2]	±0.05% FSR[3] typ, ±0.01% FSR max	*
Over Temperature	±0.15% FSR typ, ±0.3% FSR max	*
Zero Error	±0.025% FSR typ, ±0.05% FSR max	*
Over Temperature	±0.05% FSR typ, ±0.1% FSR max	*
Gain Error	±0.1% typ	*
DRIFT		
Gain	±10ppm/°C typ	*
Offset	±5ppm/°C typ	*
DYNAMIC CHARACTERISTICS		
Settling Time to ±0.01% for: 20V Step	5μs typ, 7μs max	*
10V Step	3μs typ, 5μs max	*
Output Slew Rate	20V/μs typ	*
Register Enable[4]		
Pulse Width	60ns typ	*
Setup Time Digital Data to Enable	40ns typ	*
INTERNAL REFERENCE VOLTAGE		
Voltage	+6.3V typ	*
Accuracy	±2% typ	*
External Current	2.5mA max	*
POWER SUPPLIES		
Power Supply Range: +15V Supply	+14.55V min, +15.45V max	*
−15V Supply	−14.55V max, −15.45V min	*
+5V Supply	+4.75V min, +5.25V max	*
Power Supply Rejection: +15V Supply	±0.002% FSR/% V_S typ, ±0.04% FSR/% V_S max	*
−15V Supply	±0.002% FSR/% V_S typ, ±0.004% FSR/% V_S max	*
Current Drain: +15V Supply	10mA typ, 20mA max	*
−15V Supply	−12mA typ, −30mA max	*
+5V Supply	30mA typ, 50mA max	*
Power Consumption	675mW typ, 1W max	*
TEMPERATURE RANGE		
Operating	0 to +70°C	−55°C to +125°C
Storage	−65°C to +150°C	*
PACKAGE OPTION[5]		
24-Pin DIP	HY24C	*

NOTES:

[1] Least Significant Bit (LSB).

[2] Absolute Accuracy Error includes gain, offset, linearity, noise and all other errors and is specified without adjustments.

[3] FSR is Full Scale Range and is 20V for ±10 range.

[4] The AD3860's analog output will follow its digital input when register enable is a logic "0". Digital Input data will be latched and analog output voltage constant when register enable is a logic "1".

[5] See Section 20 for package outline information.

*Same as AD3860K.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

+ 15 Volt Supply (pin 22)	+ 18V
− 15 Volt Supply (pin 14)	− 18V
+ 5 Volt Supply (pin 13)	− 0.5V to + 7V
Register Enable (pin 19)	− 0.5V to + 5.5V
Digital Inputs (pins 1–12)	− 0.5V to + 5.5V

APPLICATIONS INFORMATION

Layout Considerations

Proper layout and decoupling is necessary to obtain the AD3860's specified accuracy. Ground (pin 21) must be tied to circuit analog ground as close to the package as possible. Grounding through a large ground plane beneath the package is preferred.

Power supplies should be decoupled with electrolytic or tantalum capacitors near the unit. A 1µF capacitor in parallel with a 0.01µF ceramic capacitor on all supplies is recommended.

Coupling between analog and digital signals should be minimized to avoid noise pick up. Use short jumpers to tie the reference output (pin 24) to the reference input (pin 16) and to tie the bipolar offset (pin 17) to the summing junction (pin 20).

If the external full scale and zero adjustments are used, the series 6.8MΩ resistors should be placed as close to the unit as possible.

Reference Output

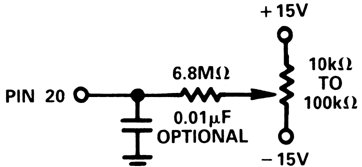
The AD3860 is laser trimmed to operate from the internal 6.3 volt voltage reference. The user has the option of supplying an external reference but for specified operation the reference output (pin 24) must be connected to the reference input (pin 16). The internal reference can be used to drive an external load, but it should be buffered if load current will exceed 100µA.

Optional Full Scale and Zero (− Full Scale) Adjustments

The AD3860 will operate as specified without adjustment, however, absolute accuracy error can be reduced to ± 1LSB by trimming as described below. Adjustments should be made after warmup. Make the full scale adjustment before the zero (− full scale) adjustment. We recommend multiturn potentiometers with maximum temperature coefficients of 100ppm/°C. Series resistors can be ± 20% carbon composition or better. If these adjustments are not used pins 20 and 23 should be connected as described in the layout considerations section.

Zero (− Full Scale) Adjustment

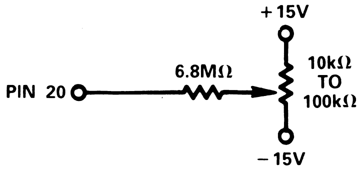
Connect the potentiometer as shown and apply all "1s" to the digital inputs. Adjust the potentiometer until the analog output is equal to zero volts for unipolar output ranges and minus full scale for bipolar output ranges.



RANGE OF ADJUSTMENT = ± 0.35% FSR

Full Scale Adjustment

Connect the potentiometer as shown and apply all "0s" to the digital inputs. Adjust the potentiometer for the maximum chosen analog output.



RANGE OF ADJUSTMENT = ± 0.2% FSR

OUTPUT VOLTAGE RANGE SELECTION

Output Range	0 to +10V	±5V	±10V
Pin Connection			
Connect Pin 24 to	16	16	16
Connect Pin 17 to	21	20	20
Connect Pin 15 to	18	18	NC
Connect Pin 19 to	Register Enable	Register Enable	Register Enable
Connect Pin 20 to	NC	17	17

INPUT LOGIC CODING

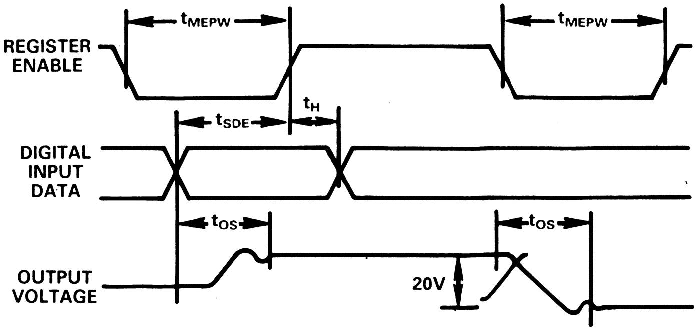
Digital Input MSB LSB	Analog Output 0 to +5V	 0 to +10V	 ±2.5V	 ±5V	 ±10V
0000 0000 0000	+4.9988V	+9.9976V	+2.4988V	+4.9976V	+9.9951V
0000 0000 0001	+4.9976V	+9.9951V	+2.4976V	+4.9951V	+9.9902V
0111 1111 1111	+2.5000V	+5.0000V	0.0000V	0.0000V	0.0000V
1000 0000 0000	+2.4988V	+4.9976V	−0.0012V	−0.0024V	−0.0049V
1111 1111 1110	+0.0012V	+0.0024V	−2.4988V	−4.9976V	−9.9951V
1111 1111 1111	0.0000V	0.0000V	−2.5000V	−5.0000V	−10.0000V

CODING NOTES:

1. For unipolar operation, the coding complementary straight binary (CSB).
2. For bipolar operation, the coding complementary offset binary (COB).
3. For FSR = 20V, 1LSB = 4.88mV.
4. For FSR = 10V, 1LSB = 2.44mV.
5. For FSR = 5V, 1LSB = 1.22mV.

REGISTER ENABLE

When the register enable (pin 19) is high (hold mode) the digital data in the input register will be latched. When the register enable is low (track mode) the converter's output will follow its input. To latch new digital data into the register, the register enable must go low for a minimum of 60ns and the digital input data must be valid for a minimum of 40ns before the register enable goes high again. See the timing diagram below.



TIMING NOTES:

t_{MEPW}	MIMINUM ENABLE PULSE WIDTH IS 60ns.
t_{SDE}	MINIMUM SETUP TIME DIGITAL INPUT DATA TO ENABLE IS 40ns.
t_H	HOLD TIME IS DEFINED AS THE REQUIRED DELAY BETWEEN THE LEADING EDGE OF REGISTER ENABLE AND THE END OF VALID INPUT DATA. THE HOLD TIME IS ZERO FOR THE AD3860.
t_{OS}	OUTPUT SETTLING TIME FOR A 20 VOLT CHANGE TO ± 1/2LSB IS 7μs MAX.

Input Register Timing Diagram

ANALOG DEVICES

CMOS LOGDAC™ Digitally Controlled Audio Attenuator

AD7110*

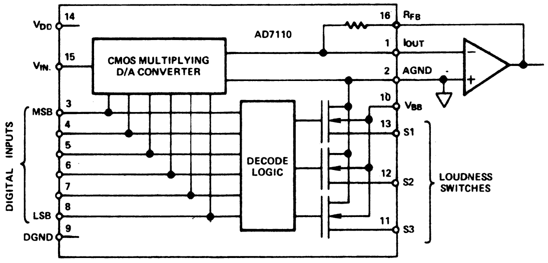
FEATURES

Attenuation Range: 0 to 88.5dB Plus Full Muting
Resolution: 1.5dB
Low Distortion: THD Better Than -98dB
IMD Better Than -92dB
Includes Switches for Loudness Compensation
Low Power Consumption
Excellent S/N Ratio: 100dB (20Hz – 20kHz)
Low Cost
Complies with DIN 45403 and DIN 45405
Latch-Proof Operation

APPLICATIONS

Digitally Controlled Audio Gain
Wide Dynamic Range D/A Converters

AD7110 FUNCTIONAL BLOCK DIAGRAM



AD7110 AUDIO ATTENUATOR

GENERAL DESCRIPTION

The AD7110 is a monolithic CMOS digitally controlled audio attenuator (patent pending). With the addition of an external operational amplifier it provides 0 to 88.5dB of attenuation in 1.5dB steps, plus full muting of the audio input signal for digital input code 1111XX, where X can be 1 or 0. The audio input is applied to the V_{IN} pin and the device delivers a logarithmically related output current which is determined by a 6-bit binary input code. Loudness compensation switches are provided on the device to enable additional bass boost at low volume settings.

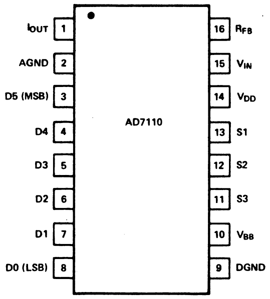
The device is manufactured using an advanced thin-film on CMOS monolithic wafer fabrication process and is packaged in a 16-pin DIP.

ORDERING INFORMATION

Model	Package	Operating Temperature Range
AD7110KN	16-Pin Plastic DIP	0 to +50°C

Package Style: (N16A)

PIN CONFIGURATION



16-PIN DIP
TOP VIEW

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*Patent Pending
LOGDAC is a trademark of Analog Devices, Inc.

AUDIO SPECIFICATIONS

(V_{DD} = +12V, V_{BB} = 0 to -12V, Pins 11-13 Open, T_A = 0 to +50°C unless otherwise noted)

PARAMETER	AD7110 WITH "IDEAL OP AMP"	AD7110 WITH TL071 OP-AMP (FIG. 1)	UNITS	TEST CONDITIONS/COMMENTS
ATTENUATION RANGE	0 to -88.5	0 to -88.5	dB	V_{IN} = 10V rms @ 1kHz
RESOLUTION	1.5 max	1.5 max	dB	Frequency Range: 20Hz to 20kHz
ATTENUATION ACCURACY (Absolute)				The AD7110 is guaranteed monotonic for all attenuation settings between 0 and -88.5dB
0dB to -48dB	±0.7 max	±0.7 max	dB	
-48dB to -88.5dB	Monotonic	Monotonic		
TOTAL HARMONIC DISTORTION (THD)	-98 max	-85 typ	dB	per DIN 45403, BLATT 2 (with input level of 1V rms)
INTERMODULATION DISTORTION (IMD)	-92 max	-79 typ	dB	per DIN 45403, BLATT 4
V_{IN}	30 max	10 max	V peak	for <1% (max) THD (Note 1)
FEEDTHROUGH ERROR	Better than -85dB @ 1kHz. Feedthrough is primarily dependent upon printed circuit board layout.			
OUTPUT NOISE VOLTAGE DENSITY	30 max	70 typ	$nV/\sqrt{Hz}$	20Hz to 20kHz (Note 2)
BANDWIDTH	D.C. to 150 min	D.C. to 250 typ	kHz	0dB Attenuation

ELECTRICAL SPECIFICATIONS

(V_{DD} = +12V, V_{BB} = 0 to -12V, Pins 11-13 Open, T_A = 0 to +50°C unless otherwise noted)

PARAMETER	LIMIT	TEST CONDITIONS/COMMENTS
ANALOG INPUT		Input resistance for a given unit is constant for all input conditions.
Input Resistance of V_{IN} (pin 15)	18kΩ max	
	9kΩ min	V_{OUT} = 0V
LOUDNESS SWITCHES		
Switch ON Resistance R_{ON}	600Ω max	Switch Current = 1mA
Switch OFF Leakage Current	1μA max	V_{switch} = +12V
Switch Coding	See Table 1	
DIGITAL INPUTS		
V_{INH}	11.5V min	
V_{INL}	0.5V max	
I_{INH}	1μA max	
I_{INL}	1μA max	
C_{IN}	5pF typ	
POWER REQUIREMENTS		
V_{DD}	+12V	
V_{DD} Range	+5V to +12V	Functionality with degraded performance.
V_{BB}	-12V	
I_{DD}	1mA max	Digital Inputs = V_{INL} or V_{INH}
I_{BB}	100μA max	
Total Power Dissipation	5mW typ	

NOTES:

[1] Output amplifier (and amplifier supplies) must be capable of 30V peak output.

[2] Output noise voltage density includes op amp noise.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

*V_{DD} (to GND)	+14V
*V_{BB} (to GND)	-14V
Voltage (pins 11, 12, 13) to GND	V_{BB}, +14V
V_{IN} (to GND)	±35V
Digital Input Voltage to GND	-0.3V to V_{DD}
Output Voltage (Pin 1) to GND	-100mV to VDD
Power Dissipation (Package)	670mW
Operating Temperature	0 to +70°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

*If Loudness Compensation Switches (S1, S2, S3) are not used, the negative power supply may be omitted and V_{BB} (Pin 10) connected instead to DGND (Pin 9). In this case the absolute maximum rating of V_{DD} is +17V.

CAUTION:

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The foam should be discharged to the destination socket before devices are removed.

TERMINOLOGY

RESOLUTION: Nominal change in attenuation when moving between two adjacent binary codes. The AD7110 resolution is 1.5dB.

MONOTONICITY: The AD7110 digitally controlled audio attenuator is monotonic if the analog output decreases (or remains constant) as the digital input code (attenuation setting) increases.

FEEDTHROUGH ERROR: That portion of the input signal which reaches the output when the digital input code is set to mute the input signal.

ANALOG CIRCUIT PERFORMANCE:

Table I gives the nominal attenuation in dB for the AD7110 for all digital input codes. It also shows the Loudness Switch states and the nominal output voltage when using an external operational amplifier (as shown in Figure 1) and a fixed -10 volt reference applied to V_{IN} (pin 15). It may be seen that the transfer function for the circuit of Figure 1 is given by

$$V_{OUT} = -V_{IN}\ 10 \exp -\left\{\frac{1.5N}{20}\right\}$$

where N is the binary input for values 0 to 59. For N = 60 through 63 the input is fully muted, that is, the attenuation is infinite.

HIGH FREQUENCY AMPLIFIERS

R_{FB} and the output capacitance of the AD7110 create a phase lag in the output amplifier's feedback circuit. This phase lag, in conjunction with the amplifier's phase lag, may cause ringing or oscillation. When using a high speed amplifier, shunting the amplifier input to output with 30–50pF of feedback capacitance (C1) ensures stability.

DC PERFORMANCE OF AD7110

For fixed-reference applications, an output amplifier with low offset voltage (less than 50μV) is required, e.g. the AD517L. This combination will provide the utmost stability at the expense of slow settling times.

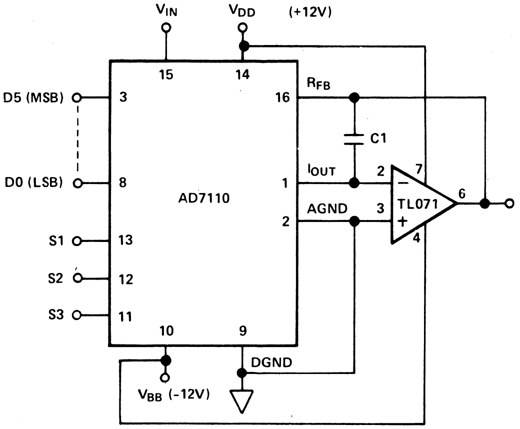


Figure 1.

Table I

N	Digital Input D5 D0	Attenuation dB	Switches[1]			V_{OUT}[2]
			S1	S2	S3	
0	00 00 00	0.0				10.00
1	00 00 01	1.5				8.414
2	00 00 10	3.0				7.079
3	00 00 11	4.5				5.957
4	00 01 00	6.0				5.012
5	00 01 01	7.5				4.217
6	00 01 10	9.0				3.548
7	00 01 11	10.5				2.985
8	00 10 00	12.0				2.512
9	00 10 01	13.5				2.113
10	00 10 10	15.0				1.778
11	00 10 11	16.5				1.496
12	00 11 00	18.0				1.259
13	00 11 01	19.5				1.059
14	00 11 10	21.0				0.891
15	00 11 11	22.5				0.750
16	01 00 00	24.0				0.631
17	01 00 01	25.5				0.531
18	01 00 10	27.0				0.447
19	01 00 11	28.5				0.376
20	01 01 00	30.0				0.316
21	01 01 01	31.5				0.266
22	01 01 10	33.0				0.224
23	01 01 11	34.5				0.188
24	01 10 00	36.0				0.158
25	01 10 01	37.5				0.133
26	01 10 10	39.0				0.112
27	01 10 11	40.5				0.0944
28	01 11 00	42.0				0.0794
29	01 11 01	43.5				0.0668
30	01 11 10	45.0				0.0562
31	01 11 11	46.5				0.0473
32	10 00 00	48.0	▨			0.0398
33	10 00 01	49.5	▨			0.0335
34	10 00 10	51.0	▨			0.0282
35	10 00 11	52.5	▨			0.0237
36	10 01 00	54.0	▨			0.0200
37	10 01 01	55.5	▨			0.0168
38	10 01 10	57.0	▨			0.0141
39	10 01 11	58.5	▨			0.0119
40	10 10 00	60.0		▨		0.0100
41	10 10 01	61.5		▨		0.00841
42	10 10 10	63.0		▨		0.00708
43	10 10 11	64.5		▨		0.00596
44	10 11 00	66.0		▨		0.00501
45	10 11 01	67.5		▨		0.00422
46	10 11 10	69.0		▨		0.00355
47	10 11 11	70.5		▨		0.00299
48	11 00 00	72.0		▨		0.00251
49	11 00 01	73.5		▨		0.00211
50	11 00 10	75.0		▨		0.00178
51	11 00 11	76.5		▨		0.00150
52	11 01 00	78.0		▨		0.00126
53	11 01 01	79.5		▨		0.00106
54	11 01 10	81.0		▨		0.000891
55	11 01 11	82.5		▨		0.000750
56	11 10 00	84.0		▨		0.000631
57	11 10 01	85.5		▨		0.000531
58	11 10 10	87.0		▨		0.000447
59	11 10 11	88.5		▨		0.000376
60	11 11 XX[3]	∞		▨	▨	

NOTES:

[1] Switch closed in shaded area.

[2] V_{IN} = −10V dc

[3] X = 1 or 0. Output is fully muted for $N \geq 60$.

Typical Performance Curves

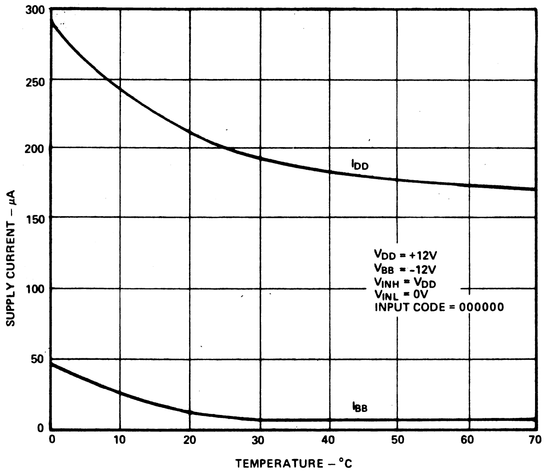


Figure 2. Power Supply Current vs. Temperature

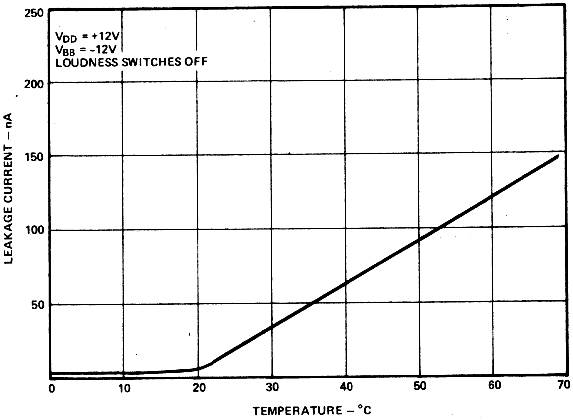


Figure 5. Loudness Switch Leakage Current vs. Temperature

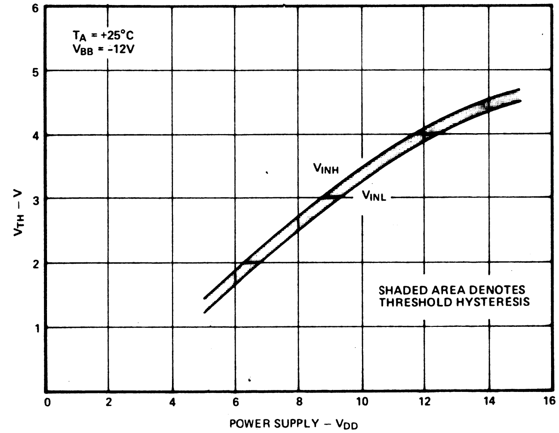


Figure 3. Digital Threshold Voltage vs. Power Supply Voltage

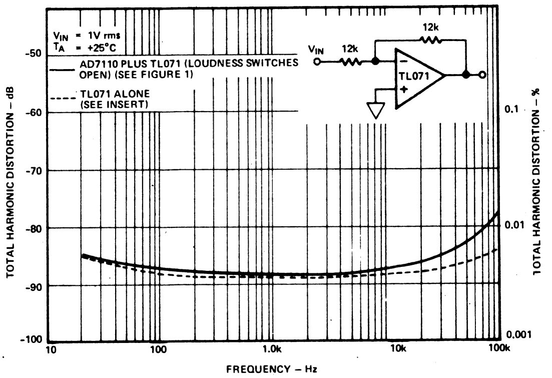


Figure 6. Total Harmonic Distortion vs. Frequency

Figure 6 shows that the total harmonic distortion of the attenuator circuit of Figure 1 is almost totally dependent on the characteristics of the operational amplifier used.

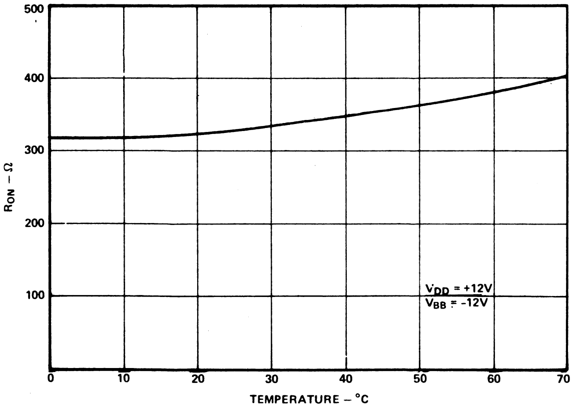


Figure 4. Loudness Switch On Resistance vs. Temperature

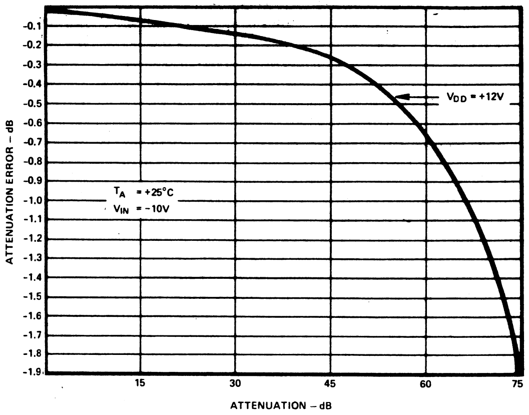


Figure 7. Typical dc Attenuation Error vs. Attenuation

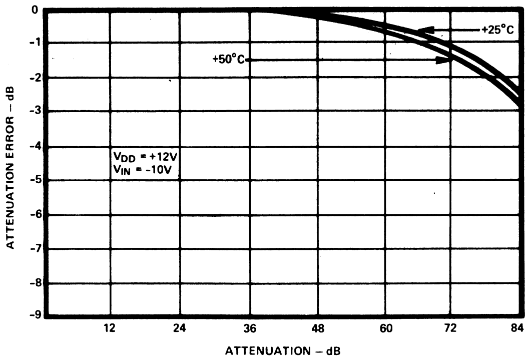


Figure 8. Typical dc Attenuation Error vs. Attenuation & Temperature

Applications Information

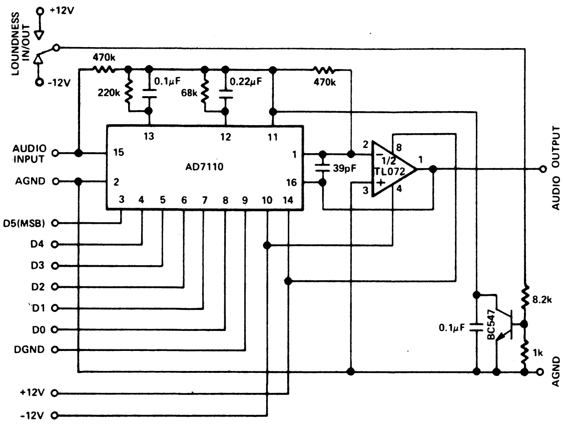


Figure 9. Single Channel Audio Attenuator with Loudness Compensation

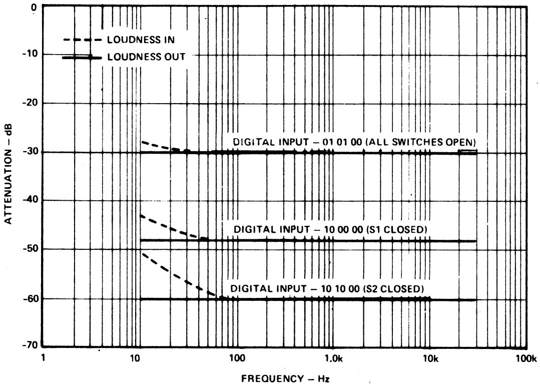


Figure 10.

Figure 10 shows the Attenuation vs. Frequency for the circuit of Figure 9. The attenuation is plotted against frequency for the two digital input codes at which the loudness compensation switches S1 and S2 are activated.

ANALOG DEVICES

LOGDAC™ CMOS Logarithmic D/A Converter

AD7111*

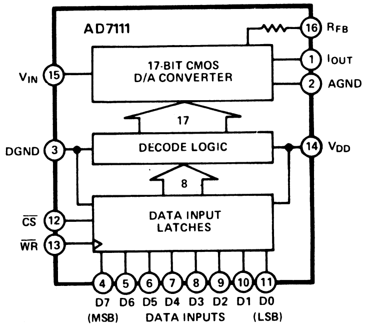
FEATURES

Dynamic Range: 88.5dB
Resolution: 0.375dB
On-Chip Data Latches
Full ±25V Input Range Multiplying DAC
Low Distortion
Single +5V Supply
Latch-Up Free (No Protection Schottky Required)

APPLICATIONS

Digitally Controlled AGC Systems
Audio Attenuators
Wide Dynamic Range A/D Converters
Sonar Systems
Function Generators

AD7111 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7111 is a CMOS multiplying D/A converter which can attenuate an analog input signal over the range 0 to -88.5dB in 0.375dB steps.

The degree of attenuation is determined by an 8-bit data word which is latched into on-chip data latches using microprocessor compatible control signals $\overline{CS}$ and $\overline{WR}$. Operating frequency range of the device is from dc to several hundred kHz.

The device is packaged in a 16-pin dual-in-line plastic, cerdip or ceramic package.

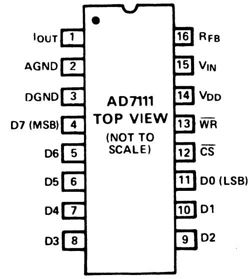
ORDERING INFORMATION

Specified Accuracy Range	Temperature Range and Package		
	Plastic 0 to +70°C	Cerdip[1,2] -25°C to +85°C	Ceramic[1] -55°C to +125°C
0 to 60dB	AD7111KN	AD7111BQ	AD7111TD
0 to 72dB	AD7111LN	AD7111CQ	AD7111UD

NOTE
[1] These parts are available screened to MIL-STD-883, method 5004 paragraph 3.1.1 through 3.1.12 for a class B device. To order add /883B to part number.
[2] Analog Devices reserves the right to ship Ceramic packages in lieu of Cerdip packages.

*Patent Pending
LOGDAC is a trademark of Analog Devices, Inc.

PIN CONFIGURATION



PACKAGE IDENTIFICATION[1]

Suffix D: Ceramic DIP (D16B)
Suffix N: Plastic DIP (N16B)
Suffix Q: Cerdip (Q16B)

[1] See Section 20 for package outline information.

SPECIFICATIONS (V_{DD} = +5V, V_{IN} = -10V dc, V_{PIN2} = V_{PIN1} = 0V, output amplifier AD544 except where stated)

	AD7111L/C/U GRADES		AD7111K/B/T GRADES			
Parameter	T_A = +25°C	T_A = T_{min}, T_{max}	T_A = +25°C	T_A = T_{min}, T_{max}	**Units**	**Conditions/Comments**
NOMINAL RESOLUTION	0.375	0.375	0.375	0.375	dB	
ACCURACY RELATIVE TO 0dB ATTENUATION						
0.375dB Steps:						
Accuracy ≤ ±0.17dB	0 to 36	0 to 36	0 to 30	0 to 30	dB min	Guaranteed attenuation ranges
Monotonic	0 to 54	0 to 54	0 to 48	0 to 48	dB min	for specified step sizes
0.75dB Steps:						
Accuracy ≤ ±0.35dB	0 to 48	0 to 42	0 to 42	0 to 36	dB min	
Monotonic	0 to 72	0 to 66	0 to 72	0 to 60	dB min	
1.5dB Steps:						
Accuracy ≤ ±0.7dB	0 to 54	0 to 48	0 to 48	0 to 42	dB min	
Monotonic	Full Range	0 to 78	0 to 85.5	0 to 72	dB min	Full Range is from 0 to 88.5dB
3.0dB Steps:						
Accuracy ≤ ±1.4dB	0 to 66	0 to 54	0 to 60	0 to 48	dB min	
Monotonic	Full Range	Full Range	Full Range	Full Range		
6.0dB Steps:						
Accuracy ≤ ±2.7dB	0 to 72	0 to 60	0 to 60	0 to 48	dB min	
Monotonic	Full Range	Full Range	Full Range	Full Range		
GAIN ERROR	±0.1	±0.15	±0.15	±0.20	dB max	
V_{IN} INPUT RESISTANCE (PIN 15)	9/11/15	9/11/15	7/11/18	7/11/18	kΩ min/typ/max	
R_{FB} INPUT RESISTANCE (PIN 16)	9.3/11.5/15.7	9.3/11.5/15.7	7.3/11.5/18.8	7.3/11.5/18.8	kΩ min/typ/max	
DIGITAL INPUTS						
V_{IH} (Input High Voltage)	2.4	2.4	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	0.8	V max	
Input Leakage Current	±1	±10	±1	±10	µA max	Digital Inputs = V_{DD}
SWITCHING CHARACTERISTICS[1]						
t_{CS}	0	0	0	0	ns min	Chip Select to Write Setup Time
t_{CH}	0	0	0	0	ns min	Chip Select to Write Hold Time
t_{WR}	350	500	350	500	ns min	Write Pulse Width
t_{DS}	175	250	175	250	ns min	Data Valid to Write Setup Time
t_{DH}	10	10	10	10	ns min	Data Valid to Write Hold Time
t_{RFSH}	3	4.5	3	4.5	µs min	Refresh Time
POWER SUPPLY						
V_{DD}	+5	+5	+5	+5	V	
I_{DD}	1	4	1	4	mA max	Digital Inputs = V_{IH} or V_{IL}
	500	1000	500	1000	µA max	Digital Inputs = 0V or V_{DD}. See Figure 7.

NOTE

[1] Sample tested at +25°C to ensure compliance.

Specifications subject to change without notice.

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for design guidance only and are not subject to test.
V_{DD} = +5V, V_{IN} = -10V dc except where stated, V_{PIN1} = V_{PIN2} = 0V, output amplifier AD544 except where stated.

	AD7111L/C/U GRADES		AD7111K/B/T GRADES			
Parameter	T_A = 25°C	T_A = T_{min}, T_{max}	T_A = +25°C	T_A = T_{min}, T_{max}	**Units**	**Conditions/Comments**
DC Supply Rejection, ΔGain/ΔV_{DD}	0.001	0.005	0.001	0.005	dB per % max	ΔV_{DD} = ±10%, Input Code = 00000000
Propagation Delay	3.0	4.5	3.0	4.5	µs max	Full Scale Change Measured from $\overline{WR}$ going high, $\overline{CS}$ = 0V.
Digital Charge Injection	100	–	100	–	nV secs typ	Measured with ADLH0032CG as Output Amplifier for Input Code Transition 10000000 to 00000000. C1 of Figure 1 is 0pF
Output Capacitance, Pin 1	185	185	185	185	pF max	
Input Capacitance, Pin 15 and Pin 16	7	7	7	7	pF max	
Feedthrough at 1kHz	-94	-72	-92	-68	dB max	Feedthrough is also determined by circuit
Total Harmonic Distortion	-91	-91	-91	-91	dB typ	layout (see Figure 4).
Output Noise Voltage Density	70	70	70	70	nV/√Hz max	V_{IN} = 6V rms at 1kHz
Digital Input Capacitance	7	7	7	7	pF max	Includes AD544 Amplifier Noise

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} (to DGND)	+7V
V_{IN} (to AGND)	±35V
Digital Input Voltage to DGND	−0.3V to V_{DD}
Output Voltage (Pin 1) to AGND	−0.3V to V_{DD}
V_{RFB} to AGND	±35V
AGND to DGND	0 to V_{DD}
DGND to AGND	0 to V_{DD}
Power Dissipation (Package)	
Plastic (Suffix N)	
To +70°C	670mW
Derates Above +70°C by	8.3mW/°C
Ceramic (Suffix D) or Cerdip (Suffix Q)	
To +75°C	450mW
Derates Above +75°C by	6mW/°C
Operating Temperature Range	
Commercial Plastic (KN, LN Versions)	0 to +70°C
Industrial Ceramic (BQ, CQ Versions)	−25°C to +85°C
Military Ceramic (TD, UD Versions)	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering 10 secs)	+300°C

***Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.**

CAUTION:

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The foam should be discharged to the destination socket before devices are removed.

WARNING!

ESD SENSITIVE DEVICE

TERMINOLOGY

RESOLUTION: Nominal change in attenuation when moving between two adjacent codes.

MONOTONICITY: The device is monotonic if the analog output decreases (or remains constant) as the digital code increases.

FEEDTHROUGH ERROR: That portion of the input signal which reaches the output when all digital inputs are high. See section on Applications.

OUTPUT LEAKAGE CURRENT: Current which appears on the I_{OUT} terminal with all digital inputs high.

TOTAL HARMONIC DISTORTION: A measure of the harmonics introduced by the circuit when a pure sinusoid is applied to the input. It is expressed as the harmonic energy divided by the fundamental energy at the output.

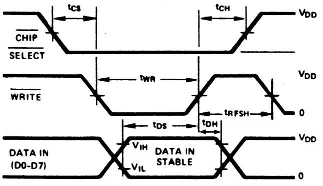
ACCURACY: The difference (measured in dB) between the ideal transfer function as listed in Table 1 and the actual transfer function as measured with the device.

OUTPUT CAPACITANCE: Capacitance from I_{OUT} to ground.

DIGITAL CHARGE INJECTION: The amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA-Secs or nV-Secs depending upon whether the glitch is measured as a current or voltage signal. Digital charge injection is measured with V_{IN} = AGND.

PROPAGATION DELAY: This is a measure of the internal delays of the circuit and is defined as the time from a digital input change to the analog output current reaching 90% of its final value.

WRITE CYCLE TIMING DIAGRAM



NOTES:
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF V_{DD}. V_{DD} = +5V, $t_r = t_f$ = 20ns.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$.

CIRCUIT DESCRIPTION

GENERAL CIRCUIT INFORMATION

The AD7111 consists of a 17-bit R-2R CMOS mutiplying D/A converter with extensive digital logic. The logic translates the 8-bit binary input into a 17-bit word which is used to drive the D/A converter. Input data on the D7–D0 bus is loaded into the input data latches using $\overline{CS}$ and $\overline{WR}$ control signals. The rising edge of $\overline{WR}$ latches the input data and initiates the internal data transfer to the decoder. A minimum time t_{RFSH}, the refresh time, is required for the data to propagate through the decoder before a new data write is attempted.

The transfer function for the circuit of Figure 1 is given by:

$$V_O = -V_{IN}\ 10\ \exp - \frac{0.375\ N}{20}$$

or

$$\left|\frac{V_O}{V_{IN}}\right|\ dB = -\ 0.375\ N$$

Where 0.375 is the step size (resolution) in dB and N is the input code in decimal for values 0 to 239. For 240⩽N⩽255 the output is zero. Table 1 gives the output attenuation relative to 0dB for all possible input codes.

The graphs on the last page give a pictorial representation of the specified accuracy and monotonic ranges for all grades of the AD7111. High attenuation levels are specified with less accuracy than low attenuation levels. The range of monotonic behavior depends upon the attenuation step size used. For example, the AD7111L is guaranteed monotonic in 0.375dB steps from 0 to -54dB inclusive and in 0.75dB steps from 0 to -72dB inclusive. To achieve monotonic operation over the entire 88.5dB range it is necessary to select input codes so that the attenuation step size at any point is consistent with the step size guaranteed for monotonic operation at that point. For further information on applications of the AD7111 the user is referred to Analog Devices Application Note "Audio Applications of Nonlinear CMOS Multiplying D/A Converters."

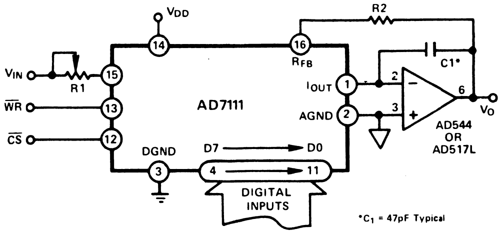


Figure 1. Typical Circuit Configuration

EQUIVALENT CIRCUIT ANALYSIS

Figure 2 shows a simplified circuit of the D/A converter section of the AD7111 and Figure 3 gives an approximate equivalent circuit.

The current source $I_{LEAKAGE}$ is composed of surface and junction leakages and as with most semiconductor devices, approximately doubles every 10°C–see Figure 11. The resistor R_O as shown in Figure 3 is the equivalent output resistance of the device which varies with input code from 0.8R to 2R. R is typically 11kΩ. C_{OUT} is the capacitance due to the N channel switches and varies from about 60pF to 185pF depending upon the digital input. For further information on CMOS multiplying D/A converters refer to "Application Guide to CMOS Multiplying D/A Converters" which is available from Analog Devices, Publication Number G479–15–8/78.

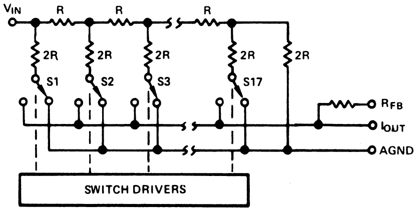
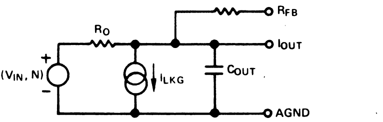


Figure 2. Simplified D/A circuit of AD7111



g(VIN, N) IS THE THEVENIN EQUIVALENT VOLTAGE GENERATOR DUE TO THE INPUT VOLTAGE VIN, THE BINARY ATTENUATION FACTOR N AND THE TRANSFER FUNCTION OF THE R-2R LADDER.

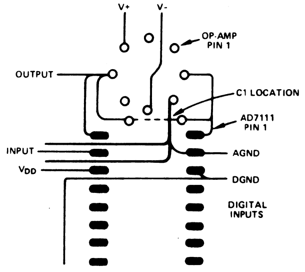
Figure 3. Equivalent Analog Output Circuit of AD7111

D3-D0 D7-D4	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	0.0	0.375	0.75	1.125	1.5	1.875	2.25	2.625	3.0	3.375	3.75	4.125	4.5	4.875	5.25	5.625
0001	6.0	6.375	6.75	7.125	7.5	7.875	8.25	8.625	9.0	9.375	9.75	10.125	10.5	10.875	11.25	11.625
0010	12.0	12.375	12.75	13.125	13.5	13.875	14.25	14.625	15.0	15.375	15.75	16.125	16.5	16.875	17.25	17.625
0011	18.0	18.375	18.75	19.125	19.5	19.875	20.25	20.625	21.0	21.375	21.75	22.125	22.5	22.875	23.25	23.625
0100	24.0	24.375	24.75	25.125	25.5	25.875	26.25	26.625	27.0	27.375	27.75	28.125	28.5	28.875	29.75	29.625
0101	30.0	30.375	30.75	31.125	31.5	31.875	32.25	32.625	33.0	33.375	33.75	34.125	34.5	34.875	35.25	35.625
0110	36.0	36.375	36.75	37.125	37.5	37.875	38.25	38.625	39.0	39.375	39.75	40.125	40.5	40.875	41.25	41.625
0111	42.0	42.375	42.75	43.125	43.5	43.875	44.25	44.625	45.0	45.375	45.75	46.125	46.5	46.875	47.25	47.625
1000	48.0	48.375	48.75	49.125	49.5	49.875	50.25	50.625	51.0	51.375	51.75	52.125	52.5	52.875	53.25	53.625
1001	54.0	54.375	54.75	55.125	55.5	55.875	56.25	56.625	57.0	57.375	57.75	58.125	58.5	58.875	59.25	59.625
1010	60.0	60.375	60.75	61.125	61.5	61.875	62.25	62.625	63.0	63.375	63.75	64.125	64.5	64.875	65.25	65.625
1011	66.0	66.375	66.75	67.125	67.5	67.875	68.25	68.625	69.0	69.375	69.75	70.125	70.5	70.875	71.25	71.625
1100	72.0	72.375	72.75	73.125	73.5	73.875	74.25	74.625	75.0	75.375	75.75	76.125	76.5	76.875	77.25	77.625
1101	78.0	78.375	78.75	79.125	79.5	79.875	80.25	80.625	81.0	81.375	81.75	82.125	82.5	82.875	83.25	83.625
1110	84.0	84.375	84.75	85.125	85.5	85.875	86.25	86.625	87.0	87.375	87.75	88.125	88.5	88.875	89.25	89.625
1111	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE

Table 1. Ideal Attenuation in dB vs. Input Code

DYNAMIC PERFORMANCE

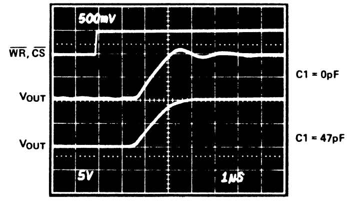
The dynamic performance of the AD7111 will depend upon the gain and phase characteristics of the output amplifier, together with the optimum choice of PC board layout and decoupling components. Figure 4 shows a printed circuit layout which minimizes feedthrough from V_{IN} to the output in multiplying applications. Circuit layout is most important if the optimum performance of the AD7111 is to be achieved. Most application problems stem from either poor layout, grounding errors, or inappropriate choice of amplifier.



LAYOUT SHOWS COPPER SIDE (i.e., BOTTOM VIEW)
GAIN TRIM RESISTORS R1 AND R2 OF FIGURE 1
ARE NOT INCLUDED.

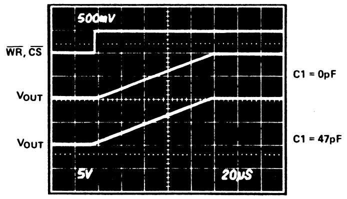
Figure 4. Suggested Layout for AD7111 and Op-Amp

It is recommended that when using the AD7111 with a high speed amplifier, a capacitor (C1) be connected in the feedback path as shown in Figure 1. This capacitor, which should be between 30pF and 50pF, compensates for the phase lag introduced by the output capacitance of the D/A converter. Figures 5 and 6 show the performance of the AD7111 using the AD517, a fully compensated high gain superbeta amplifier, and the AD544, a fast FET input amplifier. The performance without C1 is shown in the middle trace and the response with C1 in circuit is shown in the bottom trace.



DATA CHANGE FROM 80H TO 00H

Figure 5. Response of AD7111 with AD517



DATA CHANGE FROM 80H to 00H

Figure 6. Response of AD7111 with AD544

In conventional CMOS D/A converter design parasitic capacitance in the N-channel D/A converter switches can give rise to glitches on the D/A converter output. These glitches result from digital feedthrough. The AD7111 has been designed to minimize these glitches as much as possible.

For operation beyond 250kHz, capacitor C1 may be reduced in value. This gives an increase in bandwidth at the expense of a poorer transient response as shown in Figures 6 and 12. In circuits where C1 is not included the high frequency roll-off point is primarily determined by the characteristics of the output amplifier and not the AD7111.

Feedthrough and absolute accuracy are sensitive to output leakage current effects. For this reason it is recommended that the operating temperature of the AD7111 be kept as close to 25°C as is practically possible, particularly where the device's performance at high attenuation levels is important. A typical plot of leakage current vs. temperature is shown in Figure 11.

Some solder fluxes and cleaning materials can form slightly conductive films which cause leakage effects between analog input and output. The user is cautioned to ensure that the manufacturing process for circuits using the AD7111 does not allow such films to form. Otherwise the feedthrough, accuracy and maximum usable range will be affected.

STATIC ACCURACY PERFORMANCE

The D/A converter section of the AD7111 consists of a 17-bit R-2R type converter. To obtain optimum static performance at this level of resolution it is necessary to pay great attention to amplifier selection, circuit grounding, etc.

Amplifier input bias current results in a dc offset at the output of the amplifier due to the current flowing through the feedback resistor R_{FB}. It is recommended that an amplifier with an input bias current of less than 10nA be used (e.g., AD517 or AD544) to minimize this offset.

Another error arises from the output amplifier's input offset voltage. The amplifier is operated with a fixed feedback resistance, but the equivalent source impedance (the AD7111 output impedance) varies as a function of attenuation level. This has the effect of varying the "noise" gain of the amplifier, thus creating a varying error due to amplifier offset voltage. It is recommended that an amplifier with less than 50μV of input offset be used (such as the AD517 or AD OP-07) in dc applications. Amplifiers with higher offset voltage may cause audible "thumps" in ac applications due to dc output changes.

The AD7111 accuracy is specified and tested using only the internal feedback resistor. Any Gain Error (i.e., mismatch of R_{FB} to the R-2R ladder) that may exist in the AD7111 D/A converter circuit results in a constant attenuation error over the whole range. The AD7111 accuracy is specified relative to 0dB attenuation, hence "Gain" trim resistors—R1 and R2 in Figure 1—can be used to adjust $V_{OUT} = V_{IN}$ precisely (i.e., 0dB attenuation) with input code 00000000. The accuracy and monotonic range specifications of the AD7111 are not affected in any way by this gain trim procedure. For the AD7111L/C/U grades, suitable values for R1 and R2 of Figure 1 are R1 = 500Ω, R2 = 180Ω; for the K/B/T grades suitable values are R1 = 1000Ω, R2 = 270Ω. For additional information on gain error the reader is referred to Application Note "Gain Error and Gain Temperature Coefficient of CMOS Multiplying DACs" by Phil Burton available from Analog Devices Inc., Publication Number E630–10–6/81.

Typical Performance Characteristics

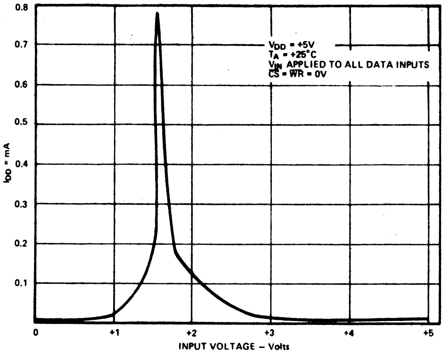


Figure 7. Typical Supply Current vs. Logic Input Level

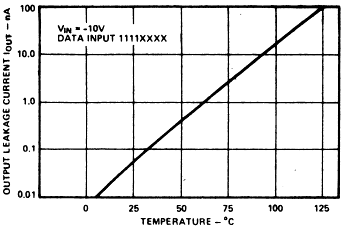


Figure 11. Output Leakage Current vs. Temperature

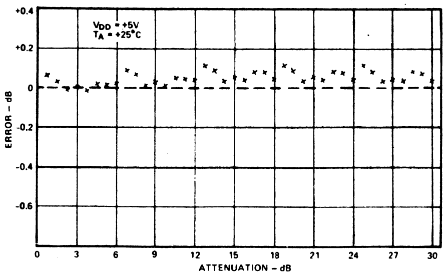


Figure 8. Typical Attenuation Error for 0.75dB Steps

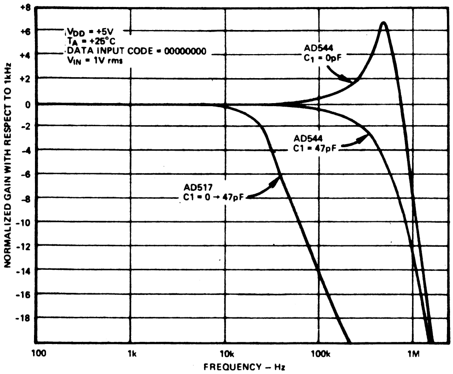


Figure 12. Frequency Response with AD544 and AD517 Amplifiers

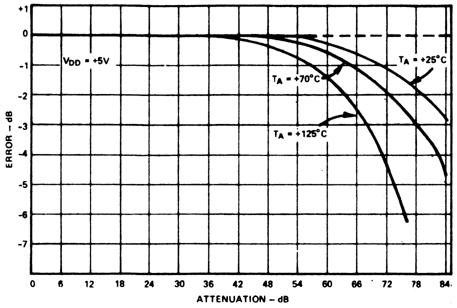


Figure 9. Typical Attenuation Error for 3dB Steps vs. Temperature

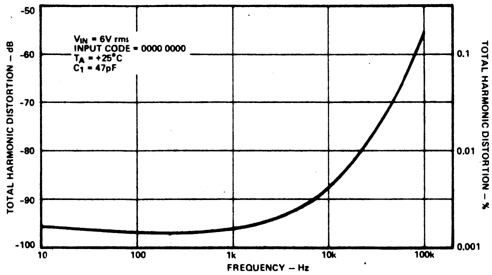


Figure 13. Distortion vs. Frequency Using AD544 Amplifier

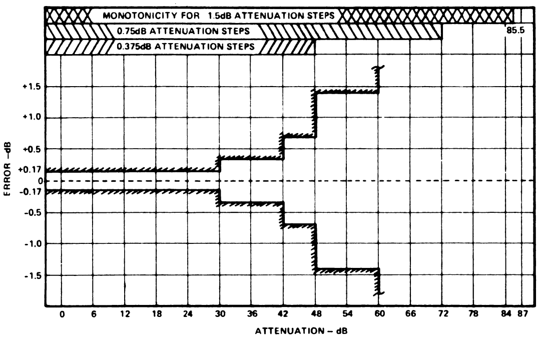


Figure 10. Accuracy Specification for K/B/T Grade Devices at T_A = +25°C

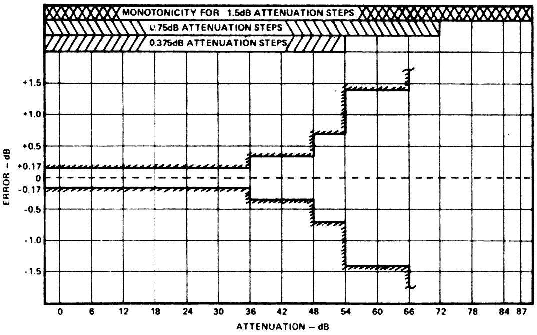


Figure 14. Accuracy Specification for L/C/U Grade Devices at T_A = +25°C

ANALOG DEVICES

LOGDAC™ CMOS Logarithmic D/A Converter

AD7118*

FEATURES
- Dynamic Range 85.5dB
- Resolution 1.5dB
- Full ±25V Input Range Multiplying DAC
- Full Military Temperature Range -55°C to +125°C
- Low Distortion
- Low Power Consumption
- Latch Proof Operation (Schottky Diodes Not Required)
- Single 5V to 15V Supply

APPLICATIONS
- Digitally Controlled AGC Systems
- Audio Attenuators
- Wide Dynamic Range A/D Converters
- Sonar Systems
- Function Generators

GENERAL DESCRIPTION
The AD7118 is a CMOS multiplying D/A converter which attenuates an analog input signal over the range 0 to -85.5dB in 1.5dB steps. The analog output is determined by a six bit attenuation code applied to the digital inputs. Operating frequency range of the device is from dc to several hundred kHz.

The device is manufacured using an advanced monolithic silicon gate thin-film on CMOS process and is packaged in a 14-pin dual-in-line package.

ORDERING INFORMATION

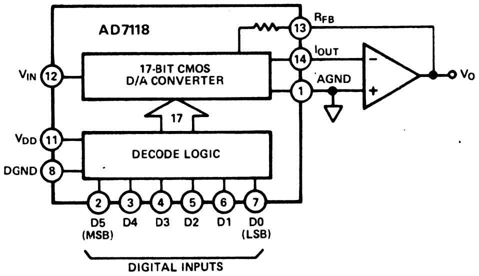
Specified Accuracy Range[1]	Temperature Range		
	0 to +70°C	-25°C to +85°C	-55°C to +125°C
0 to 42dB	AD7118KN	AD7118BD[2]	AD7118TD[2]
0 to 48dB	AD7118LN	AD7118CD[2]	AD7118UD[2]

NOTES
[1] All devices are guaranteed monotonic at +25°C (see spec).
[2] Ceramic parts are available screened to MIL-STD-883, method 5004 para 3.1.1 through 3.1.12 for a class B device. To order add/883B to part number.

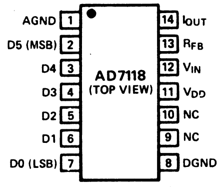
*Patent Pending

LOGDAC is a trademark of Analog Devices, Inc.

AD7118 FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



NC = NO CONNECTION

PACKAGE IDENTIFICATION[1]
Suffix D: Ceramic DIP – (D14B)
Suffix N: Plastic DIP – (N14B)

[1] See section 20 for package outline information.

SPECIFICATIONS

(V_{DD} = +5V or +15V, V_{IN} = -10V dc, $V_{PIN\ 14}$ = V_{PIN1} = 0V, output amplifier AD544 except where stated)

PARAMETER		T_A = +25°C		T_A = T_{min}, T_{max}		UNITS	TEST CONDITIONS/ COMMENTS
		V_{DD} = +5V	V_{DD} = +15V	V_{DD} = +5V	V_{DD} = +15V		
NOMINAL RESOLUTION		1.5	1.5	1.5	1.5	dB	
ACCURACY RELATIVE TO V_{IN}							
AD7118L/C/U							
0 to -30dB		±0.35	±0.35	±0.4	±0.4	dB max	Accuracy is measured using circuit of Figure 1 and includes any effects due to mismatch between R_{FB} and the R-2R ladder circuit.
-31.5 to -42dB		±0.7	±0.5	±0.8	±0.7	dB max	
-43.5 to -48dB		±1.0	±0.7	±1.3	±1.0	dB max	
AD7118K/B/T							
0 to -30dB		±0.5	±0.5	±0.5	±0.5	dB max	
-31.5 to -42dB		±0.75	±0.75	±1.0	±0.8	dB max	
MONOTONIC RANGE							
Nominal 1.5dB Steps	L/C/U Grade	Monotonic Over Full		0 to -72	0 to -72	dB	Digital Inputs 000000 to 110000
	K/B/T Grade	Code Range		0 to -66	0 to -66	dB	Digital Inputs 000000 to 101100
Nominal 3dB Steps	All Grades	Monotonic Over Full Code Range					
V_{IN} INPUT RESISTANCE	All Grades	9	9	9	9	kΩ min	
(PIN 12)	L/C/U Grade	17	17	17	17	kΩ max	
	K/B/T Grade	21	21	21	21	kΩ max	
R_{FB} INPUT RESISTANCE	All Grades	9.45	9.45	9.45	9.45	kΩ min	
(PIN 13)	L/C/U Grade	18	18	18	18	kΩ max	
	K/B/T Grade	22	22	22	22	kΩ max	
DIGITAL INPUTS							
Input High Voltage Requirements V_{IH}		3.0	13.5	3.0	13.5	V min	
Input Low Voltage Requirements V_{IL}		0.8	1.5	0.8	1.5	V max	
Input Leakage Current		±1	±1	±10	±10	μA max	Digital Inputs = V_{DD}
POWER SUPPLY							
V_{DD} for Specified Accuracy		5	–	5	–	V min	
		–	15	–	15	V max	
I_{DD}		0.5	1	1	2	mA max	Digital Inputs = 0V or V_{DD} (See Figure 7)

Specifications subject to change without notice.

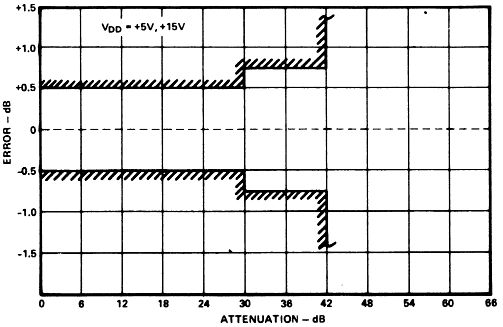
AC PERFORMANCE CHARACTERISTICS

These characteristics are included for design guidance only and are not subject to test.

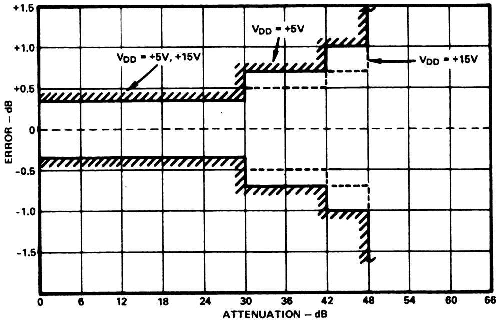
V_{DD} = +5V or +15V, V_{IN} = -10V except where stated, V_{PIN} 14 = V_{PIN}1 = 0V, output amplifier AD544 except where stated.

PARAMETER		T_A = +25°C		T_A = T_{min}, T_{max}		UNITS	
		V_{DD} = +5V	V_{DD} = +15V	V_{DD} = +5V	V_{DD} = +15V		
DC Supply Rejection, ΔGain/ΔV_{DD}		0.01	0.005	0.01	0.005	dB per % max	ΔV_{DD} = ±10%, Input code = 100000
Propagation Delay		1.8	0.4	2.2	0.5	μs max	Full Scale Change
Digital Charge Injection		225	1200	–	–	nV secs typ	Measured with ADLH0032CG as output amplifier for input code transition 100000 to 000000. C1 of Figure 1 is 0pF.
Output Capacitance (Pin 14)		100	100	100	100	pF max	
Input Capacitance Pin 12 and Pin 13		7	7	7	7	pF max	
Feedthrough at 1kHz	L/C/U Grade	-86	-86	-68	-68	dB max	Feedthrough is also determined by circuit layout
	K/B/T Grade	-80	-80	-63	-63	dB max	
Total Harmonic Distortion		-85	-85	-85	-85	dB typ	V_{IN} = 6V rms
Intermodulation Distortion		-79	-79	-79	-79	dB typ	per DIN 45403 Blatt 4
Output Noise Voltage Density		70	70	70	70	nV/$\sqrt{Hz}$ max	Includes AD544 amplifier noise
Digital Input Capacitance		7	7	7	7	pF max	

Specifications subject to change without notice.



Accuracy Specification for K/B/T Grade Devices at T_A = +25°C



Accuracy Specification for L/C/U Grade Devices at T_A = +25°C

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

V_{DD} (to DGND	+17V
V_{IN} (to AGND)	±35V
Digital Input Voltage to DGND	−0.3V to V_{DD}
Output Voltage (Pin 14) to AGND	−0.3V to V_{DD}
AGND to DGND	0 to V_{DD}
DGND to AGND	0 to V_{DD}
Power Dissipation (Package)	
Plastic (Suffix N)	
To +70°C	670mW
Derates Above +70°C by	8.3mW/°C
Ceramic (Suffix D)	
To +75°C	450mW
Derates Above +75°C by	6mW/°C
Operating Temperature Range	
Commercial Plastic (KN, LN Versions)	0 to +70°C
Industrial Ceramic (BD, CD Versions)	−25°C to +85°C
Military Ceramic (TD, UD Versions)	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering 10 secs)	+300°C

CAUTION:

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The foam should be discharged to the destination socket before devices are removed.

TERMINOLOGY

RESOLUTION: Nominal change in attenuation when moving between two adjacent binary codes.

MONOTONICITY: The device is monotonic if the analog output decreases (or remains constant) as the digital code increases.

FEEDTHROUGH ERROR: That portion of the input signal which reaches the output when all digital inputs are high. See section on Applications.

OUTPUT LEAKAGE CURRENT: Current which appears on the I_{OUT} terminal with all digital inputs high.

TOTAL HARMONIC DISTORTION: Is a measure of the harmonics introduced by the circuit when a pure sinusoid is applied to the input. It is expressed as the harmonic energy divided by the fundamental energy at the output.

ACCURACY: Is the difference (measured in dB) between the ideal transfer function as listed in Table 1 and the actual transfer function as measured with the device.

OUTPUT CAPACITANCE: Capacitance from I_{OUT} to ground.

DIGITIAL CHARGE INJECTION: The amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA-Secs or nV-Secs depending upon whether the glitch is measured as a current or voltage signal. Digital charge injection is measured with V_{IN} = AGND.

PROPAGATION DELAY: This is a measure of the internal delays of the circuit and is defined as the time from a digital input change to the analog output current reaching 90% of its final value.

INTERMODULATION DISTORTION: Is a measure of the interaction which takes place within the circuit between two sinusoids applied simultaneously to the input.

The reader is referred to Hewlett Packard Application Note 192 for further information.

CIRCUIT DESCRIPTION

GENERAL CIRCUIT INFORMATION

The AD7118 consists of a 17-bit R-2R CMOS multiplying D/A converter with extensive digital input logic. The logic translates the 6-bit binary input into a 17-bit word which is used to drive the D/A converter. Table 1 gives the nominal output voltages (and levels relative to 0dB = 10V) for all possible input codes. The transfer function for the circuit of Figure 1 is given by:

$$V_O = -V_{IN}\ 10 \exp - \left\{\frac{1.5N}{20}\right\}$$

$$\text{or } \left|\frac{V_O}{V_{IN}}\right|_{dB} = -1.5N$$

where N is the binary input for values 0 to 57. For 60⩽N⩽63 the output is zero. See note 3 at bottom of Table 1.

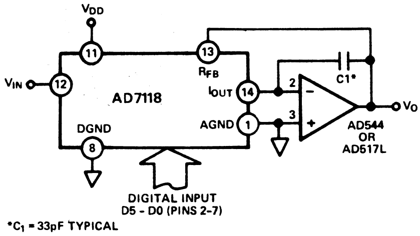


Figure 1. Typical Circuit Configuration

EQUIVALENT CIRCUIT ANALYSIS

Figure 2 shows a simplified circuit of the D/A converter section of the AD7118 and Figure 3 gives an approximate equivalent circuit.

The current source $I_{LEAKAGE}$ is composed of surface and junction leakages and as with most semiconductor devices, roughly doubles every 10°C—see Figure 10. The resistor R_O as shown in Figure 3 is the equivalent output resistance of the device which varies with input code from 0.8R to 2R. R is typically 12kΩ. C_{OUT} is the capacitance due to the N channel switches and varies from about 50pF to 80pF depending upon the digital input. For further information on CMOS multiplying D/A converters refer to "Application Guide to CMOS Multiplying D/A Converters" which is available from Analog Devices, Publication Number G479–15–8/78.

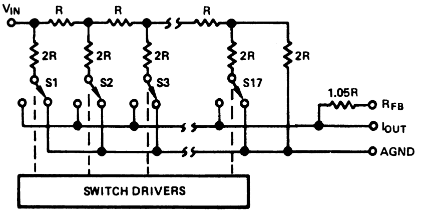
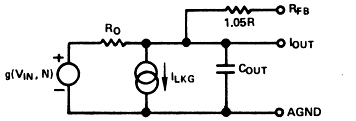


Figure 2. Simplified D/A Circuit of AD7118



g(VIN, N) IS THE THÉVENIN EQUIVALENT VOLTAGE GENERATOR DUE TO THE INPUT VOLTAGE VIN, THE BINARY ATTENUATION FACTOR N AND THE TRANSFER FUNCTION OF THE R-2R LADDER.

Figure 3. Equivalent Analog Output Circuit of AD7118

N	Digital Input D5 D0	Attenuation dB	V_{OUT}[1]
0	00 00 00	0.0	10.00
1	00 00 01	1.5	8.414
2	00 00 10	3.0	7.079
3	00 00 11	4.5	5.957
4	00 01 00	6.0	5.012
5	00 01 01	7.5	4.217
6	00 01 10	9.0	3.548
7	00 01 11	10.5	2.985
8	00 10 00	12.0	2.512
9	00 10 01	13.5	2.113
10	00 10 10	15.0	1.778
11	00 10 11	16.5	1.496
12	00 11 00	18.0	1.259
13	00 11 01	19.5	1.059
14	00 11 10	21.0	0.891
15	00 11 11	22.5	0.750
16	01 00 00	24.0	0.631
17	01 00 01	25.5	0.531
18	01 00 10	27.0	0.447
19	01 00 11	28.5	0.376
20	01 01 00	30.0	0.316
21	01 01 01	31.5	0.266
22	01 01 10	33.0	0.224
23	01 01 11	34.5	0.188
24	01 10 00	36.0	0.158
25	01 10 01	37.5	0.133
26	01 10 10	39.0	0.112
27	01 10 11	40.5	0.0944
28	01 11 00	42.0	0.0794
29	01 11 01	43.5	0.0668
30	01 11 10	45.0	0.0562
31	01 11 11	46.5	0.0473
32	10 00 00	48.0	0.0398
33	10 00 01	49.5	0.0335
34	10 00 10	51.0	0.0282
35	10 00 11	52.5	0.0237
36	10 01 00	54.0	0.0200
37	10 01 01	55.5	0.0168
38	10 01 10	57.0	0.0141
39	10 01 11	58.5	0.0119
40	10 10 00	60.0	0.0100
41	10 10 01	61.5	0.00841
42	10 10 10	63.0	0.00708
43	10 10 11	64.5	0.00596
44	10 11 00	66.0	0.00501
45	10 11 01	67.5	0.00422
46	10 11 10	69.0	0.00355
47	10 11 11	70.5	0.00299
48	11 00 00	72.0	0.00251
49	11 00 01	73.5	0.00211
50	11 00 10	75.0	0.00178
51	11 00 11	76.5	0.00150
52	11 01 00	78.0	0.00126
53	11 01 01	79.5	0.00106
54	11 01 10	81.0	0.000891
55	11 01 11	82.5	0.000750
56	11 10 00	84.0	0.000631
57	11 10 01	85.5	0.000531
58	11 10 10	87.0	0.000447
59	11 10 11	88.5	0.000376
60	11 11 XX[2]	∞	

NOTES

[1] V_{IN} = −10V dc

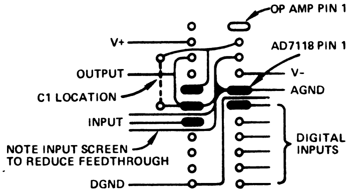
[2] X = 1 or 0. Output is fully muted for N⩾60

[3] Monotonic operation is not guaranteed for N = 58, 59

Table 1. Ideal Attenuation vs Input Code

DYNAMIC PERFORMANCE

The dynamic performance of the AD7118 will depend upon the gain and phase characteristics of the output amplifier, together with the optimum choice of PC board layout and decoupling components. Figure 4 shows a printed circuit layout which minimizes feedthrough from V_{IN} to the output in multiplying applications. Circuit layout is most important if the optimum performance of the AD7118 is to be achieved. Most application problems stem from either poor layout, grounding errors, or inappropriate choice of amplifier.



LAYOUT SHOWS COPPER SIDE (i.e., BOTTOM VIEW)

Figure 4. Suggested Layout for AD7118 and Op Amp

It is recommended that when using the AD7118 with a high speed amplifier, a capacitor C1 be connected in the feedback path as shown in Figure 1. This capacitor, which should be between 30pF and 50pF, compensates for the phase lag introduced by the output capacitance of the D/A converter. Figures 5 and 6 show the performance of the AD7118 using the AD517, a fully compensated high gain superbeta amplifier, and the AD544, a fast FET input amplifier. The performance without C1 is shown in the middle trace and the response with C1 in circuit is shown in the bottom trace.

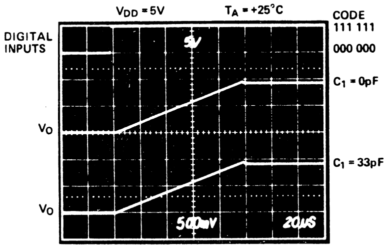


Figure 5. Response of AD7118 with AD517L

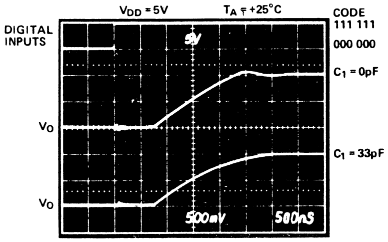


Figure 6. Response of AD7118 with AD544S

In conventional CMOS D/A converter design parasitic capacitance in the N-channel D/A converter switches can give rise to glitches on the D/A converter output. These glitches result from digital feedthrough. The AD7118 has been designed to minimize these glitches as much as possible. It is recommended that for minimum glitch energy the AD7118 be operated with V_{DD} = 5V. This will reduce the available energy for coupling across the parasitic capacitance. It should be noted that the accuracy of the AD7118 improves as V_{DD} is increased (see Figure 8) but the device maintains monotonic behavior to at least -66dB in the range $5 \leqslant V_{DD} \leqslant 15$ volts.

For operation beyond 250kHz, capacitor C1 may be reduced in value. This gives an increase in bandwidth at the expense of a poorer transient response as shown in Figures 6 and 11. In circuits where C1 is not included the high frequency roll-off point is primarily determined by the characteristics of the output amplifier and not the AD7118.

Feedthrough and absolute accuracy for attenuation levels beyond 42dB are sensitive to output leakage current effects. For this reason it is recommended that the operating temperature of the AD7118 be kept as close to 25°C as is practically possible, particularly where the device's performance at high attenuation levels is important. A typical plot of leakage current vs. temperature is shown in Figure 10.

Some solder fluxes and cleaning materials can form slightly conductive films which cause leakage effects between analog input and output. The user is cautioned to ensure that the manufacturing process for circuits using the AD7118 does not allow such films to form. Otherwise the feedthrough, accuracy and maximum usable range will be affected.

STATIC ACCURACY PERFORMANCE

The D/A converter section of the AD7118 consists of a 17-bit R-2R type converter. To obtain optimum static performance at this level of resolution it is necessary to pay great attention to amplifier selection, circuit grounding, etc.

Amplifier input bias current results in a dc offset at the output of the amplifier due to the current flowing through the feedback resistor R_{FB}. It is recommended that an amplifier with an input bias current of less than 10nA be used (e.g., AD517 or AD544) to minimize this offset.

Another error arises from the output amplifier's input offset voltage. The amplifier is operated with a fixed feedback resistance, but the equivalent source impedance (the AD7118 output impedance) varies as a function of attenuation level. This has the effect of varying the "noise" gain of the amplifier, thus creating a varying error due to amplifier offset voltage. To achieve an output offset error less than one half the smallest step size, it is recommended that an amplifier with less than 50µV of input offset be used (such as the AD517 or AD OP-07).

If dc accuracy is not critical in the application, it should be noted that amplifiers with offset voltage up to approximately 2 millivolts can be used. Amplifiers with higher offset voltage may cause audible "thumps" due to dc output changes.

The AD7118 accuracy is specified and tested using only the internal feedback resistor. It is not recommended that "gain" trim resistors be used with the AD7118 because the internal logic of the circuit executes a proprietary algorithm which approximates a logarithmic curve with a binary D/A converter: as a result no single point on the attenuator transfer function can be guaranteed to lie exactly on the theoretical curve. Any "gain-error" (i.e., mismatch of R_{FB} to the R-2R ladder) that may exist in the AD7118 D/A converter circuit results in a constant attenuation error over the whole range. Since the gain-error of CMOS multiplying D/A converters is normally less than 1%, the accuracy error contribution due to "gain-error" effects is normally less than 0.09dB.

Typical Performance Characteristics

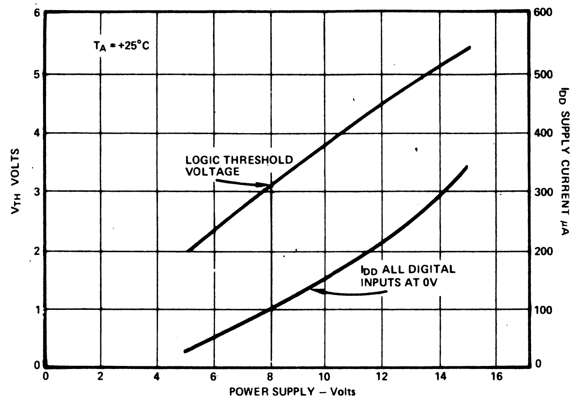


Figure 7. Digital Threshold & Power Supply Current vs Power Supply

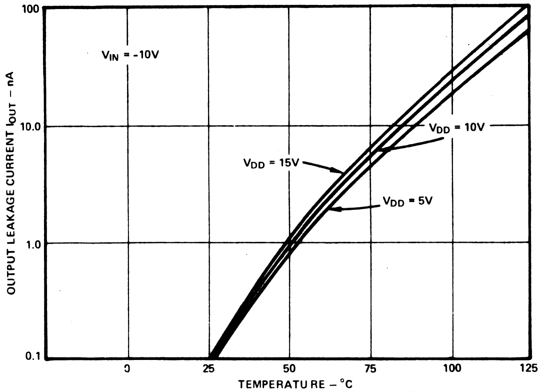


Figure 10. Output Leakage Current vs Temperature at V_{DD} = 5, 10 and 15 Volts

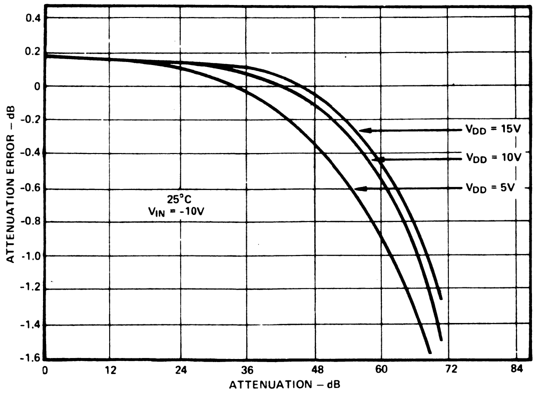


Figure 8. DC Attenuation Error vs. Attenuation & V_{DD}

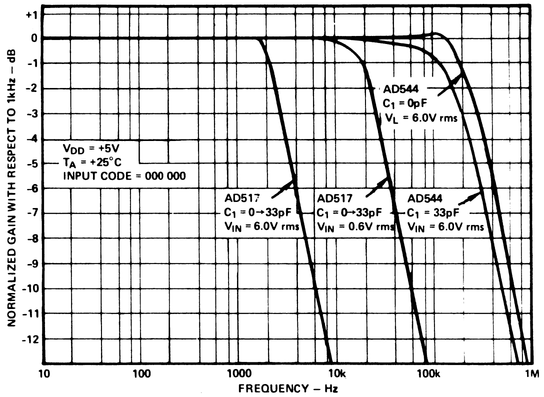


Figure 11. Frequency Response with AD544 and AD517 Amplifiers

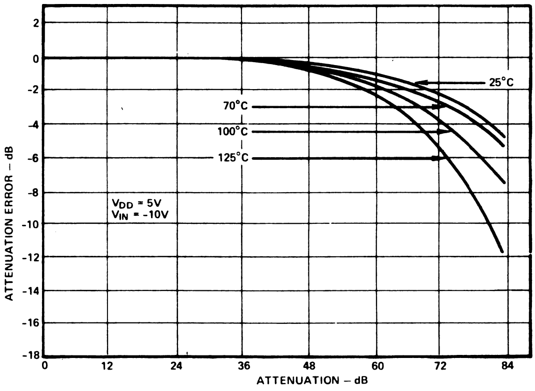


Figure 9. DC Attenuation Error vs. Attenuation & Temperature

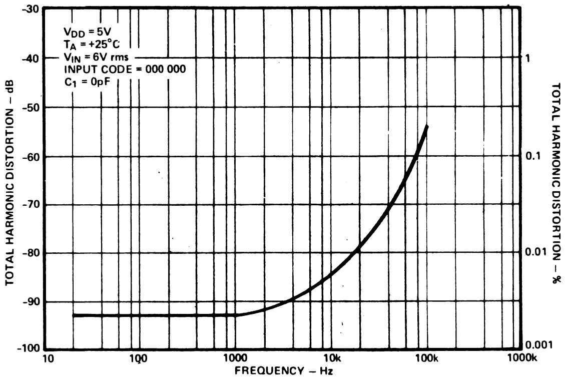


Figure 12. Distortion vs. Frequency Using AD544 Amplifier

ANALOG DEVICES

CMOS 10-& 12-Bit Monolithic Multiplying D/A Converters

AD7520, AD7521

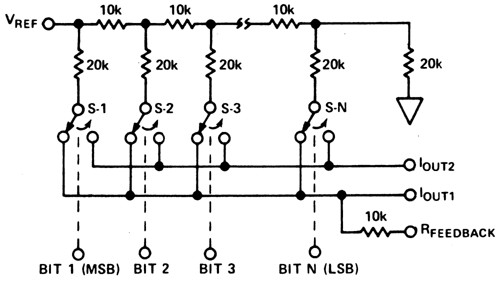
FEATURES

AD7520: 10-Bit Resolution
AD7521: 12-Bit Resolution
Linearity: 8-, 9- and 10-Bit
Nonlinearity Tempco: 2ppm of FSR/°C
Low Power Dissipation: 20mW
Current Settling Time: 500ns
Feedthrough Error: 1/2LSB @ 100kHz
TTL/DTL/CMOS Compatible

Note: AD7533 is recommended for new 10-bit designs.

AD7541, AD7542 or AD7543 is recommended for new 12-bit designs.

AD7520, AD7521 FUNCTIONAL BLOCK DIAGRAM



DIGITAL INPUTS (DTL/TTL/CMOS COMPATIBLE)

AD7520: N=10
AD7521: N=12
Logic: A switch is closed to I_{OUT1} for its digital input in a "HIGH" state.

GENERAL DESCRIPTION

The AD7520 (AD7521) is a low cost, monolithic 10-bit (12-bit) multiplying digital-to-analog converter packaged in a 16-pin (18-pin) DIP. The devices use advanced CMOS and thin wilm technologies providing up to 10-bit accuracy with TTL/DTL/CMOS compatibility.

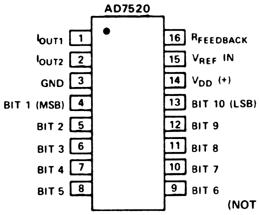
The AD7520 (AD7521) operates from +5V to +15V supply and dissipates only 20mW, including the ladder network.

Typical AD7520 (AD7521) applications include: digital/analog multiplication, CRT character generation, programmable power supplies, digitally controlled gain circuits, etc.

ORDERING INFORMATION

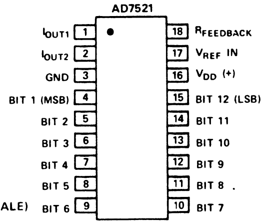
Nonlinearity	Temperature Range		
	0 to +70°C	-25°C to +85°C	-55°C to +125°C
0.2% (8-Bit)	AD7520JN AD7521JN	AD7520JD AD7521JD	AD7520SD AD7521SD
0.1% (9-Bit)	AD7520KN AD7521KN	AD7520KD AD7521KD	AD7520TD AD7521TD
0.05% (10-Bit)	AD7520LN AD7521LN	AD7520LD AD7521LD	AD7520UD AD7521UD

PIN CONFIGURATIONS



(NOT TO SCALE)

16-PIN DIP TOP VIEW



18-PIN DIP TOP VIEW

PACKAGE IDENTIFICATION[1]

Suffix D: Ceramic DIP Package
AD7520: (D16B)
AD7521: (D18B)

Suffix N: Plastic DIP Package
AD7520 (N16B)
AD7521 (N18B)

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[1] See Section 20 for package outline information.

SPECIFICATIONS (V_{DD} = +15, V_{REF} = +10V, T_A = +25°C unless otherwise noted)

PARAMETER	AD7520	AD7521	TEST CONDITIONS
DC ACCURACY[1]			
Resolution	10 Bits	12 Bits	
Nonlinearity (See Figure 5)			
	J, 0.2% of FSR max (8 Bit)	*	S,T,U: over −55°C to +125°C
	S, 0.2% of FSR max (8 Bit)	*	$-10V \leq V_{REF} \leq +10V$
	K, 0.1% of FSR max (9 Bit)	*	
	T, 0.1% of FSR max (9 Bit)	*	
	L, 0.05% of FSR max (10 Bit)	*	
	U, 0.05% of FSR max (10 Bit)	*	
Nonlinearity Tempco	2ppm of FSR/°C max	*	$-10V \leq V_{REF} \leq +10V$
Gain Error[2]	0.3% of FSR typ	*	$-10V \leq V_{REF} \leq +10V$
Gain Error Tempco[2]	10ppm of FSR/°C max	*	$-10V \leq V_{REF} \leq +10V$
Output Leakage Current (either output)	200nA max	*	Over specified temperature range
Power Supply Rejection (See Figure 6)	50ppm of FSR%/°C typ	*	
AC ACCURACY			To 0.05% of FSR
Output Current Settling Time (See Figure 10)	500ns typ	*	All digital inputs low to high and high to low
Feedthrough Error (See Figure 9)[4]	10mV p-p max	*	V_{REF} = 20V p-p, 100kHz All digital inputs low
REFERENCE INPUT			
Input Resistance[3]	5kΩ min	*	
	10kΩ typ	*	
	20kΩ max	*	
ANALOG OUTPUT			
Output Capacitance (See Figure 8) I_{OUT1}	120pF typ	*	All digital inputs high
I_{OUT2}	37pF typ	*	All digital inputs high
I_{OUT1}	37pF typ	*	All digital inputs low
I_{OUT2}	120pF typ	*	All digital inputs low
Output Noise (both outputs) (See Figure 7)	Equivalent to 10kΩ typ Johnson noise	*	
DIGITAL INPUTS[5]			
Low State Threshold	0.8V max	*	Over specified temperature range
High State Threshold	2.4V min	*	Over specified temperature range
Input Current (low-to high state)	1μA typ	*	Over specified temperature range
Input Coding	Binary	*	See Tables 1 & 2 under Applications
POWER REQUIREMENTS			
Power Supply Voltage Range	+5V to +15V	*	
I_{DD}	5nA typ	*	All digital inputs at GND
	2mA max	*	All digital inputs high or low
Total Dissipation (Including ladder)	20mW typ	*	

NOTES:

[1] Full scale range (FSR) is 10V for unipolar mode and ±10V for bipolar mode.

[2] Using the internal $R_{FEEDBACK}$

[3] Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.

[4] To minimize feedthrough with the ceramic package, the user must ground the metal lid. If the lid is not grounded, then the feedthrough is 10mV typical and 30mV maximum.

[5] Ladder and feedback resistor tempco is approximately −150ppm/°C.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

V_{DD} (to GND)	+17V
V_{REF} (to GND)	±25V
Digital Input Voltage Range	V_{DD} to GND
Output Voltage (Pin 1, Pin 2)	-100mV to V_{DD}
Power Dissipation (package)	
up to +75°C	450mW
derates above +75°C by	6mW/°C
Operating Temperature	
JN, KN, LN Versions	0 to +70°C
JD, KD, LD Versions	-25°C to +85°C
SD, TD, UD Versions	-55°C to +125°C
Storage Temperature	-65°C to +150°C

CAUTION:

1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF}.
2. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{DD} = +15V unless otherwise noted

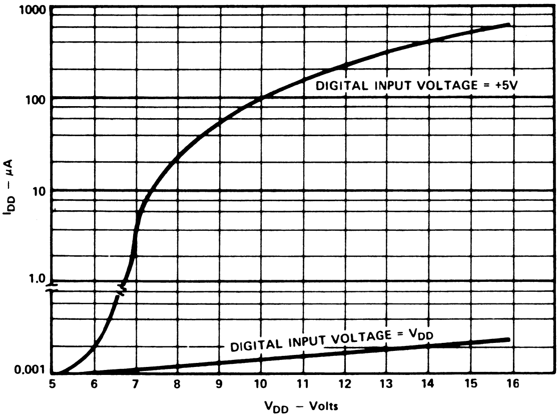


Figure 1. Supply Current vs. Supply Voltage

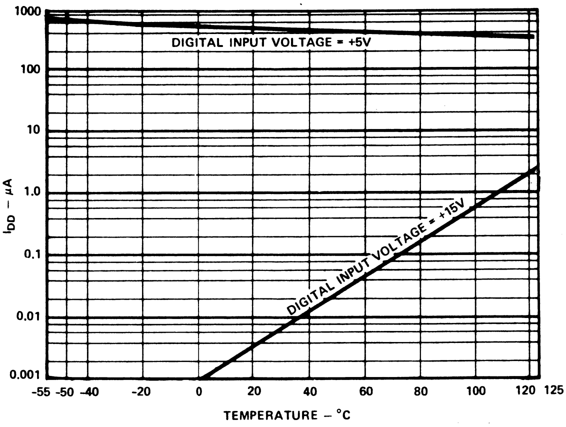


Figure 2. Supply Current vs. Temperature

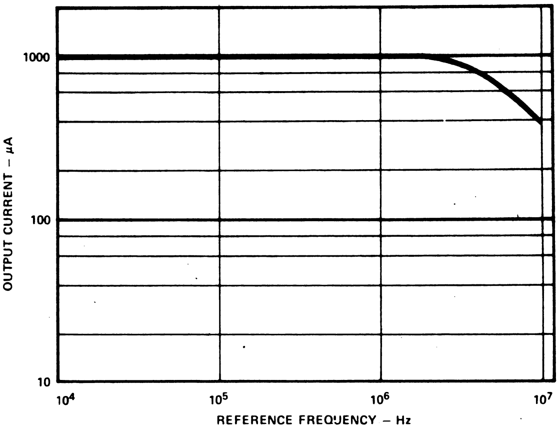


Figure 3. Output Current Bandwidth

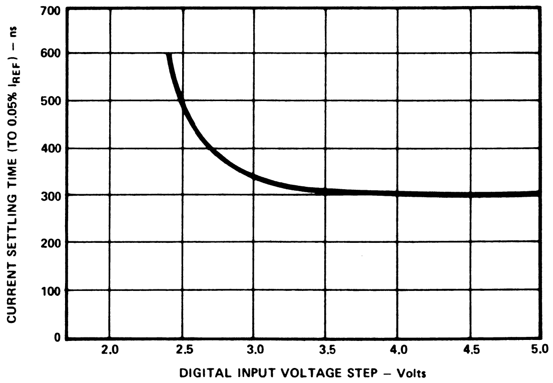


Figure 4. Output Current Settling Time vs. Digital Input Voltage

TEST CIRCUITS

Note: The following test circuits apply for the AD7520. Similar circuits can be used for the AD7521.

DC PARAMETERS

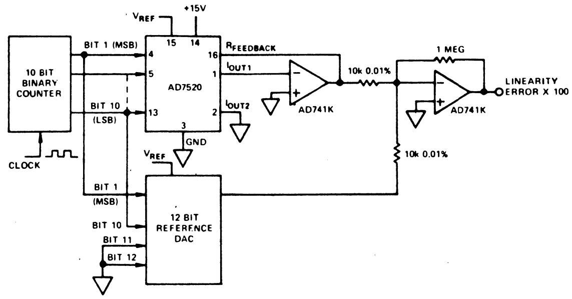


Figure 5. Nonlinearity

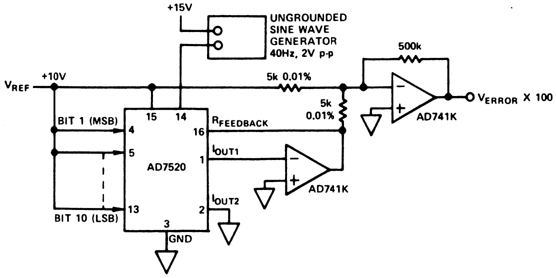


Figure 6. Power Supply Rejection

AC PARAMETERS

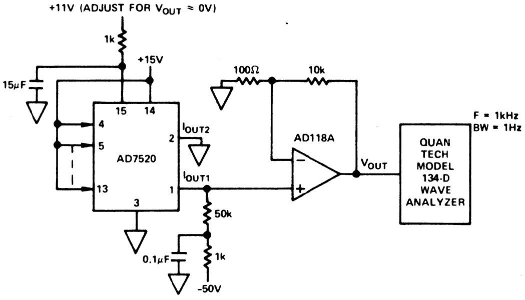


Figure 7. Noise

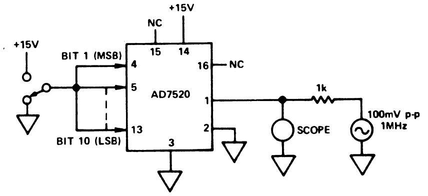


Figure 8. Output Capacitance

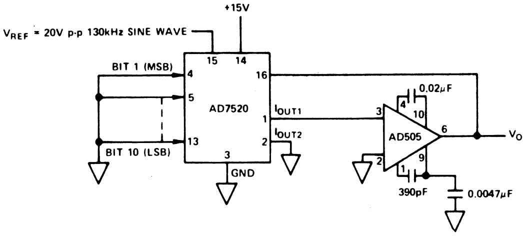


Figure 9. Feedthrough Error

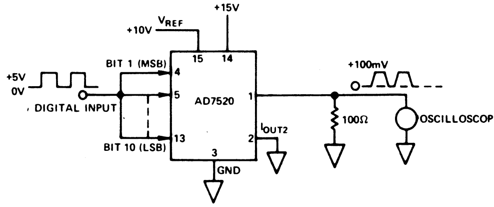


Figure 10. Output Current Settling Time

TERMINOLOGY

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of (2^{-n}) (V_{REF}). A bipolar converter of n bits has a resolution of $[2^{-(n-1)}]$ $[V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the input voltage.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from I_{OUT1} and I_{OUT2} terminals to ground.

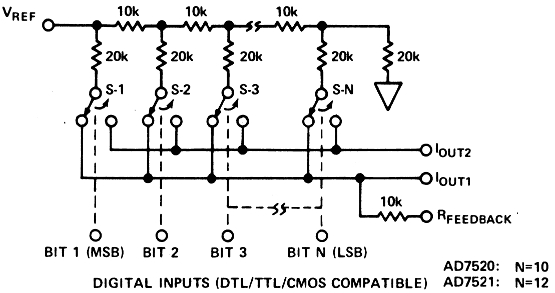
OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

CIRCUIT DESCRIPTION

GENERAL CIRCUIT INFORMATION

The AD7520 (AD7521), a 10-bit (12-bit) multiplying D/A converter, consists of a highly stable thin film R-2R ladder and ten (twelve) CMOS current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 11. An inverted R-2R ladder structure is used – that is, the binarily weighted currents are switched between the I_{OUT1} and I_{OUT2} bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.



(Switches shown for Inputs "High")

Figure 11. AD7520 (AD7521) Functional Diagram

One of the CMOS current switches is shown in Figure 12. The geometries of devices 1, 2 and 3 are optimized to make the digital control inputs DTL/TTL/CMOS compatible over the full military temperature range. The input stage drives two inverters (devices 4, 5, 6 and 7) which in turn drive the two output N-channels. The "ON" resistances of the first six switches are binarily scaled so the voltage drop across each switch is the same. For example, switch-1 of Figure 12 was designed for an "ON" resistance of 20 ohms, switch-2 of 40 ohms and so on. For a 10V reference input, the current through switch 1 is 0.5mA, the current through switch 2 is 0.25mA, and so on, thus maintaining a constant 10mV drop across each switch. It is essential that each switch voltage drop be equal if the binarily weighted current division property of the ladder is to be maintained.

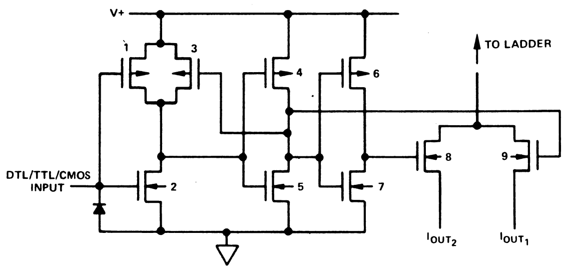


Figure 12. CMOS Switch

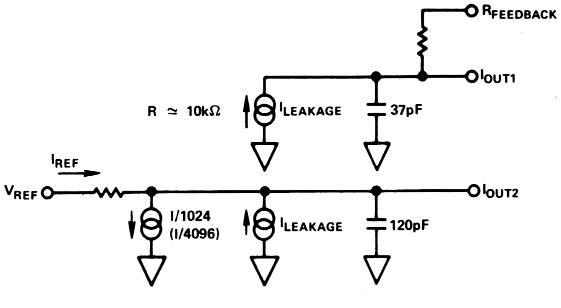


Figure 13. AD7520 (AD7521) Equivalent Circuit– All Digital Inputs Low

EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuits for all digital inputs high and all digital inputs low are shown in Figures 13 and 14. In Figure 13 with all digital inputs low, the reference current is switched to I_{OUT2}. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate while the $\frac{I}{1024}\left(\frac{I}{4096}\right)$ current source represents a constant 1-bit current drain through the termination resistor on the R-2R ladder. The "ON" capacitance of the output N channel switch is 120pF, as shown on the I_{OUT2} terminal. The "OFF" switch capacitance is 37pF, as shown on the I_{OUT1} terminal. Analysis of the circuit for all digital inputs high, as shown in Figure 14 is similar to Figure 13; however, the "ON" switches are now on terminal I_{OUT1}, hence the 120pF at that terminal.

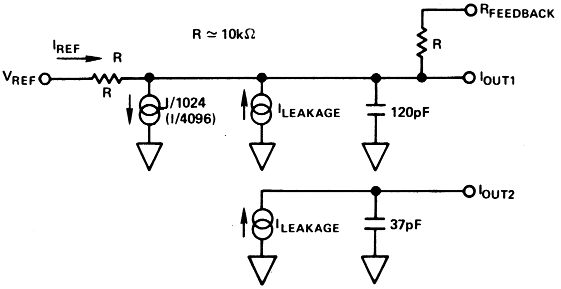


Figure 14. AD7520 (AD7521) Equivalent Circuit– All Digital Inputs High

APPLICATIONS

UNIPOLAR BINARY OPERATION

Figure 15 shows the circuit connections required for unipolar operation using the AD7520. Since V_{REF} can assume either positive or negative values, the circuit is also capable of 2-quadrant multiplication. The input code/output range table for unipolar binary operation is shown in Table 1.

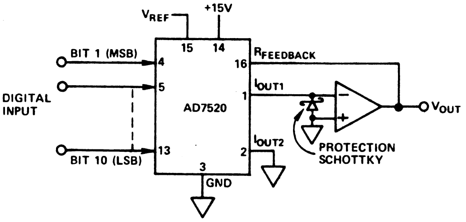


Figure 15. Unipolar Binary Operation (2-Quadrant Multiplication)

(Note: Protection Schottky not required with TRIFET output amplifier such as AD542 or AD544).

Zero Offset Adjustment

1. Tie all digital inputs to the AD7520 (AD7521) to GND potential.
2. Adjust the offset trimpot on the output operational amplifier for 0V ±1mV at V_{OUT}.

Gain Adjustment

1. Tie all digital inputs to the AD7520 (AD7521) to the +15V supply.
2. To increase V_{OUT}, place a resistor R in series with the amplifier output terminal and $R_{FEEDBACK}$ of the AD7520 (AD7521) (R = 0 to 500Ω)
3. To decrease V_{OUT}, place a resistor R in series with V_{REF}. (R = 0 to 500Ω)

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}\ (1 - 2^{-10})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}\ (1/2 + 2^{-10})$
1 0 0 0 0 0 0 0 0 0	$\frac{-V_{REF}}{2}$
0 1 1 1 1 1 1 1 1 1	$-V_{REF}\ (1/2 - 2^{-10})$
0 0 0 0 0 0 0 0 0 1	$-V_{REF}\ (2^{-10})$
0 0 0 0 0 0 0 0 0 0	0

NOTE: 1 LSB = $2^{-10}\ V_{REF}$

Table 1. Code Table – Unipolar Binary Operation

BIPOLAR (OFFSET BINARY) OPERATION

Figure 16 illustrates the AD7520 connected for bipolar operation. Since the digital input can accept bipolar numbers and V_{REF} can accept a bipolar analog input, the circuit can perform a 4-quadrant multiplying function. Input coding is offset binary (modified 2's complement) as shown in Table 2.

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}\ (1 - 2^{-9})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}\ (2^{-9})$
1 0 0 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1 1 1	$V_{REF}\ (2^{-9})$
0 0 0 0 0 0 0 0 0 1	$V_{REF}\ (1 - 2^{-9})$
0 0 0 0 0 0 0 0 0 0	V_{REF}

NOTE: 1 LSB = $2^{-9}\ V_{REF}$

Table 2. Code Table – Bipolar (Offset Binary) Operation

When a switch's control input is a Logical "1", that switch's current is steered to I_{OUT1}, forcing the output of amplifier #1 to

$$V_{OUT} = -(I_{OUT1})(10k)$$

where 10k is the value of the feedback resistor.

A Logical "0" on the control input steers the switch's current to I_{OUT2}, which is terminated into the summing junction of amplifier #2. Resistors R1 and R2 need not track the internal R-2R circuitry; however, they should closely match each other to insure that the voltage at amplifer #2's output will force a current into R2 which is equal in magnitude but opposite in polarity to the current at I_{OUT2}. This creates a push-pull effect which halves the resolution but doubles the output range for changes in the digital input.

With the MSB a Logic "1" and all other bits a Logic "0", a 1/2 LSB difference current exists between I_{OUT1} and I_{OUT2}, creating an offset of 1/2 LSB. To shift the transfer curve to zero, resistor R-9 is used to sum 1/2 LSB of current into the I_{OUT2} terminal.

Offset Adjustment

1. Make V_{REF} approximately +10V.
2. Tie all digital inputs to +15V (Logic "1").
3. Adjust amplifier #2 offset trimpot for 0V ±1mV at amplifier #2 output.
4. Tie MSB (Bit 1) to +15V, all other bits to ground.
5. Adjust amplifier #1 offset trimpot for 0V ±1mV at V_{OUT}.

Gain Adjustment

Gain adjustment is the same as for unipolar operation.

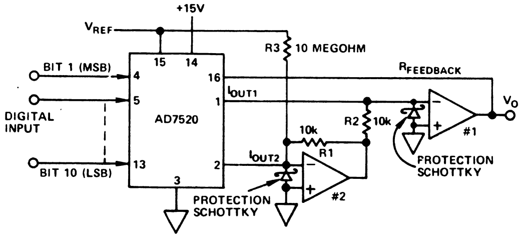


Figure 16. Bipolar Operation (4-Quadrant Multiplication)

(Note: Protection Schottky not required with TRIFET output amplifier such as AD542 or AD544).

DYNAMIC PERFORMANCE CHARACTERISTICS

The following circuits and associated waveforms illustrate the dynamic performance which can be expected using some commonly available IC amplifiers. All settling times are to 0.05% of 10V.

AD741J

Small Signal Bandwidth:	180kHz
Settling Time:	20μs

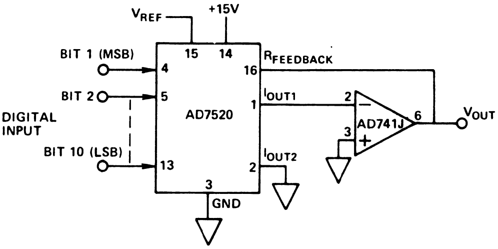


Figure 17. DAC Circuit Using AD741J

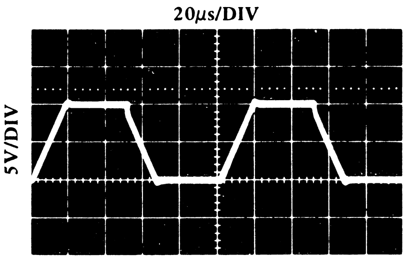


Figure 18. Output Waveform

AD518K

Small Signal Bandwidth:	1.0MHz
Settling Time:	6.0μs

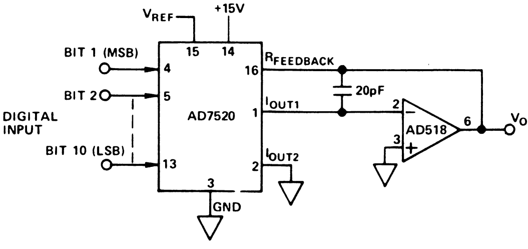


Figure 19. DAC Circuit Using AD518K

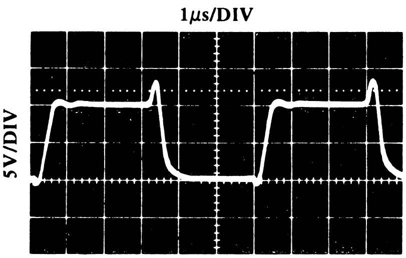


Figure 20. Output Waveform

AD505J

Small Signal Bandwidth:	1.0MHz
Settling Time:	2.5μs

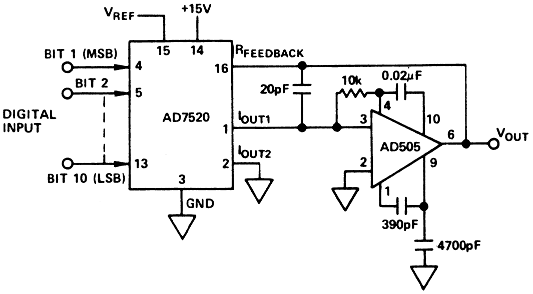


Figure 21. DAC Circuit Using AD505J

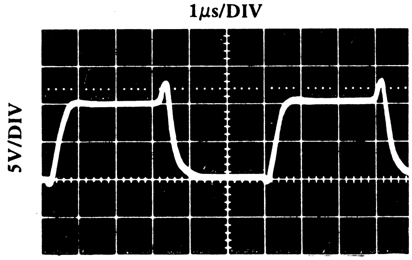


Figure 22. Output Waveform

AD509K

Small Signal Bandwidth:	1.6MHz
Settling Time:	2.0μs

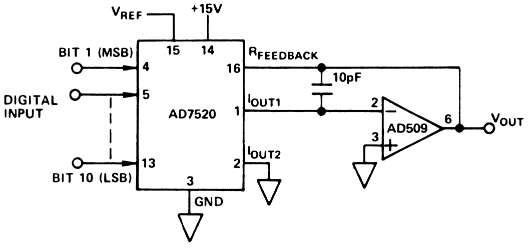


Figure 23. DAC Circuit Using AD509K

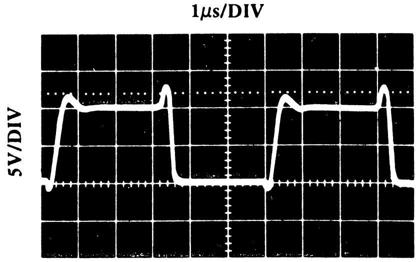


Figure 24. Output Waveform

ANALOG/DIGITAL DIVISION

With the AD7520 connected in its normal multiplying configuration as shown in Figure 15, the transfer function is

$$V_0 = -V_{IN}\left(\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \cdots \frac{A_n}{2^n}\right)$$

where the coefficients A_X assume a value of 1 for an ON bit and 0 for an OFF bit.

By connecting the DAC in the feedback of an operational amplifier, as shown in Figure 25, the transfer function becomes

$$V_0 = \left(\frac{-V_{IN}}{\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \cdots \frac{A_n}{2^n}}\right)$$

This is division of an analog variable (V_{IN}) by a digital word. With all bits off, the amplifier saturates to its bound, since division by zero isn't defined. With the LSB (Bit 10) ON, the gain is 1024. With all bits ON, the gain is 1 (±1 LSB).

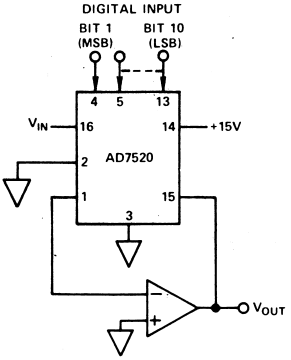


Figure 25. Analog/Digital Divider

ANALOG DEVICES

CMOS 10-Bit, Buffered Multiplying D/A Converter

AD7522

FEATURES

10-Bit Resolution
8-, 9- & 10-Bit Linearity
Microprocessor Compatible
Double Buffered Inputs
Serial or Parallel Loading
DTL/TTL/CMOS Direct Interface
Nonlinearity Tempco: 2ppm of FSR/°C
Gain Tempco: 10ppm of FSR/°C
Very Low Power Dissipation
Very Low Feedthrough

GENERAL DESCRIPTION

The AD7522 is a monolithic CMOS 10-bit multiplying D/A converter, with an input buffer and a holding register, allowing direct interface with microprocessors. Most applications require the addition of only an operational amplifier and a reference voltage.

The key to easy interface to a data bus is the AD7522's ability to load the input buffer in two bytes (an 8-bit and a 2-bit byte), and subsequently move this data to a holding register, where the digital word is converted into an analog current or voltage (with external operational amplifier). The input loading of either 8 or 10 bits can be done in a parallel or serial mode.

The AD7522 is packaged in a 28-pin DIP, and operates with a +15V main supply at 2mA max, and a logic supply of +5V for TTL interface, or +10 to +15V for CMOS interface.

A thin film on high density CMOS process, using silicon nitride passivation, ensures high reliability and excellent stability.

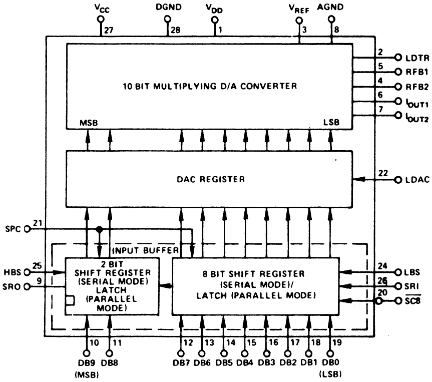
ORDERING INFORMATION

Nonlinearity	Temperature Range		
	0 to +70°C	-25°C to +85°C	-55°C to +125°C
0.2% (8-Bit)	AD7522JN	AD7522JD	AD7522SD
0.1% (9-Bit)	AD7522KN	AD7522KD	AD7522TD
0.05% (10-Bit)	AD7522LN	AD7522LD	AD7522UD

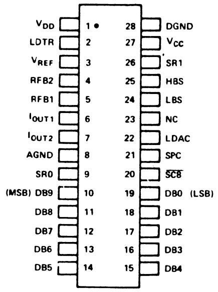
PACKAGE IDENTIFICATION[1]

Suffix "D": Ceramic DIP Package – (D28B)
Suffix "N": Plastic DIP Package – (N28A)

AD7522 FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



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[1] See section 20 for package outline information.

SPECIFICATIONS (V_{DD} = +15V, V_{CC} = +5V, V_{REF} = ±10V, TA = +25°C unless otherwise noted)

PARAMETER		TA = +25°C	OVER SPECIFIED TEMP. RANGE	TEST CONDITIONS
STATIC ACCURACY				
Resolution	All	10 Bits min	10 Bits min	$\overline{SC8}$ = "1"
Nonlinearity	AD7522J	±0.2% FSR max		-10V≤V_{REF}≤+10V
	AD7522S	±0.2% FSR max	±0.2% FSR max	
	AD7522K	±0.1% FSR max		
	AD7522T	±0.1% FSR max	±0.1% FSR max	
	AD7522L	±0.05% FSR max		
	AD7522U	±0.05% FSR max	±0.05% FSR max	
Nonlinearity Tempco[1]	AD7522J,K,L	±1ppm FSR/°C typ	±2ppm FSR/°C max	
	AD7522S,T,U		±2ppm FSR/°C max	
Gain Error	AD7522J,K,L	±0.3% Reading typ		
Gain Error Tempco[1]	AD7522J,K,L	±5ppm of Reading/°C typ	±10ppm of Reading/°C max	
	AD7522S,T,U		±10ppm of Reading/°C max	
Output Leakage Current at I_{OUT1} or I_{OUT2}	All		200nA max	I_{OUT1}: DB0 through DB9 = 0 I_{OUT2}: DB0 through DB9 = 1
Power Supply Rejection	AD7522J,K,L	50ppm of Reading/% typ		
AC ACCURACY				
Feedthrough Error[1]	All	1mV p-p typ, 10mV p-p max		V_{REF}= 20V p-p; 10kHz
Output Current Settling Time	AD7522J,K,L	500ns typ		To 0.05% of FSR for a FSR Step. HBS and LBS Low to High LDAC = 1
REFERENCE INPUT				
Input Resistance	All	5kΩ min/20kΩ max	50kΩ min/20kΩ max	
ANALOG OUTPUT				
Output Capacitance				
C_{OUT1}	AD7522J,K,L	120pF typ		All Data Input High
C_{OUT2}	AD7522J,K,L	40pF typ		
C_{OUT1}	AD7522J,K,L	40pF typ		All Data Inputs Low
C_{OUT2}	AD7522J,K,L	120pF typ		
DIGITAL INPUTS				
Low State Threshold	All	0.8V max	0.8V max	V_{CC} = +5V
	All	1.5V max	1.5V max	V_{CC} = +15V
High State Threshold	All	2.4V min	2.4V min	V_{CC} = +5V
	All	13.5V min	13.5V min	V_{CC} = +15V
Input Current	AD7522J,K,L	1μA typ		
LDAC Pulse Width[1]	All	500ns min	500ns min	LDAC: 0 to +3V
HBS, LBS Pulse Width[1]	All	500ns min	500ns min	HBS, LBS: 0 to +3V
Serial Clock Frequency[1]	All	1MHz max	1MHz max	
HBS, LBS Data Set Up[2]	All	250ns min	250ns min	
Data Hold Time[3]	All	500ns min, 200ns typ	500ns min	
POWER REQUIREMENTS				
I_{DD}	All	2mA max		In Quiescent State
I_{CC}	All	2mA max		

Notes

[1] Guaranteed by design. Not tested.

[2] Data setup time is the minimum amount of time required for DB0 - DB9 to be stable prior to strobing HBS, LBS.

[3] Data hold time is the minimum amount of time required for DB0 - DB9 to be stable after strobing HBS, LBS.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

V_{REF} to GND	±25V
V_{DD} to GND	+17V
V_{CC} to GND	+17V
V_{CC} to V_{DD}	+0.4V
Output Voltage (pins 6 & 7)	-0.3V to V_{DD}
Operating Temperature	
JN, KN, LN versions	0 to +70°C
JD, KD, LD versions	-25°C to +85°C
SD, TD, UD versions	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Power Dissipation (Package)	
Up to +50°C:	
Plastic (Suffix N)	1200mW
Ceramic (Suffix D)	1000mW
Derate Above +50°C by	
Plastic (Suffix N)	12mW/°C
Ceramic (Suffix D)	10mW/°C
Digital Input Voltage Range	V_{DD} to GND

CAUTION:

1. Do not apply voltages higher than V_{CC} to SRO.
2. Do not apply voltages higher than V_{DD} or less than GND to any other input/output terminal except V_{REF}, R_{FB1} or R_{FB2}.
3. The digital control inputs are zener protected, however permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.
4. V_{CC} should never exceed V_{DD} by more than 0.4V, especially during power ON or OFF sequencing.

TERMINOLOGY

RESOLUTION

Value of the LSB. For example, a unipolar n-bit converter has a resolution of (2^{-n}) (V_{REF}). A bipolar n-bit converter has a resolution of $[2^{-(n-1)}]$ $[V_{REF}]$. Resolution in no way implies linearity.

GAIN

The "gain" of a converter is that analog scale factor setting that establishes the nominal conversion relationship, e.g., 10V full scale. It is a linear error which can be externally adjusted (see gain adjustment on next page).

OUTPUT LEAKAGE CURRENT

Current which appears on the OUT1 terminal when the DAC register is loaded with all "0's" or on the OUT2 terminal when the DAC register is loaded with all "1's."

DAC CIRCUIT DESCRIPTION

GENERAL CIRCUIT INFORMATION

The AD7522's DAC functional block consists of a highly stable Silicon Chromium thin film R-2R ladder, and ten SPDT N-channel current steering switches. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 1. An inverted R-2R ladder structure is used – that is, the binarily weighted currents are switched between the I_{OUT1} and I_{OUT2} bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

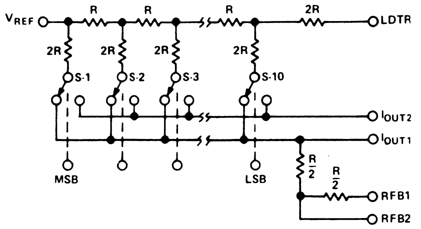


Figure 1. DAC Functional Diagram

EQUIVALENT CIRCUIT

The DAC equivalent circuit is shown in Figure 2. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate, while the $I_{REF}/1024$ current source represents the 1LSB of current lost through the ladder termination resistor to ground. The C_{OUT1} and C_{OUT2} output capacitances are as shown when the DAC latches feed the DAC with all "1's." If the DAC latches are loaded with all "0's," C_{OUT1} is 37pF, while C_{OUT2} is 120pF. In addition, C_{SD} is replaced by 10 ohms, and the 10 ohm R_{ON} in I_{OUT1} is replaced by a C_{SD} of 10pF. When fast amplifiers are used, it will be necessary to provide phase compensation (in the form of feedback capacitance) to cancel the pole formed by $R_{FEEDBACK}$ and C_{OUT} if stability is to be maintained.

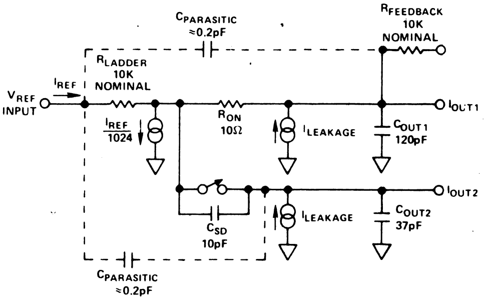


Figure 2. Equivalent Circuit (Shown for all Digital Inputs High)

PIN FUNCTION DESCRIPTION

PIN	MNEMONIC	DESCRIPTION
1	V_{DD}	+15V (nominal) Main Supply.
2	LDTR	R-2R Ladder Termination Resistor. Normally grounded for unipolar operation or terminated at I_{OUT2} for bipolar operation.
3	V_{REF}	Reference Voltage Input. Since the AD7522 is a multiplying DAC, V_{REF} may vary over the range of ±10V.
4	RFB2	$R_{FEEDBACK} \div 2$; gives full scale equal to $V_{REF}/2$.
5	RFB1	$R_{FEEDBACK}$, used for normal unity gain (at full scale) D/A conversion.
6	I_{OUT1}	DAC Current OUT1 Bus. Normally terminated at virtual ground of output amplifier.
7	I_{OUT2}	DAC Current OUT2 Bus, terminated at ground for unipolar operation, or virtual ground of op amp for bipolar operation.
8	AGND	Analog Ground. Back gate of DAC N-channel SPDT current steering switches.
9	SRO	Serial Output. An auxiliary output for recovering data in the input buffer.
10	DB9	Data Bit 9. Most significant parallel data input.
11	DB8	Data Bit 8.
12	DB7	Data Bit 7.
13	DB6	Data Bit 6.
14	DB5 Note 1	Data Bit 5.
15	DB4	Data Bit 4.
16	DB3	Data Bit 3.
17	DB2	Data Bit 2.
18	DB1	Data Bit 1.
19	DB0	Data Bit 0. Least significant parallel data input.
20	$\overline{SC8}$	8-Bit Short Cycle Control. When in serial mode, if $\overline{SC8}$ is held to Logic "0", the two least significant input latches in the input buffer are bypassed to provide proper serial loading of 8-bit serial words. If $\overline{SC8}$ is held to Logic "1", the AD7522 will accept a 10-bit serial word. Data bits 0 (LSB) and DB1 are in a parallel load mode when $\overline{SC8} = 0$ and should be tied to a logic low state to prevent false data from being loaded.
21	SPC	Serial/Parallel Control. If SPC is a Logic "0", the AD7522 will load parallel data appearing on DB0 through DB9 into the input buffer when the appropriate strobe inputs are exercised (see HBS and LBS). If SPC is a Logic "1", the AD7522 will load serial data appearing on Pin 26 into the input buffers. Each serial data bit must be "strobed" into the buffer with the HBS and LBS.
22	LDAC	Load DAC: When LDAC is a Logic "0", the AD7522 is in the "hold" mode, and digital activity in the input buffer is locked out. When LDAC is a Logic "1", the AD7522 is in the "load" mode, and data in the input buffer loads the DAC register.
23	NC	No Connection.
24	LBS	Low Byte Strobe. When in "parallel load" mode (SPC = 0), parallel data appearing on the DB0 (LSB) through DB7 inputs will be "clocked" into the input buffer on the positive going edge of the LBS. When in "serial load" mode (SPC = 1), serial data bits appearing at the serial input terminal, Pin 26, will be "clocked" into the input buffer on the positive going edge of HBS and LBS. (HBS and LBS must be clocked simultaneously when in "serial load" mode.)
25	HBS	High Byte Strobe. When in "parallel load" mode (SPC = 0), parallel data appearing on the DB9 (MSB) and DB8 data inputs will be "clocked" into the input buffer on the positive going edge of HBS. When in "serial load" mode (SPC = 1), serial data bits appearing at the serial input terminal, Pin 26, will be "clocked" into the input buffer on the positive going edges of HBS and LBS. (HBS and LBS must be clocked simultaneously when in "serial load" mode.)
26	SRI	Serial Input.
27	V_{CC}	Logic Supply. If +5V is applied, all digital inputs/outputs are TTL compatible. If +10V to +15V is applied, digital inputs/outputs are CMOS compatible.
28	DGND	Digital Ground

Note 1: Logic "1" applied to a data bit steers that bit's current to the $I_{OUT}1$ terminal.

APPLICATIONS

(Note: Protection Schottky CR3 in Figure 3 and CR3, CR4 in Figure 4 are not required when using TRI-FET amps such as the AD542 or AD544).

UNIPOLAR OPERATION

Figure 3 shows the analog circuit connections required for unipolar operation. The input code/output voltage relationship is shown in Table 1.

Zero Offset Adjustment

1. Adjust the op amp's offset potentiometer for <1mV on the amplifier junction. (Each millivolt of amplifier V_{OS} causes ±0.66mV of differential nonlinearity which adds to the ladder nonlinearity.)

Gain Adjustment

1. Set R1 and R2 to 0Ω. Load the DAC register with all "1's."
2. If analog out is greater than $-V_{REF}$, increase R1 for required full scale output. If analog out is less than $-V_{REF}$, increase R2 for required full scale output.

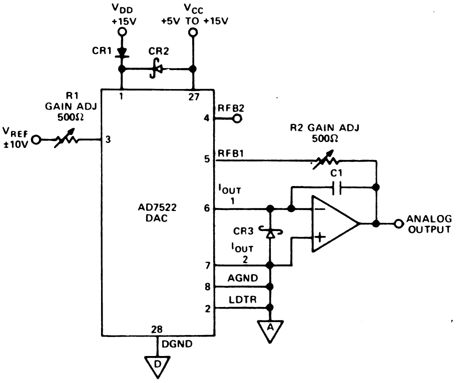


Figure 3. Unipolar Binary Operation (2-Quadrant Multiplication)

DIGITAL INPUT	ANALOG OUTPUT
1111111111	$-V_{REF}\ (1 - 2^{-10})$
1000000001	$-V_{REF}\ (1/2 + 2^{-10})$
1000000000	$-V_{REF}/2$
0111111111	$-V_{REF}\ (1/2 - 2^{-10})$
0000000001	$-V_{REF}\ (2^{-10})$
0000000000	0

Table 1. Unipolar Code Table

BIPOLAR OPERATION

Figure 4 shows the analog circuit connections required for bipolar operation. The input code/output voltage relationship is shown in Table 2.

Zero Offset Adjustment

1. Adjust the offset potentiometer of amplifier A1 and A2 for <1mV on the respective summing junctions. If the analog out for code 1000000000 is not zero, sum current into or out of the summing junction of A1 for 0V at analog out.

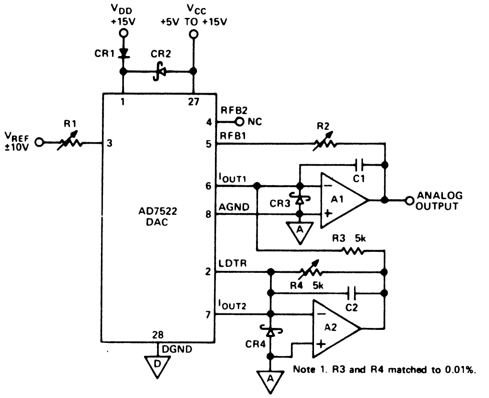


Figure 4. Bipolar Operation

Gain Adjustment

1. Load the DAC register with all "0's." Set R1 and R2 to 0Ω.
2. If analog out is greater than $+V_{REF}$, increase R2 until it reads precisely $+V_{REF}$. If analog out is less than $+V_{REF}$, increase R1 until it reads precisely V_{REF}.

DIGITAL INPUT	ANALOG OUTPUT
1111111111	$-V_{REF}\ (1 - 2^{-9})$
1000000001	$-V_{REF}\ (2^{-9})$
1000000000	0
0111111111	$V_{REF}\ (2^{-9})$
0000000001	$V_{REF}\ (1 - 2^{-9})$
0000000000	V_{REF}

Table 2. Bipolar Code Table

SINGLE BYTE PARALLEL LOADING

Figure 5 illustrates the logic connections for loading single byte parallel data into the input buffer. DB0 should be grounded on "K" and "T" versions, and DB0 and DB1 should be grounded on "J" and "S" versions for monotonic operation of the DAC. DB9 is always the MSB, whether 8-bit, 9-bit, or 10-bit linear AD7522's are used.

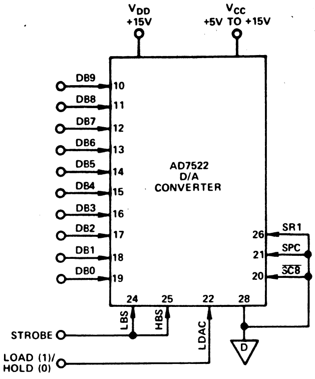


Figure 5. Single Byte Parallel Loading

When data is stable on the parallel inputs (DB0-DB9), it can be transferred into the input buffer on the positive edge of the strobe pulse.

Data is transferred from the input buffer to the DAC register when LDAC is a Logic "1." LDAC is a level-actuated (versus edge-triggered) function and must be held "high" at least 0.5μs for data transfer to occur.

TWO BYTE PARALLEL LOADING

Figures 6 and 7 show the logic connections and timing requirements for interfacing the AD7522 to an 8-bit data bus for two byte loading of a 10-bit word.

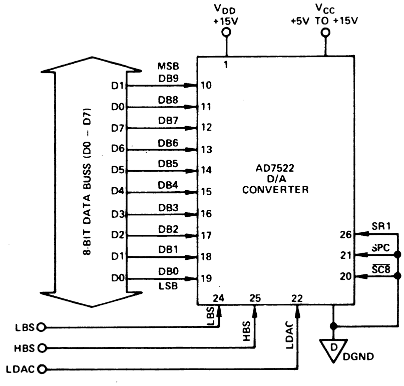
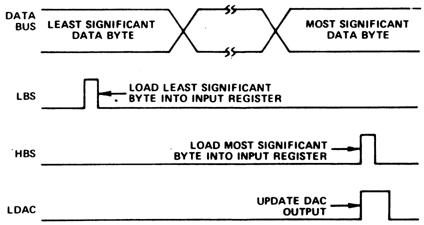


Figure 6. Two Byte Parallel Loading



DATA BUS
LEAST SIGNIFICANT DATA BYTE
MOST SIGNIFICANT DATA BYTE
LBS
LOAD LEAST SIGNIFICANT BYTE INTO INPUT REGISTER
HBS
LOAD MOST SIGNIFICANT BYTE INTO INPUT REGISTER
LDAC
UPDATE DAC OUTPUT

Figure 7. Timing Diagram

First, the least significant data byte (DB0 through DB7) is loaded into the input buffer on the positive edge of LBS. Subsequently, the data bus is used for status indication and instruction fetching by the CPU. When the most significant data byte (DB8 and DB9) is available on the bus, the input buffer is loaded on the positive edge of HBS. The DAC register updates to the new 10-bit word when LDAC is "high." LDAC may be exercised coincident with, or at any time after HBS loads the second byte of data into the input buffer.

SERIAL LOADING

Figure 8 and Figure 9 show the connections and timing diagram for serial loading.

To load a 10-bit word ($\overline{SC8}$ = 1), HBS and LBS must be strobed simultaneously with exactly 10 positive edges to clock the serial data into the input buffer. For 8-bit words (SC8 = 0), only 8 positive edges are required.

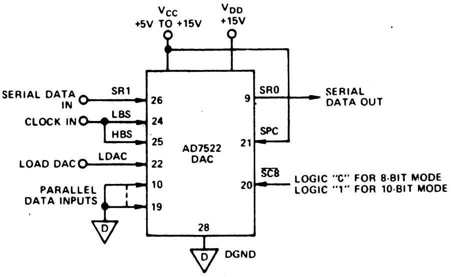


Figure 8. Serial 8- and 10-Bit Loading (Analog Outputs Not Shown for Clarity)

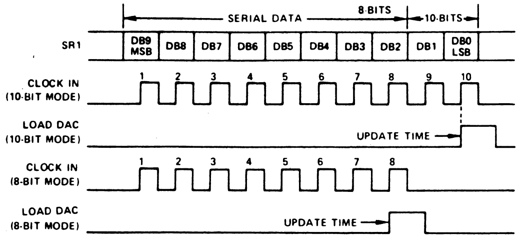


Figure 9. Timing Diagram for Serial 8- and 10-Bit Loading

APPLICATION HINTS

1. CR1 and CR2 on Figures 3 and 4 protect the AD7522 against latch-up V_{CC} exceeds V_{DD}, and may be omitted if V_{DD} and V_{CC} are driven from the same voltage.
2. Diodes CR3 on Figure 3 and CR3 and CR4 on Figure 4 clamp the amplifier junction to -300mV if they attempt to swing negative during power up or power down. The input structures of some high-speed op amps can supply substantial current under the transient conditions encountered during power sequencing. It is recommended that the PC layout be able to accommodate the diodes.
3. Fast op amps will require phase compensation for stability due to the pole formed by C_{OUT1} or C_{OUT2} and $R_{FEEDBACK}$.
4. During serial loading, all data inputs (DB0 through BD9), should be grounded.

ANALOG DEVICES

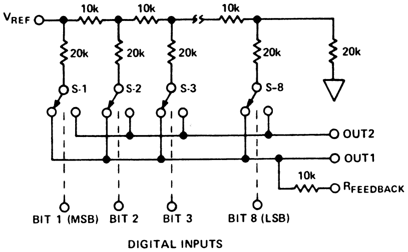
CMOS
8-Bit Multiplying D/A Converter

AD7523

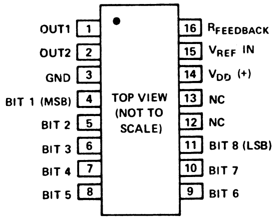
FEATURES
- Low Cost
- Fast Settling: 100ns
- Low Power Dissipation
- Low Feedthrough: ½LSB @ 200kHz
- Full Four-Quadrant Multiplying

APPLICATIONS
- Battery Operated Equipment
- Low Power, Ratiometric A/D Converters
- Digitally Controlled Gain Circuits
- Digitally Controlled Attenuators
- CRT Character Generation
- Low Noise Audio Gain Control

AD7523 FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



GENERAL DESCRIPTION

The AD7523 is a low cost, monolithic multiplying digital-to-analog converter packaged in a 16-pin DIP. The device uses an advanced monolithic, thin-film-on-CMOS technology to provide 8-bit resolution with accuracy to 10-bits and very low power dissipation.

The AD7523's excellent multiplying characteristics and low cost allow it to be used in a wide ranging field of applications such as: low noise audio gain control, CRT character generation, motor speed control, digitally controlled attenuators, etc.

ORDERING INFORMATION

Model	Linearity	Operating Temperature Range
AD7523JN	±1/2LSB	0 to +70°C
AD7523KN	±1/4LSB	
AD7523LN	±1/8LSB	
AD7523AD	±1/2LSB	-25°C to +85°C
AD7523BD	±1/4LSB	
AD7523CD	±1/8LSB	
AD7523SD	±1/2LSB	-55°C to +125°C

PACKAGE IDENTIFICATION[1]

Suffix D: Ceramic DIP – (D16B)
Suffix N: Plastic DIP – (N16B)

[1] See Section 20 for package outline information.

SPECIFICATIONS (V_{DD} = +15V, V_{REF} = +10V unless otherwise noted)

PARAMETER	T_A = +25°C	T_A = T_{min} to T_{max}	TEST CONDITION
STATIC ACCURACY			
Resolution	8 Bits min	8 Bits min	
Nonlinearity[1]			
AD7523JN, AD, SD	±1/2LSB max (±0.2% FSR max)	±1/2LSB max (±0.2% FSR max)	V_{OUT1} = V_{OUT2} = 0V
AD7523KN, BD	±1/4LSB max (±0.1% FSR max)	±1/4LSB max (±0.1% FSR max)	
AD7523LN, CD	±1/8LSB max (±0.05% FSR max)	±1/8LSB max (±0.05% FSR max)	
Monotonicity	Guaranteed over T_{min} to T_{max}		V_{OUT1} = V_{OUT2} = 0V
Gain Error[1,2,3]	-1.5% of FSR min, +1.5% of FSR max	-1.8% of FSR min, +1.8% of FSR max	Digital Inputs = V_{INH}
Power Supply Rejection (Gain)[1,2]	0.02% per % max	0.03% per % max	V_{DD} = +14V to +15V Digital Inputs = V_{INH}
Output Leakage Current			
I_{OUT1} (pin 1)	±50nA max	±200nA max	V_{OUT1} = V_{OUT2} = 0V, V_{REF} = ±10V Digital Inputs = V_{INL}
I_{OUT2} (pin 2)	±50nA max	±200nA max	V_{OUT1} = V_{OUT2} = 0V, V_{REF} = ±10V Digital Inputs = V_{INH}
DYNAMIC PERFORMANCE			
Output Current			
Settling Time[4]	150ns max	200ns max	To 0.2% FSR, Load = 100Ω Digital Inputs = V_{INH} to V_{INL} or V_{INL} to V_{INH}
Feedthrough Error[4,5]	±1/2LSB max	±1LSB max	Digital Inputs = V_{INL} V_{REF} = 20V p-p, 200kHz sinewave
REFERENCE INPUT			
Input Resistance (pin 15)	5kΩ min, 20kΩ max		V_{OUT1} = V_{OUT2} = 0V
Temperature Coefficient		-500ppm/°C max	
ANALOG OUTPUTS[4]			
Output Capacitance			
C_{OUT1} (pin 1)	100pF max	100pF max	Digital Inputs = V_{INH}
C_{OUT2} (pin 2)	30pF max	30pF max	
C_{OUT1} (pin 1)	30pF max	30pF max	Digital Inputs = V_{INL}
C_{OUT2} (pin 2)	100pF max	100pF max	
DIGITAL INPUTS			
Logic Thresholds			
V_{INH}	+14.5V min	+14.5V min	
V_{INL}	+0.5V max	+0.5V max	
Input Leakage Current			
I_{IN} (per input)	±1μA max	±1μA max	V_{IN} = 0V or +15V
Input Capacitance			
C_{IN}[4]	4pF max	4pF max	
Input Coding	Unipolar Binary of Offset Binary (see next page)		
POWER REQUIREMENTS			
V_{DD} Range	+5V min, +16V max	+5V min, +16V max	Device Functionality. Accuracy is tested and guaranteed only at V_{DD} = +15V
I_{DD} S and all /883B versions	200μA max	500μA max	
I_{DD} J, K, L, A, B, C versions	100μA max	100μA max	Digital Inputs = V_{INH} or V_{INL}

NOTES:

[1] FSR is Full Scale Range.

[2] Using internal feedback resistor, Full Scale Range (FSR) is equal to (V_{REF} - 1LSB) in the unipolar circuit on the next page.

[3] Max gain change from +25°C to T_{min} or T_{max} is ±0.3% FSR.

[4] Guaranteed by design. Not subject to test.

[5] To minimize feedthrough with the ceramic package, the user must ground the metal lid.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

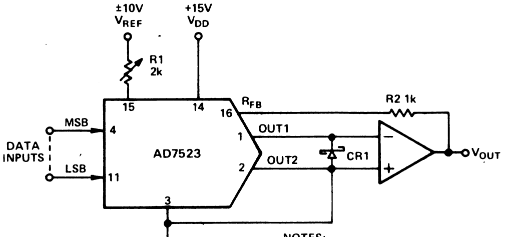
V_{DD} to GND	-0V, +17V
V_{REF} to GND	±25V
Digital Input Voltage (V_{IN}) to GND	-0.3V to V_{DD}
V_{OUT1}, V_{OUT2} (pin 1, pin 2) to GND	-0.3V to V_{DD}

Power Dissipation (package)	
To +70°C	670mW
Derate Above +70°C by	8.3mW/°C
Operating Temperature	0 to +70°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

CAUTION:

1. ESD sensitive device. The digital control inputs are Zener protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts.
2. Do not apply voltages lower than ground or higher the V_{DD} to any pin except V_{REF} (pin 15) and R_{FB} (pin 16).
3. The inputs of some IC amplifiers (especially wide bandwidth types) present a low impedance to V^- during power-up or power-down sequencing. To prevent the AD7523 OUT1 or OUT2 terminals from exceeding −300mV (which causes catastrophic substrate current) a Schottky diode (HP5082-2811 or equivalent) is recommended. The diode should be connected between OUT1 (OUT2) and ground as shown in Figure 1 and 2. Protection diodes are not required when using TRI-FET amplifiers such as the AD542 or AD544.

BASIC OPERATION



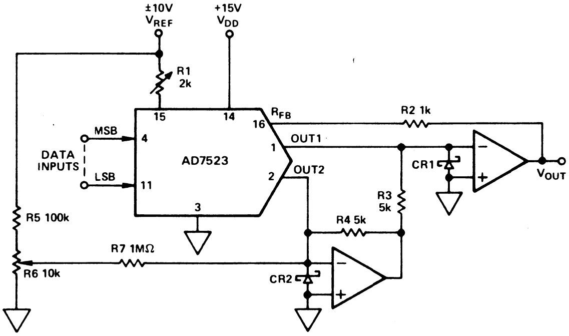
NOTES:
1. R1 AND R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
2. CR1 PROTECTS AD7523 AGAINST NEGATIVE TRANSIENTS. SEE "CAUTION" NOTE 3 AT TOP OF THIS PAGE.

Figure 1. Unipolar Binary Operation (2-Quadrant Multiplication)

DIGITAL INPUT	ANALOG OUTPUT
MSB LSB	
11111111	$-V_{REF}\left(\frac{255}{256}\right)$
10000001	$-V_{REF}\left(\frac{129}{256}\right)$
10000000	$-V_{REF}\left(\frac{128}{256}\right) = -\frac{V_{REF}}{2}$
01111111	$-V_{REF}\left(\frac{127}{256}\right)$
00000001	$-V_{REF}\left(\frac{1}{256}\right)$
00000000	$-V_{REF}\left(\frac{0}{256}\right) = 0$

Note: $1\text{LSB} = (2^{-8})(V_{REF}) = \left(\frac{1}{256}\right)(V_{REF})$

Table 1. Unipolar Binary Code Table



NOTES:
1. R3/R4 MATCH 0.1% OR BETTER.
2. R1, R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
3. R5–R7 USED TO ADJUST V_{OUT} = 0V AT INPUT CODE 10000000.
4. CR1 & CR2 PROTECT AD7523 AGAINST NEGATIVE TRANSIENTS. SEE "CAUTION" NOTE 3 AT TOP OF THIS PAGE.

Figure 2. Bipolar (4-Quadrant) Operation

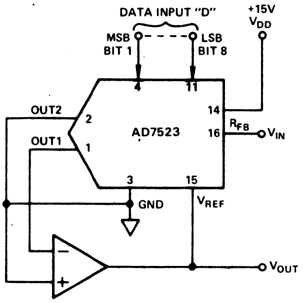
DIGITAL INPUT	ANALOG OUTPUT
MSB LSB	
11111111	$-V_{REF}\left(\frac{127}{128}\right)$
10000001	$-V_{REF}\left(\frac{1}{128}\right)$
10000000	0
01111111	$+V_{REF}\left(\frac{1}{128}\right)$
00000001	$+V_{REF}\left(\frac{127}{128}\right)$
00000000	$+V_{REF}\left(\frac{128}{128}\right)$

Note: $1\text{LSB} = (2^{-7})(V_{REF}) = \left(\frac{1}{128}\right)(V_{REF})$

Table 2. Bipolar (Offset Binary) Code Table

APPLICATIONS

DIVIDER (DIGITALLY CONTROLLED GAIN)



EQUATIONS

$$V_{OUT} = -\frac{V_{IN}}{D}$$

$$A_V = \frac{V_{OUT}}{V_{IN}} = -\frac{1}{D}$$ where: A_V = Voltage Gain

and where:

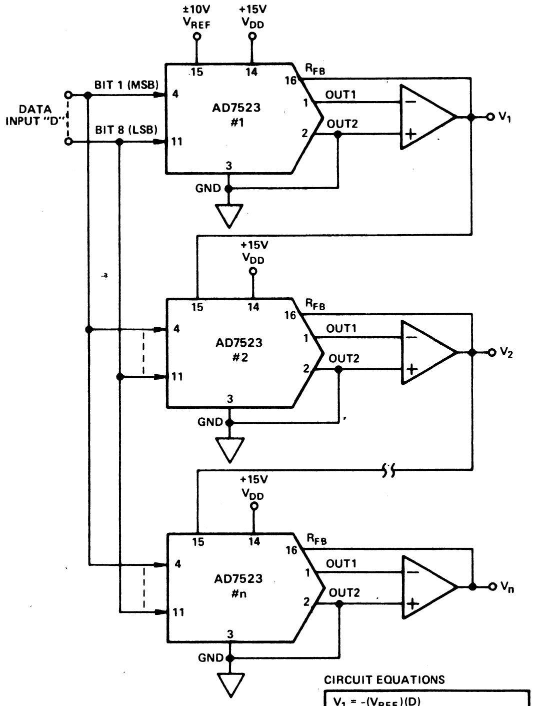
$$D = \frac{\text{BIT 1}}{2^1} + \frac{\text{BIT 2}}{2^2} + \frac{\text{BIT 8}}{2^8}$$

(BIT N = 1 or 0)

EXAMPLES

D = 00000000, $A_V = -A_{OL}$ (OP AMP)
D = 00000001, $A_V = -256$
D = 10000000, $A_V = -\frac{256}{128} = -2$
D = 11111111, $A_V = -\frac{256}{255}$

POWER GENERATION



CIRCUIT EQUATIONS

$V_1 = -(V_{REF})(D)$
$V_2 = +(V_{REF})(D^2)$
$V_n = -(V_{REF})(D^n)$, n an odd integer
$V_n = +(V_{REF})(D^n)$, n an even integer

CMOS
8-Bit Buffered Multiplying DAC
AD7524

FEATURES

Microprocessor Compatible (6800, 8085, Z80, Etc.)
TTL/CMOS Compatible Inputs
On-Chip Data Latches
End Point Linearity
Low Power Consumption
Monotonicity Guaranteed (Full Temperature Range)
Latch Free (No Protection Schottky Required)

APPLICATIONS

Microprocessor Controlled Gain Circuits
Microprocessor Controlled Attenuator Circuits
Microprocessor Controlled Function Generation
Precision AGC Circuits
Bus Structured Instruments

GENERAL DESCRIPTION

The AD7524 is a low cost, 8-bit monolithic CMOS DAC designed for direct interface to most microprocessors.

Basically an 8-bit DAC with input latches, the AD7524's load cycle is similar to the "write" cycle of a random access memory. Using an advanced thin-film on CMOS fabrication process, the AD7524 provides accuracy to 1/8LSB with a typical power dissipation of less than 10 milliwatts.

A newly improved design eliminates the protection Schottky previously required and guarantees TTL compatibility when using a +5V supply. Loading speed has been increased for compatibility with most microprocessors.

Featuring operation from +5V to +15V, the AD7524 interfaces directly to most microprocessor buses or output ports. Excellent multiplying characteristics (2- or 4-quadrant) make the AD7524 an ideal choice for many microprocessor controlled gain setting and signal control applications.

PACKAGE IDENTIFICATION[1]

Suffix D: Ceramic DIP – (D16B)
Suffix N: Plastic DIP – (N16B)

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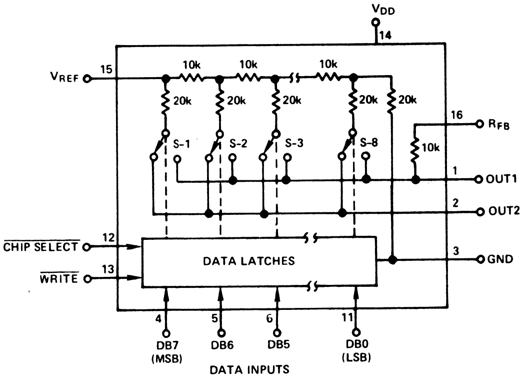
[1] See Section 20 for package outline information.

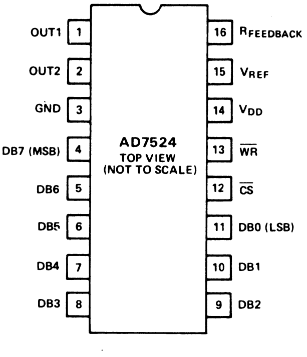
AD7524 FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Nonlinearity (V_{DD} = +5V to +15V)	Temperature Range 0 to +70°C	-25°C to +85°C	-55°C to +125°C
±1/2 LSB	AD7524JN	AD7524AD	AD7524SD
±1/4 LSB	AD7524KN	AD7524BD	AD7524TD
±1/8 LSB	AD7524LN	AD7524CD	AD7524UD

PIN CONFIGURATION



SPECIFICATIONS (V_{REF} = +10V, V_{OUT1} = V_{OUT2} = 0V unless otherwise noted)

PARAMETER	LIMIT, T_A = +25°C		LIMIT, T_{MIN}, T_{MAX}[1]		UNITS	TEST CONDITIONS/COMMENTS
	V_{DD} = +5V	V_{DD} = +15V	V_{DD} = 5V	V_{DD} = +15V		
STATIC PERFORMANCE						
Resolution	8	8	8	8	Bits	
Relative Accuracy						
AD7524JN, AD, SD	±0.2	±0.2	±0.2	±0.2	% FSR max	
AD7524KN, BD, TD	±0.2	±0.1	±0.2	±0.1	% FSR max	
AD7524LN, CD, UD	±0.2	±0.05	±0.2	±0.05	% FSR max	
Monotonicity	guaranteed	guaranteed	guaranteed	guaranteed		
Gain Error[2]	±1.0	±0.5	±1.4	±0.6	% FSR max	
Average Gain TC[3]	±0.004	±0.001	±0.004	±0.001	% FSR/°C	Gain TC measured from +25°C to T_{min} or from +25°C to T_{max}
dc Supply Rejection,[3] $\Delta Gain/\Delta V_{DD}$	0.08	0.02	0.16	0.04	% FSR/% max	ΔV_{DD} = ±10%
	0.002	0.001	0.01	0.005	% FSR/% typ	
Output Leakage Current						
I_{OUT1} (Pin 1)	±50	±50	±400	±200	nA max	DB0–DB7 = 0V; $\overline{WR}$, $\overline{CS}$ = 0V; V_{REF} = ±10V
I_{OUT2} (Pin 2)	±50	±50	±400	±200	nA max	DB0–DB7 = V_{DD}; $\overline{WR}$, $\overline{CS}$ = 0V; V_{REF} = ±10V
DYNAMIC PERFORMANCE						
Propagation Delay[3] (From digital input to 90% of final analog output current)						
AD7524JN, KN, LN, AD, BD, CD	150	65	175	80	ns max	OUT1 Load = 100Ω, C_{EXT} = 13pF; $\overline{WR}$, $\overline{CS}$ = 0V; DB0–DB7 = 0V to V_{DD} or V_{DD} to 0V.
AD7524SD, TD, UD	150	65	200	90	ns max	
ac Feedthrough[3]						
at OUT1	0.25	0.25	0.5	0.5	% FSR max	V_{REF} = ±10V, 100kHz sine wave; DB0–DB7 = 0V; $\overline{WR}$, $\overline{CS}$ = 0V
at OUT2	0.25	0.25	0.5	0.5	% FSR max	
REFERENCE INPUT						
R_{IN} (pin 15 to GND)[4]	5	5	5	5	kΩ min	
	20	20	20	20	kΩ max	
ANALOG OUTPUTS						
Output Capacitance[3]						
C_{OUT1} (pin 1)	120	120	120	120	pF max	DB0–DB7 = V_{DD}; $\overline{WR}$, $\overline{CS}$ = 0V
C_{OUT2} (pin 2)	30	30	30	30	pF max	
C_{OUT1} (pin 1)	30	30	30	30	pF max	DB0–DB7 = 0V; $\overline{WR}$, $\overline{CS}$ = 0V
C_{OUT2} (pin 2)	120	120	120	120	pF max	
DIGITAL INPUTS						
Input HIGH Voltage Requirement V_{IH}	+2.4	+13.5	+2.4	+13.5	V min	
Input LOW Voltage Requirement V_{IL}	+0.8	+1.5	+0.8	+1.5	V max	
Input Current I_{IN}	±1	±1	±10	±10	μA max	V_{IN} = 0V or V_{DD}
Input Capacitance[3]						
DB0–DB7	5	5	5	5	pF max	V_{IN} = 0V
$\overline{WR}$, $\overline{CS}$	20	20	20	20	pF max	V_{IN} = 0V
SWITCHING CHARACTERISTICS						
Chip Select to Write Setup Time[5]						See timing diagram
t_{CS}						t_{WR} = t_{CS}
AD7524JN, KN, LN, AD, BD, CD	170	100	220	130	ns max	
AD7524SD, TD, UD	170	100	240	150	ns max	
Chip Select to Write Hold Time						
t_{CH}						
All Grades	0	0	0	0	ns min	
Write Pulse Width						
t_{WR}						$t_{CS} \geqslant t_{WR}$, $t_{CH} \geqslant 0$
AD7524JN, KN, LN, AD, BD, CD	170	100	220	130	ns min	
AD7524SD, TD, UD	170	100	240	150	ns min	
Data Setup Time						
t_{DS}						
AD7524JN, KN, LN, AD, BD, CD	135	60	170	80	ns min	
AD7524SD, TD, UD	135	60	170	100	ns min	
Data Hold Time						
t_{DH}						
All Grades	10	10	10	10	ns min	
POWER SUPPLY						
I_{DD}	1	2	2	2	mA max	All Digital Inputs V_{IL} or V_{IH}
	100	100	500	500	μA max	All Digital Inputs 0V or V_{DD}

NOTES:

[1] Temperature Ranges as follows: AD7524JN, KN, LN; 0 to +70°C
AD7524AD, BD, CD; −25°C to +85°C
AD7524SD, TD, UD; −55°C to +125°C

[2] Gain error is measured using internal feedback resistor. Ideal Full Scale Range (FSR) = (V_{REF} −1LSB) as shown in Table 1.

[3] Guaranteed, not tested.

[4] DAC thin film resistor temperature coefficient is approximately −300ppm/°C.

[5] AC parameter, sample tested @ 25°C to ensure conformance to specifications.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

V_{DD} to GND	–0.3V, +17V
V_{RFB} to GND	±25V
V_{REF} to GND	±25V
Digital Input Voltage to GND	–0.3V to V_{DD}
V_{OUT1}, V_{OUT2} (pin 1, pin 2) to GND	–0.3V to V_{DD}
Power Dissipation (package)	
Plastic (N Suffix)	
To +70°C	670mW
Derate above +70°C by	8.3mW/°C
Ceramic (D Suffix)	
To +75°C	450mW
Derate above +75°C by	6mW/°C
Operating Temperature	
Commerical (JN, KN, LN) Grades	0 to +70°C
Industrial (AD, BD, CD) Grades	–25°C to +85°C
Military (SD, TD, UD) Grades	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

CAUTION

1. ESD sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts.
2. Do not apply voltages lower than ground or higher than V_{DD} to any pin except V_{REF} (pin 15) and R_{FB} (pin 16).
3. Do not insert this device into powered sockets. Remove power before insertion or removal.

TERMINOLOGY

RELATIVE ACCURACY: A measure of the deviation from a straight line through the end points of the DAC transfer function. Normally expressed as a percentage of full scale range. For the AD7524 DAC, this holds true over the entire V_{REF} range.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of $(2^{-n})(V_{REF})$. A bipolar converter of n bits has a resolution of $[2^{-(n-1)}][V_{REF}]$. Resolution in no way implies linearity.

PROPAGATION DELAY: Time required for the output current to reach 90% of its final value from a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DAC's full scale output voltage to the ideal output voltage. Ideal full scale output is V_{REF} - 1LSB. Gain error is adjustable to zero.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from OUT1 and OUT2 terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on OUT1 terminal with all digital inputs LOW or on OUT2 terminal when all inputs are HIGH. This is an error current which contributes an offset voltage at the amplifier output.

CIRCUIT DESCRIPTION

CIRCUIT INFORMATION

The AD7524, an 8-bit multiplying D/A converter, consists of a highly stable thin film R-2R ladder and eight N-channel current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 1. An inverted R-2R ladder structure is used – that is, the binarily weighted currents are switched between the OUT1 and OUT2 bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

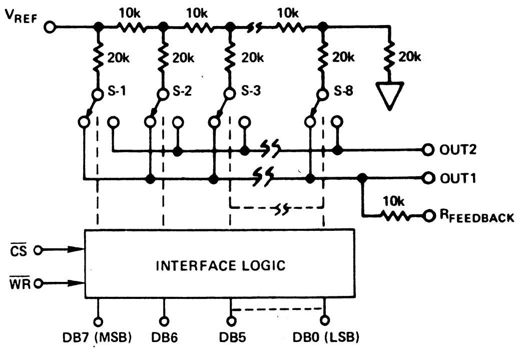


Figure 1. AD7524 Functional Diagram

EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuit for all digital inputs LOW is shown in Figures 2. In Figure 2 with all digital inputs LOW, the reference current is switched to OUT2. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate while the $\frac{I}{256}$ current source represents a constant 1-bit current drain through the termination resistor on the R-2R ladder. The "ON" capacitance of the output N-channel switches is 120pF, as shown on the OUT2 terminal. The "OFF" switch capacitance is 30pF, as shown on the OUT1 terminal. Analysis of the circuit for all digital inputs high is similar to Figure 2 however, the "ON" switches are now on terminal OUT1, hence the 120pF appears at that terminal.

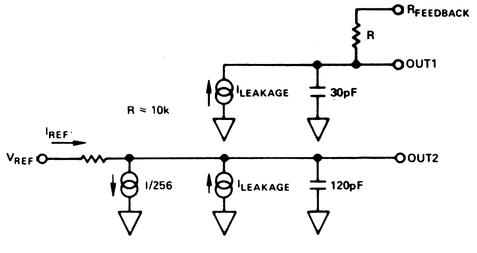


Figure 2. AD7524 DAC Equivalent Circuit – All Digital Inputs Low

INTERFACE LOGIC INFORMATION

MODE SELECTION

AD7524 mode selection is controlled by the $\overline{CS}$ and $\overline{WR}$ inputs.

WRITE MODE

When $\overline{CS}$ and $\overline{WR}$ are both LOW, the AD7524 is in the WRITE mode, and the AD7524 analog output responds to data activity at the DB0–DB7 data bus inputs. In this mode, the AD7524 acts like a nonlatched input D/A converter.

HOLD MODE

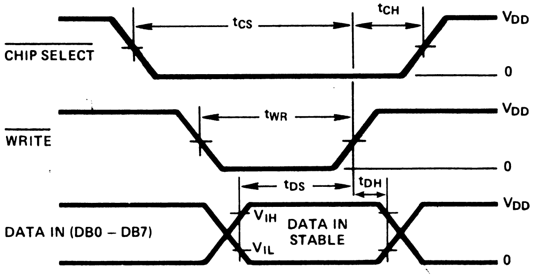
When either $\overline{CS}$ or $\overline{WR}$ is HIGH, the AD7524 is in the HOLD mode. The AD7524 analog output holds the value corresponding to the last digital input present at DB0–DB7 prior to $\overline{WR}$ or $\overline{CS}$ assuming the HIGH state.

MODE SELECTION TABLE

$\overline{CS}$	$\overline{WR}$	MODE	DAC RESPONSE
L	L	Write	DAC responds to data bus (DB0 – DB7) inputs
H	X	Hold	Data bus (DB0 – DB7) is locked out;
X	H	Hold	DAC holds last data present when $\overline{WR}$ or $\overline{CS}$ assumed HIGH state.

L = Low State, H = High State, X = Don't Care.

WRITE CYCLE TIMING DIAGRAM



NOTES:

1. All input signal rise and fall times measured from 10% to 90% of V_{DD}. V_{DD} = +5V, $t_r = t_f$ = 20ns; V_{DD} = +15V, $t_r = t_f$ = 40ns.
2. Timing Measurement Reference level is $\frac{V_{IH} + V_{IL}}{2}$
3. $t_{DS} + t_{DH}$ is approximately constant at 145ns min at +25°C, V_{DD} = +5V and t_{wr} = 170ns min. The AD7524 is specified for a minimum t_{DH} of 10ns, however, in applications where $t_{DH} > 10$ns, t_{DS} may be reduced accordingly up to the limit t_{DS} = 65ns, t_{DH} = 80ns.

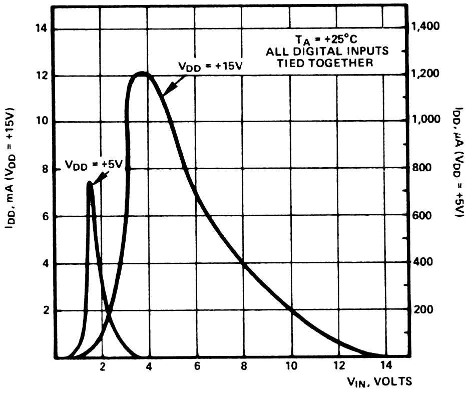
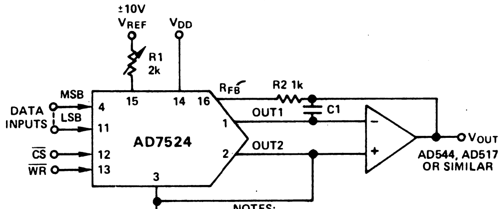


Figure 3. Supply Current vs. Logic Level

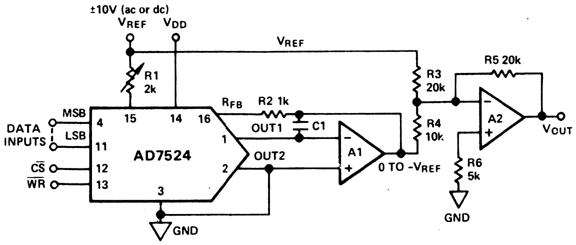
Typical plots of supply current, I_{DD}, versus logic input voltage, V_{IN}, for V_{DD} = +5V and V_{DD} = +15V are shown above.

ANALOG CIRCUIT CONNECTIONS



NOTES:
1. R1 AND R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
2. C1 PHASE COMPENSATION (10pF-15pF) IS REQUIRED WHEN USING HIGH SPEED AMPLIFIERS TO PREVENT RINGING OR OSCILLATION.

Figure 4. Unipolar Binary Operation (2-Quadrant Multiplication)



NOTES:
1. ADJUST R1 FOR V_{OUT} = 0V AT CODE 10000000.
2. C1 PHASE COMPENSATION (10 - 15pF) MAY BE REQUIRED IF A1 IS A HIGH SPEED AMPLIFIER.

Figure 5. Bipolar (4-Quadrant) Operation

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
11111111	$-V_{REF}\left(\frac{255}{256}\right)$
10000001	$-V_{REF}\left(\frac{129}{256}\right)$
10000000	$-V_{REF}\left(\frac{128}{256}\right) = -\frac{V_{REF}}{2}$
01111111	$-V_{REF}\left(\frac{127}{256}\right)$
00000001	$-V_{REF}\left(\frac{1}{256}\right)$
00000000	$-V_{REF}\left(\frac{0}{256}\right) = 0$

Note: $1\text{LSB} = (2^{-8})(V_{REF}) = \frac{1}{256}(V_{REF})$

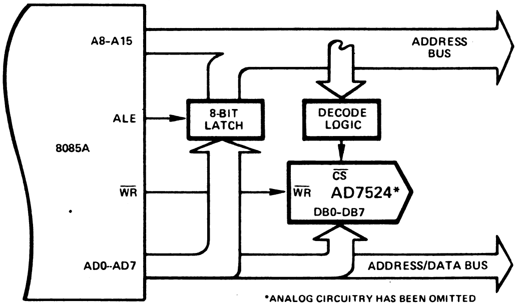
Table 1. Unipolar Binary Code Table

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
11111111	$+V_{REF}\left(\frac{127}{128}\right)$
10000001	$+V_{REF}\left(\frac{1}{128}\right)$
10000000	0
01111111	$-V_{REF}\left(\frac{1}{128}\right)$
00000001	$-V_{REF}\left(\frac{127}{128}\right)$
00000000	$-V_{REF}\left(\frac{128}{128}\right)$

Note: $1\text{LSB} = (2^{-7})(V_{REF}) = \frac{1}{128}(V_{REF})$

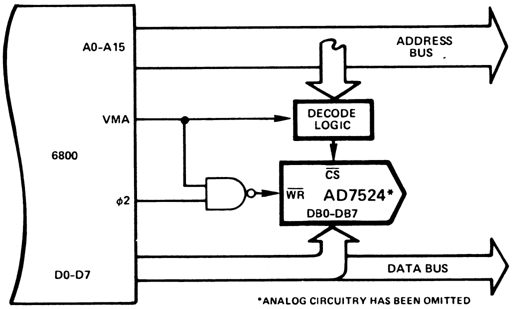
Table 2. Bipolar (Offset Binary) Code Table

MICROPROCESSOR INTERFACE



*ANALOG CIRCUITRY HAS BEEN OMITTED FOR CLARITY.

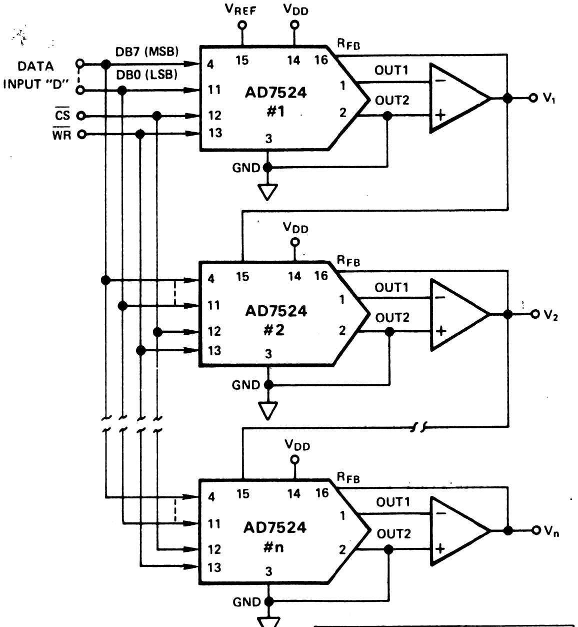
Figure 6. AD7524/8085A Interface



*ANALOG CIRCUITRY HAS BEEN OMITTED FOR CLARITY.

Figure 7. AD7524/MC6800 Interface

POWER GENERATION



CIRCUIT EQUATIONS

$V_1 = -(V_{REF})(D)$

$V_2 = +(V_{REF})(D^2)$

$V_n = -(V_{REF})(D^n)$, n an odd integer

$V_n = +(V_{REF})(D^n)$, n an even integer

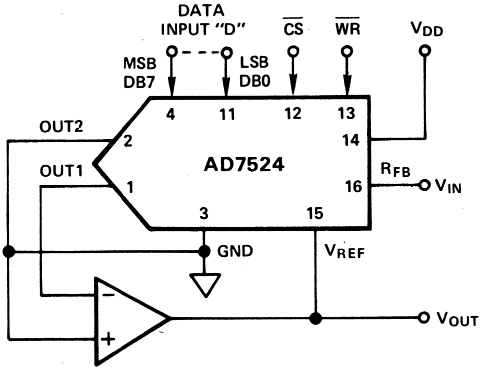
WHERE:

$$D = \frac{DB7}{2^1} + \frac{DB6}{2^2} + \ldots \frac{DB0}{2^8}$$

and

$DB_n = 1$ or 0

DIVIDER (DIGITALLY CONTROLLED GAIN)



EQUATIONS

$$V_{OUT} = \frac{-V_{IN}}{D}$$

$$A_V = \frac{-V_{OUT}}{V_{IN}} = -\frac{1}{D}$$ WHERE: A_V = VOLTAGE GAIN

and where:

$$D = \frac{DB7}{2^1} + \frac{DB6}{2^2} + \ldots \frac{DB0}{2^8}$$

$DB_N = 1$ or 0

EXAMPLES

D = 00000000, $A_V = -A_{OL}$ (OP AMP)

D = 00000001, $A_V = -256$

D = 10000000, $A_V = -\frac{256}{128} = -2$

D = 11111111, $A_V = -\frac{256}{255}$

ANALOG DEVICES

3½ Digit BCD Monolithic CMOS Digitally Controlled Potentiometer

AD7525

FEATURES

- **Resolution: 3 1/2 Digit BCD (1999 Counts)**
- **Nonlinearity: ±1/2LSB T_{min} to T_{max}**
- **Gain Error: ±0.05% FS**
- **Excellent Repeatability Accuracy**
- **Low Power Dissipation**

APPLICATIONS

- **Thumbwheel Switch Voltage Dividers**
- **Digitally Controlled Gain Circuits**
- **Digitally Controlled Attenuators**
- **BCD Multiplying DACs**
- **Low Power Converters**

GENERAL DESCRIPTION

The AD7525 is a monolithic CMOS 3½ digit BCD digitally controlled potentiometer designed for precision incremental voltage-divider applications.

With the addition of an external op amp, the output can be digitally controlled from 0 to 1.999V_{IN} with resolution of 0.001V_{IN}.

AC or DC voltage up to ±10V can be applied to the input providing high application flexibility in fields such as audio gain control, etc.

Digital control, excellent repeatability and 0.05% accuracy make the AD7525 an ideal replacement for 10-turn potentiometers or thumbwheel switch voltage dividers using discrete resistor networks.

Packaged in an 18-pin DIP, the AD7525 uses an advanced CMOS fabrication process combined with wafer laser trimming.

ORDERING INFORMATION

Package[1] and Temperature	Nonlinearity ±1/2LSB	Nonlinearity ±1LSB
18-Pin Plastic (N18B) 0 to +70°C	AD7525LN	AD7525KN
18-Pin Ceramic (D18B) -25°C to +85°C	AD7525CD AD7525CD/883B[2]	AD7525BD AD7525BD/883B[2]
18-Pin Ceramic (D18B) -55°C to +125°C	AD7525UD AD7525UD/883B[2]	AD7525TD AD7525TD/883B[2]

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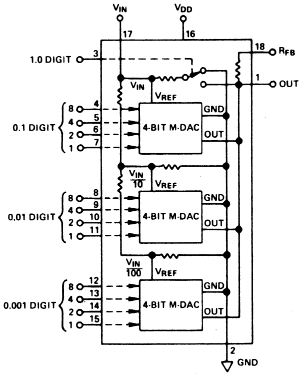
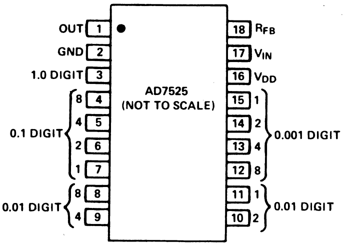
[1] See Section 20 for package outline information.

[2] 100% screened to MIL-STD-883, method 5004, para. 3.1.1 through 3.1.12 for class B device.

AD7525 FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



18-PIN DIP
TOP VIEW

SPECIFICATIONS (V_{DD}=+15V; V_{PIN1} = 0V; V_{IN} = +10V unless otherwise stated)

PARAMETER	T_A = +25°C	T_A = Operating Temperature Range	CONDITION
ACCURACY			
Resolution[1]	1 part in 2000	1 part in 2000	
Nonlinearity[2, 3]			
AD7525KN, BD, TD	±1LSB max	±1LSB max	BCD 0.000 to 1.999
AD7525LN, CD, UD	±1/2LSB max	±1/2LSB max	BCD 0.000 to 1.999
Gain Error[3, 4]	±0.05% FS typ	–	BCD = 1.999
Gain TC	±25ppm/°C max	–	BCD = 1.999
Output Leakage Current (pin 1)	100nA max	400nA max	BCD = 0.0000
DYNAMIC PERFORMANCE			
Switching Time	1μs max[5]	1μs max[6]	V_{IN} = +5V, R_{OUT} (pin 1) = 100Ω, Digital Inputs = V_{IL} to V_{IH} or V_{IL}, V_{PIN1} measured from 10% to 90%
Feedthrough Error	±0.05%V_{IN} max[6]	±0.1%V_{IN} max[6]	V_{IN} = ±10V, 20kHz sinewave
ANALOG INPUT			
Input Resistance (pin 17)[7]	2kΩ min/10kΩ max	2kΩ min/10kΩ max	
V_{IN} Range (recommended)	±10V max	±10V max	
ANALOG OUTPUT			
Output Capacitance			
C_{OUT} (pin 1)	60pF max[6]	60pF max[6]	Digital Inputs = BCD 0000
	200pF max[6]	200pF max[6]	Digital Inputs = BCD 1999
R_{FB} Resistance (pin 18 to pin 1)[7]	8kΩ min/40kΩ max	8kΩ min/40kΩ max	
DIGITIAL INPUTS			
Input HIGH Voltage			
V_{IH}[3]	+14.5V min	+14.5V min	
Input LOW Voltage			
V_{IL}[3]	+0.5V max	+0.5V max	
Input Leakage Current	±1μA max	±10μA max	Digital Input = 0V or V_{DD}
Input Capacitance	5pF max[6]	5pF max[6]	
Input Coding	3½ Digit BCD (1999 Counts)	3½ Digit BCD (1999 Counts)	
POWER SUPPLY			
V_{DD} Range	+5V to +17V	+5V to +17V	Functional with Degraded Performance
V_{DD}	+15V ±5%	+15V ±5%	Rated Accuracy
I_{DD}[3]	500μA max	1mA max	Digital Inputs = V_{IL} or V_{IH}

NOTES:

[1] Commercial devices are sample tested over temperature.

[2] Monotonicity is guaranteed on the AD7525LN, CD and UD versions over T_{min} to T_{max}.

[3] Final electrical tests on 883B screen parts are: Gain Error, Nonlinearity, V_{IH}, V_{IL}, Digital Input Leakage Current and I_{DD} at +25°C and +125°C (TD/883B Version) or +25°C and +85°C (BD/883B Version).

[4] Gain Error is measured using the AD7525 internal feedback resistor. FS is "Full Scale" (BCD = 1.999).

[5] AC parameter, sample tested at +25°C to ensure conformance to specification.

[6] Guaranteed, not tested.

[7] Thin Film resistor temperature coefficient is approximately –300ppm/°C.

Specifications subject to change without notice.

CAUTION

1. ESD (electro-static discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.
2. Do not apply voltages more negative than GND or more positive than V_{DD} to any pin except V_{IN} (pin 17) and R_{FB} (pin 18).
3. The inputs of some IC amplifiers (especially high speed types) present a low impedance to V− during power sequencing. To prevent the AD7525 OUT terminal (pin 1) from exceeding −300mV (which causes catastrophic substrate current), a Schottky diode, HSCH 1001 or equivalent, is recommended. While not required for most amplifier types, provision for the diode should be made during layout. The diode should be connected between OUT (pin 1) and GND (pin 2) as shown in Figure 4. Protection Schottkys not required when using TRI-FET output amplifiers such as the AD542 or AD544.

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

V_{DD} (to GND)	−0.3V, +17V
V_{IN} (to GND)	±25V
R_{FB} (to GND)	±25V
Digital Input Voltage (to GND)	−0.3V to V_{DD}
V_{PIN1} (to GND)	−0.3V to V_{DD}
Power Dissipation (Package)	
Plastic (Suffix N)	
To +70°C	670mW
Derates above +70°C by	8.3mW/°C
Ceramic (Suffix D)	
To +75°C	450mW
Derates above +75°C by	6mW/°C
Operating Temperature	
Commercial Plastic (KN, LN Versions)	0 to +70°C
Industrial Ceramic (BD, CD Versions)	−25°C to +85°C
Military Ceramic (TD, UD Versions)	−55°C to +125°C

TERMINOLOGY

SWITCHING TIME: In a D/A converter, the switching time is the time taken for an analog switch to change to a new state from the previous one. It includes delay time, and rise time from 10% to 90%, but does not include settling time, which is a function of the output amplifier used.

OUTPUT CAPACITANCE: Capacitance from OUT terminal (pin 1) to ground.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{IN} (pin 17) to OUT (pin 1) with all digital inputs LOW.

PRINCIPLES OF OPERATION

CIRCUIT DESCRIPTION

The AD7525, a 3½ digit BCD multiplying DAC, consists of a thin-film R/2R ladder, interquad voltage dividers and 13 N-channel MOS SPDT current steering switches. Most applications require the addition of only an external operational amplifier.

Referring to Figure 1, the "1.0 Digit" is a 1-bit multiplying DAC (composed of SW_1 and R_1) while the 0.1, 0.01, and 0.001 digits are 4-bit multiplying DAC's (DAC1, DAC2, and DAC3) connected by 10:1 dividers (composed of R_{IN2}, R_2, R_3 and R_{IN3}, R_4, R_5.

DAC1 is expanded to show the R/2R ladder and switch network. With input voltage V_{IN}, the currents in each shunt arm are (starting at the left) $V_{IN}/2R$, $V_{IN}/4R$, $V_{IN}/8R$ and $V_{IN}/16R$. A logic ONE applied to a digital input steers that shunt arm's current to OUT, while a logic ZERO steers the current to GND.

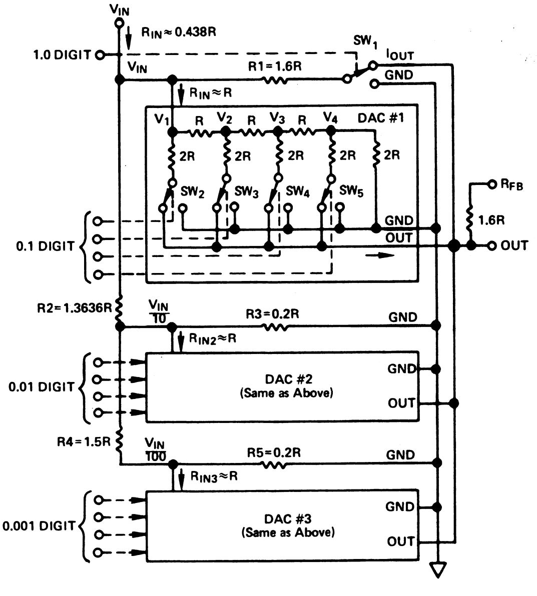


Figure 1. AD7525 Circuit Diagram

EQUIVALENT CIRCUIT

As shown in Figure 2, the AD7525 is a digitally controlled π-network attenuator with signal input "V_{IN}" (pin 17), signal output "OUT" (pin 1), signal common "GND" (pin 2) and digital control "BCD input" (pins 3–15).

With OUT (pin 1) terminated at op amp virtual ground and R_{FB} (pin 18) connected to the op amp output, the nominal transfer equation is:

$$V_{OUT} = -V_{IN}\ \mathrm{BCD}$$
$$\text{where } 0.000 \leqslant \mathrm{BCD} \leqslant 1.999$$

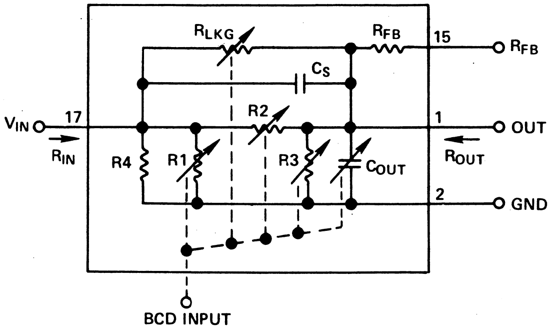


Figure 2. Functional Equivalent Circuit

OUTPUT AMPLIFIER CONSIDERATIONS

Amplifier Offset

The output resistance at OUT (pin 1) is code dependent, varying between ∞ to 0.35 R_{LDR}. For a fixed feedback resistor of value 1.6 R_{LDR} (Figure 3), the output error for a fixed amplifier offset (V_{OS}) is:

$$V_{ERROR} = \left(1 + \frac{R_{FB}}{R_{OUT}}\right) V_{OS}$$

Case 1: $(R_{OUT} = \infty)$

$$V_{ERROR} = \left(1 + \frac{R_{FB}}{\infty}\right) V_{OS}$$

$$V_{ERROR} = V_{OS}$$

Case 2: $(R_{OUT} = 0.35\ R_{LDR})$

$$V_{ERROR} = \left(1 + \frac{1.6\ R_{LDR}}{0.35 R_{LDR}}\right) V_{OS}$$

$$V_{ERROR} = (1 + 4.6)V_{OS} = 5.6\ V_{OS}$$

Cases 1 and 2 show that amplifier offset in conjunction with a changing output resistance at OUT (pin 1) create nonlinearity error, in addition to a simple offset term.

It is therefore recommended that amplifier initial offset be adjusted to less than 100μV (as measured between the amplifier input terminals). The offset voltage over the temperature range of interest should not exceed 250μV. See application hint #2, below.

Do not include the usual bias current compensation resistor in the amplifier noninverting terminal. Instead, the amplifier should have a bias current which is low over the temperature range of interest. Bias current causes "output offset" of magnitude $(I_B)R_{FB}$.

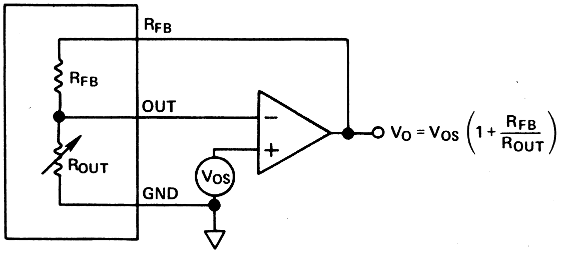


Figure 3. Noise Gain Equivalent Circuit

High Frequency Amplifiers

R_{FB} and C_{OUT} create a phase lag in the output amplifier's feedback circuit. This phase lag, in conjunction with the amplifier's phase lag, may cause ringing or oscillation. When using a high speed amplifier, shunting the amplifier input to output with 5–20pF of feedback capacitance ensures stability.

APPLICATION HINTS

1. If an output voltage range of ±19.99 volts is required (i.e., AD7525 V_{IN} = ±10V, BCD = 1.999), a high voltage output amplifier with appropriate supply voltages must be used.
2. To maintain circuit linearity, the op amp offset voltage should not exceed 2% of the circuit resolution. (Resolution = $V_{IN} \div 1000$)
3. CMOS logic inputs exhibit an input impedance on the order of 100MΩ. Unused CMOS inputs must always be tied to a known logic state. If single-pole single-throw thumbwheel switches are used to drive the digital inputs of the AD7525, external 10kΩ pull-down (pull-up if switch coding is complementary (BCD) resistors must be used.

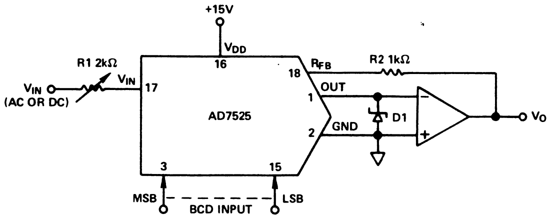


Figure 4. Digitally Controlled Attenuator Circuit

BCD INPUT					ANALOG OUTPUT	
Digital Input				Equivalent Decimal Input	V_O/V_{IN}	V_O
1.0	0.1	0.01	0.001			
1	1001	1001	1001	1.999	-1.999	$-1.999V_{IN}$
1	0000	0000	0001	1.001	-1.001	$-1.001V_{IN}$
1	0000	0000	0000	1.000	-1.000	$-1.000V_{IN}$
0	1001	1001	1001	0.999	-0.999	$-0.999V_{IN}$
0	0101	0000	0000	0.500	-0.500	$-0.500V_{IN}$
0	0000	0000	0000	0.000	0	0

Note 1:
For proper BCD coding, the 0.1 digit, 0.01 digit or 0.001 digit must not exceed BCD "9" (1001).

Table 1. Analog Input/Output Relationship vs. Digital Input

CALIBRATION PROCEDURE

Offset Adjustment:

1. Apply BCD code 0.000 (0 0000 0000 0000) to the AD7525 digital inputs.
2. Connect a high resolution, high impedance voltmeter between pins 1 and 2 of the AD7525.
3. Adjust amplifier's trimpot for minimum reading on the voltmeter (<100μV).

Gain Adjustment:

1. Apply BCD code 1.000 (1 0000 0000 0000) to the AD7525 digital input.
2. Apply +10V to the V_{IN} input of Figure 1.
3. Connect the voltmeter between V_O (amplifier output) and pin 2 of the AD7525.
4. Adjust R_1 until $V_O = -10V$.

APPLICATION – THUMBWHEEL SWITCH ATTENUATOR

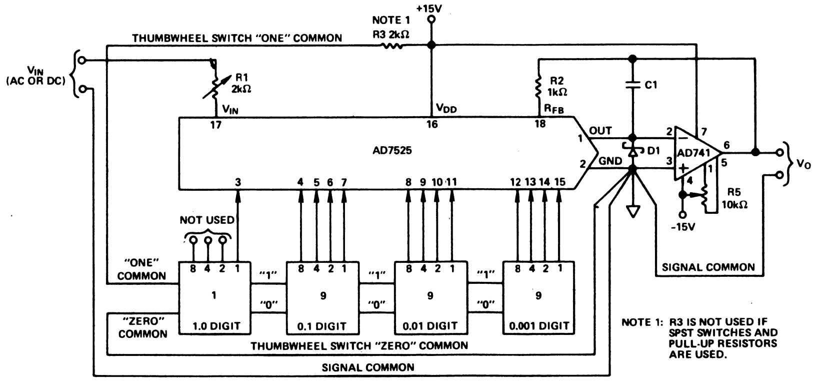


Figure 5. Thumbwheel Switch Attenuator

The circuit shown in Figure 5 is a precision voltage divider similar to 10-turn pots and thumbwheel switch incremental-voltage-divider assemblies. Advantages of the circuit are:

☐ Economy
☐ Low Output Impedance
☐ Resolution 0.1% V_{IN}
☐ Excellent Repeatability Accuracy
☐ Overrange Capability

The BCD coded thumbwheel assembly applies BCD data to the AD7525 digital inputs. The switch assembly shown has single-pole-double-throw action, thus the BCD inputs are pulled either to +15V or GND (available from AMP, Harrisburg, PA; CHERRY, Waukegan, Illinois; or SAE, Santa Clara, California). Resistor R_3 limits current if make-before-break switches are used. SPST switch assemblies can be used; however, appropriate pull-up or pull-down resistors must be used on each digital input, depending upon whether the switch coding is BCD or complementary BCD. This ensures each digital input has appropriate V_{IH} or V_{IL} levels applied.

Resistors R_1 and R_2 provide gain adjustment capability. R_5 is used to adjust the amplifier offset voltage (as measured between the amplifier input terminals) to less than 100μV. Diode D_1 (HSCH 1001) provides AD7525 output protection (see Caution note 3).

ANALOG DEVICES

CMOS 10-Bit (Systems) DAC

AD7527

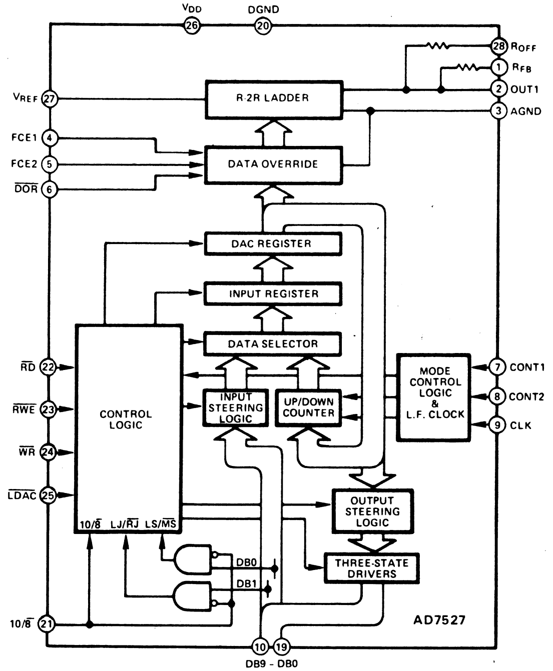
FEATURES

- Double Buffer Latches/Counter
- Data Readback
- 8- and 16-Bit Bus Compatible
- ±1LSB max Gain Error ("G" version)
- Easy Calibration Features
- Latch Proof (No Schottky Protection Required)

TYPICAL APPLICATIONS

- 4-20mA Loop Control
- Tracking ADCs
- S/D Converters
- Intelligent Instruments
- A.T.E.

AD7527 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7527 is a 10-bit monolithic CMOS systems DAC with extensive pin programmable logic functions. It interfaces directly with 8- or 16-bit data busses. The contents of the internal register can be written into and read from in left or right hand justified format.

The internal register data can be incremented or decremented using three control pins. The device includes an on-chip oscillator which may be used for incrementing or decrementing: alternatively an external clock can be used. System initialization and calibration is facilitated by a data override function which forces the DAC logic inputs to one of three override values for a zero, half or full scale output.

Two equal and matched feedback resistors are included on the die to facilitate 4-20mA circuits and other applications requiring matched resistors. The device has a low gain temperature coefficient of typically 2ppm/°C with a maximum of 5ppm/°C.

ORDERING INFORMATION

Relative Accuracy T_{min} to T_{max}	Gain Error +25°C	Temperature Range and Package		
		0 to +70°C	-25°C to +85°C	-55°C to +125°C
±1LSB	±10LSB	AD7527KN	AD7527BD	AD7527TD
±1/2LSB	±5LSB	AD7527LN	AD7527CD	AD7527UD
±1/2LSB	±1LSB	AD7527GLN	AD7527GCD	AD7527GUD

Analog Devices is offering the AD7527 in chip carriers.
For information contact the factory.

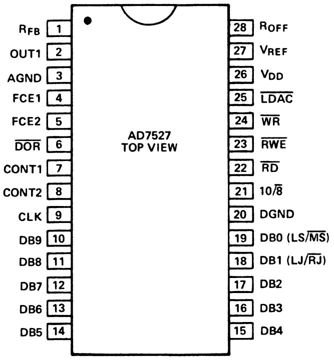
PACKAGE IDENTIFICATION[1]

Suffix D: Ceramic DIP – (D28B)
Suffix N: Plastic DIP – (N28A)

[1] See Section 20 for package outline information.

Ceramic parts are available screened to MIL-STD-883, Method 5004 Para. 3.1.1 through 3.612 for a Class B device. To order add /883B to part number.

28-PIN DIP PIN CONFIGURATION (NOT TO SCALE)



SPECIFICATIONS (V_{DD} = +5V, V_{REF} = +10V, V_{OUT1} = 0V unless otherwise noted)

Parameter	Limit[1] at T_A = +25°C	Limit[1] at 0, +70°C and -25°C, +85°C	Limit[1] at -55°C, +125°C	Units	Conditions/Comments
STATIC PERFORMANCE					
Resolution	10	10	10	Bits	
Relative Accuracy[2]					
AD7527KN, BD, TD	±1	±1	±1	LSB max	
AD7527LN, CD, UD	±0.5	±0.5	±0.5	LSB max	
AD7527GLN, GCD, GUD	±0.5	±0.5	±0.5	LSB max	
Differential Nonlinearity[2]					
AD7527KN, BD, TD	±2	±2	±2	LSB max	Guaranteed 9-Bit Monotonic, T_{min} to T_{max}
AD7527LN, CD, UD	±1	±1	±1	LSB max	Guaranteed 10-Bit Monotonic, T_{min} to T_{max}
AD7527GLN, GCD, GUD	±1	±1	±1	LSB max	Guaranteed 10-Bit Monotonic, T_{min} to T_{max}
Gain Error[2]					
AD7527KN, BD, TD	±10	±10	±10	LSB max	Using internal R_{FB} only. Gain Error can
AD7527LN, CD, UD	±5	±5	±5	LSB max	be trimmed to zero using circuits of
AD7527GLN, GCD, GUD	±1	±1	±2	LSB max	Figures 11, 12 and 13.
R_{FB} to R_{OFF} Resistance Match	±0.2	±0.2	±0.2	% max	
Average Gain Temperature Coefficient, $\Delta G/\Delta T$					
T_{min} to +25°C	–	5	5	ppm/°C max	
+25°C to T_{max}	–	5	5	ppm/°C max	
dc Supply Rejection[2]					
$\Delta Gain/\Delta V_{DD}$	0.005	0.005	0.005	% per % max	V_{DD} = +4.75V to +5.25V
Output Leakage Current[2]					
OUT1 (pin 2)	10	10	200	nA max	DAC Register Loaded with All 0s.
DYNAMIC PERFORMANCE					
DAC Register Propagation Delay[2,3]	950	950	950	ns max	OUT1 Load = 100Ω‖13pF Measured from Leading Edge of $\overline{WR}$ to 90% of Final Output Current for Full Scale Change.
Digital Charge Injection[2,3]	300	300	300	nV sec typ	Measured with ADLH0032CG as Output Amplifier. C1 of Figure 11 is 33pF. Pin 28 to AGND.
Multiplying Feedthrough Error[2,3]	2	2	4	mV p-p max	V_{REF} = ±10V, 10kHz Sine Wave. (See Application Hint Number 4). Pin 28 to AGND.
Small Signal Bandwidth	100	100	100	kHz typ	Using Circuit of Figure 11.
Input Resistance at					
V_{REF}, R_{FB}, R_{OFF}	7	7	7	kΩ min	Typical Input Resistance is 13kΩ.
(pins 27, 1, 28 Respectively)	20	20	20	kΩ max	
Input Resistance Temperature Coefficient	-300	-300	-300	ppm/°C typ	
Analog Output Capacitance					
C_{OUT1} (pin 2)[3]	230	230	230	pF max	DAC Register Loaded with 1111111111
C_{OUT1} (pin 2)[3]	75	75	75	pF max	DAC Register Loaded with 0000000000
DIGITAL CONTROL INPUTS					
Input HIGH Voltage, V_{IH}	3.0	3.0	3.0	V min	Excluding CLK (pin 9) and DATA Bus (pins 10–19)
Input LOW Voltage, V_{IL}	0.8	0.8	0.8	V max	
Input Leakage Current, I_{IN}[4]	1	1	1	µA max	V_{IN} = 0V or V_{DD}
Input Capacitance, C_{IN}[3]	8	8	8	pF max	
CLOCK INPUT (PIN 9)					
Input HIGH Voltage, V_{IH}	3.8	3.8	3.8	V min	Input is a Schmitt Trigger.
Input LOW Voltage, V_{IL}	0.5	0.5	0.5	V max	
Input HIGH Current, I_{IH}	1.5	1.5	1.5	mA max	V_{IN} = +5V
Input LOW Current, I_{IL}	±1	±1	±1	µA max	V_{IN} = 0V
DATA BUS (PINS 10–19)					
Input HIGH Voltage, V_{IH}	3.0	3.0	3.0	V min	
Input LOW Voltage, V_{IL}	0.8	0.8	0.8	V max	
Output HIGH Voltage, V_{OH}	4.0	4.0	4.0	V min	I_{SOURCE} = 40µA
Output LOW Voltage, V_{OL}	0.4	0.4	0.4	V max	I_{SINK} = 1.6mA
Leakage Current per pin	±1	±10	±10	µA max	Outputs in high impedance state.
Capacitance per pin[3]	10	10	10	pF max	Outputs in high impedance state.
POWER REQUIREMENTS					
V_{DD}	+5	+5	+5	V	
I_{DD}	5	5	5	mA max	V_{IN} = V_{IL} or V_{IH}; Data bus in high impedance state.
	500	500	500	µA max	V_{IN} = 0 or V_{DD}; Data bus in high impedance state.

NOTES:

[1] Temperature Ranges as follows: KN, LN, GLN versions, 0 to +70°C
BD, CD, GCD versions, -25°C to +85°C
TD, UD, GUD versions, -55°C to +125°C

[2] See Terminology

[3] Guaranteed but not tested.

[4] Logic inputs are MOS gates. Typical input current at +25°C is less than 1nA.

[5] Sample tested at +25°C to ensure compliance.

[6] For write timing, data bus reference levels are 0.8V (V_{IL}) and 3.0V (V_{IH}), see Figure 3. For read timing, data bus reference levels are 0.4V (V_{OL}) and 2.4V (V_{OH}), measured with a 10kΩ pull-down resistor.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[5] (V_{DD} = +5V, V_{REF} = +10V, V_{OUT1} = 0V unless otherwise noted)

Parameter	Limit[1] at T_A = +25°C	Limit[1] at 0, +70°C and -25°C, +85°C	Limit[1] at -55°C, +125°C	Units	Conditions/Comments
DATA WRITE[6]					
t_{DS}	300	360	450	ns min	Data valid setup time for 10-bit bus mode & 8-bit bus mode, right justified data.
t_{DS}	425	520	570	ns min	Data valid setup time for 8-bit bus mode, left justified data.
t_{DH}	0	0	0	ns min	Data valid hold time.
t_{WS}	240	275	325	ns min	Write control setup time.
t_{WH}	0	0	0	ns min	Write control hold time.
t_{WP}	180	220	250	ns min	Write pulse width.
DATA READ[6]					
t_{RS}	0	0	0	ns min	Read control setup time.
t_{RH}	0	0	0	ns min	Read control hold time.
t_{RP}	175	240	265	ns min	Read pulse width, C_L = 20pF
	300	400	450	ns min	C_L = 100pF
t_{RAD}	175	240	265	ns min	Data access time, C_L = 20pF
	300	400	450	ns min	C_L = 100pF
t_{RHD}	50	70	100	ns min	Data hold time.
	120	140	150	ns max	

See notes on Specifications page

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to DGND	0, +7V
V_{DD} to AGND	0, +7V
AGND to DGND	0, V_{DD}
DGND to AGND	0, V_{DD}
Digital Input Voltage to DGND (pins 4-9, 21-25)	-0.3V, +17V
Digital Bus Voltage to DGND (pins 10-19)	-0.3V, V_{DD} +0.3V
V_{PIN2} to AGND	-0.3V, +17V
V_{PIN1}, V_{PIN27}, V_{PIN28} to AGND	±25V
Operating Temperature Range	
KN, LN, GLN	0 to +70°C
BD, CD, GCD	-25°C to +85°C
TD, UD, GUD	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 secs)	+300°C
Power Dissipation (Package)	
Plastic (Suffix N)	
To +50°C	1200mW
Derate above +50°C by	12mW/°C
Ceramic (Suffix D)	
To +50°C	1000mW
Derate above +50°C by	10mW/°C

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION:

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

WARNING!

ESD SENSITIVE DEVICE

PIN FUNCTION DESCRIPTION

PIN	MNEMONIC	DESCRIPTION
1	RFB	Feedback Resistor. Used for normal unity gain (at full scale) D/A conversion.
2	OUT1	DAC Current OUT1 Bus. Normally terminated at virtual ground of output amplifier.
3	AGND	Analog Ground.
4	FCE1	Force 1 Input. See pin 6 description.
5	FCE2	Force 2 Input. See pin 6 description.
6	$\overline{\text{DOR}}$	Data Override Input. This function allows the user to force the DAC logic inputs to one of three override values for calibration and reset. The value which the DAC output assumes is determined by the logic levels on the Forcing inputs, FCE1 and FCE2.

$\overline{\text{DOR}}$	FCE2	FCE1	DAC INPUT
1	X	X	DAC Register Contents
0	0	0	0000000000
0	0	1	1000000000
0	1	X	1111111111

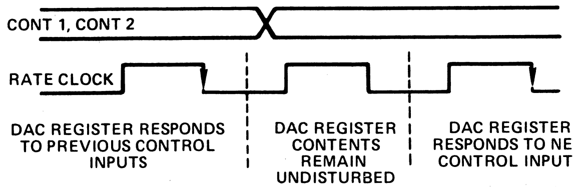
X = Don't Care

Data in the input and DAC registers are not affected in any way by the data override. They may be written to or read from as in normal operation. When the override signal is removed the DAC output returns to reflect the value in the DAC register.

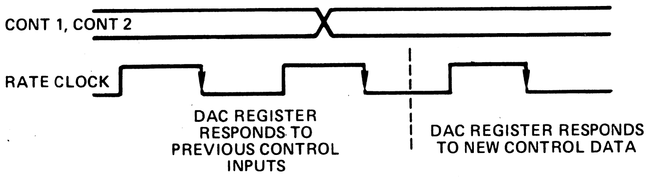
PIN	MNEMONIC	DESCRIPTION
7	CONT1	Control Input 1. See pin 8 description.
8	CONT2	Control Input 2. This signal, in combination with CONT1 (pin 7) is used to determine the AD7527 operating mode, either *load* or *count* mode. In the *load* mode all AD7527 data WRITE, READ and LOAD operations are via the data bus and control inputs. In the *count* mode external data on the data bus cannot be written into the AD7527, the $\overline{\text{WR}}$ and $\overline{\text{LDAC}}$ signals are ignored; however, the contents of the DAC register can still be read. In this mode the input and DAC registers are driven as an internal up/down counter. The up/down counter operation is controlled by the CONT1, CONT2 signals. CONT1, CONT2 encoding is as follows:

CONT1	CONT2	MODE	FUNCTION
0	0	*Load*	Control is via data bus and control inputs
0	1	*Count*	Increment input and DAC Registers
1	0	*Count*	Decrement input and DAC Registers
1	1	*Count*	Input and DAC Register contents frozen

End stop logic prevents the up/down counter from being incremented beyond all 1s or decremented below all 0s. The increment/decrement rate is controlled by the rate frequency on the CLK input (pin 9). The response of the AD7527 to a change in the control inputs depends on the state of the rate clock (HIGH or LOW) at the time the change occurs.


CONT 1, CONT 2
RATE CLOCK
DAC REGISTER RESPONDS TO PREVIOUS CONTROL INPUTS
DAC REGISTER CONTENTS REMAIN UNDISTURBED
DAC REGISTER RESPONDS TO NEW CONTROL INPUTS

Case 1. Rate Clock LOW When Controls Change


CONT 1, CONT 2
RATE CLOCK
DAC REGISTER RESPONDS TO PREVIOUS CONTROL INPUTS
DAC REGISTER RESPONDS TO NEW CONTROL DATA

Case 2. Rate Clock HIGH When Controls Change

A status flag is available via the data bus to indicate whether the AD7527 is in the *load* mode (flag HIGH) or *count* mode (flag LOW).

PIN	MNEMONIC	DESCRIPTION
9	CLK	Clock Input. Controls the input and DAC registers increment/decrement rate when the AD7527 is in the *count* mode. Connecting an external resistor to V_{DD} and capacitor to ground completes an internal low frequency clock circuit, see Figure 4. Alternatively CLK may be driven by an external clock frequency of up to 1MHz.
10	DB9	Data Bit 9. Most Significant Bit (MSB).
11	DB8	Data Bit 8.
12	DB7	Data Bit 7.
13	DB6	Data Bit 6.
14	DB5	Data Bit 5.
15	DB4	Data Bit 4.
16	DB3	Data Bit 3.
17	DB2	Data Bit 2.

18	DB1 (LJ/$\overline{RJ}$)	Pin function is dependent upon the $10/\overline{8}$ (pin 21) input. Pin 21 HIGH; pin 18 is Data Bit 1 (DB1) input. Pin 21 LOW; pin 18 is left-justified/right-justified (LJ/RJ) control input.
19	DB0 (LS/$\overline{MS}$)	Pin function is dependent upon the $10/\overline{8}$ (pin 21) input. Pin 21 HIGH; pin 19 is Data Bit 0 (DB0) input. Pin 21 LOW; pin 19 is Least Significant Byte/Most Significant Byte (LS/$\overline{MS}$) control input.
20	DGND	
21	$10/\overline{8}$	10/8-Bit Control Input. When $10/\overline{8}$ is HIGH the AD7527 data port is 10-bits wide (DB9–DB0). This allows single byte (10-bit) write and read operations when using 16-bit data busses. When $10/\overline{8}$ is LOW the AD7527 data port is reduced to 8-bits wide (DB9–DB2). This mode simplifies interfacing to 8-bit data busses and data is loaded or read in two bytes. In this double byte mode LJ/RJ (pin 18) and LS/MS (pin 19) pass data format information to the AD7527.
22	$\overline{RD}$	READ Input. This active low signal, in combination with $\overline{RWE}$ (pin 23), is used to enable the three-state drivers which place the DAC register contents on the external data bus. The data output format is dependent upon control input $10/\overline{8}$ and is shown in Figure 3. The contents of the DAC register can be read in either of the AD7527 operating modes—*count* mode or *load* mode.
23	$\overline{RWE}$	READ WRITE ENABLE Input, Active Low. When the AD7527 is in the *load* mode a LOW on $\overline{RWE}$ enables data transfers to or from the AD7527 via the external data bus. When $\overline{RWE}$ is HIGH the external data bus is locked out. Data present in the input register can still be transferred to the DAC register.
24	$\overline{WR}$	WRITE Input. This active low signal, in combination with others, is used in loading external data into the AD7527 registers and in transferring data from the input register to the DAC register. The data is latched into its destination register (input register, DAC register or both) when $\overline{WR}$ returns high. The $\overline{WR}$ input has no effect when the AD7527 is in the *count* mode.
25	$\overline{LDAC}$	Load DAC input, active low. This signal, in combination with others, is used to load the DAC register from either the input register or the external data bus. The $\overline{LDAC}$ input has no effect when the AD7527 is in the *count* mode.
26	V_{DD}	+5V Supply Input.
27	V_{REF}	Reference Voltage Input.
28	R_{OFF}	Offset Bias Resistor, $R_{OFF} = R_{LAD} = R_{FB}$. If not used, it is recommended that this pin be connected to AGND to minimize noise injection.

TERMINOLOGY

RELATIVE ACCURACY

Relative accuracy or end-point nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for ideal zero and full scale and is expressed in % or ppm of full-scale range or (sub) multiples of 1LSB.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the difference between the *measured* change and the *ideal* 1LSB change between any two adjacent codes. A specified differential nonlinearity of ±1LSB max over the operating temperature range insures monotonicity.

GAIN ERROR

Gain error or full-scale error is a measure of the output error between an ideal DAC and the actual device output. For the AD7527, ideal full-scale output is V_{REF} (1023/1024). Gain error is adjustable to zero.

OUTPUT LEAKAGE CURRENT

Current which appears at OUT1 with the DAC register loaded to all 0s.

MULTIPLYING FEEDTHROUGH ERROR

AC error due to capacitive feedthrough from V_{REF} terminal to OUT1 with DAC register loaded to all 0s.

POWER SUPPLY REJECTION

Power supply rejection is a measure of the sensitivity of the DAC full-scale output to the effect of power supply changes.

PROPAGATION DELAY

This is a measure of the internal circuit delays and is defined as the time from the leading edge of $\overline{WR}$ to the analog output current reaching 90% of its final value for a full scale change.

LSB

This is an abbreviation for Least Significant Bit. For an n-bit converter, $1\text{LSB} = V_{REF}/2^n$.

FSR

This is an abbreviation for Full Scale Range. For a 10-bit converter with a reference input of 10V the FSR is 10 X (1023/1024) volts.

DIGITAL CHARGE INJECTION

The amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA secs or nV secs. Digital charge injection is measured with V_{REF} = AGND.

GENERAL CIRCUIT INFORMATION

D/A CONVERTER SECTION

The AD7527 10-bit multiplying D/A converter section consists of a highly stable thin-film R-2R ladder and ten CMOS current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 1. The binary weighted currents are switched between the OUT1 bus line and AGND by N-channel switches, thus maintaining a constant current in each ladder leg independent of the switch state.

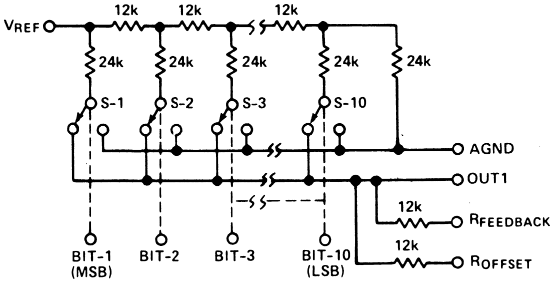


Figure 1. AD7527 Functional Diagram

The capacitance at the OUT1 bus line, C_{OUT1}, is code dependent and varies from 75pF (all switches to AGND) to 230pF (all switches to OUT1).

One of the current switches is shown in Figure 2. The input resistance at V_{REF} (Figure 1) is always equal to R_{LDR} (R_{LDR} is the R/2R ladder characteristic resistance and is equal to value "R"). Since R_{IN} at the V_{REF} pin is constant, the reference terminal can be driven by a reference voltage or a reference current, ac or dc, of positive or negative polarity. (If a current source is used, a low temperature coefficient external R_{FB} is recommended to define scale factor.)

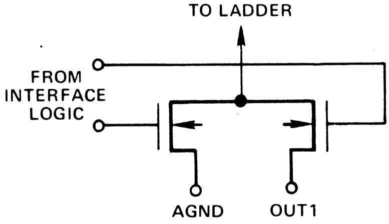
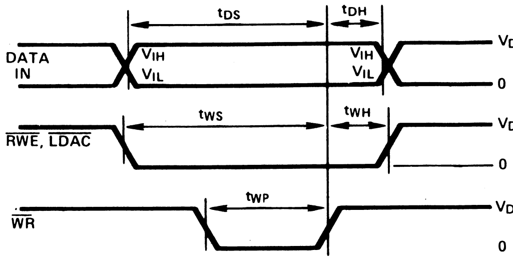


Figure 2. N-Channel Current Steering Switch

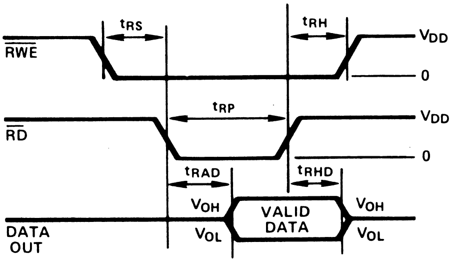
CONTROL INPUT INFORMATION

READ/WRITE

Figure 3 shows generalized WRITE and READ timing diagrams for the AD7527. Dynamic specifications are included on specifications page. A typical setup time of 250ns is required by the AD7527 when changing from the 10-bit bus mode to the 8-bit bus mode or vice versa.



a. Write Timing



b. Read Timing

NOTES:
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF V_{DD}, $t_r = t_f = 20ns$.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$
3. DATA OUT TIMING MEASUREMENTS ARE FROM $V_{OH} = 2.4V$, $V_{OL} = 0.4V$.

Figure 3. AD7527 Timing Diagrams

DATA TRANSFER

A truth table for the data transfer control inputs is shown in Table 1. When the AD7527 is in the 10-bit communications mode (10/$\overline{8}$ HIGH) each write and read function of Table 1 can be executed in a single byte operation. When the AD7527 is in the 8-bit communications mode (10/$\overline{8}$ LOW) 10-bit data write and read functions are two byte operations.

$\overline{LDAC}$	$\overline{RD}$	$\overline{WR}$	$\overline{RWE}$	Function
X	X	X	1	External Data Transfer does not take place
1	1	0	0	Write Data from input bus to Input Register
0	1	0	0	Write Data from input bus to Input Register and DAC Register
X	0	1	0	Read Data to input bus from DAC Register
0	1	0	1	Transfer Data from Input Register to DAC Register

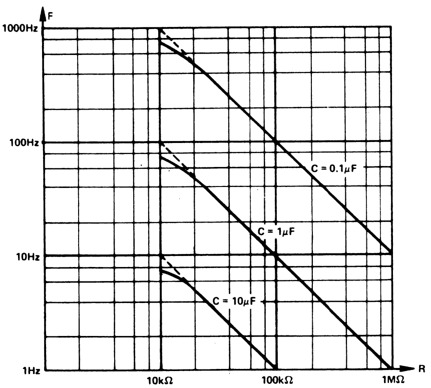
X = "Don't Care" States

Table 1. AD7527 Data Transfer Truth Table (Reading and Writing Data)

INTERNAL CLOCK

Figure 4 shows typical internal oscillator frequency versus R and C. Due to process variations the actual operating frequency for a given RC from Figure 4 can vary from device to device by up to ±10% from the calculated value. The internal oscillator frequency has a typical temperature coefficient of ±200ppm/°C.

The internal oscillator frequency supply rejection is dependent on the operating frequency. For low frequencies (tens of Hz) in the linear regions of Figure 4 it is typically ±0.01%/%. For higher frequencies (hundreds of Hz) in the linear regions of Figure 4 it is typically +0.35%/%. Operation in the nonlinear regions for any frequency will degrade the frequency supply rejection.



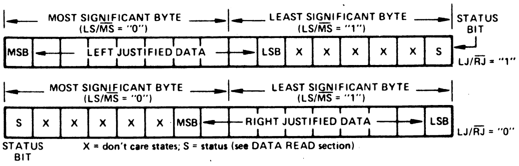
NOTE: INTERNAL OSCILLATOR WILL NOT OPERATE WITH R LESS THAN 10kΩ.

Figure 4. f_{CLK} versus R, C

8-BIT COMMUNICATIONS MODE (10/$\overline{8}$ LOW)

Data Write (8-Bit Bus Mode)

Transferring 10 bits of data over an 8-bit bus requires two write cycles and provides four possible combinations depending on control inputs LJ/$\overline{RJ}$ and LS/$\overline{MS}$. For left justified data LJ/$\overline{RJ}$ is held HIGH. For right justified data LJ/$\overline{RJ}$ is held LOW. The data protocol is determined by LS/$\overline{MS}$. A logic HIGH on LS/$\overline{MS}$ signals the least significant byte is to be loaded; a logic LOW signals the most significant byte is to be loaded. The data possibilities are shown in Figure 5.


MOST SIGNIFICANT BYTE (LS/$\overline{MS}$ = "0")
LEAST SIGNIFICANT BYTE (LS/$\overline{MS}$ = "1")
STATUS BIT
MSB
LEFT JUSTIFIED DATA
LSB
X
X
X
X
X
S
LJ/$\overline{RJ}$ = "1"
MOST SIGNIFICANT BYTE (LS/$\overline{MS}$ = "0")
LEAST SIGNIFICANT BYTE (LS/$\overline{MS}$ = "1")
S
X
X
X
X
X
MSB
RIGHT JUSTIFIED DATA
LSB
LJ/$\overline{RJ}$ = "0"
STATUS BIT

X = don't care states; S = status (see DATA READ section)

Figure 5. Formatting a 10-Bit Data Word

Two operating modes are possible for controlling the transfer of data from the input register to the DAC register, where it will update the analog output voltage. The simplest is the automatic transfer mode, which causes the data transfer to occur at the time of the second write cycle. Figure 6 shows the timing diagram for this mode. A third write cycle is required for the strobed transfer mode. This allows the AD7527 DAC updating to be synchronized with a master strobe signal in systems where update timing is important. Figure 7 illustrates the timing of this mode.

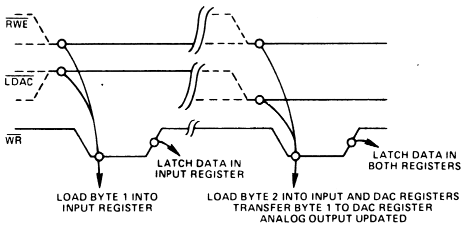

$\overline{RWE}$
$\overline{LDAC}$
$\overline{WR}$
LATCH DATA IN INPUT REGISTER
LATCH DATA IN BOTH REGISTERS
LOAD BYTE 1 INTO INPUT REGISTER
LOAD BYTE 2 INTO INPUT AND DAC REGISTERS TRANSFER BYTE 1 TO DAC REGISTER ANALOG OUTPUT UPDATED

Figure 6. 8-Bit Loading, Automatic Transfer Mode

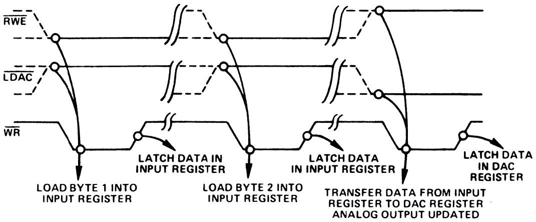

$\overline{RWE}$
$\overline{LDAC}$
$\overline{WR}$
LATCH DATA IN INPUT REGISTER
LATCH DATA IN INPUT REGISTER
LATCH DATA IN DAC REGISTER
LOAD BYTE 1 INTO INPUT REGISTER
LOAD BYTE 2 INTO INPUT REGISTER
TRANSFER DATA FROM INPUT REGISTER TO DAC REGISTER ANALOG OUTPUT UPDATED

Figure 7. 8-Bit Loading, Strobed Transfer Mode

Data Read (8-Bit Bus Mode)
Two read cycles are required to place the contents of the 10-bit DAC register onto the external data bus. Since the data in the DAC register is already either left or right justified the data format control input LJ/$\overline{\text{RJ}}$ must reflect this formatting to avoid data misinterpretation. The LS/$\overline{\text{MS}}$ control input determines which byte is placed on the bus. The three-state drivers are enabled when $\overline{\text{RD}}$ goes low.

The status flag which indicates whether the AD7527 is in the *load* or *count* mode is only available when control input 10/$\overline{8}$ is low. The status flag can only be read. From Figure 5 the status bit is the most right-hand bit in a 16-bit left justified word and the most left-hand bit in a 16-bit right justified word. The status bit can be shifted into a microprocessor's accumulator carry position for testing. Note that the "don't care" states of Figure 5 are driven by the AD7527 three-state drivers during a data read operation. The status flag is high when the AD7527 is in the *load* mode and low when in the *count* mode.

10-BIT COMMUNICATIONS MODE (10/$\overline{8}$ HIGH)

Data Write (10-Bit Bus Mode)
If the available data bus is at least 10 bits wide (e.g., when using 16-bit µPs) then full 10-bit parallel loading is possible. This is the simplest method of AD7527 data loading. A right justified or left justified data format is selected by bus wiring. Like the 8-bit communications mode, two operating modes are possible for controlling the transfer of data from the input register to the DAC register. The simplest is the automatic transfer mode which causes both the input and DAC registers to be loaded simultaneously with a single write cycle (see Figure 8). A second write cycle is required for the strobed transfer mode to allow DAC updating to be synchronized with a master strobe. Figure 9 illustrates this mode timing.

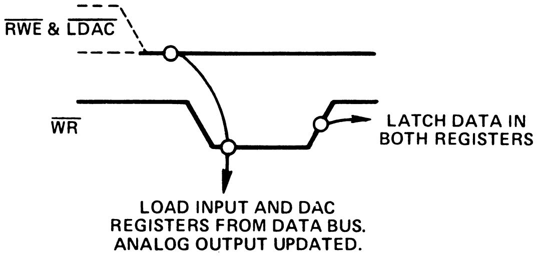

$\overline{\text{RWE}}$ & $\overline{\text{LDAC}}$
$\overline{\text{WR}}$
LATCH DATA IN BOTH REGISTERS
LOAD INPUT AND DAC REGISTERS FROM DATA BUS. ANALOG OUTPUT UPDATED.

Figure 8. 10-Bit Loading, Automatic Transfer Mode

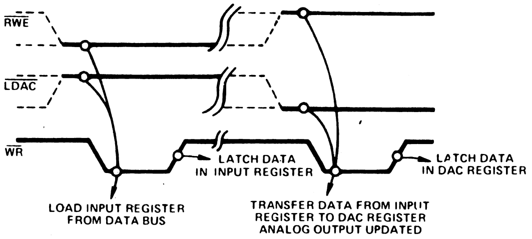

$\overline{\text{RWE}}$
$\overline{\text{LDAC}}$
$\overline{\text{WR}}$
LATCH DATA IN INPUT REGISTER
LATCH DATA IN DAC REGISTER
LOAD INPUT REGISTER FROM DATA BUS
TRANSFER DATA FROM INPUT REGISTER TO DAC REGISTER ANALOG OUTPUT UPDATED

Figure 9. 10-Bit Loading, Strobed Transfer Mode

Data Read (10-Bit Bus Mode)
One read cycle is required to place the contents of the DAC register onto the external data bus. The three-state drivers are enabled when $\overline{\text{RD}}$ goes low.

The status flag is not directly available in the 10-bit communications mode but it can be obtained by using software control to switch the AD7527 to the 8-bit bus mode (see Figure 10). The two pull-up resistors on DB0 and DB1 automatically select, when 10/$\overline{8}$ goes low, the left justified data format, least significant byte. The processor can now read the status bit on DB2. When it has done so, it switches the AD7527 back to the 10-bit communications mode.

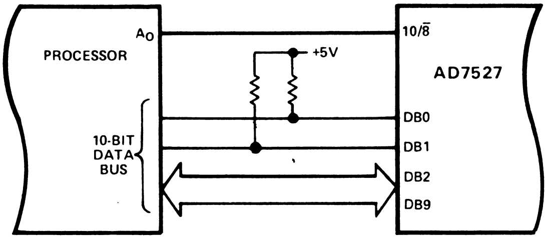


Figure 10. Reading Status Flag in 10-Bit Communications Mode

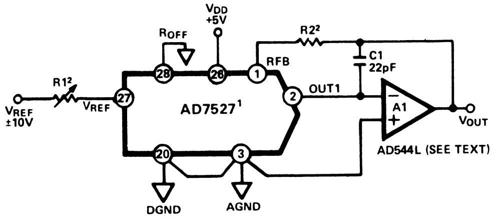
UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 11 shows the analog circuit connections required for unipolar binary (2-quadrant multiplication) operation. The logic inputs are omitted for clarity and the AD7527 offset input, R_{OFF} (pin 28), is tied to AGND. With a dc reference voltage or current (positive or negative polarity) applied at pin 27, the circuit is a unipolar D/A converter. With an ac reference voltage or current the circuit provides 2-quadrant multiplication (digitally controlled attenuation). The input/output relationship is shown in Table 2. When an offset voltage V_{OFF} is applied to pin 28, an extra term $-V_{OFF}$ is added to the analog output, V_{OUT}, of Table 2. To keep feedthrough to a minimum it is recommended that pin 28 be returned to a low impedance point, either AGND or an op-amp output.

For full scale trimming the DAC input is forced to 1111111111 either by using the data override function or by loading the DAC register with 1111111111. R1 is then adjusted for $V_{OUT} = -V_{REF}$ (1023/1024). Alternatively, full scale can be adjusted by omitting R1 and R2 and trimming the reference voltage magnitude.

Phase compensation capacitor C1 (10 to 25pF) may be required for stability when using high speed amplifiers. C1 is used to cancel the pole formed by the DAC internal feedback resistance and output capacitance at OUT1.

Amplifier A1 should be selected or trimmed to provide $V_{OS} \leqslant 10\%$ of an LSB. Additionally, the amplifier should exhibit a bias current which is low over the temperature range of interest (bias current causes output offset at V_{OUT} equal to I_B times the DAC feedback resistance, nominally 12kΩ). The AD544L is a high-speed implanted FET-input op amp with low, factory-trimmed V_{OS} and low I_B.



NOTES: 1. LOGIC INPUTS OMITTED FOR CLARITY
2. SEE APPLICATION HINT NO. 5

Figure 11. Unipolar Binary Operation (2-Quadrant Multiplication)

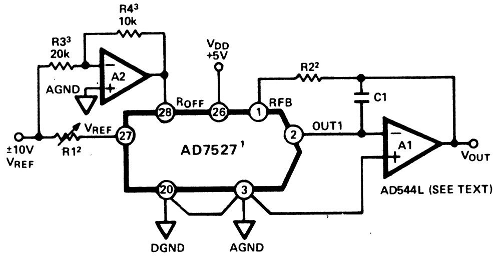
BINARY NUMBER IN DAC REGISTER MSB LSB	ANALOG OUTPUT, V_{OUT}
1111111111	$-V_{REF}\left(\frac{1023}{1024}\right)$ = Full Scale
1000000000	$-V_{REF}\left(\frac{512}{1024}\right) = -1/2\ V_{REF}$
0000000001	$-V_{REF}\left(\frac{1}{1024}\right)$
0000000000	0V = Zero Scale

Table 2. Unipolar Binary Code Table for Circuit of Figure 11

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

Figure 12 and Table 3 illustrate the circuitry and code relationship for bipolar operation with offset binary coding. For half scale trimming (V_{OUT} = 0V) the DAC input is forced to 1000000000 either by using the data override function or by loading the DAC register with 1000000000. The ratio of R3 to R4 is then adjusted for V_{OUT} = 0V. Full scale trimming is similarly accomplished by forcing the DAC input to 1111111111 and adjusting R1 for $V_{OUT} = -V_{REF}/2$ (511/512). Alternatively full scale can be adjusted by omitting R1 and R2 and trimming the reference voltage input.

As in unipolar operation, A1 must be chosen for low V_{OS} and low I_B. In fixed reference applications A2 can be a slow amplifier to minimize cost e.g., AD542L. However, A2 should still exhibit good offset and bias characteristics. For multiplying DAC applications A2 requires a bandwidth consistent with the V_{REF} bandwidth. R3 and R4 should be selected for matching and tracking over the temperature range of interest. Any mismatch will cause both offset and full scale errors. Phase compensation capacitor C1 (10pF to 25pF) may be required for stability.



NOTES: 1. LOGIC INPUTS OMITTED FOR CLARITY
2. SEE APPLICATION HINT NO. 5
3. R3, R4 MATCH 0.05% OR BETTER

Figure 12. Bipolar Operation (4-Quadrant Multiplication)

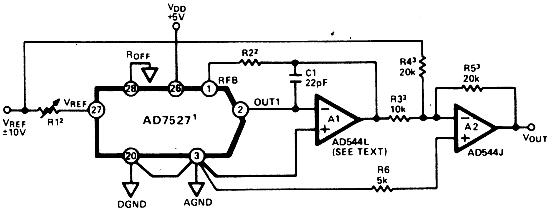
BINARY NUMBER IN DAC REGISTER MSB LSB	ANALOG OUTPUT, V_{OUT}
1111111111	$-\frac{V_{REF}}{2}\left(\frac{511}{512}\right)$
1000000001	$-\frac{V_{REF}}{2}\left(\frac{1}{512}\right)$
1000000000	0V
0111111111	$+\frac{V_{REF}}{2}\left(\frac{1}{512}\right)$
0000000000	$+\frac{V_{REF}}{2}\left(\frac{512}{512}\right)$

Table 3. Bipolar Code Table for Offset Binary Circuit of Figure 12

If the required analog output in bipolar operation is $V_{OUT} = \pm V_{REF}$ (as opposed to $\pm V_{REF}/2$ with Figure 12) then the AD7527 should be connected as shown in Figure 13. Table 4 illustrates the code relationship for this case.

For half scale trimming (V_{OUT} = 0V) the DAC input is forced to 1000000000 either by using the data override function or by loading the DAC register with 1000000000. R1 is then adjusted for V_{OUT} = 0V. Alternatively, one can omit R1 and R2 and adjust the ratio of R3 to R4 for V_{OUT} = 0V. Full scale trimming is similarly accomplished by forcing the DAC input to 1111111111 and adjusting R5 for $V_{OUT} = +V_{REF}$ (511/512) or by varying the amplitude of V_{REF}.

As in unipolar operation, A1 must be chosen for low V_{OS} and low I_B. R3, R4 and R5 must be selected for matching and tracking over the temperature range of interest. Mismatch of 2R3 to R4 causes both offset and full scale error. Mismatch of R5 and R4 and 2R3 causes full scale error. Phase compensation capacitor C1 (10pF to 25pF) may be required for stability.



NOTES: 1. LOGIC INPUTS OMITTED FOR CLARITY
2. SEE APPLICATION HINTS NO. 5
3. R3, R4, R5 MATCH 0.05% OR BETTER

Figure 13. Bipolar Operation (4-Quadrant Multiplication)

BINARY NUMBER IN DAC REGISTER MSB LSB	ANALOG OUTPUT, V_{OUT}
1111111111	$+V_{REF}\left(\frac{511}{512}\right)$
1000000001	$+V_{REF}\left(\frac{1}{512}\right)$
1000000000	0V
0111111111	$-V_{REF}\left(\frac{1}{512}\right)$
0000000000	$-V_{REF}\left(\frac{512}{512}\right)$

Table 4. Bipolar Code Table for Offset Binary Circuit of Figure 13

Figure 14 illustrates an arrangement to generate with two SPDT switches, one with center off, mode control signals for the AD7527. The truth table for CONT1 and CONT2 signals is shown under the pin function description of pin 8.

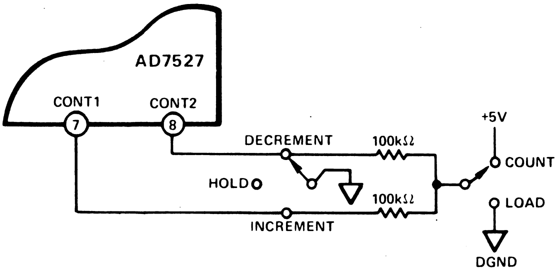
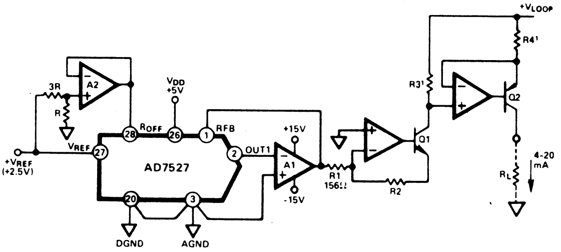


Figure 14. Typical Front Panel Mode Control Circuitry

4-20mA LOOP CIRCUITS



NOTES 1 R3, R4 MATCH TO 5%

Figure 15. R_L Referenced to AGND

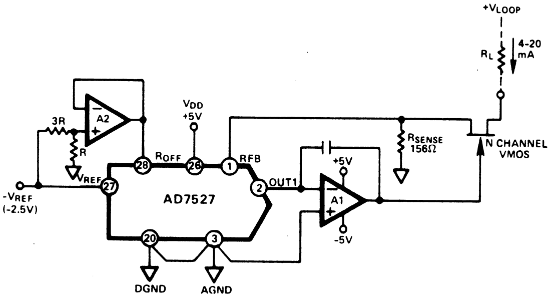


Figure 16. R_L Referenced to Positive Loop Supply

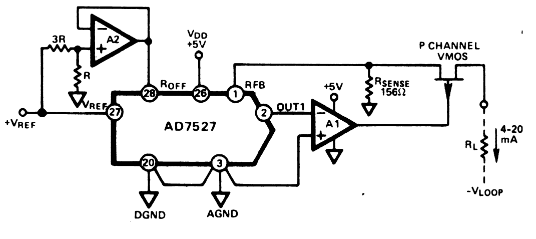


Figure 17. R_L Referenced to Negative Loop Supply (Note Single Supply Operation)

APPLICATION HINTS

To ensure system performance consistent with AD7527 specifications, careful attention must be given to the following points:

1. GENERAL GROUND MANAGEMENT: Voltage differences between the AD7527 AGND and DGND cause loss of accuracy (dc voltage difference between the grounds introduces gain error. AC or transient voltages between the grounds cause noise injection into the analog output). The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7527. In more complex systems where the AGND-DGND intertie is on the back-plane, it is recommended that diodes be connected back-to-back between the AD7527 AGND and DGND pins (1N914 or equivalent).
2. OUTPUT AMPLIFIER OFFSET: CMOS DACs exhibit a code-dependent output resistance which in turn causes a code-dependent amplifier noise gain. The effect is a code-dependent differential nonlinearity term at the amplifier output of maximum magnitude 0.67 V_{OS} (V_{OS} is amplifier input offset voltage). This differential nonlinearity term adds to the R/2R differential nonlinearity. To maintain monotonic operation, it is recommended that amplifier V_{OS} be no greater than 10% of 1LSB over the temperature range of interest [output resolution = $V_{REF}(2^{-n})$ where n is the number of bits exercised].
3. HIGH FREQUENCY CONSIDERATIONS: AD7527 output capacitance works in conjunction with the amplifier feedback resistance to add a pole to the open loop response. This can cause ringing or oscillation. Stability can be restored by adding a phase compensation capacitor in parallel with the feedback resistor.
4. FEEDTHROUGH: The dynamic performance of the AD7527 will depend upon the gain and phase stability of the output amplifier, together with the optimum choice of PC board layout and decoupling components. A suggested printed circuit layout for Figure 11 is shown below which minimizes feedthrough from V_{REF} to the output in multiplying applications.

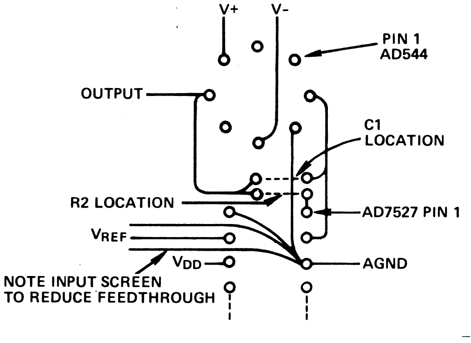


Figure 18. Suggested Layout Shows Copper Side (i.e. Bottom View)

5. GAIN TEMPERATURE COEFFICIENTS: The gain temperature coefficient of the AD7527 has a maximum value of 5ppm/°C and a typical value of 2ppm/°C. This corresponds to worst case gain shifts of 0.51LSBs and 0.2LSBs respectively over a 100°C temperature range. When trim resistors are used to adjust full scale range as shown in Figures 11, 12 and 13, the temperature coefficients of the trim resistors should also be taken into account. It may be shown that the additional gain temperature coefficients introduced by R1 and R2 may be approximately expressed as follows:

$$\text{Temperature Coefficient Contribution Due to R1} = -\frac{R1}{R_{IN}}(\gamma 1 + 300)$$

$$\text{Temperature Coefficient Contribution Due to R2} = +\frac{R2}{R_{IN}}(\gamma 2 + 300)$$

Where $\gamma 1$ and $\gamma 2$ are the temperature coefficients in ppm/°C of R1 and R2 respectively and R_{IN} is the DAC input resistance at the V_{REF} terminal (pin 27). For high quality wire-wound resistors $\gamma = +50$ppm/°C and for trimming potentiometers $\gamma = \pm 50$ppm/°C.

It will be seen that if R1 and R2 are small compared with R_{IN}, their contribution to gain temperature coefficient will be small. For the standard AD7527TD gain error specification of ±10LSBs it is recommended that R1 = 200Ω and R2 = 100Ω.

However if the AD7527GUD is used which has a specified gain error of ±1LSB it is recommended that R1 = 10Ω and R2 = 5Ω. With these values the maximum gain temperature coefficient is increased by only 0.34ppm/°C. Where possible R1 should be a select on test fixed resistor since the resulting gain temperature coefficient will be tighter in all cases. For further gain T.C. information refer to application note, "Gain Error and Gain Temperature Coefficients of CMOS Multiplying DACs", Publication Number E630–10–6/81 available from Analog Devices.

6. For additional information on multiplying DACs refer to "Applications Guide to CMOS Multiplying D/A Converters", Publication Number G479–15–8/78, available from Analog Devices.

ANALOG DEVICES

CMOS
Dual 8-Bit Buffered Multiplying DAC

AD7528

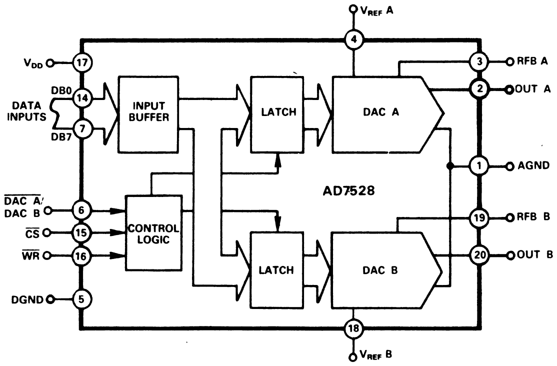
FEATURES

On-Chip Latches for Both DACs
+5V to +15V Operation
DACs Matched to 1%
Four Quadrant Multiplication
TTL/CMOS Compatible
Latch Free (Protection Schottkys not Required)

APPLICATIONS

Digital Control of:
- **Gain/Attenuation**
- **Filter Parameters**
- **Stereo Audio Circuits**
- **X–Y Graphics**

AD7528 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7528 is a monolithic dual 8-bit digital/analog converter produced in a small 0.3″ wide 20-pin DIP, featuring excellent DAC-to-DAC matching.

Separate on-chip latches are provided for each DAC to allow easy microprocessor interface.

Data is transferred into either of the two DAC data latches via a common 8-bit TTL/CMOS compatible input port. Control input $\overline{\text{DAC A}}$/DAC B determines which DAC is to be loaded. The AD7528's load cycle is similar to the write cycle of a random access memory and the device is bus compatible with most 8-bit microprocessors, including 6800, 8080, 8085, Z80.

The device operates from a +5V to +15V power supply, dissipating only 20mW of power.

Both DACs offer excellent four quadrant multiplication characteristics with a separate reference input and feedback resistor for each DAC.

PRODUCT HIGHLIGHTS

1. DAC to DAC matching: since both of the AD7528 DACs are fabricated at the same time on the same chip, precise matching and tracking between DAC A and DAC B is inherent. The AD7528's matched CMOS DACs make a whole new range of applications circuits possible, particularly in the audio, graphics and process control areas.
2. Small package size: combining the inputs to the on-chip DAC latches into a common data bus and adding a $\overline{\text{DAC A}}$/DAC B select line has allowed the AD7528 to be packaged in a small 20-pin 0.3″ wide DIP.

SPECIFICATIONS (V_{REF} A = V_{REF} B = +10V; OUT A = OUT B = 0V unless otherwise specified)

Parameter	Version[1]	V_{DD} = +5V T_A = +25°C	 T_{min}, T_{max}	V_{DD} = +15V T_A = +25°C	 T_{min}, T_{max}	Units	Test Conditions/Comments
STATIC PERFORMANCE[2]							
Resolution	All	8	8	8	8	Bits	
Relative Accuracy	J, A, S	±1	±1	±1	±1	LSB max	This is an Endpoint Linearity Specification
	K, B, T	±½	±½	±½	±½	LSB max	
	L, C, U	±½	±½	±½	±½	LSB max	
Differential Nonlinearity	All	±1	±1	±1	±1	LSB max	All Grades Guaranteed Monotonic Over Full Operating Temperature Range
Gain Error	J, A, S	±4	±6	±4	±5	LSB max	Measured Using Internal RFB A and RFB B.
	K, B, T	±2	±4	±2	±3	LSB max	Both DAC Latches Loaded with 11111111.
	L, C, U	±1	±3	±1	±1	LSB max	Gain Error is Adjustable Using Circuits of Figures 4 and 5.
Gain Temperature Coefficient ΔGain/ΔTemperature	All	±0.007	±0.007	±0.0035	±0.0035	%/°C max	
Output Leakage Current							
OUT A (Pin 2)	All	±50	±400	±50	±200	nA max	DAC Latches Loaded with 00000000
OUT B (Pin 20)	All	±50	±400	±50	±200	nA max	
Input Resistance (V_{REF} A, V_{REF} B)	All	8	8	8	8	kΩ min	Input Resistance TC = −300ppm/°C, Typical
		15	15	15	15	kΩ max	Input Resistance is 11kΩ
V_{REF} A/V_{REF} B Input Resistance Match	All	±1	±1	±1	±1	% max	
DIGITAL INPUTS[3]							
Input High Voltage V_{IH}	All	2.4	2.4	13.5	13.5	V min	
Input Low Voltage V_{IL}	All	0.8	0.8	1.5	1.5	V max	
Input Current I_{IN}	All	±1	±10	±1	±10	μA max	V_{IN} = 0 or V_{DD}
Input Capacitance							
DB0–DB7	All	30	30	30	30	pF max	
$\overline{WR}$, $\overline{CS}$, DAC A/$\overline{DAC B}$	All	30	30	30	30	pF max	
SWITCHING CHARACTERISTICS[4]							See Timing Diagram
Chip Select to Write Set Up Time t_{CS}	All	200	230	60	80	ns min	
Chip Select to Write Hold Time t_{CH}	All	10	15	20	30	ns min	
DAC Select to Write Set Up Time t_{AS}	All	200	230	60	80	ns min	
DAC Select to Write Hold Time t_{AH}	All	10	15	20	30	ns min	
Data Valid to Write Set Up Time t_{DS}	All	30	40	110	130	ns min	
Data Valid to Write Hold Time t_{DH}	All	0	0	0	0	ns min	
Write Pulse Width t_{WR}	All	60	80	180	200	ns min	
POWER SUPPLY							See Figure 3
I_{DD}	All	1	1	1	1	mA max	All Digital Inputs V_{IL} or V_{IH}
		100	500	100	500	μA max	All Digital Inputs 0V or V_{DD}

AC PERFORMANCE CHARACTERISTICS[5] (Measured Using Recommended P.C. Board Layout (Figure 7) and AD644 as Output Amplifiers)

Parameter	Version[1]	V_{DD} = +5V T_A = +25°C	 T_{min}, T_{max}	V_{DD} = +15V T_A = +25°C	 T_{min}, T_{max}	Units	Test Conditions/Comments
DC SUPPLY REJECTION (ΔGAIN/ΔV_{DD})	All	0.02	0.04	0.01	0.02	% per % max	ΔV_{DD} = ±5%
PROPAGATION DELAY (From Digital Input to 90% of Final Analog Output Current)	All	220	270	80	100	ns max	V_{REF} A = V_{REF} B = +10V OUT A, OUT B Load = 100Ω C_{EXT} = 13pF $\overline{WR}$, $\overline{CS}$ = 0V DB0–DB7 = 0V to V_{DD} or V_{DD} to 0V
DIGITAL CHARGE INJECTION	All	160	–	440	–	nV sec typ	For Code Transition 00000000 to 11111111
OUTPUT CAPACITANCE							
C_{OUT} A	All	50	50	50	50	pF max	DAC Latches Loaded with 00000000
C_{OUT} B		50	50	50	50	pF max	
C_{OUT} A		120	120	120	120	pF max	DAC Latches Loaded with 11111111
C_{OUT} B		120	120	120	120	pF max	
AC FEEDTHROUGH[6]							
V_{REF} A to OUT A	All	−70	−65	−70	−65	dB max	V_{REF} A, V_{REF} B = 20V p-p Sine Wave
V_{REF} B to OUT B		−70	−65	−70	−65	dB max	@ 100kHz
CHANNEL TO CHANNEL ISOLATION							Both DAC Latches Loaded with 11111111.
V_{REF} A to OUT B	All	−77	–	−77	–	dB typ	V_{REF} A = 20V p-p Sine Wave @ 100kHz V_{REF} B = 0V see Figure 6.
V_{REF} B to OUT A		−77	–	−77	–	dB typ	V_{REF} A = 20V p-p Sine Wave @ 100kHz V_{REF} A = 0V see Figure 6.
DIGITAL CROSSTALK	All	30	–	60	–	nV sec typ	Measured for Code Transition 00000000 to 11111111
HARMONIC DISTORTION	All	−85	–	−85	–	dB typ	V_{IN} = 6V rms @ 1kHz

NOTES:

[1] Temperature Ranges are JN, KN, LN : 0 to +70°C
AQ, BQ, CQ : −25°C to +85°C
ST, TD, UD : −55°C to +125°C

[2] Specification applies to both DACs in AD7528.

[3] Logic inputs are MOS Gates. Typical input current (+25°C) is less than 1nA.

[4] Guaranteed by design but not production tested.

[5] These characteristics are for design guidance only and are not subject to test.

[6] Feedthrough can be further reduced by connecting the metal lid on the ceramic package (suffix D) to DGND.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND	0V, +17V
V_{DD} to DGND	0V, +17V
AGND to DGND	V_{DD}
DGND to AGND	V_{DD}
Digital Input Voltage to DGND	−0.3V, +15V
V_{PIN2}, V_{PIN20} to AGND	−0.3V, +15V
V_{REF} A, V_{REF} B to AGND	±25V
V_{RFB} A, V_{RFB} B to AGND	±25V
Power Dissipation (Any Package) to +75°C	450mW
Derates above +75°C by	6mW/°C
Operating Temperature Range	
Commercial (JN, KN, LN) Grades	0 to +70°C
Industrial (AQ, BQ, CQ) Grades	−25°C to +85°C
Military (SD, TD, UD) Grades	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 secs.)	+300°C

CAUTION:

1. ESD sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts.
2. Do not insert this device into powered sockets. Remove power before insertion or removal.

TERMINOLOGY

Relative Accuracy:

Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale and is normally expressed in LSBs or as a percentage of full scale reading.

ORDERING INFORMATION

Relative Accuracy	Gain Error T_A = +25°C	Temperature Range and Package[1]		
		Plastic[2] 0 to +70°C	Cerdip[3,4] −25°C to +85°C	Ceramic[4] −55°C to +125°C
±1LSB	±4LSB	AD7528JN	AD7528AQ	AD7528SD
±1/2LSB	±2LSB	AD7528KN	AD7528BQ	AD7528TD
±1/2LSB	±1LSB	AD7528LN	AD7528CQ	AD7528UD

NOTES:

[1] The AD7528 is available in chip carriers—contact the factory for information.

[2] Plastic version will be available by early, 1982.

[3] Analog Devices reserves the right to ship ceramic packages in lieu of Cerdip packages.

[4] 883B version is available. To order add "/883B" to part number shown.

Differential Nonlinearity:

Differential nonlinearity is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. A specified differential nonlinearity of ±1LSB max over the operating temperature range ensures monotonicity.

Gain Error:

Gain error or full-scale error is a measure of the output error between an ideal DAC and the actual device output. For the AD7528, ideal full-scale output is V_{REF} − 1LSB. Gain error of both DACs is adjustable to zero with external resistance.

Output Capacitance:

Capacitance from OUT A or OUT B to AGND.

Digital Charge Injection:

The amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA-secs or nV-secs depending upon whether the glitch is measured as a current or voltage signal. Digital charge injection is measured with V_{REF} A, V_{REF} B = AGND.

Propagation Delay:

This is a measure of the internal delays of the circuit and is defined as the time from a digital input change to the analog output current reaching 90% of its final value.

Channel-to-Channel Isolation:

The proportion of input signal from one DAC's reference input which appears at the output of the other DAC, expressed as a ratio in dB.

Digital Crosstalk:

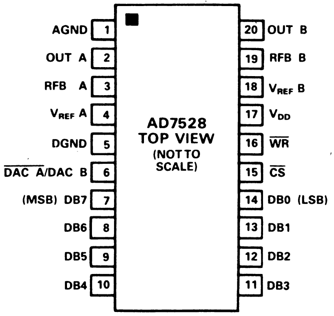
The glitch energy transferred to the output of one converter due to a change in digital input code to the other converter. Specified in nV secs.

PACKAGE IDENTIFICATION[1]

Suffix D: Ceramic DIP (D20A)
Suffix Q: Cerdip (Q20A)
Suffix N: Plastic DIP (N20A)

[1] See Section 20 for package outline information.

PIN CONFIGURATION



INTERFACE LOGIC INFORMATION

DAC Selection:

Both DAC latches share a common 8-bit input port. The control input $\overline{\text{DAC A}}$/DAC B selects which DAC can accept data from the input port.

Mode Selection:

Inputs $\overline{CS}$ and $\overline{WR}$ control the operating mode of the selected DAC. See Mode Selection Table below.

Write Mode:

When $\overline{CS}$ and $\overline{WR}$ are both low the selected DAC is in the write mode. The input data latches of the selected DAC are transparent and its analog output responds to activity on DB0–DB7.

Hold Mode:

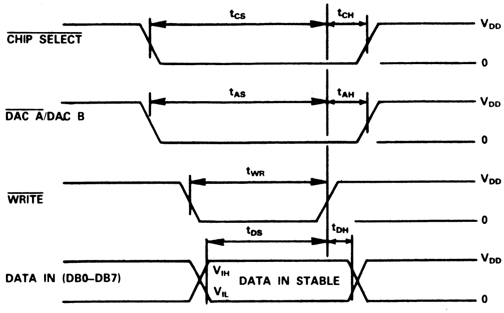
The selected DAC latch retains the data which was present on DB0–DB7 just prior to $\overline{CS}$ or $\overline{WR}$ assuming a high state. Both analog outputs remain at the values corresponding to the data in their respective latches.

$\overline{\text{DAC A}}$/ DAC B	$\overline{CS}$	$\overline{WR}$	DAC A	DAC B
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

L = Low State H = High State X = Don't Care

Mode Selection Table

WRITE CYCLE TIMING DIAGRAM



NOTES:
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF V_{DD}.
V_{DD} = +5V, $t_r = t_f$ = 20ns;
V_{DD} = +15V, $t_r = t_f$ = 40ns.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$

CIRCUIT INFORMATION–D/A SECTION

The AD7528 contains two identical 8-bit multiplying D/A converters, DAC A and DAC B. Each DAC consists of a highly stable thin film R-2R ladder and eight N-channel current steering switches. A simplified D/A circuit for DAC A is shown in Figure 1. An inverted R-2R ladder structure is used, that is, binary weighted currents are switched between the DAC output and AGND thus maintaining fixed currents in each ladder leg independent of switch state.

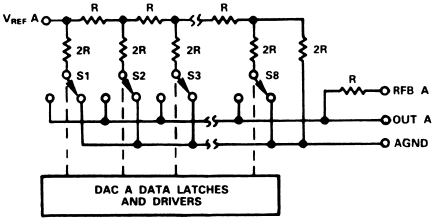


Figure 1. Simplified Functional Circuit for DAC A

EQUIVALENT CIRCUIT ANALYSIS

Figure 2 shows an approximate equivalent circuit for one of the AD7528's D/A converters, in this case DAC A. A similar equivalent circuit can be drawn for DAC B. Note that AGND (Pin 1) is common for both DAC A and DAC B.

The current source $I_{LEAKAGE}$ is composed of surface and junction leakages and, as with most semiconductor devices, approximately doubles every 10°C. The resistor R_O as shown in Figure 2 is the equivalent output resistance of the device which varies with input code from 0.8R to 2R. R is typically 11kΩ. C_{OUT} is the capacitance due to the N-channel switches and varies from about 50pF to 120pF depending upon the digital input. $g(V_{REF}\ A, N)$ is the Thevenin equivalent voltage generator due to the reference input voltage V_{REF} A and the transfer function of the R-2R ladder.

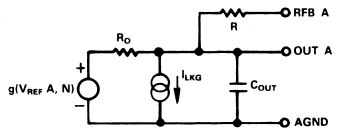


Figure 2. Equivalent Analog Output Circuit of DAC A

For further information on CMOS multiplying D/A converters refer to "Application Guide to CMOS Multiplying D/A Converters" available from Analog Devices, Publication Number G479–15–8/78.

CIRCUIT INFORMATION–DIGITAL SECTION

The input buffers are simple CMOS inverters designed such that when the AD7528 is operated with V_{DD} = 5V, the buffer converts TTL input levels (2.4V and 0.8V) into CMOS logic levels. When V_{IN} is in the region of 2.0 volts to 3.5 volts the input buffers operate in their linear region and pass a quiescent current, see Figure 3. To minimize power supply currents it is recommended that the digital input voltages be as close to the supply rails (V_{DD} and DGND) as is practically possible.

The AD7528 may be operated with any supply voltage in the range $5 \leq V_{DD} \leq 15$ volts. With V_{DD} = +15V the input logic levels are CMOS compatible only, i.e., 1.5V and 13.5V.

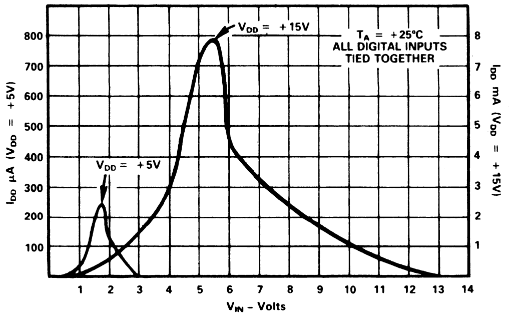


Figure 3. Typical Plots of Supply Current, I_{DD} vs. Logic Input Voltage V_{IN}, for V_{DD} = +5V and +15V

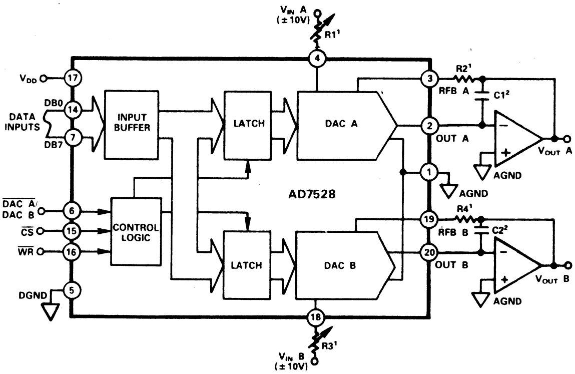


Figure 4. Dual DAC Unipolar Binary Operation (2 Quadrant Multiplication). See Table 1.

NOTES:

[1] R1, R2 AND R3, R4 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED. SEE TABLE 3 FOR RECOMMENDED VALUES.

[2] C1, C2 PHASE COMPENSATION (10pF–15pF) IS REQUIRED WHEN USING HIGH SPEED AMPLIFIERS TO PREVENT RINGING OR OSCILLATION.

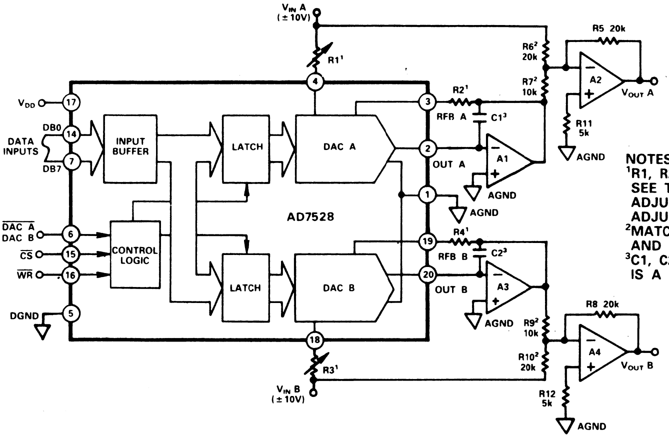


Figure 5. Dual DAC Bipolar Operation (4 Quadrant Multiplication). See Table 2.

NOTES:

[1] R1, R2 AND R3, R4 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED. SEE TABLE 3 FOR RECOMMENDED VALUES. ADJUST R1 FOR V_{OUT} A = 0V WITH CODE 10000000 IN DAC A LATCH. ADJUST R3 FOR V_{OUT} B = 0V WITH CODE 10000000 IN DAC B LATCH.

[2] MATCHING AND TRACKING IS ESSENTIAL FOR RESISTOR PAIRS R6, R7 AND R9, R10.

[3] C1, C2 PHASE COMPENSATION (10pF–15pF) MAY BY REQUIRED IF A1/A3 IS A HIGH-SPEED AMPLIFIER.

DAC Latch Contents MSB LSB	Analog Output (DAC A or DAC B)
11111111	$-V_{IN}\left(\frac{255}{256}\right)$
10000001	$-V_{IN}\left(\frac{129}{256}\right)$
10000000	$-V_{IN}\left(\frac{128}{256}\right) = -\frac{V_{IN}}{2}$
01111111	$-V_{IN}\left(\frac{127}{256}\right)$
00000001	$-V_{IN}\left(\frac{1}{256}\right)$
00000000	$-V_{IN}\left(\frac{0}{256}\right) = 0$

Note: 1LSB = $(2^{-8})(V_{IN}) = \frac{1}{256}(V_{IN})$

Table 1. Unipolar Binary Code Table

DAC Latch Contents MSB LSB	Analog Output (DAC A or DAC B)
11111111	$+V_{IN}\left(\frac{127}{128}\right)$
10000001	$+V_{IN}\left(\frac{1}{128}\right)$
10000000	0
01111111	$-V_{IN}\left(\frac{1}{128}\right)$
00000001	$-V_{IN}\left(\frac{127}{128}\right)$
00000000	$-V_{IN}\left(\frac{128}{128}\right)$

Note: 1LSB = $(2^{-7})(V_{IN}) = \frac{1}{128}(V_{IN})$

Table 2. Bipolar (Offset Binary) Code Table

Trim Resistor	JN/AQ/SD	KN/BQ/TD	LN/CQ/UD
R1;R3	1k	500	200
R2;R4	330	150	82

Table 3. Recommended Trim Resistor Values vs. Grade

APPLICATIONS INFORMATION

Application Hints

To ensure system performance consistent with AD7528 specifications, careful attention must be given to the following points:

1. GENERAL GROUND MANAGEMENT: AC or transient voltages between the AD7528 AGND and DGND can cause noise injection into the analog output. The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7528. In more complex systems where the AGND–DGND intertie is on the back-plane, it is recommended that diodes be connected in inverse parallel between the AD7528 AGND and DGND pins (1N914 or equivalent).
2. OUTPUT AMPLIFIER OFFSET: CMOS DACs exhibit a code-dependent output resistance which in turn causes a code-dependent amplifier noise gain. The effect is a code-dependent differential nonlinearity term at the amplifier output of maximum magnitude 0.67 V_{OS} (V_{OS} is amplifier input offset voltage). This differential nonlinearity term adds to the R/2R differential nonlinearity. To maintain monotonic operation, it is recommended that amplifier V_{OS} be no greater than 10% of 1LSB over the temperature range of interest.
3. HIGH FREQUENCY CONSIDERATIONS: The output capacitance of a CMOS DAC works in conjunction with the amplifier feedback resistance to add a pole to the open loop response. This can cause ringing or oscillation. Stability can be restored by adding a phase compensation capacitor in parallel with the feedback resistor.

DYNAMIC PERFORMANCE

The dynamic performance of the two DACs in the AD7528 will depend upon the gain and phase characteristics of the output amplifiers together with the optimum choice of the PC board layout and decoupling components. Figure 6 shows the relationship between input frequency and channel to channel isolation. Figure 7 shows a printed circuit layout for the AD7528 and the AD644 dual op-amp which minimizes feedthrough and crosstalk.

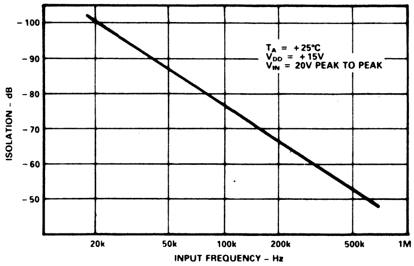
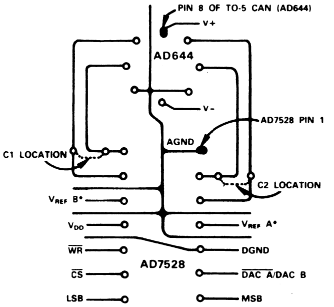


Figure 6. Channel to Channel Isolation



*NOTE INPUT SCREENS TO REDUCE FEEDTHROUGH.
LAYOUT SHOWS COPPER SIDE (i.e., BOTTOM VIEW).

Figure 7. Suggested P.C. Board Layout for AD7528 with AD644 Dual Op-Amp

SINGLE SUPPLY APPLICATIONS

The AD7528 DAC R-2R ladder termination resistors are connected to AGND within the device. This arrangement is particularly convenient for single supply operation because AGND may be biased at any voltage between DGND and V_{DD}. Figure 8 shows a circuit which provides two +5V to +8V analog outputs by biasing AGND +5V up from DGND. The two DAC reference inputs are tied together and a reference input voltage is obtained without a buffer amplifier by making use of the constant and matched impedances of the DAC A and DAC B reference inputs. Current flows through the two DAC R-2R ladders into R1 and R1 is adjusted until the V_{REF} A and V_{REF} B inputs are at +2V. The two analog output voltages range from +5V to +8V for DAC codes 00000000 to 11111111.

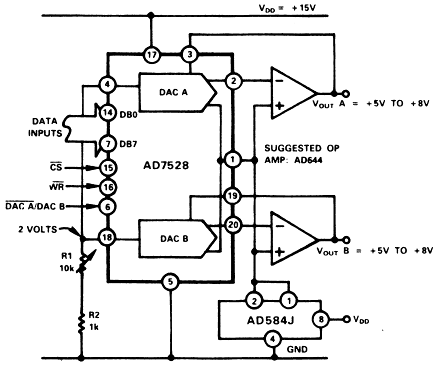


Figure 8. AD7528 Single Supply Operation

Figure 9 shows DAC A of the AD7528 connected in a positive reference, voltage switching mode. This configuration is useful in that V_{OUT} is the same polarity as V_{IN} allowing single supply operation. However, to retain specified linearity, V_{IN} must be in the range 0 to +2.5V and the output buffered or loaded with a high impedance, see Figure 10. Note that the input voltage is connected to the DAC OUT A and the output voltage is taken from the DAC V_{REF} A pin.

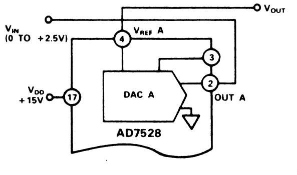


Figure 9. AD7528 in Single Supply, Voltage Switching Mode

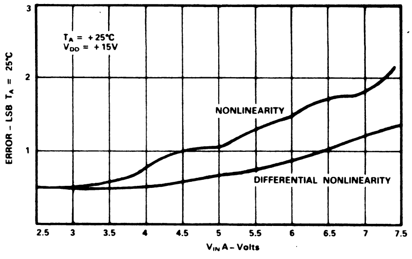
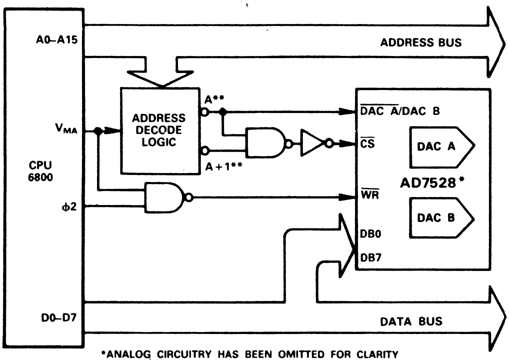


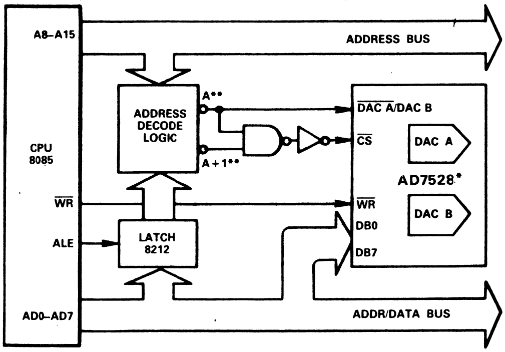
Figure 10. Typical AD7528 Performance in Single Supply Voltage Switching Mode (K/B/T, L/C/U Grades)

MICROPROCESSOR INTERFACE



*ANALOG CIRCUITRY HAS BEEN OMITTED FOR CLARITY
**A = DECODED 7528 ADDR DAC A
A + 1 = DECODED 7528 ADDR DAC B

Figure 11. AD7528 Dual DAC to 6800 CPU Interface



*ANALOG CIRCUITRY HAS BEEN OMITTED FOR CLARITY.
**A = DECODED 7528 ADDR DAC A
A + 1 = DECODED 7528 ADDR DAC B

NOTE:
8085 INSTRUCTION SHLD (STORE H & L DIRECT) CAN UPDATE BOTH DACS WITH DATA FROM H AND L REGISTERS

Figure 12. AD7528 Dual DAC to 8085 CPU Interface

PROGRAMMABLE WINDOW COMPARATOR

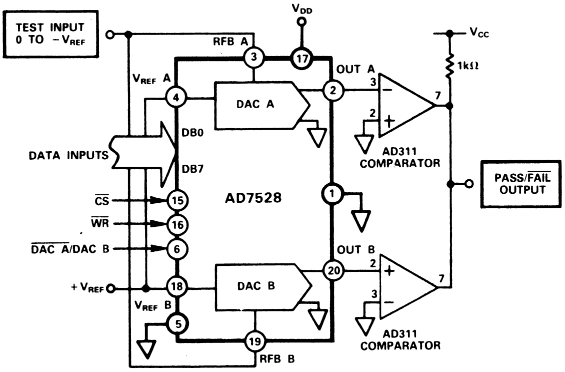
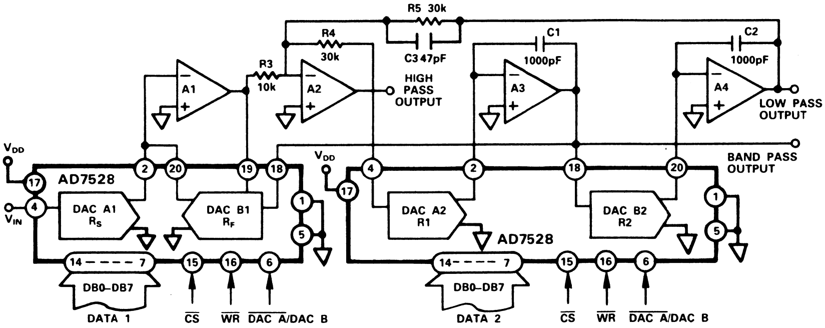


Figure 13. Digitally Programmable Window Comparator (Upper and Lower Limit Detector)

In the circuit of Figure 13 the AD7528 is used to implement a programmable window comparator. DACs A and B are loaded with the required upper and lower voltage limits for the test, respectively. If the test input is not within the programmed limits, the pass/fail output will indicate a fail (logic zero).

PROGRAMMABLE STATE VARIABLE FILTER



CIRCUIT EQUATIONS

$$C_1 = C_2,\ R_1 = R_2,\ R_4 = R_5$$

$$f_C = \frac{1}{2\pi R_1 C_1}$$

$$Q = \frac{R_3}{R_4} \cdot \frac{R_F}{R_{FBB1}}$$

$$A_O = -\frac{R_F}{R_S}$$

Note:
DAC equivalent resistance equals

$$\frac{256 \times (\text{DAC Ladder resistance})}{\text{DAC Digital Code}}$$

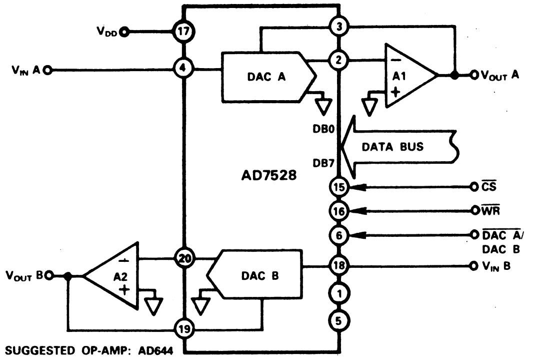
Figure 14. Digitally Controlled State Variable Filter

In this state variable or universal filter configuration (Figure 14) DACs A1 and B1 control the gain and Q of the filter characteristic while DACs A2 and B2 control the cut-off frequency, fc. DACs A2 and B2 must track accurately for the simple expression for fc to hold. This is readily accomplished by the AD7528. Op amps are 2 × AD644. C3 compensates for the effects of op amp gain-bandwidth limitations.

The filter provides low pass, high pass and band pass outputs and is ideally suited for applications where microprocessor control of filter parameters is required, e.g., equalizer, tone controls, etc.

Programmable range for component values shown is $f_c = 0$ to 15kHz and $Q = 0.3$ to 4.5.

DIGITALLY CONTROLLED DUAL TELEPHONE ATTENUATOR



In this configuration the AD7528 functions as a 2-channel digitally controlled attenuator. Ideal for stereo audio and telephone signal level control applications. Table 4 gives input codes vs. attenuation for a 0 to 15.5dB range.

$$\text{Input Code} = 256 \times 10\ \exp\left(-\frac{\text{Attenuation, dB}}{20}\right)$$

Figure 15. Digitally Controlled Dual Telephone Attenuator

Attn. dB	DAC Input Code	Code In Decimal	Attn. dB	DAC Input Code	Code In Decimal
0	1 1 1 1 1 1 1 1	255	8.0	0 1 1 0 0 1 1 0	102
0.5	1 1 1 1 0 0 1 0	242	8.5	0 1 1 0 0 0 0 0	96
1.0	1 1 1 0 0 1 0 0	228	9.0	0 1 0 1 1 0 1 1	91
1.5	1 1 0 1 0 1 1 1	215	9.5	0 1 0 1 0 1 1 0	86
2.0	1 1 0 0 1 0 1 1	203	10.0	0 1 0 1 0 0 0 1	81
2.5	1 1 0 0 0 0 0 0	192	10.5	0 1 0 0 1 1 0 0	76
3.0	1 0 1 1 0 1 0 1	181	11.0	0 1 0 0 1 0 0 0	72
3.5	1 0 1 0 1 0 1 1	171	11.5	0 1 0 0 0 1 0 0	68
4.0	1 0 1 0 0 0 1 0	162	12.0	0 1 0 0 0 0 0 0	64
4.5	1 0 0 1 1 0 0 0	152	12.5	0 0 1 1 1 1 0 1	61
5.0	1 0 0 1 0 0 0 0	144	13.0	0 0 1 1 1 0 0 1	57
5.5	1 0 0 0 1 0 0 0	136	13.5	0 0 1 1 0 1 1 0	54
6.0	1 0 0 0 0 0 0 0	128	14.0	0 0 1 1 0 0 1 1	51
6.5	0 1 1 1 1 0 0 1	121	14.5	0 0 1 1 0 0 0 0	48
7.0	0 1 1 1 0 0 1 0	114	15.0	0 0 1 0 1 1 1 0	46
7.5	0 1 1 0 1 1 0 0	108	15.5	0 0 1 0 1 0 1 1	43

Table 4. Attenuation vs. DAC A, DAC B Code for the Circuit of Figure 15

For further applications information the reader is referred to Analog Devices Application Note on the AD7528.

ANALOG DEVICES

CMOS 10- & 12-Bit Monolithic Multiplying D/A Converters

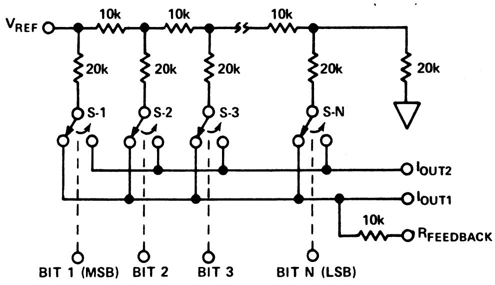
AD7530, AD7531

FEATURES

AD7530: 10-Bit Resolution
AD7531: 12-Bit Resolution
8-, 9- and 10-Bit Linearity
DTL/TTL/CMOS Compatible
Nonlinearity Tempco: 2ppm of FSR/°C
Low Power Dissipation: 20mW
Current Settling Time: 500ns
Feedthrough Error: 10mV p-p @ 50kHz
Low Cost

Note: AD7533 is recommended for new 10-bit designs. AD7541, AD7542 or AD7543 is recommended for new 12-bit designs.

AD7530, AD7531 FUNCTIONAL BLOCK DIAGRAM



DIGITAL INPUTS (DTL/TTL/CMOS COMPATIBLE)

AD7530: N = 10
AD7531: N = 12
(Switches shown in "High" state)

GENERAL DESCRIPTION

The AD7530 (AD7531) is a low cost, monolithic 10-bit (12-bit) multiplying digital-to-analog converter packaged in a 16-pin (18-pin) DIP. The device uses advanced CMOS and thin film technologies providing up to 10-bit accuracy with DTL/TTL/CMOS compatibility.

The AD7530 (AD7531) operates from a +5V to +15V supply and dissipates only 20mW, including the ladder network.

Typical applications include: digital/analog multiplication, CRT character generation, programmable power supplies, digitally controlled gain circuits, etc.

PACKAGE IDENTIFICATION[1]

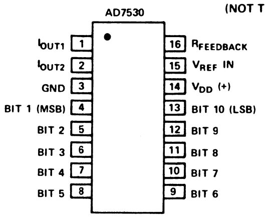
Suffix D: Ceramic DIP
AD7530: (D16A)
AD7531: (D18A)
Suffix N: Plastic DIP
AD7530: (N16A)
AD7531: (N16B)

ORDERING INFORMATION

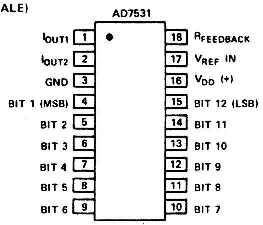
Nonlinearity	Temperature Range	
	0 to +70°C	−25°C to +85°C
0.2% (8-Bit)	AD7530JN	AD7530JD
	AD7531JN	AD7531JD
0.1% (9-Bit)	AD7530KN	AD7530KD
	AD7531KN	AD7531KD
0.05% (10-Bit)	AD7530LN	AD7530LD
	AD7531LN	AD7531LD

PIN CONFIGURATION

(NOT TO SCALE)



16-PIN DIP TOP VIEW



18-PIN DIP TOP VIEW

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[1] See Section 20 for package outline information.

SPECIFICATIONS (V_{DD} = +15, V_{REF} = +10V, T_A = +25°C unless otherwise noted)

PARAMETER		AD7530	AD7531	TEST CONDITIONS
DC ACCURACY (Note 1)				
Resolution		10 Bits	12 Bits	
Nonlinearity	AD7530J	0.2% of FSR max (8 Bit)	*	
	AD7530K	0.1% of FSR max (9 Bit)	*	
	AD7530L	0.05% of FSR max (10 Bit)	*	-10V < V_{REF} < +10V
Nonlinearity Tempco		2ppm of FSR/°C max	*	
Gain Error		0.3% of FSR typ	*	
Gain Error Tempco		10ppm of FSR/°C max	*	
Output Leakage Current (Either Output)		300nA max	*	Over specified temperature range.
Power Supply Rejection		50ppm of FSR/% typ	*	
AC ACCURACY				To 0.05%
Output Current Settling Time		500ns typ	*	All digital inputs low to high and high to low
Feedthrough Error		10mV p-p max	*	V_{REF} = 20V p-p, 50kHz. All digital inputs low
REFERENCE INPUT		±10V	*	
Input Range		±1mA	*	
Input Resistance		10kΩ typ	*	
ANALOG OUTPUT				
Output Current Range (Both Outputs)		±1mA	*	
Output Capacitance	I_{OUT1}	120pF typ	*	All digital inputs high
	I_{OUT2}	37pF typ	*	
	I_{OUT1}	37pF typ	*	All digital input low
	I_{OUT2}	120pF typ	*	
Output Noise (Both Outputs)		Equivalent to 10kΩ Johnson noise typ	*	
DIGITAL INPUTS (Note 2)				
Low State Threshold		0.8V max	*	Over specified temperature range
High State Threshold		2.4V min	*	Over specified temperature range
Input Current (low to high state)		1µA typ	*	
Input Coding		Binary	*	See Tables 1 & 2
POWER REQUIREMENTS				
Power Supply Voltage Range		+5V to +15V	*	
I_{DD}		5nA typ	*	All digital inputs at GND
		2mA max	*	All digital inputs high or low
Total Dissipation		20mW typ	*	

NOTES:

[1] Full scale range (FSR) is 10V for unipolar mode and ±10V for bipolar mode.

[2] Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.

*Same specifications as for AD7530.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

V_{DD} (to Gnd)	+17V
V_{REF} (to Gnd)	±25V
Digital Input Voltage Range	V_{DD} to Gnd
Voltage at Pin 1, Pin 2	−100mV to V_{DD}
Power Dissipation (package) up to +75°C	450mW
Operating Temperature	
JN, KN, LN Versions	0 to +75°C
JD, KD, LD Versions	−25°C to +85°C
Storage Temperature	−65°C to +150°C

CAUTION:

1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF}.
2. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

APPLICATIONS

UNIPOLAR BINARY OPERATION

Figure 1 shows the circuit connections required for unipolar operation. Since V_{REF} can assume either positive or negative values, the circuit is also capable of 2-quadrant multiplication. The input code/output range table for unipolar binary operation is shown in Table 1. Protection Schottky shown is not required when using TRI-FET output amplifiers such as the AD542 or AD544.

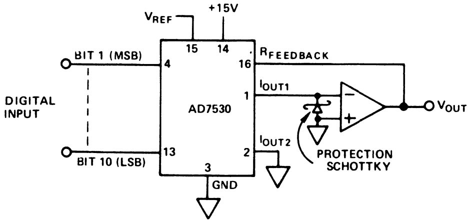


Figure 1. Unipolar Binary Operation (2-Quadrant Multiplication)

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}\ (1 - 2^{-10})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}\ (1/2 + 2^{-10})$
1 0 0 0 0 0 0 0 0 0	$\frac{-V_{REF}}{2}$
0 1 1 1 1 1 1 1 1 1	$-V_{REF}\ (1/2 - 2^{-10})$
0 0 0 0 0 0 0 0 0 1	$-V_{REF}\ (2^{-10})$
0 0 0 0 0 0 0 0 0 0	0

NOTE: 1 LSB = $2^{-10}\ V_{REF}$

Table 1. Code Table – Unipolar Binary Operation

BIPOLAR (OFFSET BINARY) OPERATION

Figure 2 illustrates the AD7530 connected for bipolar operation. Since the digital input can accept bipolar numbers and V_{REF} can accept a bipolar analog input, the circuit can perform a 4-quadrant multiplying function. Input coding is offset binary (modified 2's complement) as shown in Table 2.

When a switch's control input is a Logical "1", that switch's current is steered to I_{OUT1}, forcing the output of amplifier #1 to

$$V_{OUT} = -(I_{OUT1})\ (10k)$$

where 10k is the value of the feedback resistor.

A Logical "0" on the control input steers the switch's current to I_{OUT2}, which is terminated into the summing junction of amplifier #2. Resistors R1 and R2 need not track the internal R-2R circuitry; however, they should closely match each other to insure that the voltage at amplifer #2's output will force a current into R2 which is equal in magnitude but opposite in polarity to the current at I_{OUT2}. This creates a push-pull effect which halves the resolution but doubles the output range for changes in the digital input.

With the MSB a Logic "1" and all other bits a Logic "0", a 1/2 LSB difference current exists between I_{OUT1} and I_{OUT2}, creating an offset of 1/2 LSB. To shift the transfer curve to zero, resistor R-9 is used to sum 1/2 LSB of current into the I_{OUT2} terminal. Protection Schottky is not required if using TRIFET output amplifiers such as the AD542 or AD544.

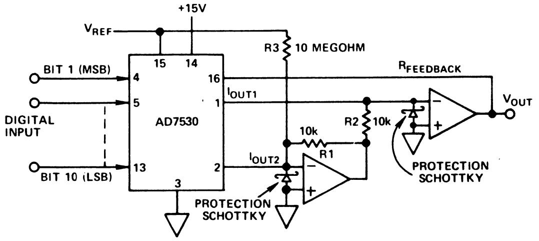


Figure 2. Bipolar Operation (4-Quadrant Multiplication)

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}\ (1 - 2^{-9})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}\ (2^{-9})$
1 0 0 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1 1 1	$V_{REF}\ (2^{-9})$
0 0 0 0 0 0 0 0 0 1	$V_{REF}\ (1 - 2^{-9})$
0 0 0 0 0 0 0 0 0 0	V_{REF}

NOTE: 1 LSB = $2^{-9}\ V_{REF}$

Table 2. Code Table – Bipolar (Offset Binary) Operation

TERMINOLOGY

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of (2^{-n}) (V_{REF}). A bipolar converter of n bits has a resolution of $[2^{-(n-1)}]$ $[V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the input voltage.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from I_{OUT1} and I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

ANALOG DEVICES

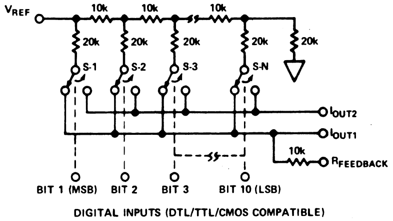
CMOS
Low Cost 10-Bit Multiplying DAC

AD7533

FEATURES
- Lowest Cost 10-Bit DAC
- Low Cost AD7520 Replacement
- Linearity: 1/2, 1 or 2LSB
- Low Power Dissipation
- Full Four-Quadrant Multiplying DAC
- CMOS/TTL Direct Interface
- Latch Free (Protection Schottky not Required)
- End-Point Linearity

APPLICATIONS
- Digitally Controlled Attenuators
- Programmable Gain Amplifiers
- Function Generation
- Linear Automatic Gain Control

AD7533 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION
The AD7533 is a low cost 10-bit 4-quadrant multiplying DAC manufactured using an advanced thin-film-on-monolithic-CMOS wafer fabrication process.

Pin and function equivalent to the industry standard AD7520, the AD7533 is recommended as a lower cost alternative for old AD7520 sockets or new 10-bit DAC designs.

AD7533 application flexibility is demonstrated by its ability to interface to TTL or CMOS, operate on +5V to +15V power, and provide proper binary scaling for reference inputs of either positive or negative polarity.

PACKAGE IDENTIFICATION[1]
Suffix D: Ceramic DIP – (D16B)
Suffix N: Plastic DIP – (N16B)

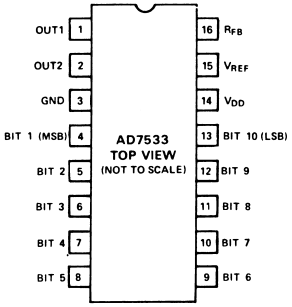
[1] See Section 20 for package outline information.

ORDERING INFORMATION

Nonlinearity	Temperature Range		
	Commercial 0 to +70°C	Industrial -25°C to +85°C	Military -55°C to +125°C
±0.2%	AD7533JN	AD7533AD AD7533AD/883B[1]	AD7533SD AD7533SD/883B[1]
±0.1%	AD7533KN	AD7533BD AD7533BD/883B[1]	AD7533TD AD7533TD/883B[1]
±0.05%	AD7533LN	AD7533CD AD7533CD/883B[1]	AD7533UD AD7533UD/883B[1]

[1] 100% screened to MIL-STD-883, method 5004, para. 3.1.1 through 3.1.12 for Class B device.

PIN CONFIGURATION



SPECIFICATIONS (V_{DD} = +15V; V_{OUT1} = V_{OUT2} = 0V; V_{REF} = +10V unless otherwise noted)

PARAMETER	T_A = 25°C	T_A = Operating Range[1]	Test Conditions
STATIC ACCURACY			
Resolution	10 Bits	10 Bits	
Relative Accuracy[2,3]			
AD7533JN, AD, SD	±0.2% FSR max	±0.2% FSR max	
AD7533KN, BD, TD	±0.1% FSR max	±0.1% FSR max	
AD7533LN, CD, UD	±0.05% FSR max	±0.05% FSR max	
Gain Error[3,4,5]	±1.4% FS max	±1.5% FS max	Digital Inputs = V_{INH}
Supply Rejection[6]			
$\Delta Gain/\Delta V_{DD}$	0.005%/%	0.008%/%	Digital Inputs = V_{INH}; V_{DD} = +14V to +17V
Output Leakage Current			
I_{OUT1} (pin 1)	±50nA max	±200nA max	Digital Inputs = V_{INL}; V_{REF} = ±10V
I_{OUT2} (pin 2)	±50nA max	±200nA max	Digital Inputs = V_{INH}; V_{REF} = ±10V
DYNAMIC ACCURACY			
Output Current Settling Time	600ns max[7]	800ns[6]	To 0.05% FSR; R_{LOAD} = 100Ω; Digital Inputs = V_{INH} to V_{INL} or V_{INL} to V_{INH}
Feedthrough Error	±0.05% FSR max[6]	±0.1% FSR max[6]	Digital Inputs = V_{INL}; V_{REF} = ±10V, 100kHz sinewave.
REFERENCE INPUT			
Input Resistance (pin 15)	5kΩ min, 20kΩ max	5kΩ min, 20kΩ max[8]	
ANALOG OUTPUTS			
Output Capacitance			
C_{OUT1} (pin 1)	100pF max[6]	100pF max[6]	Digital Inputs = V_{INH}
C_{OUT2} (pin 2)	35pF max[6]	35pF max[6]	
C_{OUT1} (pin 1)	35pF max[6]	35pF max[6]	Digital Inputs = V_{INL}
C_{OUT2} (pin 2)	100pF max[6]	100pF max[6]	
DIGITAL INPUTS			
Input High Voltage			
V_{INH}[3]	2.4V min	2.4V min	
Input Low Voltage			
V_{INL}[3]	0.8V max	0.8V max	
Input Leakage Current			
I_{IN}[3]	±1μA max	±1μA max	V_{IN} = 0V and V_{DD}
Input Capacitance			
C_{IN}	5pF max[6]	5pF max[6]	
POWER REQUIREMENTS			
V_{DD}	+15V ±10%	+15V ±10%	Rated Accuracy
V_{DD} Range[6]	+5V to +16V	+5V to +16V	Functionality with degraded performance
I_{DD}[3]	2mA max	2mA max	Digital Inputs = V_{INL} or V_{INH}

NOTES:

[1] Plastic (JN, KN, LN versions): 0 to +70°C
Commercial Ceramic (AD, BD, CD versions): -25°C to +85°C
Military Ceramic (SD, TD, UD versions): -55°C to +125°C

[2] "FSR" is Full Scale Range.

[3] Final electrical tests are: Relative Accuracy, Gain Error, Output Leakage Current, V_{INH}, V_{INL}, I_{IN} and I_{DD} at +25°C and +125°C (SD, TD, UD versions) or +25°C and +85°C (AD, BD, CD versions).

[4] Full Scale (FS) = $-(V_{REF})\left(\frac{1023}{1024}\right)$

[5] Max gain change from T_A = +25°C to T_{min} or T_{max} is ±0.1% FSR.

[6] Guaranteed, not tested.

[7] AC parameter, sample tested to ensure specification compliance.

[8] Absolute temperature coefficient is approximately -300ppm/°C.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS
(T_A = +25°C unless otherwise noted)

V_{DD} to GND	–0.3V, +17V
R_{FB} to GND	±25V
V_{REF} to GND	±25V
Digital Input Voltage Range	–0.3V to V_{DD}
Output Voltage (pin 1, pin 2)	–0.3V to V_{DD}
Power Dissipation (Package)	
Plastic (Suffix N)	
To +70°C	670mW
Derates above +70°C by	8.3mW/°C
Ceramic (Suffix D)	
To +70°C	450mW
Derates above +75°C by	6mW/°C
Operating Temperature Range	
Commercial (JN, KN, LN versions)	0 to +70°C
Industrial (AD, BD, CD versions)	–25°C to +85°C
Military (SD, TD, UD versions)	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

CAUTION:

1. ESD sensitive device. The digital control inputs are Zener protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts.
2. Do not apply voltages lower than ground or higher than V_{DD} to any pin except V_{REF} (pin 15) and R_{FB} (pin 16).

TERMINOLOGY

RELATIVE ACCURACY: Relative accuracy or end-point nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for ideal zero and full scale and is expressed in % or ppm of full-scale range or (sub) multiples of 1LSB.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of $(2^{-n})(V_{REF})$. A bipolar converter of n bits has a resolution of $[2^{-(n-1)}][V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN ERROR: Gain error or full-scale error is a measure of the output error between an ideal DAC and the actual device output.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from I_{OUT1} and I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

CIRCUIT DESCRIPTION

GENERAL CIRCUIT INFORMATION

The AD7533, a 10-bit multiplying D/A converter, consists of a highly stable thin film R-2R ladder and ten CMOS current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 1. An inverted R-2R ladder structure is used – that is, the binarily weighted currents are switched between the I_{OUT1} and I_{OUT2} bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

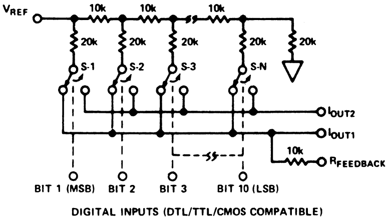


Figure 1. AD7533 Functional Diagram

One of the CMOS current switches is shown in Figure 2. The geometries of devices 1, 2 and 3 are optimized to make the digital control inputs DTL/TTL/CMOS compatible over the full military temperature range. The input stage drives two inverters (devices 4, 5, 6 and 7) which in turn drive the two output N-channels. The "ON" resistances of the switches are binarily sealed so the voltage drop across each switch is the same. For example, switch 1 of Figure 2 was designed for an "ON" resistance of 20 ohms, switch 2 for 40 ohms and so on. For a 10V reference input, the current through switch 1 is 0.5mA, the current through switch 2 is 0.25mA, and so on, thus maintaining a constant 10mV drop across each switch. It is essential that each switch voltage drop be equal if the binarily weighted current division property of the ladder is to be maintained.

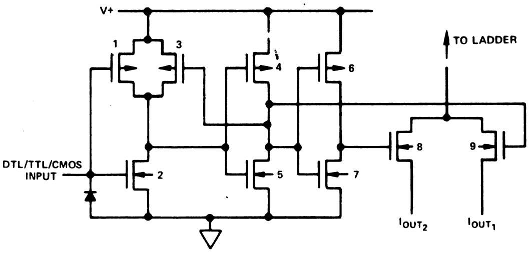


Figure 2. CMOS Switch

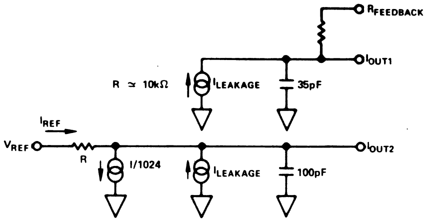


Figure 3. AD7533 Equivalent Circuit – All Digital Inputs Low

EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuits for all digital inputs high and all digital inputs low are shown in Figures 3 and 4. In Figure 3 with all digital inputs low, the reference current is switched to I_{OUT2}. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate while the $\frac{I}{1024}$ current source represents a constant 1-bit current drain through the termination resistor on the R-2R ladder. The "ON" capacitance of the output N channel switch is 100pF, as shown on the I_{OUT2} terminal. The "OFF" switch capacitance is 35pF, as shown on the I_{OUT1} terminal. Analysis of the circuit for all digital inputs high, as shown in Figure 4, is similar to Figure 3; however, the "ON" switches are now on terminal I_{OUT1}, hence the 100pF at that terminal.

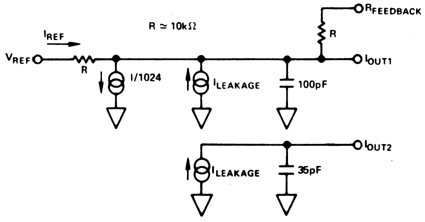
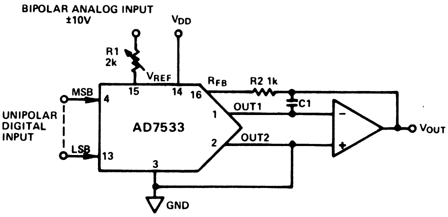


Figure 4. AD7533 Equivalent Circuit – All Digital Inputs High

OPERATION

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)



NOTES:
1. R1 AND R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
2. C1 PHASE COMPENSATION (5 – 15pF) MAY BE REQUIRED WHEN USING HIGH SPEED AMPLIFIER.

Figure 5. Unipolar Binary Operation (2-Quadrant Multiplication)

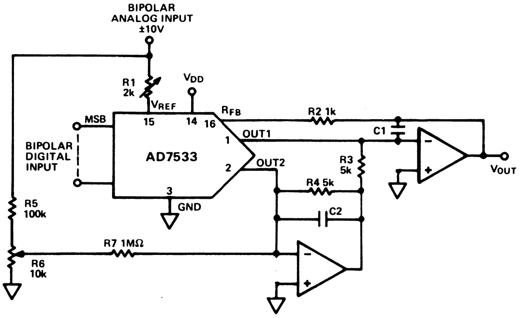
DIGITAL INPUT MSB LSB	NOMINAL ANALOG OUTPUT (V_{OUT} as shown in Figure 5)
1111111111	$-V_{REF}\left(\frac{1023}{1024}\right)$
1000000001	$-V_{REF}\left(\frac{513}{1024}\right)$
1000000000	$-V_{REF}\left(\frac{512}{1024}\right) = \frac{V_{REF}}{2}$
0111111111	$-V_{REF}\left(\frac{511}{1024}\right)$
0000000001	$-V_{REF}\left(\frac{1}{1024}\right)$
0000000000	$-V_{REF}\left(\frac{0}{1024}\right) = 0$

NOTES:

1. Nominal Full Scale for the circuit of Figure 5 is given by FS = $-V_{REF}\left(\frac{1023}{1024}\right)$
2. Nominal LSB magnitude for the circuit of Figure 5 is given by LSB = $V_{REF}\left(\frac{1}{1024}\right)$

Table 1. Unipolar Binary Code Table

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)



NOTES:
1. R3/R4 MATCH 0.05% OR BETTER.
2. R1, R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED
3. C1, C2 PHASE COMPENSATION (5 - 15pF) MAY BE REQUIRED WHEN USING HIGH SPEED AMPLIFIERS.

Figure 6. Bipolar Operation (4-Quadrant Multiplication)

DIGITAL INPUT MSB LSB	NOMINAL ANALOG OUTPUT (V_{OUT} as shown in Figure 6)
1111111111	$-V_{REF}\left(\frac{511}{512}\right)$
1000000001	$-V_{REF}\left(\frac{1}{512}\right)$
1000000000	0
0111111111	$+V_{REF}\left(\frac{1}{512}\right)$
0000000001	$+V_{REF}\left(\frac{511}{512}\right)$
0000000000	$+V_{REF}\left(\frac{512}{512}\right)$

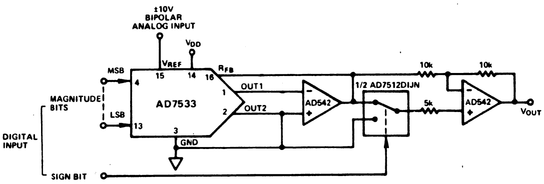
NOTES:

1. Nominal Full Scale Range for the circuit of Figure 6 is given by FSR = $V_{REF}\left(\frac{1023}{512}\right)$
2. Nominal LSB magnitude for the circuit of Figure 6 is given by LSB = $V_{REF}\left(\frac{1}{512}\right)$

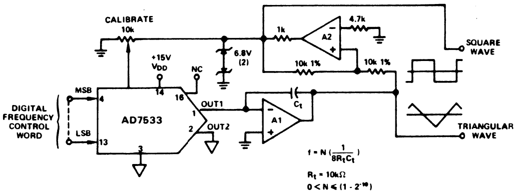
Table 2. Bipolar (Offset Binary) Code Table

APPLICATIONS

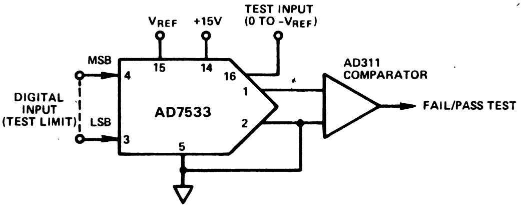
10-BIT AND SIGN MULTIPLYING DAC



PROGRAMMABLE FUNCTION GENERATOR

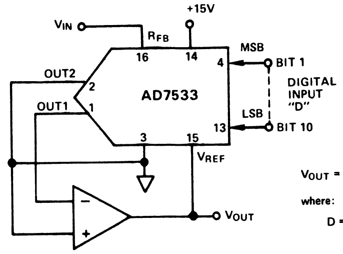


DIGITALLY PROGRAMMABLE LIMIT DETECTOR



APPLICATIONS (continued)

DIVIDER (DIGITALLY CONTROLLED GAIN)



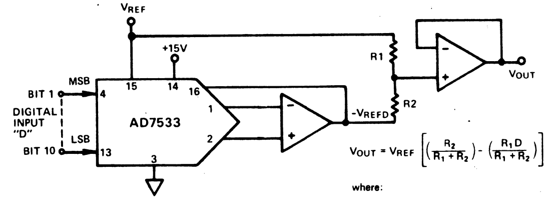
$$V_{OUT} = \frac{-V_{IN}}{D}$$

where:

$$D = \frac{BIT\ 1}{2^1} + \frac{BIT\ 2}{2^2} + \ldots \frac{BIT\ 10}{2^{10}}$$

$$0 < D \leq \frac{1023}{1024}$$

MODIFIED SCALE FACTOR AND OFFSET



$$V_{OUT} = V_{REF}\left[\left(\frac{R_2}{R_1 + R_2}\right) - \left(\frac{R_1 D}{R_1 + R_2}\right)\right]$$

where:

$$D = \frac{BIT\ 1}{2^1} + \frac{BIT\ 2}{2^2} + \ldots \frac{BIT\ 10}{2^{10}}$$

$$\left(0 \leq D \leq \frac{1023}{1024}\right)$$

ANALOG DEVICES

CMOS 12-Bit Monolithic Multiplying DAC

AD7541

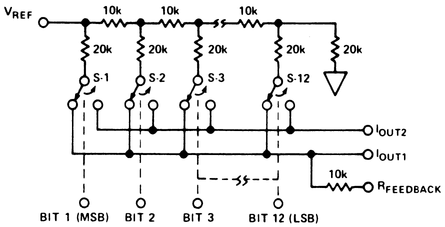
FEATURES

- Full Four Quadrant Multiplication
- 12-Bit Linearity (±1/2LSB)
- Pretrimmed Gain
- TTL/CMOS Compatible
- Low Power Consumption
- Low Feedthrough Error
- Low Cost

APPLICATIONS

- Digital/Synchro Conversion
- Programmable Amplifiers
- Ratiometric A/D Conversion
- Function Generation

AD7541 FUNCTIONAL BLOCK DIAGRAM



DIGITAL INPUTS (DTL/TTL/CMOS COMPATIBLE)
Logic: A switch is closed to I_{OUT1} for its digital input in a "HIGH" state.

GENERAL DESCRIPTION

The Analog Devices AD7541 is a low cost, high performance 12-bit monolithic multiplying digital-to-analog converter fabricated using advanced double-layer-metal CMOS technology and packaged in a standard 18-pin DIP.

Pin compatible with the AD7521, this new device uses laser wafer trimming to provide full 12-bit linearity and excellent absolute accuracy.

The inherently low power dissipation, coupled with the current switching R-2R ladder, ensures that the performance is maintained over the full temperature range.

ORDERING INFORMATION

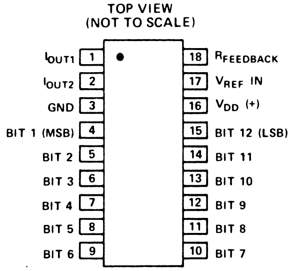
	Temperature Range and Package		
Nonlinearity	Plastic 0 to +70°C	Ceramic -25°C to +85°C	Ceramic -55°C to +125°C
0.02%	AD7541JN	AD7541AD	AD7541SD
0.01%	AD7541KN	AD7541BD	AD7541TD

PACKAGE IDENTIFICATION[1]

Suffix D: Ceramic DIP (D18B)
Suffix N: Plastic DIP (N18B)

[1] See Section 20 for package outline information.

PIN CONFIGURATION



SPECIFICATIONS (V_{DD} = 15V, V_{REF} = +10V unless otherwise noted)

PARAMETER	T_A = +25°C	T_A = min-max	TEST CONDITION
STATIC ACCURACY			
Resolution	12 Bits min	12 Bits min	V_{OUT1} = V_{OUT2} = 0V
Nonlinearity			
AD7541JN, AD7541AD, AD7541SD[1]	±1LSB max	±1LSB max	
AD7541KN, AD7541BD, AD7541TD[2]	±1/2LSB max	±1/2LSB max	
Gain Error[3,4]	±12.5LSB max	±16.7LSB max	
Power Supply Rejection	±0.01% per % max	±0.02% per % max	V_{DD} = 14.5V – 15.5V
Output Leakage Current	±50nA max	±200nA max	V_{REF} = ±10V
DYNAMIC PERFORMANCE			
Output Current Settling Time[5]	1μs max	1μs max	To ±1/2LSB of Full Scale Range
Feedthrough Error[5]	1mV p-p max	1mV p-p max	V_{REF} = 20V p-p @ 10kHz
REFERENCE INPUT			
Input Resistance	5kΩ min, 20kΩ max	5kΩ min, 20kΩ max	
DIGITAL INPUTS			
V_{INH}	2.4V min	2.4V min	
V_{INL}	0.8V max	0.8V max	
Input Leakage Current	±1μA max	±1μA max	V_{IN} = 0 or 15V
Input Capacitance[5]	8pF max	8pF max	
Input Coding	Binary or Offset Binary (See Applications)		
ANALOG OUTPUTS			
Output Capacitance[5]			
C_{OUT1}	200pF max	200pF max	Digital Inputs = V_{INH}
C_{OUT2}	60pF max	60pF max	
C_{OUT1}	60pF max	60pF max	Digital Inputs = V_{INL}
C_{OUT2}	200pF max	200pF max	
POWER REQUIREMENTS			
V_{DD} Range	+5V min, +16V max	+5V min, +16V max	Accuracy is not guaranteed over this range.
I_{DD}	2mA max	2mA max	Digital Inputs = V_{INH} or V_{INL}

NOTES

[1] J, A and S versions are monotonic to 11 bits.

[2] K, B and T versions are monotonic to 12 bits.

[3] Using internal feedback resistor.

[4] Max gain change from +25°C to T_{min} or T_{max} is ±4.2LSB max.

[5] Guaranteed by design, not subject to test.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

V_{DD} (to GND)	+17V
V_{REF} (to GND)	±25V
Digital Input Voltage Range	V_{DD} to GND
Output Voltage (Pin 1, Pin 2)	–0.3V to V_{DD}
Power Dissipation (Package)	
Up to +75°C	450mW
Derate above +75°C by	6mW/°C
Operating Temperature	
JN, KN Versions	0 to +70°C
AD, BD Versions	–25°C to +85°C
SD, TD Versions	–55°C to +125°C
Storage Temperature	–65°C to +150°C

CAUTION

1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF}.
2. The digital control inputs are zener protected; however permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused inputs in conductive foam at all times.

SPECIFICATION DEFINITIONS

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of $(2^{-n})(V_{REF})$. A bipolar converter of n bits has a resolution of $[2^{-(n-1)}][V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the input voltage.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from I_{OUT1} and I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

TYPICAL PERFORMANCE CHARACTERISTICS

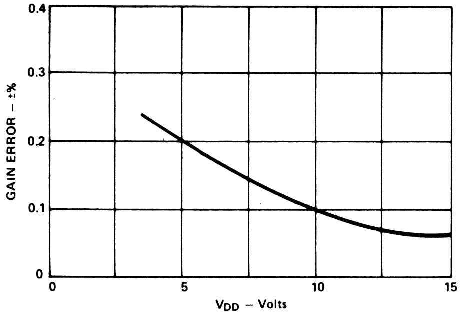


Figure 1. Gain Error vs. Supply Voltage

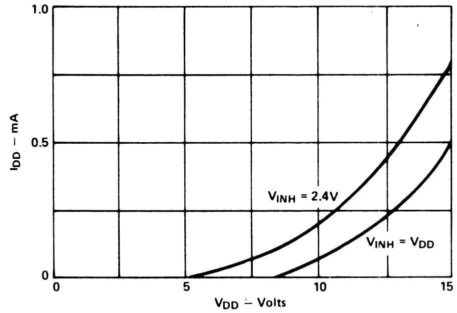


Figure 2. Supply Current vs. Supply Voltage

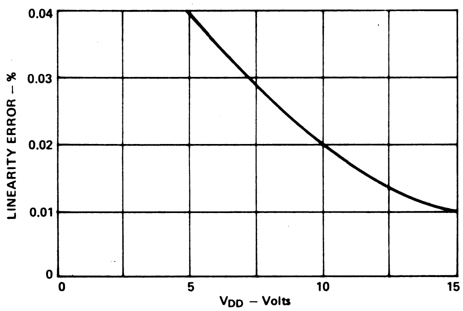


Figure 3. Linearity Error vs. Supply Voltage

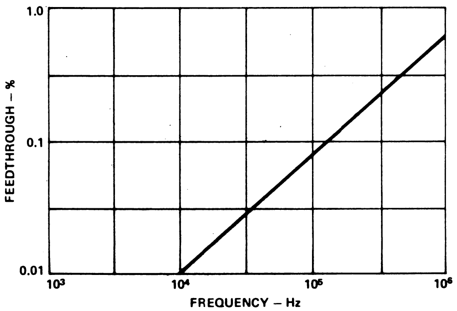


Figure 4. Feedthrough Error vs. Frequency

APPLICATION HINTS

Linearity depends upon the potential of I_{OUT1} and I_{OUT2} (pin 1 and pin 2) being exactly equal to GND (pin 3) and the output amplifiers non-inverting (+) input. Careful PC board layout and adjustment and selection of the amplifiers offset voltage and bias current is necessary.

The input structures of some high speed operational amplifiers can attempt to draw substantial current during switch-on. Schottky diodes should be used in these circumstances to prevent the absolute maximum rating for V_{OUT1} and V_{OUT2} being exceeded.

The power supply should be carefully checked for noise, which would affect performance, and overshoot which could damage the device.

Unused digital inputs must always be grounded or taken to V_{DD} to ensure correct operation. Particular care should be taken when digital inputs are routed to another PC card. It is recommended that inputs open-circuited when PC cards are disconnected be taken to V_{DD} or GND via high value (1MΩ) resistors to prevent the accumulation of static charges.

CIRCUIT DESCRIPTION

GENERAL CIRCUIT INFORMATION

The AD7541, a 12-bit multiplying D/A converter, consists of a highly stable thin film R-2R ladder and twelve CMOS current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 5. An inverted R-2R ladder structure is used – that is, the binarily weighted currents are switched between the I_{OUT1} and I_{OUT2} bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

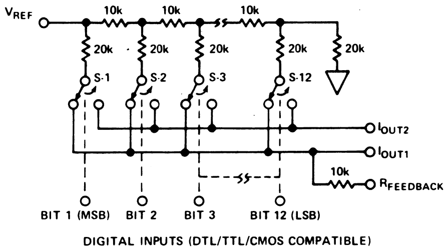


Figure 5. AD7541 Functional Diagram (Inputs "HIGH")

One of the CMOS current switches is shown in Figure 6. The geometries of devices 1, 2 and 3 are optimized to make the digital control inputs DTL/TTL/CMOS compatible over the full military temperature range. The input stage drives two inverters (devices 4, 5, 6 and 7) which in turn drive the two output N-channels. The "ON" resistances of the switches are binarily scaled so the voltage drop across each switch is the same. For example, switch 1 of Figure 6 was designed for an "ON" resistance of 10 ohms, switch 2 of 20 ohms and so on. For a 10V reference input, the current through switch 1 is 0.5mA, the current through switch 2 is 0.25mA, and so on, thus maintaining a constant 5mV drop across each switch. It is essential that each switch voltage drop be equal if the binarily weighted current division property of the ladder is to be maintained.

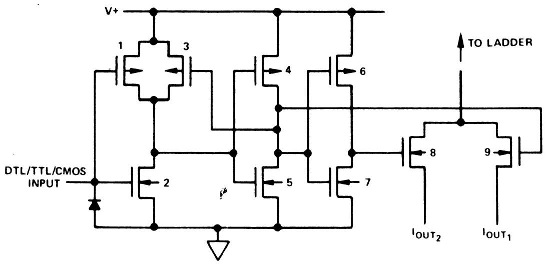


Figure 6. CMOS Switch

EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuits for all digital inputs high and all digital inputs low are shown in Figures 7 and 8. In Figure 7 with all digital inputs low, the reference current is switched to I_{OUT2}. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate while the 1/4096 current source represents a constant 1-bit current drain through the termination resistor on the R-2R ladder. The "ON" capacitance of the output N-channel switch is 200pF, as shown on the I_{OUT2} terminal. Analysis of the circuit for all digital inputs high, as shown in Figure 8, is similar to Figure 7; however, the "ON" switches are now on terminal I_{OUT1}, hence the 200pF at that terminal.

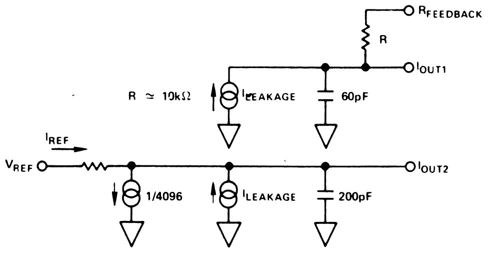


Figure 7. AD7541 Equivalent Circuit – All Digital Inputs Low

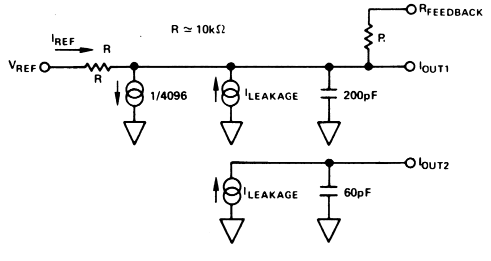


Figure 8. AD7541 Equivalent Circuit – All Digital Inputs High

DYNAMIC PERFORMANCE

OUTPUT IMPEDANCE

The preceding circuit analysis shows that the output capacitance is dependent upon the digital code, as is the output resistance. Looking back into I_{OUT1} the resistance seen is anything between 10kΩ ($R_{FEEDBACK}$ alone) and 5kΩ (R_{FB} in parallel with the 10kΩ network resistance).

This variation affects both static accuracy and dynamic performance. The effect on static accuracy is further considered in the Applications section under Output Amplifier Considerations. The dynamic performance of the AD7541 will depend upon the gain and phase stability of the output amplifier, together with the optimum choice of PC board layout and decoupling components.

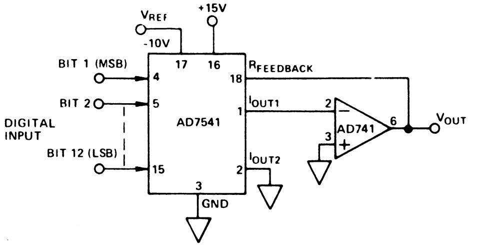


Figure 9. DAC Circuit Using AD741K

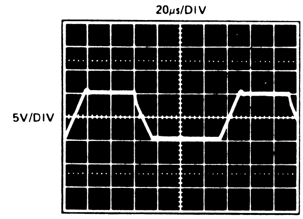


Figure 10. Output Waveform

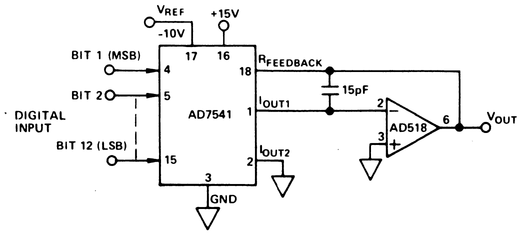


Figure 11. DAC Circuit Using AD518K

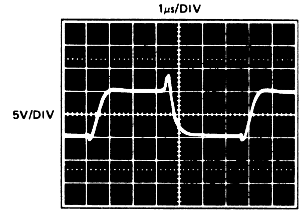


Figure 12. Output Waveform

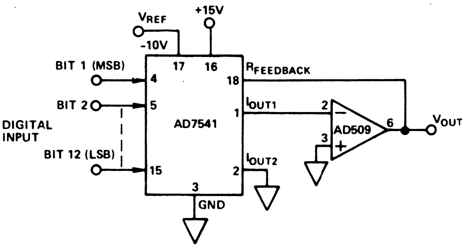


Figure 13. DAC Circuit Using AD509K

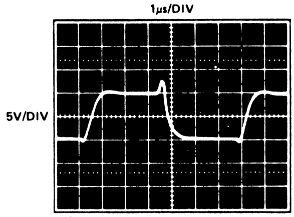


Figure 14. Output Waveform

The circuits and waveforms shown in Figures 9 to 14 are representative of the three principal types of output amplifiers. A general purpose low drift (AD741K), a high speed low cost (AD518), and a fast settling unit (AD509).

Points to remember when applying high speed amplifiers include:

1. Protection diodes as shown in Figures 15 and 16.
2. Phase compensation for the DAC's output capacitance.
3. Power supply decoupling and correct load earthing.

APPLICATIONS

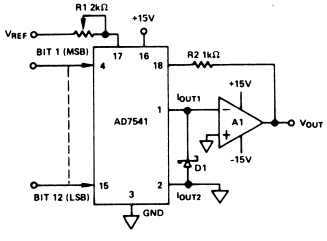


Figure 15. Unipolar Binary Operation

UNIPOLAR BINARY OPERATION

The connections required for unipolar digital binary operation are shown above. V_{REF} may be positive or negative so 2-quadrant multiplication may be performed. Schottky diode D1 (HP 5082-2811 or equivalent) prevents I_{OUT1} from negative excursions which could damage the device. This precaution is only necessary with certain high speed amplifiers. The diodes are not required when using TRI-FET amplifiers such as the AD542 or AD544.

BIPOLAR (4-QUADRANT) BINARY OPERATION

The digital input is offset binary coded and multiplies V_{REF} according to Table 2. Resistors R3 and R4 should be equal within 0.1% at all temperatures, but need not track the resistors within the AD7541. D1 and D2 perform the same function as in Figure 15. Network R5, R6, R7 sum 1/2LSB of current into I_{OUT2} to ensure correct coding at zero.

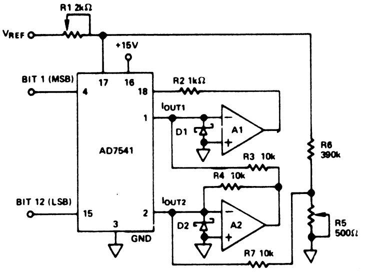


Figure 16. Bipolar (4-Quadrant) Binary Operation

R1 can be adjusted to produce the outputs shown in Table 1. However, it is recommended that when the application permits it, R1 and R2 be omitted. The maximum gain error in this condition is 0.3% of full scale. The offset voltage of amplifier A1 should be adjusted to less than 0.5mV over the temperature range.

DIGITAL INPUT	NOMINAL ANALOG OUTPUT
111111111111	$-0.99975\ V_{REF}$
100000000000	$-0.50000\ V_{REF}$
011111111111	$-0.49975\ V_{REF}$
000000000000	0

Table 1. Code Table for Circuit of Figure 15.

DIGITAL INPUT	NOMINAL ANALOG OUTPUT
111111111111	$-0.99951\ V_{REF}$
100000000001	$-0.00049\ V_{REF}$
100000000000	0
010000000000	$+0.50000\ V_{REF}$
000000000000	$+1.00000\ V_{REF}$

Table 2. Code Table for Circuit of Figure 16.

Amplifiers A1 and A2 should be adjusted to an input offset of less than 0.1mV and should be better than 0.5mV over the temperature range. With V_{REF} set to approximately 10V, R5 should be adjusted so that with code 10000000000 V_{OUT} = 0V ±0.2mV. R1 should be adjusted so that with code 000000000000 $V_{OUT} = V_{REF}$.

As with the unipolar circuit R1 and R2 can be omitted, with a resulting maximum gain error of 0.3% of full scale. R5 may be replaced by a 100Ω fixed resistor. The maximum zero error if this is done is 0.015% of F.S.R.

OUTPUT AMPLIFIER CONSIDERATIONS

It has already been pointed out that the DAC output resistance varies with the digital code. The effect this has on static accuracy will now be considered.

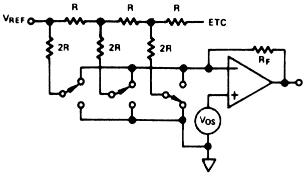


Figure 17.

$$\text{The error voltage} = V_{OS}\left(1 + \frac{R_F}{R_O}\right)$$

R_O is a function of the digital code.
$R_O \cong 10\text{k}\Omega$ for any more than 4-bits Logic 1.
$R_O \cong 30\text{k}\Omega$ for any single bit Logic 1.

The gain for offset, therefore, changes as follows:

$$\text{At code } 001111111111 \; V_{ERROR1} = V_{OS}\left(1 + \frac{10k}{10k}\right) = 2\,V_{OS}$$

$$\text{At code } 010000000000 \; V_{ERROR2} = V_{OS}\left(1 + \frac{10k}{30k}\right) = \frac{4}{3}\,V_{OS}$$

The error difference is therefore $\frac{2}{3}\,V_{OS}$

Since, for a 12-bit resolution DAC, one LSB has a weight (for $V_{REF} = +10V$) of 2.5mV, it is clearly important that V_{OS} be nulled, either using the amplifiers nulling facility or an external network.

It is important to realize that an offset can be caused by including the usual bias current compensation resistor in the amplifiers non-inverting input terminal. This should not be included. Instead the amplifier should have a bias current which is low over the temperature range of interest, and should certainly not exceed 75nA.

ANALOG/DIGITAL DIVISION

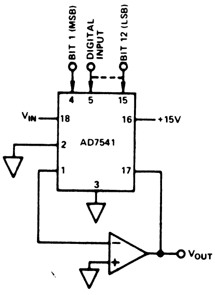


Figure 18. Analog/Digital Divider

With the AD7541 connected in its normal multiplying configuration as shown in Figure 15, the transfer function is

$$V_O = -V_{IN}\left(\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \ldots\ldots \frac{A_{12}}{A^{12}}\right)$$

where the coefficients A_X assume a value of 1 for an ON bit and 0 for an OFF bit.

By connecting the DAC in the feedback of an operational amplifier, as shown in Figure 18, the transfer function becomes

$$V_O = \left(\frac{-V_{IN}}{\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \ldots\ldots \frac{A_{12}}{A^{12}}}\right)$$

This is division of an analog variable (V_{IN}) by a digital word. With all bits off, the amplifier saturates to its bound, since division by zero is not defined. With the LSB (Bit 12) ON, the gain is 4096. With all bits ON, the gain is 1 (±1LSB).

DIGITAL/SYNCHRO CONVERTER

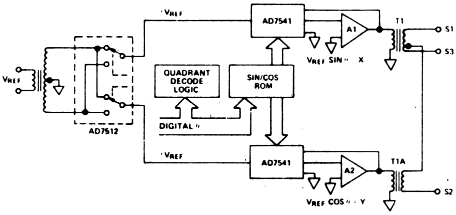


Figure 19. 14-Bit Digital to Synchro Converter

The low cost and high accuracy available from the AD7541, together with its bipolar multiplying capability is exploited fully in the circuit of Figure 19. V_{REF} is commonly 400Hz but by replacing the transformers with dc coupled circuits coordinate transformation may be performed.

The SIN/COS ROM is readily available at low cost and the AD7512 switch enables greater resolution to be obtained.

Resolver-to-synchro transformation is performed by the Scott connected pair T1 and T1A. The power available to the load connected to S1, S2 and S3 is determined by the amplifiers A1 and A2. A particular advantage of the circuit shown in Figure 19 is that it is invariant with respect to θ, and may be used to directly drive equipment such as CRT displays.

ANALOG DEVICES

CMOS 12-Bit Monolithic Multiplying DAC

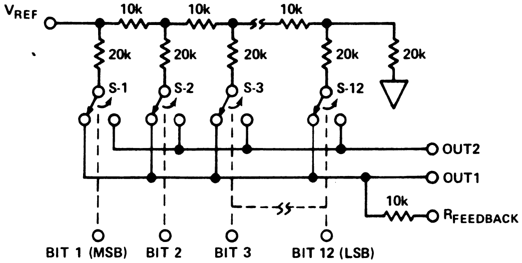
AD7541A

PRELIMINARY

FEATURES

Full Four Quadrant Multiplication
12-Bit Linearity (End-Point)
± 1LSB Gain Error
All Parts Guaranteed Monotonic
TTL/CMOS Compatible
Low Cost
Protection Schottky not Required

AD7541A FUNCTIONAL BLOCK DIAGRAM



DIGITAL INPUTS (DTL/TTL/CMOS COMPATIBLE)
Logic: A switch is closed to I_{OUT1} for its digital input in a "HIGH" state.

GENERAL DESCRIPTION

The Analog Devices' AD7541A is a low cost, high performance 12-bit monolithic multiplying digital to analog converter. It is fabricated using advanced, low noise, thin film on CMOS technology and packaged in a standard 18-pin DIP.

The AD7541A is functionally and pin compatible with the industry standard AD7541 devices and offers improved specifications and performance. The improved design ensures that the device is latch-up free so no output Schottky protection diodes are required.

This new device uses laser wafer trimming to provide full 12-bit end-point linearity with several new high performance grades providing 1/4LSB maximum nonlinearity and 1/2LSB maximum differential nonlinearity.

ORDERING INFORMATION

Relative Accuracy T_{min} to T_{max}	Gain Error T_A = +25°C	Temperature Range		
		0 to +70°C	−25°C to +85°C[1]	−55°C to +125°C[1]
± 1LSB	± 6LSB	AD7541AJN	AD7541AAQ	AD7541ASD
± 1/2LSB	± 4LSB	AD7541AKN	AD7541ABQ	AD7541ATD
± 1/2LSB	± 1LSB	–	–	AD7541AGTD
± 1/4LSB	± 4LSB	AD7541ALN	AD7541ACQ	–
± 1/4LSB	± 1LSB	AD7541AGLN	AD7541AGCQ	–

NOTES:
[1] 883B version is available, to order ADD "/883B" to part number.

PACKAGE IDENTIFICATION[1]

Suffix "N" – Plastic DIP (N18B)
Suffix "Q" – Cerdip[2] (Q18A)
Suffix "D" – Ceramic DIP (D18B)

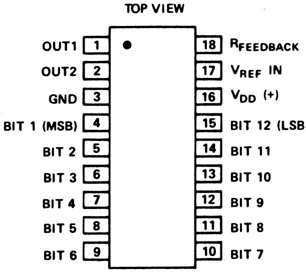
PRODUCT HIGHLIGHTS

Compatability: The AD7541A can be used as a direct replacement for any AD7541–type device. As with the Analog Devices AD7541 the digital inputs are TTL/CMOS compatible and have been designed to have a ± 1μA maximum input current requirement so as not to load the driving circuitry.

Improvements: The AD7541A offers the following improved specifications over the AD7541:

1. Gain Error for all grades has been reduced and a special G grade version with a maximum gain error of ± 1LSB is available to eliminate the need for gain trimming.
2. Gain Error temperature coefficient has been reduced to 2ppm/°C typical and 6ppm/°C maximum.
3. Digital to analog charge injection energy for this new device is typically 20% less than the standard AD7541 part.
4. Latch-up proof.

PIN CONFIGURATION (NOT TO SCALE)



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[1] See Section 20 for package outline information.
[2] Analog Devices reserves the right to ship ceramic packages in lieu of Cerdip packages.

SPECIFICATIONS (V_{DD} = +15V, V_{REF} = +10V; V_{PIN1} = V_{PIN2} = 0V unless otherwise specified)

Parameter	Version	T_A = +25°C	T_A = T_{min}, T_{max}[1]	Units	Test Conditions/Comments
ACCURACY					
Resolution	All	12	12	Bits	
Relative Accuracy	J, A, S	±1	1	LSB max	±1LSB = 0.024%
	K, B, T, GT	±½	±½	LSB max	±½ = 0.012%
	L, C, GL, GC	±¼	±¼	LSB max	±¼ = 0.006%
Differential Nonlinearity	J, A, S	±1	±1	LSB max	All grades guaranteed monotonic.
	B, T, G, T	±½	±½	LSB max	T_{min} to T_{max}
	L, C, GL, GC	±½	±½	LSB max	
Gain Error	J, A, S	±6	±9	LSB max	Measured using internal R_{FB} and includes
	K, B, T	±4	±7	LSB max	effect of leakage current and gain T.C.
	L, C	±4	±6	LSB max	Gain error can be trimmed to zero.
	GL, GC, GT	±1	±4	LSB max	
Gain Temperature Coefficient[2]					
ΔGain/ΔTemperature	All	6	6	ppm/°C max	Typical value is 2ppm/°C.
Output Leakage Current					
OUT1 (Pin 1)	J, K, L, GL	±5	±10	nA max	All digital inputs = 0V.
	A, B, C, GC	±5	±10	nA max	
	S, T, GT	±5	±200	nA max	
OUT 2 (Pin 2)	J, K, L, GL	±5	±10	nA max	All digital inputs = V_{DD}.
	A, B, C, GC	±5	±10	nA max	
	S, T, GT	±5	±200	nA max	
REFERENCE INPUT					
Input Resistance (Pin 17 to GND)	All	7–18	7–18	kΩ min/max	Typical input resistance = 11kΩ. Typical input resistance temperature coefficient = −300ppm/°C.
DIGITAL INPUTS					
V_{IH} (Input HIGH Voltage)	All	2.4	2.4	V max	
V_{IL} (Input LOW Voltage)	All	0.8	0.8	V min	
I_{IN} (Input Current)	All	±1	±1	µA max	Logic inputs are MOS gates. I_{IN} typ (25°C) = 1nA.
C_{IN} (Input Capacitance)	All	8	8	pF max	V_{IN} = 0V
POWER SUPPLY					
V_{DD} Range	All	+5 to +16	+5 to +16	V min/V max	Accuracy is not guaranteed over this range.
I_{DD}	All	2	2	mA max	All digital inputs V_{IL} or V_{IN}.
		100	500	µA max	All digital inputs 0V or V_{DD}.

AC PERFORMANCE CHARACTERISTICS

These Characteristics are Included for Design Guidance Only and are not Subject to Test.
V_{DD} = +15V, V_{IN} = −10V except where stated, V_{PIN1} = V_{PIN2} = 0V, Output Amp is AD544 except where stated.

Parameter	Version[1]	T_A = +25°C	T_A = T_{min}, T_{max}[1]	Units	Test Conditions/Comments
PROPAGATION DELAY (From Digital Input Change to 90% of Final Analog Output)	All	100	–	ns typ	OUT 1 Load = 100Ω C_{EXT} = 13pF Digital Inputs = 0V to V_{DD} or V_{DD} to 0V.
DIGITAL TO ANALOG CHARGE INJECTION (Q.D.A.)	All	1000	–	nV-sec typ	V_{REF} = 0V. Measured using ADLH0032CG as output amplifier.
MULTIPLYING FEEDTHROUGH ERROR[3] (V_{REF} to OUT1)	All	1.0	1.0	mV p-p typ	V_{REF} = ± 10V, 10kHz sine wave.
OUTPUT CURRENT SETTLING TIME	All	1	–	µs typ	To 0.01% of full scale range. OUT1 load = 100Ω, C_{EXT} = 13pF. Digital inputs = 0V to V_{DD} or V_{DD} to 0V
POWER SUPPLY REJECTION					
ΔGain/ΔV_{DD}	All	±0.01%	±0.02%	%per%/max	ΔV_{DD} = ±5%
OUTPUT CAPACITANCE					
C_{OUT1} (Pin 1)	All	200	200	pF max	Digital Inputs
C_{OUT2} (Pin 2)	All	70	70	pF max	= V_{IH}
C_{OUT1} (Pin 1)	All	70	70	pF max	Digital Inputs
C_{OUT2} (Pin 2)	All	200	200	pF max	= V_{IL}
OUTPUT NOISE VOLTAGE DENSITY (10Hz–100kHz)	All	22	–	nV/$\sqrt{\text{Hz}}$ typ	Johnson noise for 11kΩ resistor is 13.5nV/$\sqrt{\text{Hz}}$.

NOTES

[1] Temperature range as follows: JN, KN, LN, GLN versions: 0 to +70°C
AQ, BQ, CQ, GCQ versions: −25°C to +85°C
ST, TD, GTD versions: −55°C to +125°C.

[2] Guaranteed by design but not production tested.

[3] To minimize feedthrough in the ceramic package (Suffix D) the user must ground the metal lid.

Specifications subject to change without notice.

ANALOG DEVICES

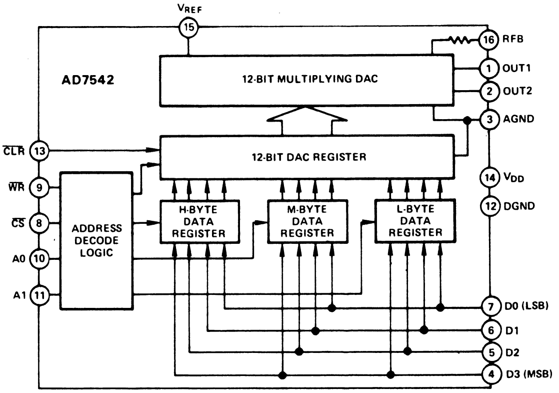
CMOS µP Compatible 12-Bit DAC

AD7542

FEATURES

- Resolution: 12 Bits
- Nonlinearity: ±1/2LSB T_{min} to T_{max}
- Low Gain Drift: 2ppm/°C typ, 5ppm/°C max
- Microprocessor Compatible
- Full 4-Quadrant Multiplication
- Low Multiplying Feedthrough
- Low Power Dissipation: 40mW max
- Low Cost
- Small Size: 16-Pin DIP
- Latch Free (Protection Schottky Not Required)

AD7542 FUNCTIONAL BLOCK DIAGRAM



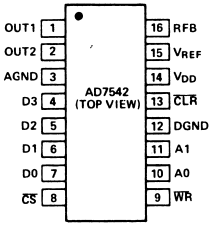
GENERAL DESCRIPTION

The AD7542 is a precision 12-bit CMOS multiplying DAC designed for direct interface to 4- or 8-bit microprocessors.

The functional diagram shows the AD7542 to consist of three 4-bit data registers, a 12-bit DAC register, address decoding logic and a 12-bit CMOS multiplying DAC. Data is loaded into the data registers in three 4-bit bytes, and subsequently transferred to the 12-bit DAC register. All data loading or data transfer operations are identical to the WRITE cycle of a static RAM. A clear input allows the DAC register to be easily reset to all zeros when powering up the device.

The AD7542 is manufactured using an advanced thin-film on monolithic CMOS fabrication process. Multiplying capability, low power dissipation, +5V operation, small size (16-pin DIP) and easy µP interface make the AD7542 ideal for many instrumentation, industrial control and avionics applications.

PIN CONFIGURATION



ORDERING INFORMATION

		Temperature Range and Package		
Relative Accuracy (T_{min} to T_{max})	Gain Error +25°C	Commercial (Plastic) 0 to +70°C	Industrial (Ceramic) -25°C to +85°C	Military (Ceramic) -55°C to +125°C
±1LSB	±12.3LSB	AD7542JN	AD7542AD AD7542AD/883B[1]	AD7542SD AD7542SD/883B[1]
±1/2LSB	±12.3LSB	AD7542KN	AD7542BD AD7542BD/883B[1]	AD7542TD AD7542TD/883B[1]
±1/2LSB	±1LSB	AD7542GKN	AD7542GBD AD7542GBD/883B[1]	AD7542GTD/ AD7542GTD/883B[1]

[1] 100% screened to MIL-STD-883, Method 5004, paragraph 3.1.1 through 3.1.12 for Class B device.

PACKAGE IDENTIFICATION[1]

Suffix D: Ceramic DIP – (D16B)
Suffix N: Plastic DIP – (N16B)

[1] See Section 20 for package outline information.

SPECIFICATIONS (V_{DD} = +5V, V_{REF} = +10V, V_{OUT1} = V_{OUT2} = 0V unless otherwise noted)

Parameter	Limit At T_A = +25°C	Limit At[1] T_A = 0, +70°C, -25°C & +85°C	Limit At[1] T_A = -55°C & +125°C	Units	Conditions/Comments
ACCURACY					
Resolution	12	12	12	Bits	
Relative Accuracy[2]					
JN, AD, SD Versions	±1	±1	±1	LSB max	
KN, BD, TD Versions	±1/2	±1/2	±1/2	LSB max	
GKN, GBD, GTD Versions	±1/2	±1/2	±1/2	LSB max	
Differential Nonlinearity[2]					
JN, AD, SD Versions	±2	±2	±2	LSB max	Monotonic to 11 bits from T_{min} to T_{max}
KN, BD, TD Versions	±1	±1	±1	LSB max	Monotonic to 12 bits from T_{min} to T_{max}
GKN, GBD, GTD Versions	±1	±1	±1	LSB max	Monotonic to 12 bits from T_{min} to T_{max}
Gain Error[2]					
JN, KN, AD, BD, SD, TD	±12.3	±13.5	±14.5	LSB max	Using internal RFB only (gain error can be
GKN, GBD, GTD	±1	±1	±2	LSB max	trimmed to zero using circuits of Figures 5 & 6)
Gain Temperature Coefficient					
ΔGain/ΔTemperature	5	5	5	ppm/°C max	Typical value is 2ppm/°C
Power Supply Rejection					
ΔGain/ΔV_{DD}	0.005	0.01	0.01	% per % max	V_{DD} = +4.75V to +5.25V
Output Leakage Current					
I_{OUT1} (Pin 4)	1	10	200	nA max	DAC Register loaded with all 0s
I_{OUT2} (Pin 5)	1	10	200	nA max	DAC Register loaded with all 1s
DYNAMIC PERFORMANCE					
Current Settling Time[3]	2.0	2.0	2.0	μs max	To 1/2LSB. OUT1 load = 100Ω. DAC output measured from falling edge of $\overline{WR}$.
Multiplying Feedthrough Error[3]	2.5	2.5	2.5	mV p-p max	V_{REF} = ±10V, 10kHz sine wave
REFERENCE INPUT					
Input Resistance (pin 15)	8/15/25	8/15/25	8/15/25	kΩ min/typ/max	
ANALOG OUTPUTS					
Output Capacitance					
C_{OUT1}[3]	75	75	75	pF max	DAC register loaded to 0000 0000 0000
C_{OUT1}[3]	260	260	260	pF max	DAC register loaded to 1111 1111 1111
C_{OUT2}[3]	75	75	75	pF max	DAC register loaded to 1111 1111 1111
C_{OUT2}[3]	260	260	260	pf max	DAC register loaded to 0000 0000 0000
LOGIC INPUTS					
V_{INH} (Logic HIGH Voltage)	+3.0	+3.0	+3.0	V min	
V_{INL} (Logic LOW Voltage)	+0.8	+0.8	+0.8	V max	
I_{IN}[4]	1	1	1	μA max	V_{IN} = 0V or V_{DD}
C_{IN} (Input Capacitance)[3]	8	8	8	pF max	
Input Coding	12-Bit Unipolar Binary or 12-Bit Offset Binary (see Figures 5 and 6). Data is loaded into data registers in 4-bit bytes.				
SWITCHING CHARACTERISTICS[5]	(See Figure 7)				
t_{WR}	120	220	220	ns min	t_{WR}: WRITE pulse width
t_{AWH}	50	65	65	ns min	t_{AWH}: Address-to-WRITE hold time
t_{CWH}	50	100	100	ns min	t_{CWH}: Chip select-to-WRITE hold time
t_{CLR}	200	300	300	ns min	t_{CLR}: Minimum CLEAR pulse width
Byte Loading					
t_{CWS}	60	130	130	ns min	t_{CWS}: Chip select-to-WRITE setup time
t_{AWS}	80	180	180	ns min	t_{AWS}: Address valid-to-WRITE setup time
t_{DS}	50	65	65	ns min	t_{DS}: Data setup time
t_{DH}	50	65	65	ns min	t_{DH}: Data hold time
DAC Loading					
t_{CWS}	60	150	150	ns min	t_{CWS}: Chip select-to-WRITE setup time
t_{AWS}	120	240	240	ns min	t_{AWS}: Address valid-to-WRITE setup time
POWER SUPPLY					
V_{DD} (Supply Voltage)	+5	+5	+5	V	±5% for specified performance
I_{DD} (Supply Current)	8	8	8	mA max	Digital Inputs = V_{INH} or V_{INL}

NOTES:

[1] Temperature Ranges as follows: AD7542JN, KN, GKN: 0 to +70°C
AD7542AD, BD, GBD: -25°C to +85°C
AD7542SD, TD, GTD: -55°C to +125°C

[2] See definitions on next page.

[3] Guaranteed but not tested.

[4] Logic inputs are MOS gates. Typical input current (+25°C) is less than 1nA.

[5] Sample tested at +25°C to ensure compliance.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND	0V, +7V
V_{DD} to DGND	0V, +7V
AGND to DGND	V_{DD}
DGND to AGND	V_{DD}
Digital Input Voltage to DGND (pins 4–11, 13)	−0.3V, +15.3V
V_{PIN1}, V_{PIN2} to AGND	−0.3V, +15V
V_{REF} to AGND	±25V
V_{RFB} to AGND	±25V
Power Dissipation (Package)	
Plastic (Suffix N)	
To +70°C	670mW
Derates above +70°C by	8.3mW/°C
Ceramic (Suffix D)	
To +75°C	450mW
Derates above +75°C by	6mW/°C
Operating Temperature Range	
Commercial Plastic (JN, KN, GKN versions)	0 to +70°C
Industrial Ceramic (AD, BD, GBD versions)	−25°C to +85°C
Military Ceramic (SD, TD, GTD versions)	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 secs)	+300°C

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION:

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

TERMINOLOGY

RELATIVE ACCURACY

Relative accuracy on endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale and is expressed in % of ppm of full scale range on (sub) multiples of 1LSB.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the difference between the *measured* change and the *ideal* 1LSB change between any two adjacent codes. A specified differential nonlinearity of ±1LSB max over the operating temperature range insures monotonicity.

GAIN ERROR

Gain is defined as the ratio of the DAC's Full Scale output to its reference input voltage. An *ideal* AD7542 would exhibit a gain of −4095/4096. Gain error is adjustable using external trims as shown in Figures 5 and 6.

OUTPUT LEAKAGE CURRENT

Current which appears at OUT1 with the DAC register loaded to all 0s or at OUT2 with the DAC register loaded to all 1s.

MULTIPLYING FEEDTHROUGH ERROR

AC error due to capacitive feedthrough from V_{REF} terminal to OUT1 with DAC register loaded to all 0s.

PIN	MNEMONIC	FUNCTION	PIN	MNEMONIC	FUNCTION
1	OUT1	DAC current output bus. Normally terminated at op amp virtual ground	7	D0	Data Input (LSB)
			8	$\overline{CS}$	Chip Select Input
			9	$\overline{WR}$	WRITE Input
2	OUT2	DAC current output bus. Normally terminated at ground	10	A0	Address Bus Input
			11	A1	Address Bus Input
3	AGND	Analog Ground	12	DGND	Digital Ground
4	D3	Data Input (MSB)	13	$\overline{CLR}$	Clear Input
5	D2	Data Input	14	V_{DD}	+5V Supply Input
6	D1	Data Input	15	V_{REF}	Reference Input
			16	R_{FB}	DAC Feedback Resistor

Table 1. Pin Function Description

Analog Circuit Description

GENERAL CIRCUIT INFORMATION

The AD7542, a 12-bit multiplying D/A converter, consists of a highly stable thin film R-2R ladder and twelve N-channel current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 1. An inverted R-2R ladder structure is used—that is, the binarily weighted currents are switched between the OUT1 and OUT2 bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

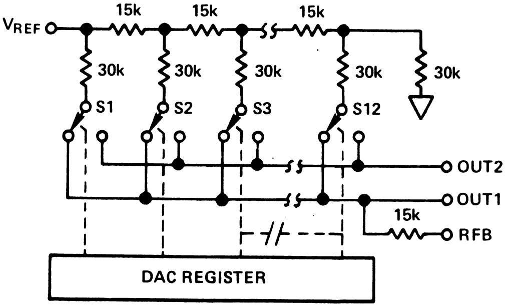


Figure 1. AD7542 Functional Diagram

One of the current switches is shown in Figure 2. The input resistance at V_{REF} (Figure 1) is always equal to R_{LDR} (R_{LDR} is the R/2R ladder characteristic resistance and is equal to value "R"). Since R_{IN} at the V_{REF} pin is constant, the reference terminal can be driven by a reference voltage or a reference current, ac or dc, of positive or negative polarity. (If a current source is used, a low temperature coefficient external R_{FB} is recommended to define scale factor.)

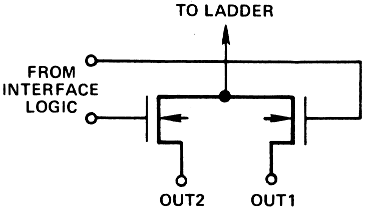


Figure 2. N-Channel Current Steering Switch

EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuits for all digital inputs LOW and all digital inputs HIGH are shown in Figures 3 and 4. In Figure 3 with all digital inputs LOW, the reference current is switched to OUT2. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate, while the 1/4096 current source represents a constant 1-bit current drain through the termination resistor on the R-2R ladder. The "ON" capacitance of the output N-channel switch is 260pF, as shown on the OUT2 terminal. The "OFF" switch capacitance is 75pF, as shown on the OUT1 terminal. Analysis of the circuit for all digital inputs HIGH, as shown in Figure 4, is similar to Figure 3; however, the "ON" switches are now on terminal OUT1, hence the 260pF at that terminal.

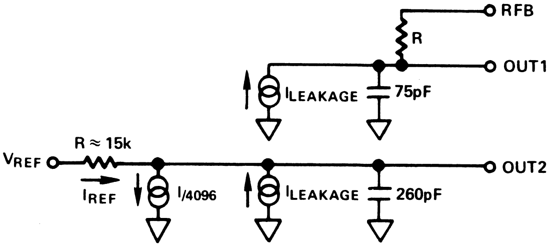


Figure 3. AD7542 DAC Equivalent Circuit All Digital Inputs LOW

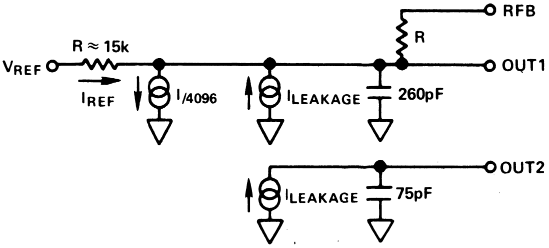


Figure 4. AD7542 DAC Equivalent Circuit All Digital Inputs HIGH

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 5 shows the analog circuit connections required for unipolar binary (2-quadrant multiplication) operation. The logic inputs are omitted for clarity. With a dc reference voltage or current (positive or negative polarity) applied at pin 15, the circuit is a unipolar D/A converter. With an ac reference voltage or current the circuit provides 2-quadrant multiplication (digitally controlled attenuation). The input/output relationship is shown in Table 2.

R1 provides full scale trim capability [i.e.–load the DAC register to 1111 1111 1111, adjust R1 for $V_{OUT} = -V_{REF}$ (4095/4096)]. Alternatively, Full Scale can be adjusted by omitting R1 and R2 and trimming the reference voltage magnitude.

C1 phase compensation (10 to 25pF) may be required for stability when using high speed amplifiers. (C1 is used to cancel the pole formed by the DAC internal feedback resistance and output capacitance at OUT1).

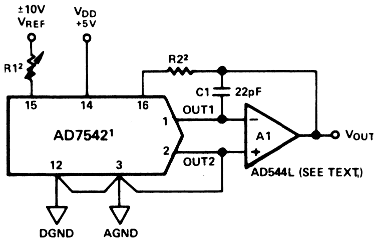
Amplifier A1 should be selected or trimmed to provide $V_{OS} \leq 10\%$ of the voltage resolution at V_{OUT}. Additionally, the amplifier should exhibit a bias current which is low over the temperature range of interest (bias current causes output offset at V_{OUT} equal to I_B times the DAC feedback resistance, nominally 15kΩ). The AD544L is a high-speed implanted FET-input op amp with low, factory-trimmed V_{OS}.

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

Figure 6 and Table 3 illustrate the circuitry and code relationship for bipolar operation. With a dc reference (positive or negative polarity) the circuit provides offset binary operation. With an ac reference, the eleven LSBs provide digitally controlled attenuation of the ac reference while the MSB provides polarity control.

With the DAC register loaded to 1000 0000 0000, adjust R1 for $V_{OUT} = 0V$ (alternatively, one can omit R1 and R2 and adjust the ratio of R3 to R4 for $V_{OUT} = 0V$). Full scale trimming can be accomplished by adjusting the amplitude of V_{REF} or by varying the value of R5.

As in unipolar operation, A1 must be chosen for low V_{OS} and low I_B. R3, R4 and R5 must be selected for matching and tracking. Mismatch of 2R3 to R4 causes both offset and Full Scale error. Mismatch of R5 to R4 or 2R3 causes Full Scale error. C1 phase compensation (10pF to 25pF) may be required for stability.

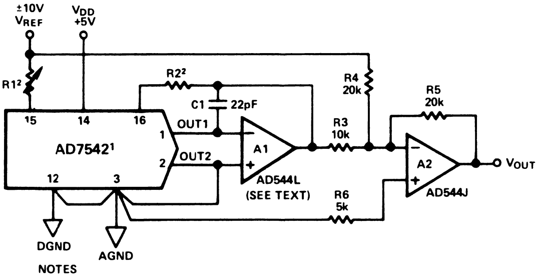


NOTES
1. LOGIC INPUTS OMITTED FOR CLARITY
2. SEE APPLICATION HINT NO. 4.

Figure 5. Unipolar Binary Operation (2-Quadrant Multiplication)

BINARY NUMBER IN DAC REGISTER MSB LSB	ANALOG OUTPUT, V_{OUT}
1111 1111 1111	$-V_{REF}\left(\frac{4095}{4096}\right)$
1000 0000 0000	$-V_{REF}\left(\frac{2048}{4096}\right) = -1/2\ V_{REF}$
0000 0000 0001	$-V_{REF}\left(\frac{1}{4096}\right)$
0000 0000 0000	0V

Table 2. Unipolar Binary Code Table for Circuit of Figure 5



NOTES
1. LOGIC INPUTS OMITTED FOR CLARITY
2. SEE APPLICATION HINT NO. 4

Figure 6. Bipolar Operation (4-Quadrant Multiplication)

BINARY NUMBER IN DAC REGISTER MSB LSB	ANALOG OUTPUT, V_{OUT}
1111 1111 1111	$+V_{REF}\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{REF}\left(\frac{1}{2048}\right)$
1000 0000 0000	0V
0111 1111 1111	$-V_{REF}\left(\frac{1}{2048}\right)$
0000 0000 0000	$-V_{REF}\left(\frac{2048}{2048}\right)$

Table 3. Bipolar Code Table for Offset Binary Circuit of Figure 6

INTERFACE LOGIC

INTERFACE LOGIC INFORMATION

The AD7542 is designed to interface as a memory-mapped output device.

A typical system configuration is shown in Figure 8. $\overline{CS}$ is the decoded *device* address, and is derived by decoding the three higher order address bits. A0 and A1 is the AD7542 *operation* address, and is decoded internally in the AD7542 to point to the desired loading operation (i.e. load high byte, middle byte, low byte or DAC register). Table 4 shows the AD7542 truth table.

All data loading operations are identical to the write cycle of a RAM as shown in Figure 7.

Additionally, the CLR input allows the AD7542 DAC register to be cleared asynchronously to 0000 0000 0000. When operating the AD7542 in a unipolar mode (Figure 5), a CLEAR causes the DAC output to assume 0V. In the bipolar mode (Figure 6), a CLEAR causes the DAC output to go to $-V_{REF}$.

In summary:

1. The AD7542 DAC register can be asynchronously cleared with the $\overline{CLR}$ input.
2. Each AD7542 requires 4 locations in memory.
3. Performing any of the four basic loading operations (i.e. load low byte data register, middle byte data register, high byte data register or 12-bit DAC register) is accomplished by executing a memory WRITE operation to the applicable address location for the required DAC operation.

AD7542 Control Inputs					AD7542 Operation	
A_1	A_0	$\overline{CS}$	$\overline{WR}$	$\overline{CLR}$		
X	X	X	X	0	Resets DAC 12-Bit Register to Code 0000 0000 0000	
X	X	1	X	1	No Operation Device Not Selected	
0	0	0	↑	1	Load LOW Byte[5] Data Register On Edge As Shown	Load Applicable Data Register With Data At $D_0 - D_3$
0	1	0	↑	1	Load MIDDLE Byte[5] Data Register On Edge As Shown	
1	0	0	↑	1	Load HIGH Byte[5] Data Register On Edge As Shown	
1	1	0	⊔	1	Load 12-Bit DAC Register With Data In LOW Byte, MIDDLE Byte & HIGH Byte Data Registers[6]	

NOTES:

[1] 1 indicates logic HIGH

[2] 0 indicates logic LOW

[3] X indicates don't care

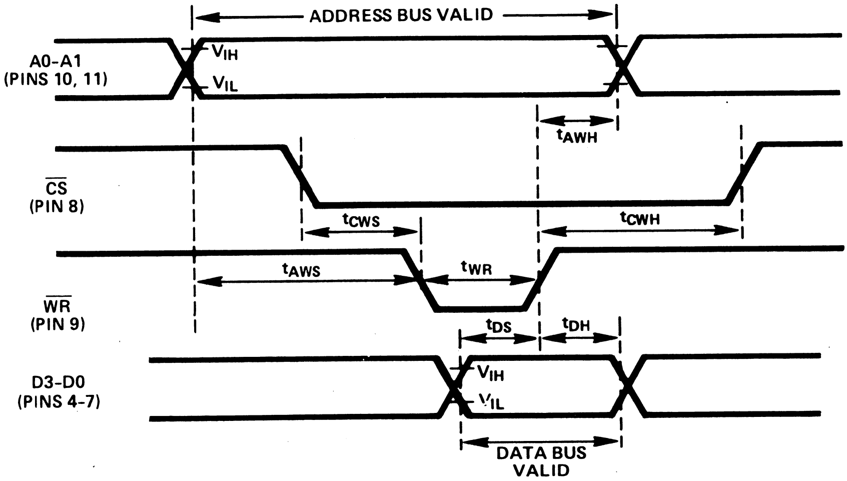
[4] ↑ indicates LOW to HIGH transition

[5] MSB → XXXX XXXX XXXX ← LSB

	high byte	middle byte	low byte	
MSB →	XXXX	XXXX	XXXX	← LSB

[6] These control signals are level triggered.

Table 4. AD7542 Truth Table



NOTE: TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$

Figure 7. AD7542 Timing Diagram

APPLICATION HINTS

The AD7542 is a precision 12-bit multiplying DAC designed for system interface. To ensure system performance consistent with AD7542 specifications, careful attention must be given to the following points:

1. GENERAL GROUND MANAGEMENT: Voltage differences between the AD7542 AGND and DGND cause loss of accuracy (dc voltage difference between the grounds introduces gain error. AC or transient voltages between the grounds cause noise injection into the analog output). The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7542. In more complex systems where the AGND-DGND intertie is on the back-plane, it is recommended that diodes be connected back-to-back between the AD7542 AGND and DGND pins (1N913 or equivalent).

2. OUTPUT AMPLIFIER OFFSET: CMOS DACs exhibit a code-dependent output resistance which in turn causes a code-dependent amplifier noise gain. The effect is a differential nonlinearity term at the amplifier output of magnitude $0.67V_{OS}$ (V_{OS} is amplifier input offset voltage). This differential nonlinearity term adds to the R/2R differential nonlinearity. To maintain monotonic operation, it is recommended that amplifier V_{OS} be no greater than 10% of the DAC's output resolution over the temperature range of interest [output resolution = $V_{REF}(2^{-n})$ where n is the number of bits exercised].

3. HIGH FREQUENCY CONSIDERATIONS: AD7542 output capacitance works in conjunction with the amplifier feedback resistance to add a pole to the open loop response. This not only reduces closed loop bandwidth, but can also cause ringing or oscillation if the spurious pole frequency is less than the amplifier's 0dB crossover frequency. Stability can be restored by adding a phase compensation capacitor in parallel with the feedback resistor.

4. GAIN TEMPERATURE COEFFICIENTS: The gain temperature coefficient of the AD7542 has a maximum value of 5ppm/°C and a typical value of 2ppm/°C. This corresponds to gain shifts of 2.0LSBs and 0.82LSBs respectively over a 100°C temperature range. When trim resistors are used to adjust full-scale range as shown in Figures 5 and 6 the temperature coefficient of R1 and R2 should be taken into account. It may be shown that the additional gain temperature coefficients introduced by R1 and R2 may be approximately expressed as follows:–

$$\text{Temperature Coefficient contribution due to R1} = -\frac{R_1}{R_{IN}}(\gamma_1 + 300)$$

$$\text{Temperature Coefficient contribution due to R2} = +\frac{R_2}{R_{IN}}(\gamma_2 + 300)$$

5. For additional information on multiplying DACs refer to "Application Guide to CMOS Multiplying D/A Converters", Publication Number G479–15–8/78, available from Analog Devices.

Where γ_1 and γ_2 are the temperature coefficients in ppm/°C of R1 and R2 respectively and R_{IN} is the DAC input resistance at the V_{REF} terminal (pin 2). For high quality wire-wound resistors and trimming potentiometers γ is of the order of 50ppm/°C. It will be seen that if R1 and R2 are small compared with R_{IN}, their contribution to gain temperature coefficient will also be small. For the standard AD7542 gain error specification of ±12.3LSBs it is recommended that R1 = 120Ω and R2 = 60Ω. With γ = 50 these values result in an overall maximum gain error temperature coefficient of:

$$5 + \frac{0.06}{7}(50 + 300) = 8\text{ppm}/^\circ\text{C}$$

However, if the AD7542GTD is used which has a specified gain error of ±1LSB, then with R1 = 10Ω and R2 = 5Ω the overall maximum gain temperature coefficient is increased by only 0.25ppm/°C. Where possible R1 should be a select on test fixed resistor since the resulting gain temperature coefficient will be tighter in all cases. For further gain T.C. information refer to application note, "Gain Error and Gain Temperature Coefficients of CMOS Multiplying DACs", Publication Number E630–10–6/81 available from Analog Devices.

AD7542 INTERFACE TO MC6800

A typical 6800 system configuration is shown in Figure 8. Since the AD7542 contains four registers, each AD7542 is assigned four locations in memory. A0 and A1 provides the operational addresses and are decoded internally to point to the desired register. Register loading is accomplished by executing a memory WRITE instruction to one of the four addresses. The AD7542 $\overline{WR}$ input is gated by $\phi 2$ from the 6800. Table 5 gives a sample loading subroutine written in re-entrant form.

Choosing an arbitrary start address of PPQQ, locations PPQQ, PPQQ+1 and PPQQ+2 select the low, middle and high byte registers respectively while address PPQQ+3 selects the 12-bit DAC register. The 12-bit data to be passed to the subroutine is stored in locations XXYY and XXYY+1. The four most significant data bits are assumed to occupy the lower half of XXYY+1.

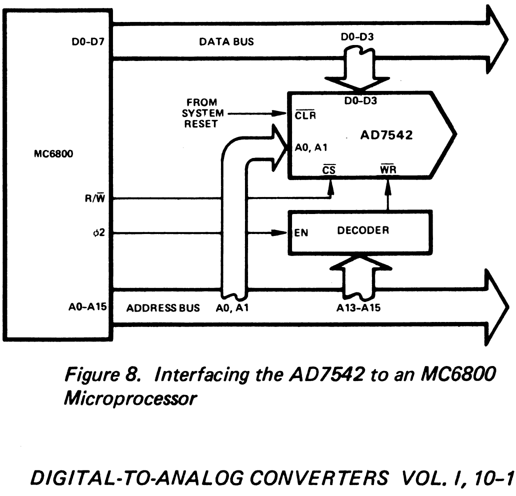


Figure 8. Interfacing the AD7542 to an MC6800 Microprocessor

```
        JSR      WWZZ
WWZZ    PSH  A                PUSH ACC. A ONTO STACK
        TPA
        PSH A                 PUSH CCR ONTO STACK
        LDA A    XXYY
        STA A    PPQQ         LOAD LOW BYTE
        ROR A
        ROR A
        ROR A
        ROR A
        STA A    PPQQ+1       LOAD MIDDLE BYTE
        LDA A    XXYY+1
        STA A    PPQQ+2       LOAD HIGH BYTE
        STA A    PPQQ+3       LOAD DAC REGISTER
        POP A
        TAP                   POP CCR FROM STACK
        POP A                 POP ACC. A FROM STACK
        RTS                   RETURN TO MAIN PROGRAM
```

Table 5. Sample Routine for AD7542–6800 Interface

```
        CALL     7542
7542    PUSH     PSW          PUSH REGISTER CONTENTS
        PUSH     B            ONTO STACK
        PUSH     H
        LX1      H, XXYY
        MOV      A, M
        STA      PPQQ         LOAD LOW BYTE
        MV1      B, 04
LOOP    RAR
        DCR      B
        JNZ      LOOP
        STA      PPQQ+1       LOAD MIDDLE BYTE
        INX      H
        MOV      A, M
        STA      PPQQ+2       LOAD HIGH BYTE
        STA      PPQQ+3       LOAD DAC REGISTER
        POP      H            POP REGISTER CONTENTS
        POP      B            FROM STACK
        POP      PSW
        RET                   RETURN TO MAIN PROGRAM
```

Table 6. Sample Routine for AD7542–8085 Interface

AD7542 INTERFACE TO 8085

A typical 8085 system configuration is shown in Figure 9. The AD7542 $\overline{CS}$ input is decoded from the three high order address lines A13–A15. The 8085 $\overline{WR}$ output is directly connected to the $\overline{WR}$ input of the AD7542. Table 6 gives a sample loading subroutine written in re-entrant form. The 12-bit data to be passed to the subroutine is stored in locations XXYY and XXYY+1. The four most significant data bits are assumed to occupy the lower half of XXYY+1. As before, arbitrary addresses PPQQ to PPQQ+3 select the low byte, middle byte, high byte and DAC registers respectively.

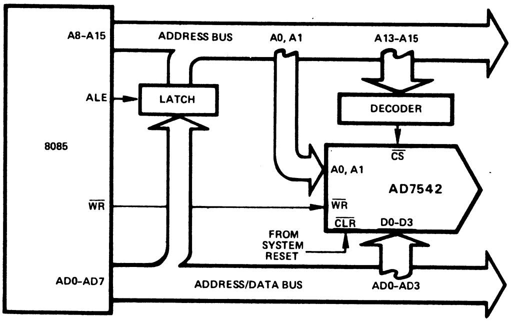


Figure 9. Interfacing the AD7542 to an 8085 Microprocessor

ANALOG DEVICES

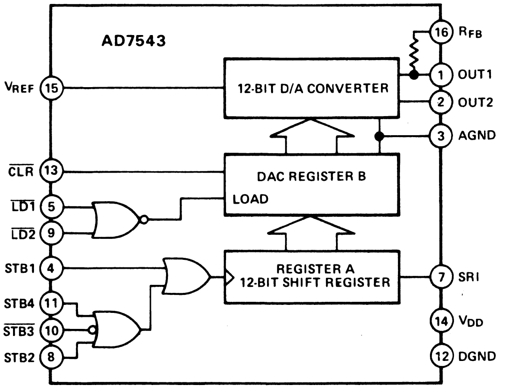
CMOS Serial Input 12-Bit DAC

AD7543

FEATURES

Resolution: 12 Bits
Nonlinearity: ±1/2LSB T_{min} to T_{max}
Low Gain T.C.: 2ppm/°C typ, 5ppm/°C max
Serial Load on Positive or Negative Strobe
Asynchronous CLEAR Input for Initialization
Full 4-Quadrant Multiplication
Low Multiplying Feedthrough: 1LSB max @ 10kHz
Requires no Schottky Diode Output Protection
Low Power Dissipation: 40mW max
+5V Supply
Small Size: 16-Pin DIP
Low Cost

AD7543 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

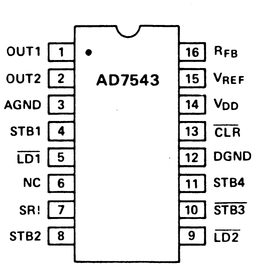
The AD7543 is a precision 12-bit monolithic CMOS multiplying DAC designed for serial interface applications.

The DAC's logic circuitry consists of a 12-bit serial-in parallel-out shift register (Register A) and a 12-bit DAC input register (Register B). Serial data at the AD7543 SRI pin is clocked into Register A on the leading or trailing edge (user selected) of the strobe input. Once Register A is full its contents are loaded into Register B under control of the LOAD inputs.

Initialization is simplified by the use of the CLR input which provides an asynchronous reset of Register B.

Packaged in a 16-pin DIP, the AD7543 features excellent gain T.C. (2ppm/°C typ; 5ppm/°C max), +5V operation and latch-free operation. (No protection Schottky diodes required.)

PIN CONFIGURATION



TOP VIEW
NOT TO SCALE

ORDERING INFORMATION

Relative Accuracy T_{min} to T_{max}	Gain Error +25°C	Commercial (Plastic) 0 to +70°C	Industrial (Ceramic) -25°C to +85°C	Military (Ceramic) -55°C to +125°C
±1LSB	±12.3LSB	AD7543JN	AD7543AD AD7543AD/883B	AD7543SD AD7543SD/883B
±1/2LSB	±12.3LSB	AD7543KN	AD7543BD AD7543BD/883B	AD7543TD AD7543TD/883B
±1/2LSB	±1LSB	AD7543GKN	AD7543GBD AD7543GBD/883B	AD7543GTD AD7543GTD/883B

PACKAGE IDENTIFICATION[1]

Suffix D: Ceramic DIP – (D16B)
Suffix N: Plastic DIP – (N16B)

[1] See Section 20 for package outline information.

SPECIFICATIONS (V_{DD} = +5V, V_{REF} = +10V, V_{OUT1} = V_{OUT2} = 0V, unless otherwise noted)

Parameter	Limit At T_A = +25°C	Limit At[1] T_A = 0, +70°C, -25°C & +85°C	Limit At[1] T_A = -55°C & +125°C	Units	Conditions/Comments
ACCURACY					
Resolution	12	12	12	Bits	
Relative Accuracy[2]					
JN, AD, SD Versions	±1	±1	±1	LSB max	
KN, BD, TD Versions	±1/2	±1/2	±1/2	LSB max	
GKN, GBD, GTD Versions	±1/2	±1/2	±1/2	LSB max	
Differential Nonlinearity[2]					
JN, AD, SD Versions	±2	±2	±2	LSB max	Monotonic to 11 bits from T_{min} to T_{max}
KN, BD, TD Versions	±1	±1	±1	LSB max	Monotonic to 12 bits from T_{min} to T_{max}
GKN, GBD, GTD Versions	±1	±1	±1	LSB max	Monotonic to 12 bits from T_{min} to T_{max}
Gain Error[2]					
JN, KN, AD, BD, SD, TD	±12.3	±13.5	±14.5	LSB max	Using internal RFB only (gain error can be trimmed to zero using circuits of Figures 6 & 7)
GKN, GBD, GTD	±1	±1	±2	LSB max	
Gain Temperature Coefficient ΔGain/ΔTemperature	5	5	5	ppm/°C max	Typical value is 2ppm/°C
Power Supply Rejection ΔGain/ΔV_{DD}	0.005	0.01	0.01	% per % max	V_{DD} = +4.75V to +5.25V
Output Leakage Current					
I_{OUT1} (Pin 4)	1	10	200	nA max	DAC Register loaded with all 0s
I_{OUT2} (Pin 5)	1	10	200	nA max	DAC Register loaded with all 1s
DYNAMIC PERFORMANCE					
Current Settling Time[3]	2.0	2.0	2.0	μs max	To 1/2LSB. OUT1 load = 100Ω. DAC output measured from falling edge of $\overline{LD1}$ and $\overline{LD2}$, see Figure 5.
Multiplying Feedthrough Error[3]	2.5	2.5	2.5	mV p-p max	V_{REF} = ±10V, 10kHz sine wave
REFERENCE INPUT					
Input Resistance (pin 15)	8/15/25	8/15/25	8/15/25	kΩ min/typ/max	Typical temperature coefficient is -150ppm/°C
ANALOG OUTPUTS					
Output Capacitance					
C_{OUT1}[3]	75	75	75	pF max	Register B loaded to 0000 0000 0000
C_{OUT1}[3]	260	260	260	pF max	Register B loaded to 1111 1111 1111
C_{OUT2}[3]	75	75	75	pF max	Register B loaded to 1111 1111 1111
C_{OUT2}[3]	260	260	260	pf max	Register B loaded to 0000 0000 0000
LOGIC INPUTS					
V_{INH} (Logic HIGH Voltage)	+3.0	+3.0	+3.0	V min	
V_{INL} (Logic LOW Voltage)	+0.8	+0.8	+0.8	V max	
I_{IN}[4]	1	1	1	μA max	V_{IN} = 0V or V_{DD}
C_{IN} (Input Capacitance)[3]	8	8	8	pF max	
Input Coding	12-Bit Unipolar Binary or 12-Bit Offset Binary (see Figures 6 and 7), serial load (MSB First)				
SWITCHING CHARACTERISTICS[5]					
t_{DS1}	50	100	100	ns min	Serial Input to Strobe Setup Time: STB1 used as a strobe
t_{DS4}	0	0	0	ns min	STB4 used as a strobe
t_{DS3}	0	0	0	ns min	$\overline{STB3}$ used as a strobe
t_{DS2}	20	40	40	ns min	STB2 used as a strobe
t_{DH1}	30	60	60	ns min	Serial Input to Strobe Hold Time: STB1 used as a strobe
t_{DH4}	80	160	160	ns min	STB4 used as a strobe
t_{DH3}	80	160	160	ns min	$\overline{STB3}$ used as a strobe
t_{DH2}	60	120	120	ns min	STB2 used as a strobe
t_{SRI}	80	160	160	ns min	SRI data pulse width
t_{STB1}	80	160	160	ns min	STB1 pulse width
t_{STB4}	100	200	200	ns min	STB4 pulse width
t_{STB3}	100	200	200	ns min	$\overline{STB3}$ pulse width
t_{STB2}	80	160	160	ns min	STB2 pulse width
t_{LD1}, t_{LD2}	150	300	300	ns min	Load pulse width
t_{ASB}	0	0	0	ns min	Min time between strobing LSB into Register A and loading Register B
t_{CLR}	200	400	400	ns min	CLR pulse width
POWER SUPPLY					
V_{DD} (Supply Voltage)	+5	+5	+5	V	
I_{DD} (Supply Current)	8	8	8	mA max	Digital Inputs = V_{INH} or V_{INL}

NOTES:

[1] Temperature ranges as follows: AD7543JN, KN, GKN: 0 to +70°C
AD7543AD, BD, GBD: -25°C to +85°C
AD7543SD, TD, GTD: -55°C to +125°C

[2] See Terminology on following page.

[3] Guaranteed but not tested.

[4] Logic inputs are MOS gates. Typical input current (+25°C) is less than 1nA.

[5] Sample tested at +25°C to ensure compliance.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to A_{GND}	0V, +7V
V_{DD} to D_{GND}	0V, +7V
A_{GND} to D_{GND}	V_{DD}
D_{GND} to A_{GND}	V_{DD}
Digital Input Voltage to D_{GND} (pins 4 - 11, 13)	−0.3V, +15V
V_{PIN1}, V_{PIN2} to A_{GND}	−0.3V, +15V
V_{REF} to A_{GND}	±25V
V_{RFB} to A_{GND}	±25V
Power Dissipation (Package)	
Plastic (Suffix N)	
To +70°C	670mW
Derates above +70°C by	8.3mW/°C
Ceramic (Suffix D)	
To +75°C	450mW
Derates above +75°C by	6mW/°C
Operating Temperature Range	
Commercial Plastic (JN, KN, GKN versions)	0 to +70°C
Industrial Ceramic (AD, BD, GBD versons)	−25°C to +85°C
Military Ceramic (SD, TD, GTD versions)	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 secs.)	+300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION:

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

WARNING!

ESD SENSITIVE DEVICE

TERMINOLOGY

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the difference between the *measured* change and the *ideal* 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB max over the operating temperature range ensures monotonicity.

GAIN ERROR

Gain is defined as the ratio of the DAC's Full Scale output to its reference input voltage. An *ideal* AD7543 would exhibit a gain of −4095/4096. Gain error is adjustable using external trims as shown in Figures 6 and 7.

OUTPUT LEAKAGE CURRENT

Current which appears at OUT1 with Register B loaded to all 0's or at OUT 2 with Register B loaded to all 1's.

MULTIPLYING FEEDTHROUGH ERROR

AC error due to capacitive feedthrough from V_{REF} terminal to OUT1 with DAC register loaded to all 0's.

PIN	MNEMONIC	FUNCTION
1	OUT1	DAC current output bus. Normally terminated at op amp virtual ground
2	OUT2	DAC current output bus. Normally terminated at AGND
3	AGND	Analog Ground
4	STB1	Register A Strobe 1 input, see Table 2
5	$\overline{LD1}$	DAC Register B Load 1 input. When $\overline{LD1}$ and $\overline{LD2}$ go low the contents of Register A are loaded into DAC Register B
6	N/C	No Connection
7	SRI	Serial Data Input to Register A
8	STB2	Register A Strobe 2 input, see Table 2
9	$\overline{LD2}$	DAC Register B Load 2 input. When $\overline{LD1}$ and $\overline{LD2}$ go low the contents of Register A are loaded into DAC Register B
10	$\overline{STB3}$	Register A Strobe 3 input, see Table 2
11	STB4	Register A Strobe 4 input, see Table 2
12	DGND	Digital Ground
13	$\overline{CLR}$	Register B CLEAR input (active LOW), can be used to asynchronously reset Register B to 0000 0000 0000
14	V_{DD}	+5V Supply Input
15	V_{REF}	Reference input. Can be positive or negative dc voltage or ac signal
16	R_{FB}	DAC Feedback Resistor

Table 1. Pin Function Description

GENERAL CIRCUIT INFORMATION

The AD7543, a 12-bit multiplying D/A converter, consists of a highly stable thin film R-2R ladder and twelve N-channel current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 1. An inverted R-2R ladder structure is used—that is, the binarily weighted currents are switched between the OUT1 and OUT2 bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

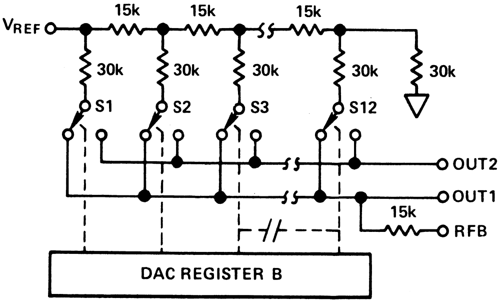


Figure 1. AD7543 Functional Diagram

One of the current switches is shown in Figure 2. The input resistance at V_{REF} (Figure 2) is always equal to R_{LDR} (R_{LDR} is the R/2R ladder characteristic resistance and is equal to value "R"). The reference terminal can be driven by a reference voltage or a reference current, ac or dc, of positive or negative polarity. If a current source is used, a low temperature coefficient external R_{FB} is recommended to define scale factor.

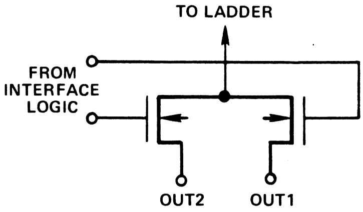


Figure 2. N-Channel Current Steering Switch

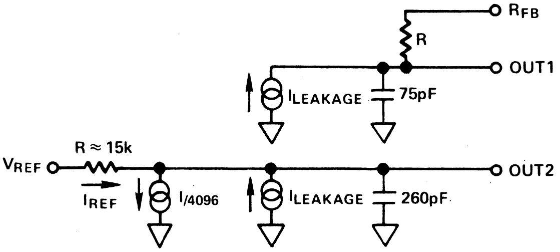


Figure 3. AD7543 DAC Equivalent Circuit All Digital Inputs LOW

EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuits for all digital inputs LOW and all digital inputs HIGH are shown in Figures 3 and 4. In Figure 3 with all digital inputs LOW, the reference current is switched to OUT2. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate, while the I/4096 current source represents a constant 1 least significant bit current drain through the termination resistor on the R-2R ladder. The "ON" capacitance of the output N-channel switch is 260pF, as shown on the OUT2 terminal. The "OFF" switch capacitance is 75pF, as shown on the OUT1 terminal. Analysis of the circuit for all digital inputs HIGH, as shown in Figure 4, is similar to Figure 3; however, the "ON" switches are now on terminal OUT1, hence the 260pF at that terminal.

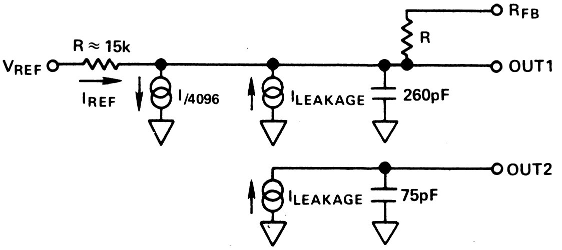


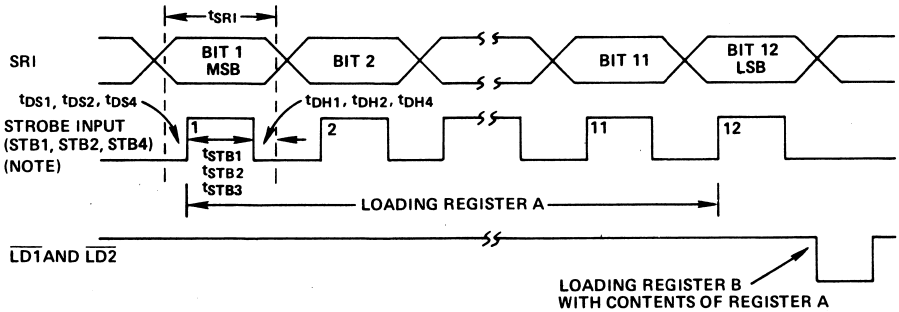
Figure 4. AD7543 DAC Equivalent Circuit All Digital Inputs HIGH

INTERFACE LOGIC INFORMATION

Shown in the AD7543 Functional Diagram Register A is a 12-bit shift register. Serial data appearing at pin SR1 is clocked into the shift register on the positive edge of STB1, STB2 or STB4 or on the negative edge of $\overline{\text{STB3}}$. Table 2 defines the various logic states required on the Register A control inputs, while Figure 5 illustrates the Register A loading sequence.

Once Register A is full, the data is transferred to Register B by bringing $\overline{\text{LD1}}$ and $\overline{\text{LD2}}$ momentarily LOW.

Register B can be asynchronously reset to 0000 0000 0000 by bringing $\overline{\text{CLR}}$ momentarily LOW. This allows the DAC output voltage to be set to a known condition, thus simplifying system initialization procedure. When operating the AD7543 in the unipolar circuit of Figure 6, a CLEAR causes the DAC output voltage to equal 0V. When using the bipolar circuit of Figure 7, a CLEAR causes the DAC output to equal $-V_{REF}$.


tSRI
SRI
BIT 1 MSB
BIT 2
BIT 11
BIT 12 LSB
tDS1, tDS2, tDS4
tDH1, tDH2, tDH4
STROBE INPUT (STB1, STB2, STB4) (NOTE)
1
2
11
12
tSTB1 tSTB2 tSTB3
LOADING REGISTER A
$\overline{\text{LD1}}$ AND $\overline{\text{LD2}}$
LOADING REGISTER B WITH CONTENTS OF REGISTER A

NOTE:
STROBE WAVEFORM IS INVERTED IF $\overline{\text{STB3}}$ IS USED TO STROBE SERIAL DATA BITS INTO REGISTER A.

Figure 5. Timing Diagram

AD7543 Logic Inputs							AD7543 Operation	Notes
Register A Control Inputs				Register B Control Inputs				
STB4	$\overline{\text{STB3}}$	STB2	STB1	$\overline{\text{CLR}}$	$\overline{\text{LD2}}$	$\overline{\text{LD1}}$		
0	1	0	↑	X	X	X	Data Appearing At SRI Strobed Into Register A	2,3
0	1	↑	0	X	X	X	Data Appearing At SRI Strobed Into Register A	2,3
0	↓	0	0	X	X	X	Data Appearing At SRI Strobed Into Register A	2,3
↑	1	0	0	X	X	X	Data Appearing At SRI Strobed Into Register A	2,3
1	X	X	X				No Operation (Register A)	3
X	0	X	X					
X	X	1	X					
X	X	X	1					
				0	X	X	Clear Register B To Code 0000 0000 0000 (Asynchronous Operation)	1,3
				1	1	X	No Operation (Register B)	3
				1	X	1		
				1	0	0	Load Register B With The Contents Of Register A	3

NOTES:
1. CLR = 0 Asynchronously resets Register B to 0000 0000 0000, but has no effect on Register A.
2. Serial data is loaded into Register A MSB first, on edges shown ↑ is positive edge ↓ is negative edge.
3. 0 = Logic LOW, 1 = Logic HIGH, X = Don't Care.

Table 2. AD7543 Truth Table

APPLYING THE AD7543

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 6 shows the analog circuit connections required for unipolar binary (2-quadrant multiplication) operation. The logic inputs are omitted for clarity. With a dc reference voltage or current (positive or negative polarity) applied at pin 15, the circuit is a unipolar D/A converter. With an ac reference voltage or current (again of + or - polarity) the circuit provides 2-quadrant multiplication (digitally controlled attenuation). The input/output relationship is shown in Table 3.

R1 provides full scale trim capability [i.e.—load the DAC register to 1111 1111 1111, adjust R1 for $V_{OUT} = -V_{REF}$ (4095/4096)]. Alternatively, Full Scale can be adjusted by omitting R1 and R2 and trimming the reference voltage magnitude.

C1 phase compensation (10pF to 25pF) may be required for stability when using high speed amplifiers. (C1 is used to cancel the pole formed by the DAC internal feedback resistance and output capacitance at OUT1).

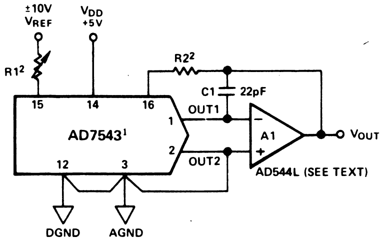
Amplifier A1 should be selected or trimmed to provide $V_{OS} \leqslant 10\%$ of the voltage resolution at V_{OUT}. Additionally, the amplifier should exhibit a bias current which is low over the temperature range of interest (bias current causes output offset at V_{OUT} equal to I_B times the DAC feedback resistance, nominally 15kΩ). The AD544L is a high-speed implanted FET-input op amp with low, factory-trimmed V_{OS}.

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

Figure 7 and Table 4 illustrate the circuitry and code relationship for bipolar operation. With a dc reference (positive or negative polarity) the circuit provides offset binary operation. With an ac reference, the eleven LSBs provide digitally controlled attenuation of the ac reference while the MSB provides polarity control.

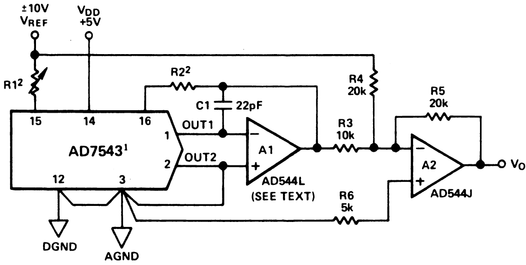
With the DAC register loaded to 1000 0000 0000, adjust R1 for $V_{OUT} = 0V$ (alternatively, one can omit R1 and R2 and adjust the ratio of R3 to R4 for $V_{OUT} = 0V$). Full scale trimming can be accomplished by adjusting the amplitude of V_{REF} or by varying the value of R5.

As in unipolar operation, A1 must be chosen for low V_{OS} and low I_B. R3, R4 and R5 must be selected for matching and tracking. Mismatch of 2R3 to R4 causes both offset and Full Scale error. Mismatch of R5 to R4 to 2R3 causes Full Scale error. C1 phase compensation (10pF to 25pF) may be required for stability.



NOTES
1. LOGIC INPUTS OMITTED FOR CLARITY.
2. SEE APPLICATION HINT NO. 4.

Figure 6. Unipolar Binary Operation (2-Quadrant Multiplication)



NOTES
1. LOGIC INPUTS OMITTED FOR CLARITY.
2. SEE APPLICATION HINT NO. 4.

Figure 7. Bipolar Operation (4-Quadrant Multiplication)

BINARY NUMBER IN DAC REGISTER MSB LSB	ANALOG OUTPUT, V_{OUT}
1111 1111 1111	$-V_{REF}\left(\frac{4095}{4096}\right)$
1000 0000 0000	$-V_{REF}\left(\frac{2048}{4096}\right) = -1/2\ V_{REF}$
0000 0000 0001	$-V_{REF}\left(\frac{1}{4096}\right)$
0000 0000 0000	0V

Table 3. Unipolar Binary Code Table for Circuit of Figure 6

BINARY NUMBER IN DAC REGISTER MSB LSB	ANALOG OUTPUT, V_{OUT}
1111 1111 1111	$+V_{REF}\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{REF}\left(\frac{1}{2048}\right)$
1000 0000 0000	0V
0111 1111 1111	$-V_{REF}\left(\frac{1}{2048}\right)$
0000 0000 0000	$-V_{REF}\left(\frac{2048}{2048}\right)$

Table 4. Bipolar Code Table for Offset Binary Circuit of Figure 7

APPLICATION HINTS

The AD7543 is a precision 12-bit multiplying DAC designed for serial interface. To ensure system performance consistent with AD7543 specifications, careful attention must be given to the following points:

1. GENERAL GROUND MANAGEMENT: Voltage differences between the AD7543 AGND and DGND cause loss of accuracy (dc voltage difference between the grounds introduces gain error. AC or transient voltages between the grounds cause noise injection into the analog output). The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7543. In more complex systems where the AGND-DGND connection is on the back-plane, it is recommended that diodes be connected back-to-back between the AD7543 AGND and DGND pins to prevent possible device damage.
2. OUTPUT AMPLIFIER OFFSET: CMOS DACs exhibit a code-dependent output resistance which in turn causes a code-dependent amplifier noise gain. The effect is a differential nonlinearity term at the amplifier output of magnitude 0.67 V_{OS} (V_{OS} is amplifier input offset voltage). This differential nonlinearity term adds to the R/2R differential nonlinearity. To maintain monotonic operation, it is recommended that amplifier V_{OS} be no greater than 10% of the DAC's output resolution over the temperature range of interest [output resolution = $V_{REF}\ 2^{-n}$ where n is the number of bits exercised].
3. HIGH FREQUENCY CONSIDERATIONS: AD7543 output capacitance works in conjunction with the amplifier feedback resistance to add a pole to the open loop response. This not only reduces closed loop bandwidth, but can also cause ringing or oscillation if the spurious pole frequency is less than the amplifier's 0dB crossover frequency. Stability can be restored by adding a phase compensation capacitor in parallel with the feedback resistor.
4. GAIN TEMPERATURE COEFFICIENTS: The gain temperature coefficient of the AD7543 has a maximum value of 5ppm/°C and a typical value of 2ppm/°C. This corresponds to gain shifts of 2.0LSBs and 0.82LSBs respectively over a 100°C temperature range. When trim resistors are used to adjust full-scale range as shown in Figures 6 and 7 the temperature coefficient of R1 and R2 should be taken into account. It may be shown that the additional gain temperature coefficients introduced by R1 and R2 may be approximately expressed as follows:—

   $$\text{Temperature Coefficient contribution due to R1} = -\frac{R_1}{R_{IN}}(\gamma_1 + 300)$$

   $$\text{Temperature Coefficient contribution due to R2} = +\frac{R_2}{R_{IN}}(\gamma_2 + 300)$$

5. For additional information on multiplying DACS refer to "Application Guide to CMOS Multiplying D/A Converters". Publication Number G479–15–8/78, available from Analog Devices.

Where γ_1 and γ_2 are the temperature coefficients in ppm/°C of R1 and R2 respectively and R_{IN} is the DAC input resistance at the V_{REF} terminal (pin 2). For high quality wirewound resistors and trimming potentiometers γ is of the order of 50ppm/°C. It will be seen that if R1 and R2 are small compared with R_{IN}, their contribution to gain temperature coefficient will also be small. For the standard AD7543 gain error specification of ±12.3LSBs it is recommended that R1 = 120Ω and R2 = 60Ω. With $\gamma = 50$ these values result in an overall maximum gain error temperature coefficient of:

$$5 + \frac{0.06}{7}(50 + 300) = 8\text{ppm}/^\circ\text{C}$$

However, if the AD7543GTD is used which has a specified gain error of ±1LSB, then with R1 = 10Ω and R2 = 5Ω the overall maximum gain temperature coefficient is increased by only 0.25ppm/°C. Where possible R1 should be a select on test fixed resistor since the resulting gain temperature coefficient will be tighter in all cases. For further gain T.C. information refer to application note, "Gain Error and Gain Temperature Coefficients of CMOS Multiplying DACs", Publication Number E630–10–6/81 available from Analog Devices.

AD7543 INTERFACE TO MC6800

In this example, it is assumed that the 12-bit data is contained in two memory locations (0000 and 0001). The four most significant bits are assumed to occupy the lower half of memory location 0000. The eight least significant bits occupy memory location 0001. The data is presented bit by bit on the D7 line and strobed into the AD7543 by executing memory write instructions. In this case the strobe signal (STB1) is supplied by decoding address 2000, R/$\overline{W}$ and ϕ_2. A memory write instruction to a different address (4000) loads the data from Register A to the DAC register.

Figure 8 shows the interface circuitry and Table 5 gives a listing of the procedure.

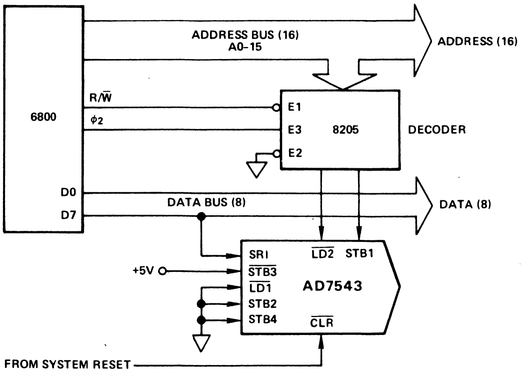


Figure 8. AD7543–MC6800 Interface

```
LABEL   MNEMONIC  OPERAND   COMMENT
        LDA       B, 04
        LDA       A, 0000   Load 4 Most Significant Bits
LOOP    ROL       A         Reposition the Data
        DEC       B           in ACC A
        BNE       LOOP
        LDA       B, 04
        BSR       SHIFT     Output Data
        LDA       B, 08
        LDA       A, 0001   Load 8 Least Significant Bits
        BSR       SHIFT     Output Data
        STA       A, 4000   Load DAC Register
        RTS                 Return to Main Program
SHIFT   STA       A,2000      Strobe Data
        ROL       A           into AD7543
        DEC       B
        BNE       SHIFT
        RTS
```

Table 5. Sample Routine for AD7543–MC6800 Interface

```
LABEL   MNEMONIC  OPERAND   COMMENT
        MVI       B, 05     Shift Data Up to
LOOP    CALL      SHIFT     Most Significant
        DCR       B         Segment of HL with
        JWZ       LOOP      MSB as Carry
        MVI       B, 0C
LUP     MVI       A, 80     SOD Enable in ACC
        RAR                 Shift in MSB of H
        SIM                 Set Interrupt Mask
        STA       8000      Strobe Data into AD7543
        CALL      SHIFT     Get Next Bit into Carry
        DCR       B
        JNZ       LUP       Go Back if Not Finished
        STA       A000      Load DAC Register of AD7543
        RET                 Return to Main Program
SHIFT   MOV       A, L      Shift H and L Left
        RAL                 One Place and
        MOV       L, A      Leave Uppermost Bit
        MOV       A, H      of H in Carry
        RAL
        MOV       H, A
        RET
```

Table 6. Sample Routine for AD7543–8085 Interface

AD7543 INTERFACE TO MCS-85

Figure 9 shows the AD7543 interfaced to the 8085. This system makes use of the serial output facility (SOD) on the 8085.

The data is presented serially on the SOD line and strobed into the AD7543 by executing memory write instructions. In this example the strobe signal $\overline{\text{STB2}}$) is supplied by decoding address 8000 and $\overline{\text{WR}}$. A memory write instruction to a different address (A000) loads the DAC Register with Register A data. Table 6 gives a listing of this procedure. Note, it is assumed that the required serial data is already present in right-justified format in Registers H and L when this procedure is implemented.

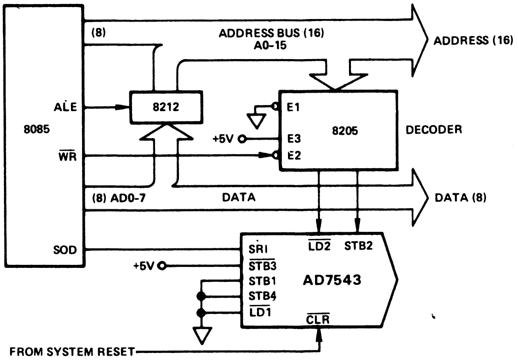


Figure 9. AD7543–8085 Interface

ANALOG DEVICES

CMOS 12-Bit, 6 Word, FIFO, DAC

AD7544

PRELIMINARY TECHNICAL DATA

FEATURES

- ±1/2LSB Nonlinearity from T_{min} to T_{max}
- Monotonicity Guaranteed for 11- and 12-Bit Versions
- Twelve-Bit Wide, Six-Word Deep First-In First-Out (FIFO) Buffer Memory
- FIFO Status Flags for Input/Output Handshaking
- Directly Interfaces with 16-Bit Microprocessors
- Low Gain Drift, Typically 2ppm/°C
- ±1LSB max Gain Error
- Latch-Up Proof
- Single +5V Supply

GENERAL DESCRIPTION

The AD7544 is a 12-bit monolithic CMOS DAC with a 12-bit wide, 6-word deep, First-In First-Out (FIFO) Register stack. Twelve-bit words are written to the top of the stack under the control of $\overline{WR}$ (Write) and $\overline{WREN}$ (Write Enable). The 12-bit word then falls through the stack into the last empty register nearest the bottom of the stack. Hence, the stack is full after six write instructions. There are two status flags associated with the stack, SFUL (Stack Full) and SAMT (Stack Almost Empty, one word remaining).

The contents of the stack can be rolled down towards the DAC register under control of $\overline{RL}$ (Roll) and $\overline{RLEN}$ (Roll ENable). The DAC register, under control of LDAC (Load DAC), may be loaded with either word 1 or word 2 of the stack depending upon the word-selector control input $W1/\overline{W2}$. System Reset $\overline{RST}$ loads all 0s into the DAC register and resets the stack register control flip-flops to allow a full six-word load operation.

ORDERING INFORMATION

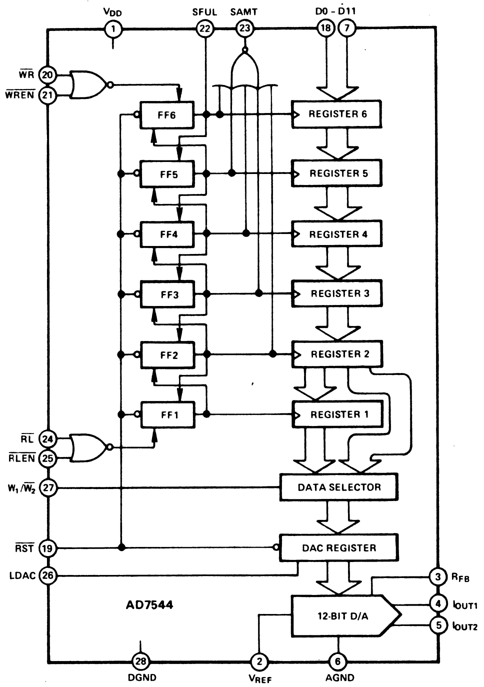
Relative Accuracy (T_{min} to T_{max})	Gain Error +25°C	Temperature Range		
		0 to +70°C	-25°C to +85°C	-55°C to +125°C
±1LSB	±12.3LSBs	AD7544JN	AD7544AD	AD7544SD
±1/2LSB	±12.3LSBs	AD7544KN	AD7544BD	AD7544TD
±1/2LSB	±1LSB	AD7544GKN	AD7544GBD	AD7544GTD

PACKAGE IDENTIFICATION[1]

Suffix D: Ceramic DIP – (D28B)

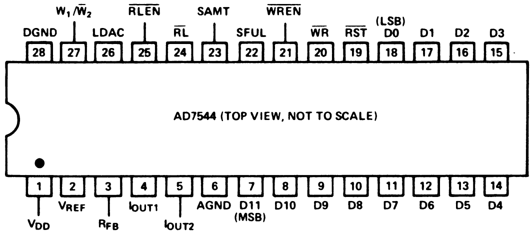
Suffix N: Plastic DIP – (N28A)

AD7544 FUNCTIONAL BLOCK DIAGRAM



28-PIN DIP

PIN CONFIGURATION



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[1] See Section 20 for outline information.

SPECIFICATIONS (V_{DD} = 5V, V_{REF} = +10V, V_{OUT1} = V_{OUT2} = 0V unless otherwise noted)

Parameter	Limit At T_A = +25°C	Limit At[1] T_A = 0, +70°C, -25°C & +85°C	Limit At[1] T_A = -55°C & +125°C	Units	Conditions/Comments
ACCURACY					
Resolution	12	12	12	Bits	
Relative Accuracy[2]					
JN, AD, SD Versions	±1	±1	±1	LSB max	
KN, BD, TD Versions	±1/2	±1/2	±1/2	LSB max	
GKN, GBD, GTD Versions	±1/2	±1/2	±1/2	LSB max	
Differential Nonlinearity[2]					
JN, AD, SD Versions	±2	±2	±2	LSB max	Monotonic to 11 bits from T_{min} to T_{max}
KN, BD, TD Versions	±1	±1	±1	LSB max	Monotonic to 12 bits from T_{min} to T_{max}
GKN, GBD, GTD Versions	±1	±1	±1	LSB max	Monotonic to 12 bits from T_{min} to T_{max}
Gain Error[2]					
JN, KN, AD, BD, SD, TD	±12.3	±13.5	±14.5	LSB max	Using internal RFB only (gain error can be
GKN, GBD, GTD	±1	±1	±2	LSB max	trimmed to zero using circuits of Figures 4 & 5)
Gain Temperature Coefficient					
ΔGain/ΔTemperature	5	5	5	ppm/°C max	Typical value is 2ppm/°C
Power Supply Rejection					
ΔGain/ΔV_{DD}	0.002	0.01	0.01	% per % max	V_{DD} = +4.75V to +5.25V
Output Leakage Current					
I_{OUT1} (Pin 4)	1	10	200	nA max	DAC Register loaded with all 0s
I_{OUT2} (Pin 5)	1	10	200	nA max	DAC Register loaded with all 1s
DYNAMIC PERFORMANCE					
Propagation Delay[2]	185	230	250	ns max	I_{OUT1} load = 100Ω, C_{EXT} = 13pF. Measured from LDAC (Pin 26) going high to 90% of final output current for a full-scale change.
Stack Propagation Delay	1.26	1.4	1.6	μs max	I_{OUT1} load = 100Ω, C_{EXT} = 13pF. LDAC held HIGH. Measured from WR (Pin 20) going high to 90% of final output current for a full-scale data input change.
Digitial Charge Injection[2]	700	700	700	nVsecs typ	Typical value included for design guidance only
Multiplying Feedthrough Error[2]	2.5	2.5	2.5	mV p-p max	V_{REF} = ±10V, 10kHz Sine Wave
REFERENCE INPUT					
Input Resistance (Pin 2)	7/12/20	7/12/20	7/12/20	kΩ min/typ/max	
Input Resistance Temperature Coefficient	-300	-300	-300	ppm/°C typ	
ANALOG OUTPUTS					
Output Capacitance[3]					
C_{OUT1}	75	75	75	pF max	DAC Register loaded with all 0s
C_{OUT2}	260	260	260	pF max	
C_{OUT1}	260	260	260	pF max	DAC Register loaded with all 1s
C_{OUT2}	75	75	75	pF max	
DIGITAL INPUTS					
V_{IH} (Input High Voltage)	3.0	3.0	3.0	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	V max	
I_{IN}, Input Current[4]	1	1	1	μA max	V_{IN} = 0V or V_{DD}
CIN, Input Capacitance[3]	8	8	8	pF max	
Input Coding	Binary or Offset Binary				See Tables 5 & 6
DIGITAL OUTPUTS					
V_{OH} (Output High Voltage)	+4.0	+4.0	+4.0	V min	I_{SOURCE} = -40μA
V_{OL} (Output Low Voltage)	+0.6	+0.8	+0.8	V max	I_{SINK} = 1.6mA
SWITCHING CHARACTERISTICS[5]					
t_{WR}	75	75	95	ns min	Write Pulse Width
t_{WRS}	0	0	0	ns min	Write Enable Setup Time
t_{WRH}	0	0	0	ns min	Write Enable Hold Time
t_{WDS}	220	290	330	ns max	Write to Data Setup Time
t_{WDH}	270	320	375	ns min	Write to Data Hold Time
t_{WMT}	400	500	600	ns max	Stack Almost Empty Flag LOW Response Time
t_{WFL}	320	420	450	ns max	Stack Full Flag HIGH Response Time
t_{RL}	75	75	95	ns min	Roll Pulse Width
t_{RLS}	0	0	0	ns min	Roll Enable Setup Time
t_{RLH}	0	0	0	ns min	Roll Enable Hold Time
t_{RFL}	1.1	1.3	1.44	μs max	Stack Full Flag LOW Response Time
t_{RMT}	380	500	580	ns max	Stack Almost Empty Flag HIGH Response Time
t_{LDAC}	120	160	180	ns min	Load DAC Pulse Width
t_{WSS}	135	165	230	ns min	Word Select Setup Time
t_{WSH}	0	0	0	ns min	Word Select Hold Time
$t_{\overline{RST}}$	75	100	140	ns min	Reset Pulse Width
POWER SUPPLY					
V_{DD}	+5	+5	+5	V	
I_{DD}	2	2	2	mA max	Digital Inputs = V_{IH} or V_{IL}
	100	500	500	μA max	Digital Inputs = 0V or V_{DD}

NOTES

[1] Temperature range as follows: JN, KN, LN, GKN Versions: 0 to +70°C
AD, BD, CD, GBD Versions: -25°C to +85°C
SD, TD, UD, GTD Versions: -55°C to +125°C

[2] See definition on next page.

[3] Guaranteed but not tested.

[4] Logic inputs are MOS gates. Typical input current at +25°C is 1nA.

[5] Sample tested at +25°C to ensure compliance.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to DGND	0V, +7V
V_{DD} to AGND	0V, +7V
AGND to DGND	$\pm V_{DD}$
DGND to AGND	$\pm V_{DD}$
Digital Input Voltage to DGND (pins 7 - 21, 24 - 27)	-0.3V, +15V
Digital Output Voltage to DGND (pins 22, 23)	-0.3V, +15V
V_{PIN4}, V_{PIN5} to AGND	-0.3V, +15V
V_{REF} to AGND	±25V
V_{RFB} to AGND	±25V
Operating Temperature Range	
JN, KN, GKN Versions	0 to +70°C
AD, BD, GBD Versions	-25°C to +85°C
SD, TD, GTD Versions	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 secs)	+300°C
Power Dissipation (Package)	
Plastic (Suffix N) to +50°C	1200mW
Derate Above +50°C by	12mW/°C
Ceramic (Suffix D) to +50°C	1000mW
Derate Above +50°C by	10mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION:

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The foam should be discharged to the destination socket before devices are removed.

TERMINOLOGY

RELATIVE ACCURACY

Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale and is normally expressed as a percentage of full-scale range.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the difference between the *measured* change and the *ideal* 1LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB max over the operating temperature range ensures monotonicity.

GAIN ERROR

Gain error or full-scale error is a measure of the output error between an ideal DAC and the actual device output. For the AD7544, ideal full-scale output is V_{REF} - 1LSB. Gain error is adjustable to zero.

DIGITIAL CHARGE INJECTION

The amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA secs or nV secs depending upon whether the glitch is measured as a current or voltage signal. Digitial charge injection is measured with the reference input of the DAC connected to ground.

PROPAGATION DELAY

This is a measure of the internal delays of the circuit and is defined as the time from LDAC going high to the analog output current reaching 90% of its final value for a full-scale change.

FSR

This is an abbreviation for Full Scale Range. For a 12-bit converter with a reference input of 10V the FSR is 10 X (4095/4096) Volts.

OUTPUT LEAKAGE CURRENT

Current which appears at OUT1 with DAC Register loaded to all 0s or at OUT2 with DAC Register loaded to all 1s.

MULTIPLYING FEEDTHROUGH ERROR

AC error due to capacitive feedthrough from V_{REF} terminal to OUT1 with DAC register loaded to all 0s.

Pin No.	Name	Function	Pin No.	Name	Function
1	V_{DD}	+5V Supply	18	D0	Data Input (LSB)
2	V_{REF}	±20V Reference Voltage	19	$\overline{RST}$	Reset, when low resets DAC Register and stack control flip-flops to zero.
3	R_{FB}	DAC Feedback Resistor	20	$\overline{WR}$	Write, with $\overline{WREN}$ low, the trailing edge of $\overline{WR}$ loads data into the lowest available empty register of the stack.
4	I_{OUT1}	Output from R-2R Ladder	21	$\overline{WREN}$	Write Enable.
5	I_{OUT2}	Output from R-2R Ladder	22	SFUL	Stack Full Flag. When HIGH, indicates stack is full. When LOW, indicates less than six words remain in stack.
6	AGND	Analog Ground	23	SAMT	Stack Almost Empty Flag. When HIGH, indicates one word or less remains in the stack. When LOW, indicates more than one word contained in the stack.
7	D11	Data Input (MSB)	24	$\overline{RL}$	Roll, with $\overline{RLEN}$ low the trailing edge of $\overline{RL}$ rolls information down the FIFO stack past the register data-selector.
8	D10	Data Input	25	$\overline{RLEN}$	Roll Enable.
9	D9	Data Input	26	LDAC	Load DAC. Loads information from one of two stack registers into the DAC register (see $W_1/\overline{W}_2$).
10	D8	Data Input	27	$W_1/\overline{W}_2$	WORD1/$\overline{\text{WORD2}}$. A HIGH enables WORD 1 through the data-selector, a LOW enables WORD 2.
11	D7	Data Input	28	DGND	Digital Ground.
12	D6	Data Input			
13	D5	Data Input			
14	D4	Data Input			
15	D3	Data Input			
16	D2	Data Input			
17	D1	Data Input			

Table 1. Pin Function Description

AD7544 OPERATION

The AD7544 FIFO stack consists of six 12-bit Data Registers as shown in the Functional Block Diagram. Internally a Stack Register is considered to be empty if the output from its control flip-flop, FFN (Figure 1), is LOW. After a Reset Signal $\overline{RST}$ all control flip-flops are reset LOW and the DAC Register is loaded with all 0s.

Twelve-bit data is written into the stack by exercising $\overline{WR}$ and $\overline{WREN}$. Initially, this data is latched into the top Register of the stack (Register 6) and the output of the FF6 control flip-flop momentarily goes HIGH. If at this instant the output of FF5 is LOW then FF6 subsequently returns LOW. FF6 returning LOW sets the output of FF5 momentarily HIGH and in doing so loads data from Register 6 into Register 5. This process is repeated down the stack until the input data reaches Register 1, FF1 going HIGH and remaining HIGH. Note that the SAMT flag, which was set HIGH after the Reset $\overline{RST}$, is unchanged. Register 1 is now no longer affected by subsequent write operations. Although all the other Stack Registers have the data of Register 1 in them, their control flip-flops are Low hence this data can be overwritten. The next Write operation initiates a similar sequence of events with data falling through to Register 2. The SAMT flag now goes LOW. After four further Write operations, the SFUL flag is set HIGH indicating the stack is full. See Table 2 and Functional Block Diagram.

By exercising $\overline{RLEN}$ and RL the output of the FF1 Control flip-flop is reset LOW. Register 1 will now appear empty and a roll-down sequence similar to that described above is initiated automatically. The data originally in Register 1 is lost and the SFUL flag is reset LOW. See Table 3 and Figure 1. Although not shown in Table 2 or Table 3 any arbitrary sequence of stack Write and Roll operations is permissible.

Data from Register 1 or Register 2 (selected by W1/$\overline{\text{W2}}$ control) may be loaded into the 12-bit DAC Register by exercising LDAC. See Table 4 and Figure 2. Note that a load DAC operation does not affect word positions in the stack hence stack flags, SFUL and SAMT, remain unchanged. LDAC is a level-triggered (as opposed to edge-triggered) control signal.

WRITE TIMING

The ripple-through nature of the stack leads to an apparent time skew (or delay) between Write signals and valid input data. Due to this delay, the input data to the device need not be valid on the trailing edge of $\overline{WR}$ (the normal constraint when writing) but must be valid some time later, t_{WDS}. This point is illustrated in the Functional Block Diagram. Input data must remain valid for some time after t_{WDS} max to allow the input latches to settle with the correct data. The hold time has been specified from the trailing edge of $\overline{WR}$ to the minimum data settling time required—t_{WDH} min—thus incorporating the internal time skewing. See Functional Block Diagram.

SAMT FLAG TIMING

Referring to the AD7544 Functional Diagram, the Stack Almost Empty (SAMT) flag is derived from a five-input NOR gate monitoring control flip-flops FF2 through FF6. After a $\overline{RST}$ signal all control flip-flop outputs are reset LOW and the SAMT flag is HIGH. When the first 12-bit word is written to the top of the stack, Register 6 control flip-flop momentarily goes HIGH as previously explained. The SAMT flag will go LOW and remain LOW while the word propagates down the stack. When the input data is finally latched in the Register 1 position, flip-flops FF2 through FF6 are again LOW and the SAMT flag will return HIGH. When the second word is written to the top of the stack, SAMT goes LOW and remains LOW since the word will fall-through to Register 2, FF2 going HIGH and remaining HIGH. Notice that SAMT flag behavior is dependent upon the Write frequency. If the time between Write cycles is less than the stack propagation delay (typ 2μs), then the SAMT flag will go LOW after the first $\overline{WR}$ signal and remain LOW since the next word will start falling-through before the first word has reached Register 1. If the SAMT flag is used as an interrupting input to the system microprocessor (rising edge triggered), the interrupt input should be masked during writing to avoid an erroneous interrupt call. During roll operations the interrupt mask should be removed since there is no possibility of glitches on the flag output.

STACK OPERATIONS—WRITING TO THE FIFO STACK

	FIFO Stack Control Inputs					Data Input	Resulting Stack Register Contents						Output Flags	
Operation	$\overline{\text{RLEN}}$	$\overline{\text{RL}}$	$\overline{\text{WREN}}$	$\overline{\text{WR}}$	$\overline{\text{RST}}$	D0-D11	R6	R5	R4	R3	R2	R1	SFUL	SAMT
Clear DAC Latch, Reset Stack F/Fs	X	X	X	X	0	X	Ⓧ	Ⓧ	Ⓧ	Ⓧ	Ⓧ	Ⓧ	0	1
Write Word A into Stack	1	X	0	↑	1	A	Ⓐ	Ⓐ	Ⓐ	Ⓐ	Ⓐ	A	0	1
Write Word B into Stack	1	X	0	↑	1	B	Ⓑ	Ⓑ	Ⓑ	Ⓑ	B	A	0	↓
Write Word C into Stack	1	X	0	↑	1	C	Ⓒ	Ⓒ	Ⓒ	C	B	A	0	0
Write Word D into Stack	1	X	0	↑	1	D	Ⓓ	Ⓓ	D	C	B	A	0	0
Write Word E into Stack	1	X	0	↑	1	E	Ⓔ	E	D	C	B	A	0	0
Write Word F into Stack	1	X	0	↑	1	F	F	E	D	C	B	A	↑	0
Write Word G into Stack	1	X	0	↑	1	G	F	E	D	C	B	A	1	0

NOTES
1 indicates logic HIGH
0 indicates logic LOW
X indicates "don't care"

Ⓧ, Ⓐ, Ⓑ etc. indicates data which can be overwritten
↑ indicates LOW to HIGH transition
↓ indicates HIGH to LOW transition

Table 2. Truth Table for Stack Write Operations

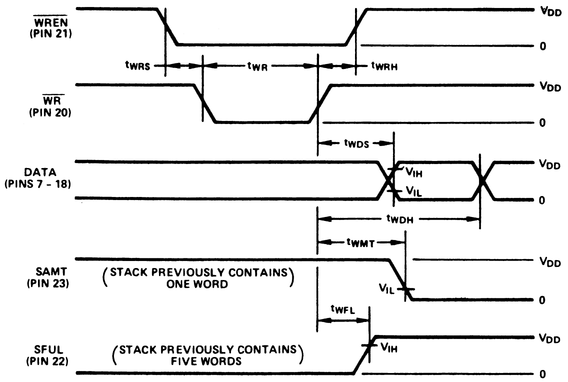

$\overline{\text{WREN}}$ (PIN 21)
VDD
0
tWRS
tWR
tWRH
$\overline{\text{WR}}$ (PIN 20)
VDD
0
tWDS
DATA (PINS 7 - 18)
VIH
VIL
VDD
0
tWDH
tWMT
SAMT (PIN 23)
(STACK PREVIOUSLY CONTAINS ONE WORD)
VIL
VDD
0
tWFL
SFUL (PIN 22)
(STACK PREVIOUSLY CONTAINS FIVE WORDS)
VIH
VDD
0

Figure 1. Timing Diagram for Write Operations

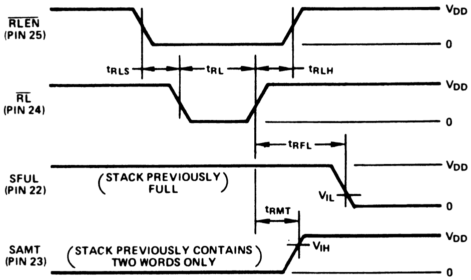

$\overline{\text{RLEN}}$ (PIN 25)
VDD
0
tRLS
tRL
tRLH
$\overline{\text{RL}}$ (PIN 24)
VDD
0
tRFL
SFUL (PIN 22)
(STACK PREVIOUSLY FULL)
VIL
VDD
0
tRMT
SAMT (PIN 23)
(STACK PREVIOUSLY CONTAINS TWO WORDS ONLY)
VIH
VDD
0

Figure 2. Timing Diagram for Stack Roll Operations

ROLLING THE FIFO STACK

	FIFO Stack Control Inputs					Data Input	Resulting Stack Register Contents						Output Flags	
Operation	$\overline{\text{RLEN}}$	$\overline{\text{RL}}$	$\overline{\text{WREN}}$	$\overline{\text{WR}}$	$\overline{\text{RST}}$	D0 - D11	R6	R5	R4	R3	R2	R1	SFUL	SAMT
Roll Down[1]	0	↑	1	X	1	X	Ⓕ	F	E	D	C	B	↓	0
Roll Down	0	↑	1	X	1	X	Ⓕ	Ⓕ	F	E	D	C	0	0
Roll Down	0	↑	1	X	1	X	Ⓕ	Ⓕ	Ⓕ	F	E	C	0	0
Roll Down	0	↑	1	X	1	X	Ⓕ	Ⓕ	Ⓕ	Ⓕ	F	E	0	0
Roll Down	0	↑	1	X	1	X	Ⓕ	Ⓕ	Ⓕ	Ⓕ	Ⓕ	F	0	↑
Roll Down	0	↑	1	X	1	X	Ⓕ	Ⓕ	Ⓕ	Ⓕ	Ⓕ	Ⓕ	0	1
Roll Down	0	↑	1	X	1	X	Ⓕ	Ⓕ	Ⓕ	Ⓕ	Ⓕ	Ⓕ	0	1

Note
[1] Initially stack registers R1 to R6 contain words A to F respectively.
See Table 2 notes.

Table 3. Truth Table for Stack Roll Operations

LOADING THE DAC

	DAC Control Inputs			
Operation	W1/$\overline{\text{W2}}$	LDAC	$\overline{\text{RST}}$	DAC Output
Load DAC Register with all "0"s	X	X	0	Unipolar Mode; Output Assumes 0V Bipolar Mode; Output Assumes $-V_{REF}$
Load DAC Register from Word 1 Register	1	1	1	DAC Converts Word 1
Load DAC Register from Word 2 Register	0	1	1	DAC Converts Word 2

Table 4. Truth Table for DAC Register Loading

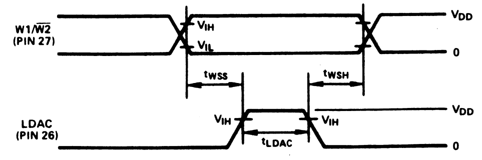


Figure 3. Timing Diagram for DAC Register Loading

NOTE: All input signal rise and fall times measured from 10% to 90% of V_{DD}, $t_r = t_f = 20ns$. Timing Measurement Reference level is $\frac{V_{IH} + V_{IL}}{2}$

APPLYING THE AD7544

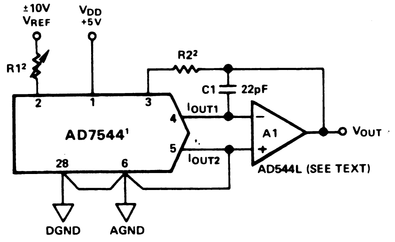
UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 4 shows the analog circuit connections required for unipolar binary (2-quadrant multiplication) operation. The logic inputs are omitted for clarity. With a dc reference voltage or current (positive or negative polarity) applied at pin 2, the circuit is a unipolar D/A converter. With an ac reference voltage or current the circuit provides 2-quadrant multiplication (digitally controlled attenuation). The input/output relationship is shown in Table 5.

R1 provides full scale trim capability [i.e.—load the DAC register to 1111 1111 1111, adjust R1 for $V_{OUT} = -V_{REF}$ (4095/4096)]. Alternatively, Full Scale can be adjusted by omitting R1 and R2 and trimming the reference voltage magnitude.

Phase compensation capacitor C1 (10 to 25pF) may be required for stability when using high speed amplifiers. This capacitor cancels the pole formed by the DAC internal feedback resistance and output capacitance at OUT1.

Amplifier A1 should be selected or trimmed to provide $V_{OS} \leqslant 10\%$ of the voltage resolution at V_{OUT}. Additionally, the amplifier should exhibit a bias current which is low over the temperature range of interest. Bias current causes an output offset at V_{OUT} equal to I_B times the DAC feedback resistance (nominally 15kΩ). The AD544L is a high-speed implanted FET-input op amp with low, factory-trimmed V_{OS}, and low I_B.



NOTES: 1. LOGIC INPUTS OMITTED FOR CLARITY
2. SEE APPLICATION HINT NUMBER 4

Figure 4. Unipolar Binary Operation (2-Quadrant Multiplication)

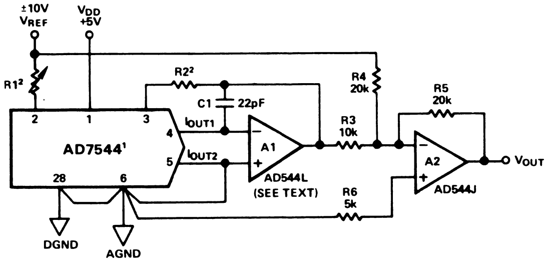
BINARY NUMBER IN DAC REGISTER MSB LSB	ANALOG OUTPUT, V_{OUT}
1111 1111 1111	$-V_{REF}\left(\frac{4095}{4096}\right)$
1000 0000 0000	$-V_{REF}\left(\frac{2048}{4096}\right) = -1/2\ V_{REF}$
0000 0000 0001	$-V_{REF}\left(\frac{1}{4096}\right)$
0000 0000 0000	0V

Table 5. Unipolar Binary Code Table for Circuit of Figure 4

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

Figure 5 and Table 6 illustrate the circuitry and code relationship for bipolar operation. With a dc reference (positive or negative polarity) the circuit provides offset binary operation. With an ac reference, the eleven LSBs provide digitally controlled attenuation of the ac reference while the MSB provides polarity control.

With the DAC register loaded to 1000 0000 0000, adjust R1 for $V_{OUT} = 0V$ (alternatively, one can omit R1 and R2 and adjust the ratio of R3 to R4 for $V_{OUT} = 0V$). Full scale trimming can be accomplished by adjusting the amplitude of V_{REF} or by varying the value of R5.



NOTES: 1. LOGIC INPUTS OMITTED FOR CLARITY
2. SEE APPLICATION HINT NUMBER 4

Figure 5. Bipolar Operation (4-Quadrant Multiplication)

As in unipolar operation, A1 must be chosen for low V_{OS} and low I_B. R3, R4 and R5 must be selected for matching and tracking. Mismatch of 2R3 to R4 causes both offset and Full Scale error. Mismatch of R5 to R4 and 2R3 causes Full Scale error. C1 phase compensation (10 to 25pF) may be required for stability.

BINARY NUMBER IN DAC REGISTER MSB LSB	ANALOG OUTPUT, V_{OUT}
1111 1111 1111	$+V_{REF}\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{REF}\left(\frac{1}{2048}\right)$
1000 0000 0000	0V
0111 1111 1111	$-V_{REF}\left(\frac{1}{2048}\right)$
0000 0000 0000	$-V_{REF}\left(\frac{2048}{2048}\right)$

Table 6. Bipolar Code Table for Offset Binary Circuit of Figure 5

CRT VECTOR GENERATION

The AD7544 can be used for vector generation in real-time CRT displays and intelligent X-Y plotters. Figures 6 and 7 show the waveforms and circuitry for a vector stroke or vector refresh display which generates a graphic display vector by vector. This is achieved by adding a linear ramp voltage to each starting point coordinate; the amplitude of this ramp being the difference between the start and finish coordinates of the vector. Two AD7544s are required for each axis. The fifth AD7544 in Figure 7 controls the CRT Z-mod input to vary the vector intensity with vector length; the intensity data having been previously computed.

Consider the two X-channel FIFO Registers of XDAC1 and XDAC2 to be simultaneously loaded with X axis coordinates. Word 1 (X1) of XDAC1 and Word 2 (X2) of XDAC2 are selected via the hard wired $W1/\overline{W2}$ control inputs. Hence the A1 output, after loading the DAC registers is,

$$V_{OX} = -X1\ (V_{REF1})\ -X2\ (V_{REF2})$$

V_{REF1} and V_{REF2} are the reference voltages for XDAC1 and XDAC2 respectively;

$$V_{REF1} = V_{FS} - V(t)$$

and $V_{REF2} = V(t)$

where V_{FS} is the required full scale output voltage and V(t) is a positive ramp voltage of period T and maximum amplitude of V_{FS}. See waveforms of Figure 6.

Now $V_{OX} = -X1\ (V_{FS}) + V(t)\ (X1 - X2)$
at t = 0; V(t) = 0

and $V_{OX} = -X1\ (V_{FS})$

at t = T; $V(t) = V_{FS}$

and $V_{OX} = -X2\ (V_{FS})$

Thus a vector has been generated between X1 and X2. To generate the next vector between X2 and X3 the reference ramp is reset, both AD7544 stacks are rolled and their DAC registers subsequently loaded. The output voltage is now

$$V_{OX} = -X2\ (V_{REF1}) - X3\ (V_{REF2})$$

Operation of the two Y-channel AD7544s is identical to the above. During vector generation the constant reference voltage to the Z-mod AD7544 is multiplied by the appropriate brightness data in its DAC register. During ramp resetting and DAC register loading the polarity of this reference voltage is changed causing screen blanking.

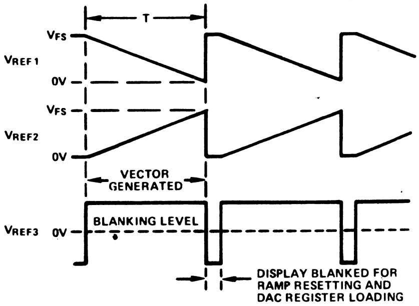


Figure 6. CRT Vector Generation Waveforms

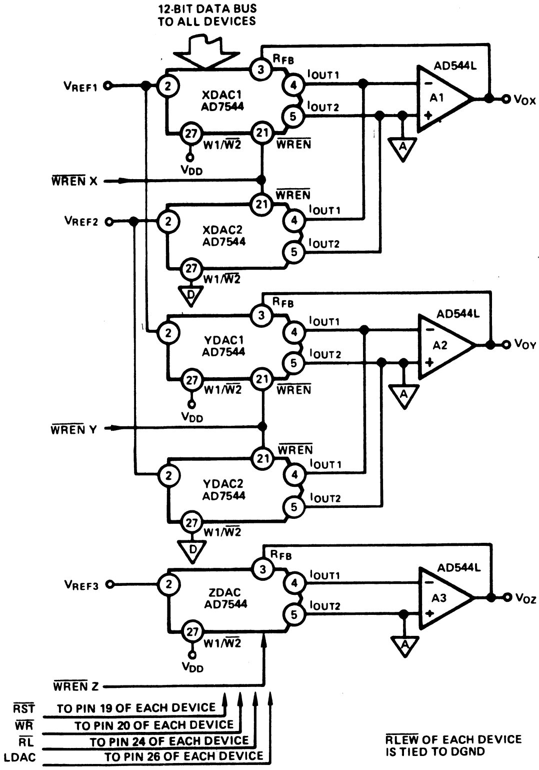

12-BIT DATA BUS TO ALL DEVICES
VREF1
RFB
IOUT1
IOUT2
XDAC1 AD7544
W1/W2
WREN
VDD
AD544L
A1
VOX
WREN X
VREF2
XDAC2 AD7544
YDAC1 AD7544
AD544L
A2
VOY
WREN Y
YDAC2 AD7544
VREF3
ZDAC AD7544
AD544L
A3
VOZ
WREN Z
RST TO PIN 19 OF EACH DEVICE
WR TO PIN 20 OF EACH DEVICE
RL TO PIN 24 OF EACH DEVICE
LDAC TO PIN 26 OF EACH DEVICE
RLEW OF EACH DEVICE IS TIED TO DGND

Figure 7. CRT Vector Generation Application

APPLICATION HINTS

The AD7544 is a precision 12-bit multiplying DAC designed for system interface. For a detailed description of multiplying DACs the reader is referred to Analog Devices "Application Guide to CMOS Multiplying D/A Converters". To ensure system performance consistent with AD7544 specifications, careful attention must be given to the following points:

1. GENERAL GROUND MANAGEMENT: Voltage differences between the AD7544 AGND and DGND cause loss of accuracy (dc voltage difference between the grounds introduces gain error. AC or transient voltages between the grounds cause noise injection into the analog output). The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7544. In more complex systems where the AGND - DGND intertie is on the back-plane, it is recommended that diodes be connected back-to-back between the AD7544 AGND and DGND pins (1N914 or equivalent).
2. OUTPUT AMPLIFIER OFFSET: CMOS DACs exhibit a code-dependent output resistance which in turn causes a code-dependent amplifier noise gain. The effect is a differential nonlinearity term at the amplifier output of magnitude $0.67V_{OS}$ (V_{OS} is amplifier input offset voltage). This differential nonlinearity term adds to the R/2R differential nonlinearity. To maintain monotonic operation, it is recommended the amplifier V_{OS} be no greater than 10% of the DAC's output resolution over the temperature range of interest [output resolution = $V_{REF}(2^{-n})$ where n is the number of bits exercised].
3. HIGH FREQUENCY CONSIDERATIONS: AD7544 output capacitance works in conjunction with the amplifier feedback resistance to add a pole to the open loop response. This not only reduces closed loop bandwidth, but can also cause ringing or oscillation if the spurious pole frequency is less than the amplifier's 0dB crossover frequency. Stability can be restored by adding a phase compensation capacitor in parallel with the feedback resistor.
4. GAIN TEMPERATURE COEFFICIENTS: The gain temperature coefficient of the AD7544 has a maximum value of 5ppm/°C and a typical value of 2ppm/°C. This corresponds to gain shifts of 2.0LSBs and 0.82LSBs respectively over a 100°C temperature range. When trim resistors are used to adjust full-scale range as shown in Figures 5 and 6 the temperature coefficient of R1 and R2 should be taken into account. It may be shown that the additional gain temperature coefficients introduced by R1 and R2 may be approximately expressed as follows:—

$$\text{Temperature Coefficient contribution due to R1} = -\frac{R_1}{R_{IN}}(\gamma_1 + 300)$$

$$\text{Temperature Coefficient contribution due to R2} = +\frac{R_2}{R_{IN}}(\gamma_2 + 300)$$

Where γ_1 and γ_2 are the temperature coefficients in ppm/°C of R1 and R2 respectively and R_{IN} is the DAC input resistance at the V_{REF} terminal (pin 2). For high quality wirewound resistors and trimming potentiometers γ is of the order of 50ppm/°C. It will be seen that if R1 and R2 are small compared with R_{IN}, their contribution to gain temperature coefficient will also be small. For the standard AD7544 gain error specification of ±12.3LSBs it is recommended that R1 = 120Ω and R2 = 60Ω. With $\gamma = 50$ these values result in an overall maximum gain error temperature coefficient of:

$$5 + \frac{0.06}{7}(50 + 300) = 8\text{ppm}/^\circ\text{C}$$

However, if the "G" version of the AD7544 is used which has a specified gain error of ±1LSB, then with R1 = 10Ω and R2 = 5Ω the overall maximum gain temperature coefficient is increased by only 0.25ppm/°C.

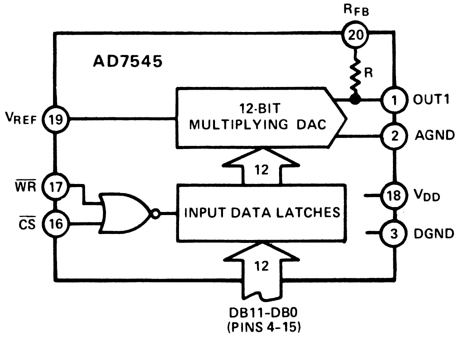
ANALOG DEVICES

CMOS 12-Bit Buffered Multiplying DAC

AD7545

FEATURES
- **12-Bit Resolution**
- **Low Gain T.C.: 2ppm/°C typ**
- **Fast TTL Compatible Data Latches**
- **Single +5V to +15V Supply**
- **Small 20-Pin 0.3" DIP**
- **Latch Free (Schottky Protection Diode Not Required)**
- **Low Cost**
- **Ideal for Battery Operated Equipment**

AD7545 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7545 is a monolithic 12-bit CMOS multiplying DAC with on-board data latches. It is loaded by a single 12-bit wide word and interfaces directly to most 12- and 16-bit bus systems. Data is loaded into the input latches under the control of the $\overline{CS}$ and $\overline{WR}$ inputs; tying these control inputs low makes the input latches transparent allowing direct unbuffered operation of the DAC.

The AD7545 is particularly suitable for single supply operation and applications with wide temperature variations.

The AD7545 can be used with any supply voltage from +5V to +15V. With CMOS logic levels at the inputs the device dissipates less than 0.5mW for V_{DD} = +5V.

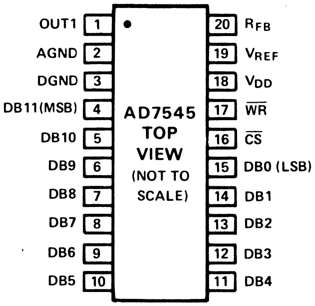
ORDERING INFORMATION

Relative Accuracy	Maximum Gain Error T_A = +25°C V_{DD} = +5V	Temperature Range 0 to +70°C	-25°C to +85°C[1]	-55°C to +125°C[1]
±2LSB	±20LSB	AD7545JN	AD7545AQ	AD7545SD
±1LSB	±10LSB	AD7545KN	AD7545BQ	AD7545TD
±1/2LSB	±5LSB	AD7545LN	AD7545CQ	AD7545UD
±1/2LSB	±1LSB	AD7545GLN	AD7545GCQ	AD7545GUD

NOTE:

[1] 883B version is available. To order add "/883B" to part number shown.

PIN CONFIGURATION



PACKAGE IDENTIFICATION[1,2]

Suffix "N": Plastic[3] DIP – (N20A)
Suffix "Q": Cerdip[4] – (Q20B)
Suffix "D": Ceramic DIP – (D20B)

NOTES

[1] See Section 20 for package outline information.

[2] Analog Devices is offering the AD7545 in chip carriers, for further information contact the factory.

[3] Plastic encapsulated units will be available by early 1982.

[4] Analog Devices reserves the right to ship ceramic packages in lieu of Cerdip packages.

SPECIFICATIONS (V_{REF} = +10V, V_{OUT1} = 0V, AGND = DGND unless otherwise specified)

Parameter	Version	V_{DD} = +5V Limits		V_{DD} = +15V Limits		Units	Test Conditions/Comments
		T_A = +25°C	T_{min}, T_{max}[1]	T_A = +25°C	T_{min}, T_{max}[1]		
STATIC PERFORMANCE							
Resolution	All	12	12	12	12	Bits	
Relative Accuracy	J, A, S	±2	±2	±2	±2	LSB max	
	K, B, T	±1	±1	±1	±1	LSB max	
	L, C, U	±1/2	±1/2	±1/2	±1/2	LSB max	
	GL, GC, GU	±1/2	±1/2	±1/2	±1/2	LSB max	
Differential Nonlinearity	J, A, S	±4	±4	±4	±4	LSB max	10-Bit Monotonic T_{min} to T_{max}
	K, B, T	±1	±1	±1	±1	LSB max	12-Bit Monotonic T_{min} to T_{max}
	L, C, U	±1	±1	±1	±1	LSB max	12-Bit Monotonic T_{min} to T_{max}
	GL, GC, GU	±1	±1	±1	±1	LSB max	12-Bit Monotonic T_{min} to T_{max}
Gain Error (Using Internal RFB)[2]	J, A, S	±20	±20	±25	±25	LSB max	DAC Register Loaded with
	K, B, T	±10	±10	±15	±15	LSB max	1111 1111 1111
	L, C, U	±5	±6	±10	±10	LSB max	Gain Error is Adjustable Using
	GL, GC, GU	±1	±2	±6	±7	LSB max	the Circuits of Figures 4, 5 and 6
Gain Temperature Coefficient[3] ΔGain/ΔTemperature	All	±5	±5	±10	±10	ppm/°C max	Typical Value is 2ppm/°C for V_{DD} = +5V
DC Supply Rejection[3] ΔGain/ΔV_{DD}	All	0.015	0.03	0.01	0.02	% per % max	ΔV_{DD} = ±5%
Output Leakage Current at OUT1	J, K, L, GL	10	50	10	50	nA max	DB0–DB11 = 0V; $\overline{WR}$, $\overline{CS}$ = 0V
	A, B, C, GC	10	50	10	50	nA max	
	S, T, U, GU	10	200	10	200	nA max	
DYNAMIC PERFORMANCE							
Propagation Delay[3] (from Digital Input Change to 90% of final Analog Output)	All	300	–	250	–	ns max	OUT1 LOAD = 100Ω C_{EXT} = 13pF[4]
Digital Charge Injection	All	400	–	250	–	nV sec typ	V_{REF} = AGND
AC Feedthrough[5] At I_{OUT1}	All	5	5	5	5	mV p-p typ	V_{REF} = ±10V, 10kHz Sine Wave:
REFERENCE INPUT							
Input Resistance (Pin 19 to GND)	All	7	7	7	7	kΩ min	Input Resistance TC = –300ppm/°C max
		25	25	25	25	kΩ max	Typical Input Resistance = 11kΩ
ANALOG OUTPUTS							
Output Capacitance[3] C_{OUT1}	All	70	70	70	70	pF max	DB0–DB11 = 0V, $\overline{WR}$, $\overline{CS}$ = 0V
C_{OUT1}	All	200	200	200	200	pF max	DB0–DB11 = V_{DD}, $\overline{WR}$, $\overline{CS}$ = 0V
DIGITAL INPUTS							
Input High Voltage V_{IH}	All	2.4	2.4	13.5	13.5	V min	
Input Low Voltage V_{IL}	All	0.8	0.8	1.5	1.5	V max	
Input Current[6] I_{IN}	All	±1	±10	±1	±10	μA max	V_{IN} = 0 or V_{DD}
Input Capacitance[3] DB0–DB11	All	5	5	5	5	pF max	V_{IN} = 0
$\overline{WR}$, $\overline{CS}$	All	20	20	20	20	pF max	V_{IN} = 0
SWITCHING CHARACTERISTICS[7]							
Chip Select to Write Setup Time t_{CS}	All	280	380	180	200	ns min	See Timing Diagram
		200	270	120	150	ns typ	
Chip Select to Write Hold Time t_{CH}	All	0	0	0	0	ns min	
Write Pulse Width t_{WR}	All	250	400	160	240	ns min	$t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$
		175	280	100	170	ns typ	
Data Setup Time t_{DS}	All	140	210	90	120	ns min	
		100	150	60	80	ns typ	
Data Hold Time t_{DH}	All	10	10	10	10	ns min	
POWER SUPPLY							
I_{DD}	All	2	2	2	2	mA max	All Digital Inputs V_{IL} or V_{IH}
		100	500	100	500	μA max	All Digital Inputs 0V or V_{DD}
		10	10	10	10	μA typ	All Digital Inputs 0V or V_{DD}

NOTES

[1] Temperature Ranges as follows:
JN, KN, LN, GLN: 0 to +70°C
AQ, BQ, CQ, GCQ: –25°C to +85°C
ST, TD, UD, GUD: –55°C to +125°C

[2] This includes the effect of 5ppm max gain TC.

[3] Guaranteed but not tested.

[4] DB0–DB11 = 0V to V_{DD} or V_{DD} to 0V.

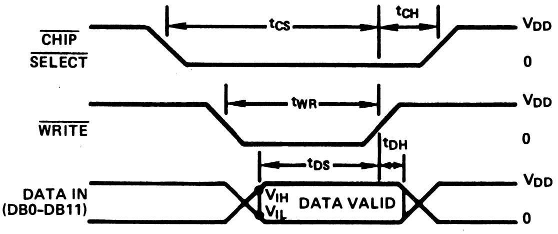
[5] Feedthrough can be further reduced by connecting the metal lid on the ceramic package (suffix D) to DGND.

[6] Logic inputs are MOS gates. Typical input current (+25°C) is less than 1nA.

[7] Sample tested at +25°C to ensure compliance.

Specifications subject to change without notice.

WRITE CYCLE TIMING DIAGRAM



MODE SELECTION

WRITE MODE:	HOLD MODE:
$\overline{\text{CS}}$ and $\overline{\text{WR}}$ low, DAC responds to data bus (DB0-DB11) inputs.	Either $\overline{\text{CS}}$ or $\overline{\text{WR}}$ high, data bus (DB0-DB11) is locked out; DAC holds last data present when $\overline{\text{WR}}$ or $\overline{\text{CS}}$ assumed high state.

NOTES:
$V_{DD} = +5V$; $t_r = t_f = 20ns$
$V_{DD} = +15V$; $t_r = t_f = 40ns$
All input signal rise and fall times measured from 10% to 90% of V_{DD}.
Timing measurement reference level is $\frac{V_{IH} + V_{IL}}{2}$.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to DGND . . . . -0.3V, +17V
Digital Input Voltage to DGND . . . . -0.3V, V_{DD}
V_{RFB}, V_{REF} to DGND . . . . ±25V
V_{PIN1} to DGND . . . . -0.3V, V_{DD}
AGND to DGND . . . . -0.3V, V_{DD}
Power Dissipation (Any Package) to 75°C 450mW
Derates above 75°C by . . . . 6mW/°C
Operating Temperature
Commercial (JN, KN, LN, GLN) Grades . . . . . 0 to +70°C
Industrial (AQ, BQ, CQ, GCQ) Grades . . . . -25°C to +85°C
Military (SD, TD, UD, GUD) Grades . . . . -55°C to +125°C
Storage Temperature . . . . -65°C to +150°C
Lead Temperature (Soldering 10 Seconds) . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to above maximum rating conditions for extended periods may affect device reliability.

CAUTION:

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

TERMINOLOGY

RELATIVE ACCURACY: The amount by which the D/A converter transfer function differs from the ideal transfer function after the zero and full scale points have been adjusted. This is an end point linearity measurement.

DIFFERENTIAL NONLINEARITY: The difference between the measured change and the ideal change between any two adjacent codes. If a device has a differential nonlinearity of less than 1LSB then it will be monotonic, i.e., the output will always increase for an increase in digital code applied to the D/A converter.

PROPAGATION DELAY: This is a measure of the internal delay of the circuit and is measured from the time a digital input changes to the point at which the analog output at OUT1 reached 90% of its final value.

DIGITAL CHARGE INJECTION: This is a measure of the amount of charge injected from the digital inputs to the analog outputs when the inputs change state. It is usually specified as the area of the glitch in nVecs and is measured with V_{REF} = AGND and an ADLH0032CG as the output op amp, C1 (phase compensation) = 33pF.

CIRCUIT INFORMATION – D/A CONVERTER SECTION

Figure 1 shows a simplified circuit of the D/A converter section of the AD7545 and Figure 2 gives an approximate equivalent circuit. Note that the ladder termination resistor is connected to AGND. R is typically 11kΩ.

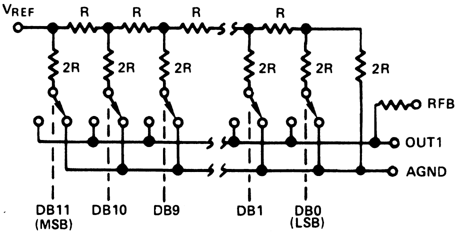


Figure 1. Simplified D/A Circuit of AD7545

The binary weighted currents are switched between the OUT1 bus line and AGND by N-channel switches, thus maintaining a constant current in each ladder leg independent of the switch state.

The capacitance at the OUT1 bus line, C_{OUT1}, is code dependent and varies from 70pF (all switches to AGND) to 200pF (all switches to OUT1).

One of the current switches is shown in Figure 2. The input resistance at V_{REF} (Figure 1) is always equal to R_{LDR} (R_{LDR} is the R/2R ladder characteristic resistance and is equal to value "R"). Since R_{IN} at the V_{REF} pin is constant, the reference terminal can be driven by a reference voltage or a reference current, ac or dc, of positive or negative polarity. (If a current source is used, a low temperature coefficient external R_{FB} is recommended to define scale factor.)

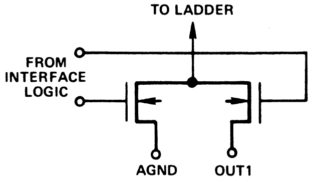


Figure 2. N-Channel Current Steering Switch

CIRCUIT INFORMATION–DIGITAL SECTION

Figure 3 shows the digital structure for one bit.

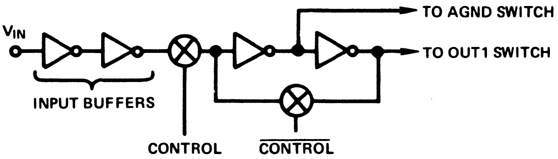


Figure 3. Digital Input Structure

The digital signals CONTROL and $\overline{\text{CONTROL}}$ are generated from $\overline{\text{CS}}$ and $\overline{\text{WR}}$.

The input buffers are simple CMOS inverters designed such that when the AD7545 is operated with V_{DD} = 5V, the buffers convert TTL input levels (2.4V and 0.8V) into CMOS logic levels. When V_{IN} is in the region of 2.0 volts to 3.5 volts the input buffers operate in their linear region and draw current from the power supply. To minimize power supply currents it is recommended that the digital input voltages be as close to the supply rails (V_{DD} and DGND) as is practically possible.

The AD7545 may be operated with any supply voltage in the range $5 \leqslant V_{DD} \leqslant 15$ volts. With V_{DD} = +15V the input logic levels are CMOS compatible only, i.e., 1.5V and 13.5V.

BASIC APPLICATIONS

Figures 4 and 5 show simple unipolar and bipolar circuits using the AD7545. Resistor R1 is used to trim for full scale. The "G" versions (AD7545GLN, AD7545GCQ, AD7545GUD) have a guaranteed maximum gain error of ±1LSB at +25°C (V_{DD} = +5V) and in many applications it should be possible to dispense with gain trim resistors altogether. Capacitor C1 provides phase compensation and helps prevent overshoot and ringing when using high speed op amps. Note that all the circuits of Figures 4, 5 and 6 have constant input impedance at the V_{REF} terminal.

The circuit of Figure 4 can either be used as a fixed reference D/A converter so that it provides an analog output voltage in the range 0 to $-V_{IN}$ (note the inversion introduced by the op amp) or V_{IN} can be an ac signal in which case the circuit behaves as an attenuator (2-Quadrant Multiplier). V_{IN} can be any voltage in the range $-20 \leqslant V_{IN} \leqslant +20$ volts (provided the op amp can handle such voltages) since V_{REF} is permitted to exceed V_{DD}. Table 2 shows the code relationship for the circuit of Figure 4.

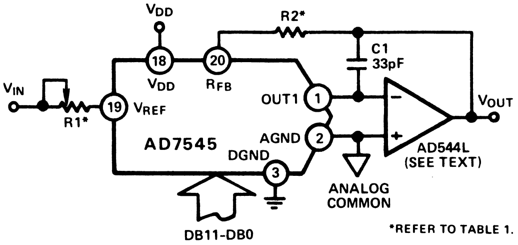


Figure 4. Unipolar Binary Operation

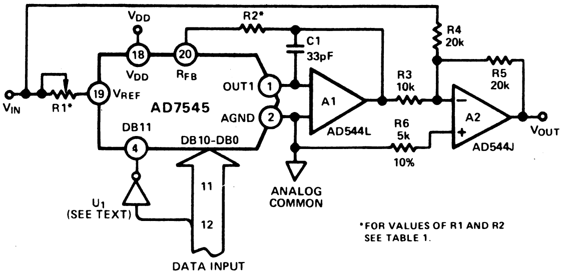
TRIM RESISTOR	JN/AQ/SD	KN/BQ/TD	LN/CQ/TD	GLN/GCQ/GUD
R1	500Ω	100Ω	50Ω	10Ω
R2	100Ω	47Ω	22Ω	4.7Ω

Table 1. Recommended Trim Resistor Values vs. Grades

Binary Number in DAC Register	Analog Output
1111 1111 1111	$-V_{IN}\left\{\frac{4095}{4096}\right\}$
1000 0000 0000	$-V_{IN}\left\{\frac{2048}{4096}\right\} = -1/2\ V_{IN}$
0000 0000 0001	$-V_{IN}\left\{\frac{1}{4096}\right\}$
0000 0000 0000	0 Volts

Table 2. Unipolar Binary Code Table for Circuit of Figure 4

Figure 5 and Table 3 illustrate the recommended circuit and code relationship for bipolar operation. The D/A function itself uses offset binary code and inverter U_1 on the MSB line converts 2's complement input code to offset binary code. If appropriate, inversion of the MSB may be done in software using an exclusive -OR instruction and the inverter omitted. R3, R4 and R5 must be selected to match within 0.01% and they should be the same type of resistor (preferably wirewound or metal foil), so that their temperature coefficients match. Mismatch of R3 value to R4 causes both offset and full scale error. Mismatch of R5 to R4 and R3 causes full scale error.



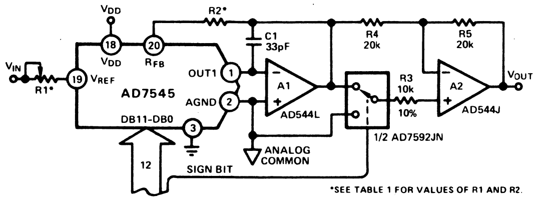
*FOR VALUES OF R1 AND R2 SEE TABLE 1.

Figure 5. Bipolar Operation (2's Complement Code)

Data Input	Analog Output
0111 1111 1111	$+V_{IN} \cdot \left\{\frac{2047}{2048}\right\}$
0000 0000 0001	$+V_{IN} \cdot \left\{\frac{1}{2048}\right\}$
0000 0000 0000	0 Volts
1111 1111 1111	$-V_{IN} \cdot \left\{\frac{1}{2048}\right\}$
1000 0000 0000	$-V_{IN} \cdot \left\{\frac{2048}{2048}\right\}$

Table 3. 2's Complement Code Table for Circuit of Figure 5

Figure 6 shows an alternative method of achieving bipolar output. The circuit operates with sign plus magnitude code and has the advantage that it gives 12-bit resolution in each quadrant compared with 11-bit resolution per quadrant for the circuit of Figure 5. The AD7592 is a fully protected CMOS change-over switch with data latches. R4 and R5 should match each other to 0.01% to maintain the accuracy of the D/A converter. Mismatch between R4 and R5 introduces a gain error.



*SEE TABLE 1 FOR VALUES OF R1 AND R2.

Figure 6. 12-Bit Plus Sign Magnitude D/A Converter

Sign Bit	Binary Numbers in DAC Register	Analog Output
0	1111 1111 1111	$+V_{IN} \cdot \left\{\frac{4095}{4096}\right\}$
0	0000 0000 0000	0 Volts
1	0000 0000 0000	0 Volts
1	1111 1111 1111	$-V_{IN} \cdot \left\{\frac{4095}{4096}\right\}$

Note: Sign bit of "0" connects R3 to GND.

Table 4. 12-Bit Plus Sign Magnitude Code Table for Circuit of Figure 6.

APPLICATIONS HINTS

Output Offset: CMOS D/A converters exhibit a code dependent output resistance which in turn can cause a code dependent error voltage at the output of the amplifer. The maximum amplitude of this offset, which adds to the D/A converter nonlinearity, is 0.67 V_{OS} where V_{OS} is the amplifier input offset voltage. To maintain monotonic operation it is recommended that V_{OS} be no greater than (25×10^{-6}) (V_{REF}) over the temperature range of operation. Suitable op amps are AD517L and AD544L. The AD517L is best suited for fixed reference applications with low bandwidth requirements: it has extremely low offset (50μV) and in most applications will not require an offset trim. The AD544L has a much wider bandwidth and higher slew rate and is recommended for multiplying and other applications requiring fast settling. An offset trim on the AD544L may be necessary in some circuits.

General Ground Management: AC or transient voltages between AGND and DGND can cause noise injection into the analog output. The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7545. In more complex systems where the AGND and DGND intertie is on the backplane, it is recommended that two diodes be connected in inverse parallel between the AD7545 AGND and DGND pins (1N914 or equivalent).

Digital Glitches: When $\overline{WR}$ and $\overline{CS}$ are both low the latches are transparent and the D/A converter inputs follow the data inputs. In some bus systems, data on the data bus is not always valid for the whole period during which $\overline{WR}$ is low and as a result invalid data can briefly occur at the D/A converter inputs during a write cycle. Such invalid data can cause unwanted glitches at the output of the D/A converter. The solution to this problem, if it occurs, is to retime the write pulse $\overline{WR}$ so that it only occurs when data is valid.

Another cause of digital glitches is capacitive coupling from the digital lines to the OUT1 and AGND terminals. This should be minimized by screening the analog pins of the AD7545 (Pins 1, 2, 19, 20) from the digital pins by a ground track run between pins 2 and 3 and between pins 18 and 19 of the AD7545. Note how the analog pins are at one end of the package and separated from the digital pins by V_{DD} and DGND to aid screening at the board level. On-chip capacitive coupling can also give rise to crosstalk from the digital to analog sections of the AD7545, particularly in circuits with high currents and fast rise and fall times. This type of crosstalk is minimized by using V_{DD} = +5 volts. However, great care should be taken to ensure that the +5V used to power the AD7545 is free from digitally induced noise.

Temperature Coefficients: The gain temperature coefficient of the AD7545 has a maximum value of 5ppm/°C and a typical value of 2ppm/°C. This corresponds to worst case gain shifts of 2LSBs and 0.8LSBs respectively over a 100°C temperature range. When trim resistors R1 and R2 are used to adjust full scale range, the temperature coefficient of R1 and R2 should also be taken into account. The reader is referred to Analog Devices Application Note "Gain Error and Gain Temperature Coefficient of CMOS Multiplying DACs", Publication Number E630–10–6/81.

SINGLE SUPPLY OPERATION

The ladder termination resistor of the AD7545 (Figure 1) is connected to AGND. This arrangement is particularly suitable for single supply operation because OUT 1 and AGND may be biased at any voltage between DGND and V_{DD}. OUT1 and AGND should never go more than 0.3 volts less than DGND or an internal diode will be turned on and a heavy current may flow which will damage the device. (The AD7545 is, however, protected from the SCR latch-up phenomenon prevalent in many CMOS devices.)

Figure 7 shows the AD7545 connected in a voltage switching mode. OUT1 is connected to the reference voltage and AGND is connected to DGND. The D/A converter output voltage is available at the V_{REF} pin and has a constant output impedance equal to R. R_{FB} is not used in this circuit.

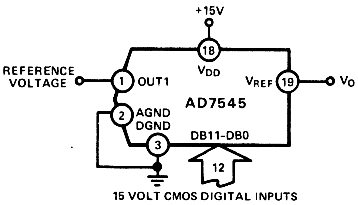


Figure 7. Single Supply Operation Using Voltage Switching Mode

The loading on the reference voltage source is code dependent and the response time of the circuit is often determined by the behavior of the reference voltage with changing load conditions. To maintain linearity, the voltages at OUT1 and AGND should remain within 2.5 volts of each other, for a V_{DD} of 15 volts. If V_{DD} is reduced from 15V or the differential voltage between OUT1 and AGND is increased to more than 2.5V the differential nonlinearity of the DAC will increase and the linearity of the DAC will be degraded. Figures 8 and 9 show typical curves illustrating this effect for various values of reference voltage and V_{DD}. If the output voltage is required to be offset from ground by some value, then OUT1 and AGND may be biased up. The effect on linearity and differential nonlinearity will be the same as reducing V_{DD} by the amount of the offset.

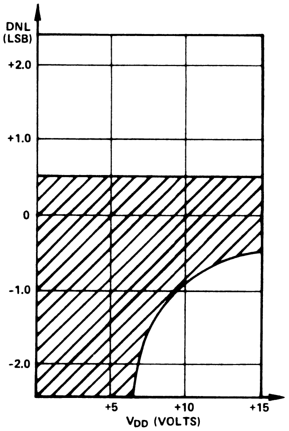


Figure 8. Differential Nonlinearity vs. V_{DD} for Figure 7 Circuit. Reference Voltage = 2.5 Volts. Shaded Area Shows Range of Values of Differential Nonlinearity that Typically Occur for L, C and U Grades.

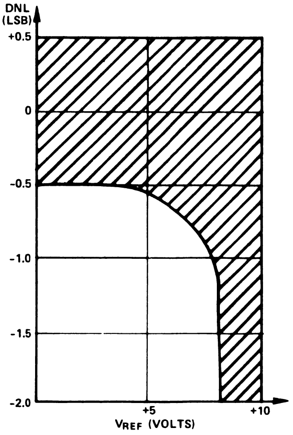


Figure 9. Differential Nonlinearity vs. Reference Voltage for Figure 7 Circuit. V_{DD} = 15 Volts. Shaded Area Shows Range of Values of Differential Nonlinearity that Typically Occur for L, C, and U Grades.

The circuits of Figures 4, 5 and 6 can all be converted to single supply operation by biasing AGND to some voltage between V_{DD} and DGND. Figure 10 shows the 2's Complement Bipolar circuit of Figure 5 modified to give a range from +2V to +8V about a "pseudo-analog ground" of 5V. This voltage range would allow operation from a single V_{DD} of +10V to +15V. The AD584 pin-programmable reference fixes AGND at +5V. V_{IN} is set at +2V by means of the series resistors R1 and R2. There is no need to buffer the V_{REF} input to the AD7545 with an amplifier because the input impedance of the D/A converter is constant. Note, however, that since the temperature coefficient of the D/A reference input resistance is typically -300ppm/°C, applications which experience wide temperature variations may require a buffer amplifier to generate the +2.0V at the AD7545 V_{REF} pin. Other output voltage ranges can be obtained by changing R4 to shift the zero point and (R1 + R2) to change the slope, or gain of the D/A transfer function. V_{DD} must be kept at least 5V above OUT1 to ensure that linearity is preserved.

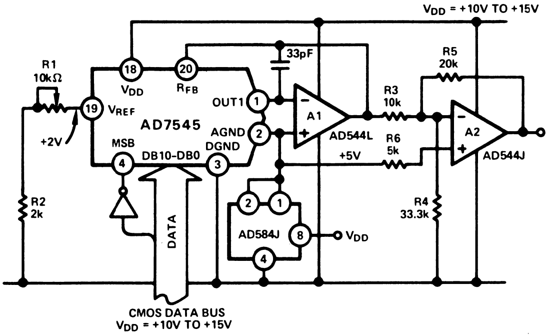


Figure 10. Single Supply "Bipolar" 2's Complement D/A Converter

MICROPROCESSOR INTERFACING OF THE AD7545

The AD7545 can interface directly to both 8- and 16-bit microprocessors via its 12-bit wide data latch using standard $\overline{CS}$ and $\overline{WR}$ control signals.

A typical interface circuit for an 8-bit processor is shown in Figure 11. This arrangement uses two memory addresses, one for the lower 8 bits of data to the DAC and one for the upper 4 bits of data into the DAC via the latch.

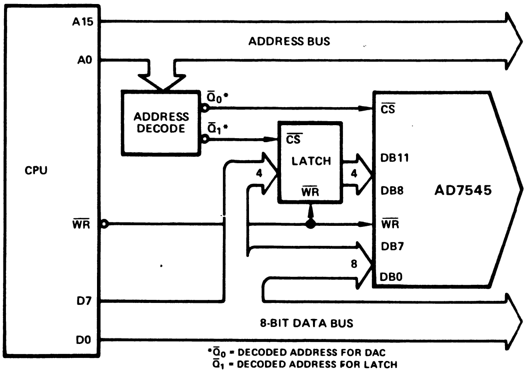


Figure 11. 8-Bit Processor to AD7545 Interface

Figure 12 shows an alternative approach for use with 8-bit processors which have a full 16-bit wide address bus such as 6800, 8080, Z80. This technique uses the 12 lower address lines of the processor address bus to supply data to the DAC, thus each AD7545 connected in this way uses 4k bytes of address locations. Data is written to the DAC using a single memory write instruction. The address field of the instruction is organized so that the lower 12 bits contain the data for the DAC and the upper 4 bits contain the address of the 4k block at which the DAC resides.

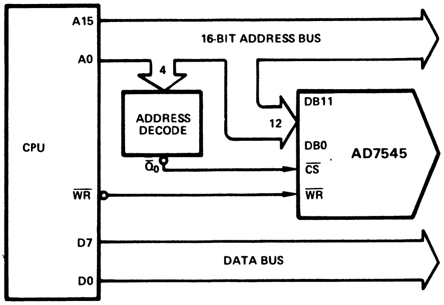


Figure 12. Connecting the AD7545 to 8-Bit Processors via the Address Bus

SUPPLEMENTAL APPLICATION MATERIAL

For further information on CMOS multiplying D/A converters the reader is referred to the following texts:

Application Guide to CMOS Multiplying D/A converters available from Analog Devices, Publication Number G479.

Gain Error and Gain Temperature Coefficient of CMOS Multiplying DACS – Application Note, Publication Number E630–10–6/81 available from Analog Devices.

Analog-Digital Conversion Notes – available from Analog Devices, price $5.95.

ANALOG
DEVICES

CMOS
16-Bit Multiplying DAC

AD7546

FEATURES

- **Monotonic to 16 Bits Over Temperature**
- **On-Chip Deglitch Switch**
- **Unipolar and Bipolar Operation**
- **Microprocessor Compatible**
- **TTL/CMOS Compatible Latched Inputs**
- **Voltage Output (Constant Output Impedance)**
- **Low Cost**
- **Low Power Consumption: 50mW typ**

GENERAL DESCRIPTION

The AD7546 is a 16-bit voltage-output DAC with input data latches for interfacing to 16-bit microprocessors. It uses a novel design consisting of a 12-bit R-2R DAC, operated in the voltage switching mode, which is supplied with a reference voltage from a 4-bit segment DAC under the control of the four most significant bits. A monolithic CMOS device, the AD7546 offers outstanding differential nonlinearity specifications; ±0.006% (14-bit monotonicity) and ±0.0015% (16-bit monotonicity).

An on-chip deglitch switch which is synchronized with the latch loading signal is provided for use with track/hold circuits.

ORDERING INFORMATION

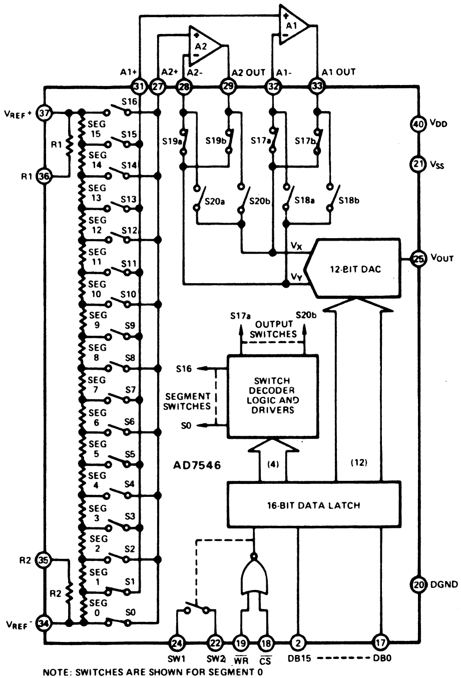
Relative Accuracy	Differential Nonlinearity	Temperature Range 0 to +70°C	 -25°C to +85°C
±0.05%	±0.006%	AD7546JN	AD7546AD
±0.012%	±0.0015%	AD7546KN	AD7546BD

PACKAGE IDENTIFICATION[1]

Suffix D: Ceramic DIP – (D40A)
Suffix N: Plastic DIP – (N40A)

[1] See Section 20 for package outline information.

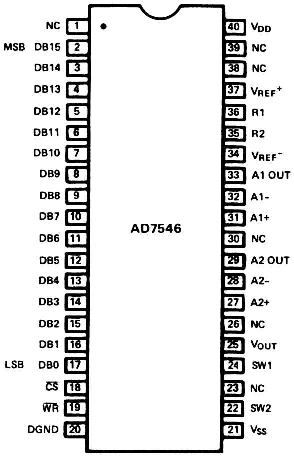
AD7546 FUNCTIONAL BLOCK DIAGRAM



NOTE: SWITCHES ARE SHOWN FOR SEGMENT 0 i.e., INPUT CODE OF 0XXXH.

40-PIN DIP

PIN CONFIGURATION



SPECIFICATIONS (V_{DD} = +15V, V_{SS} = -5V, V_{REF}^+ = +4V, V_{REF}^- = -4V, A1, A2 = AD544K, unless otherwise noted)

Parameter	Limit at T_A = +25°C	Limit at $T_A = T_{min}, T_{max}$[1]	Units	Conditions/Comments
ACCURACY				
Resolution				
All Grades	16	16	Bits	
Relative Accuracy				
AD7546JN, AD	±0.05	±0.05	% FSR max[2]	This is an end-point linearity specification
AD7546KN, BD	±0.012	±0.012	% FSR max	assuming zero offset voltage for A1, A2.
Differential Nonlinearity				
AD7546JN, AD	±0.006	±0.006	% FSR max	Guaranteed monotonic to 14 bits (DB0 and DB1 = 0).
AD7546KN, BD	±0.0015	±0.0015	% FSR max	Guaranteed monotonic to 16 bits over temperature.
Gain Error[3]				
Positive Full Scale	–0.02	–0.02	% FSR max	DAC latches loaded with $FFFF_H$
Negative Full Scale	–0.02	–0.02	% FSR max	DAC latches loaded with 0000_H
Gain T.C.[4]	±2	±2	ppm of FS/°C max	
dc Supply Rejection				
$\Delta Gain/\Delta V_{DD}$	100	100	µV per V typ	V_{DD} = +14.5V to +15.5V
DYNAMIC PERFORMANCE				
Voltage Settling Time[5]	4	4	µs typ	To 0.01% of final value.
	5	5	µs typ	To 0.003% of final value.
	10	10	µs typ	To 0.00076% of final value. Measured using the circuit of Figure 6.
SWITCHING CHARACTERISTICS[6]				With +5V input logic levels.
t_{CWS}	0	0	ns min	Chip select to WRITE setup time
t_{CWH}	0	0	ns min	Chip select to WRITE hold time
t_{WR}	400	600	ns min	WRITE pulse width
t_{DS}	200	300	ns min	Data setup time
t_{DH}	100	150	ns min	Data hold time
REFERENCE INPUTS				
Resistance				
V_{REF}^+ to V_{REF}^-	20/32/50	20/32/50	kΩ, min/typ/max	Typical Resistance TC is –300ppm/°C
R1, R2	20/30/50	20/30/50	kΩ, min/typ/max	
R1, R2 Match				
AD7546JN, AD	0.5	0.5	% max	Typical TC of R1, R2 match is ±1ppm/°C
AD7546 KN, BD	0.1	0.1	% max	
Voltage Range				
V_{REF}^+	+5	+5	V max	The AD7546 is tested with V_{REF}^+ =
V_{REF}^-	-5	-5	V max	+4V, V_{REF}^- = –4V
ANALOG OUTPUT				
R_{OUT} (Output Resistance)	10/15/25	10/15/25	kΩ, min/typ/max	
C_{OUT} (Output Capacitance)	8	8	pF max	
DEGLITCH SWITCH				
R_{ON}	300/600	450/900	Ω typ/max	
$I_{LEAKAGE}$	1	10	nA max	Off switch leakage
LOGIC INPUTS				
V_{IH}	2.4	2.4	V min	
V_{IL}	0.8	0.8	V max	
I_{IN} (Input Leakage Current)	1	1	µA max	V_{IN} = 0V or V_{DD}
C_{IN} (Input Capacitance)	8	8	pF max	
Input Coding	16-Bit Unipolar Binary			See Figure 7
	16-Bit Offset Binary			See Figure 8
POWER SUPPLY				
V_{DD}	+15	+15	V	±5% for specified performance
V_{SS}	-5	-5	V	±5% for specified performance
I_{DD}	4	4	mA max	$V_{IN} = V_{IL}$ or V_{IH}
I_{DD}	200	200	µA max	V_{IN} = 0V or V_{DD}, $\overline{CS} = \overline{WR}$ = 0V
I_{SS}	100	100	µA max	

NOTES

[1] Temperature ranges as follows: AD7546JN, KN; 0 to +70°C
AD7546AD, BD; -25°C to +85°C

[2] FSR is Full Scale Range

[3] These gain error specifications have assumed an input offset voltage for A2 of 0V. Actual gain error figures should include amplifier A2 input offset voltage.

[4] Gain TC specifications have assumed a zero input offset voltage drift with temperature for A2. Actual gain TC figures should include amplifier A2 drift with temperature.

[5] Voltage settling time will be a function of the time constant RC seen at the buffer amplifier inputs. The resistance component of this time constant is the equivalent output impedance of the resistor string and will vary depending on which segment is decoded. Maximum equivalent resistance occurs at mid-scale. Worst case settling thus occurs from zero to mid-scale or from full-scale to mid-scale.

[6] +15V logic can be used to reduce power dissipation but no improvement is achieved in the timing specifications. All control signals are measured with $t_r = t_f$ = 20ns for +5V logic and timed from $\frac{(V_{IH} + V_{IL})}{2}$. Data is timed from V_{IH} or V_{IL}. Sample tested at +25°C to ensure conformance.

[7] Guaranteed but not tested.

Specifications subject to change without notice.

CAUTION:

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

(Note that cavity lid on Ceramic Package is Electrically Connected to V_{DD})

V_{DD} (Pin 40) to DGND	0V, +17V
V_{SS} (Pin 21) to DGND	0V, -7V
V_{REF}^+ (Pin 37) to DGND	V_{DD}, V_{REF}^-
V_{REF}^- (Pin 34) to DGND	V_{SS}, V_{REF}^+
R1 (Pin 36) to DGND	±25V
R2 (Pin 35) to DGND	±25V
DB12 LOW (S17, S19 Closed)	
A1 - (Pin 32) or A1 Out (Pin 33)	
to A2 - (Pin 28) or A2 Out (Pin 29)	-0.3V, +5V
DB12 HIGH (S18, S20 Closed)	
A2 - (Pin 28) or A2 Out (Pin 29)	
to A1 - (Pin 32) or A1 Out (Pin 33)	-0.3V, +5V
A1 + (Pin 31), A2 + (Pin 27) to DGND	V_{SS}, V_{DD}
V_{OUT} (Pin 25) to DGND	±25V
SW1 (Pin 24), SW2 (Pin 22) to DGND	V_{SS}, V_{DD}
Digital Inputs (Pins 2 -19) to DGND	-0.3V, +17V

Power Dissipation (Package)	
Plastic (AD7546JN, KN)	
Up to +50°C	1200mW
Derates above +50°C by	12mW/°C
Ceramic (AD7546AD, BD)	
Up to +50°C	1000mW
Derates above +50°C by	10mW/°C

STRESS

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ACCURACY SPECIFICATIONS

Two types of nonlinearity errors exist in D/A converters, relative accuracy and differential nonlinearity. Relative accuracy is the error resulting from departure of the DAC transfer characteristic from the ideal straight line drawn between measured zero and measured full scale.

Differential Nonlinearity (DNL) is the difference between the measured output voltage change between two adjacent input codes and the ideal change of 1LSB. A specified DNL of ±1 LSB guarantees monotonicity (i.e. the output voltage will never decrease for any increase in input code). To ensure that the output voltage will always increase when the input code is increased requires a DNL specification of less than ±1LSB. This point is illustrated in Figure 1.

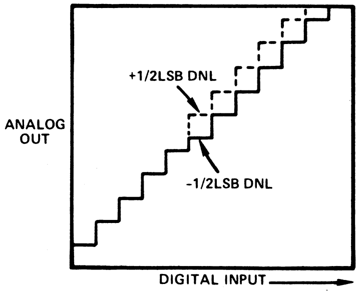


Figure 1a. ±1/2LSB Differential Nonlinearity

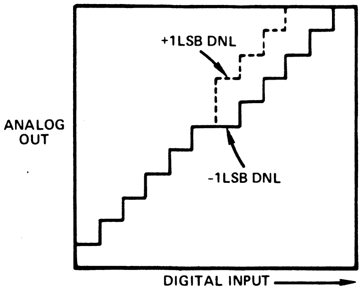


Figure 1b. ±1LSB Differential Nonlinearity

Many applications require high resolution DACs with guaranteed monotonicity (but not necessarily with an equivalent relative accuracy) for fine control of temperature, position and other physical parameters. Good differential nonlinearity is essential in such systems to maintain an even degree of control over the full range. Monotonicity is particularly important in feedback systems where nonmonotonic behavior constitutes positive feedback which may lead to catastrophic results. To ensure monotonic behavior of a particular device, only those bits which are guaranteed monotonic for that grade should be exercised e.g., for the AD7546JN (14-bit monotonic), DB0 and DB1 should be tied LOW and DB2 - DB15 exercised.

THEORY OF OPERATION OF THE AD7546

The traditional solution to achieving high resolution DACs with guaranteed monotonicity is the R-2R ladder approach. This technique usually constrains the converter to have ±1/2LSB nonlinearity in order to guarantee monotonicity, which in turn requires very tight resistor matching and tracking. The resistor ladder tolerance is most critical for the major carry where, in a 16-bit DAC, the 15LSBs turn off and the most significant bit turns on. If the MSB is more than 0.0015% low, the converter will be nonmonotonic. Table 1 shows the maximum tracking error which can be allowed over a 60°C range to maintain monotonicity, which is ±1LSB DNL. A standard R-2R approach therefore imposes severe constraints on resistor matching.

The design technique used in the AD7546 sidesteps the penalty inherent in the R-2R design (i.e. that tight differential nonlinearity figures require tight nonlinearity figures). The block diagram of the AD7546 is shown in Figure 2. The top four bits of the 16-bit input data are decoded to select, via the segment switches, one of the 16 voltage segments available along the resistor chain. This voltage segment, $\frac{V_{REF}^{+} - V_{REF}^{-}}{16}$,

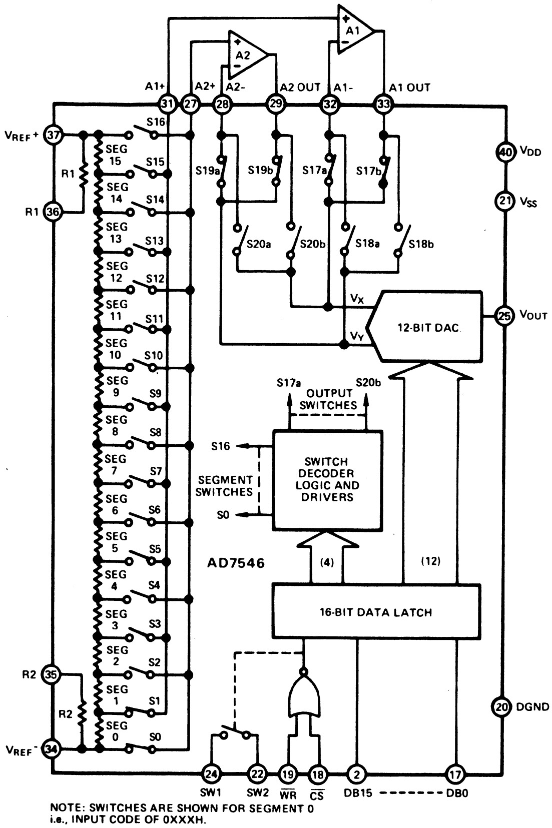


Figure 2. AD7546 Functional Diagram

Converter Type	Initial Matching Required for:		Tracking Required for:	
	±1LSB DNL	±1/2LSB DNL	±1LSB DNL (1/2LSB INITIAL DNL)	±1/2LSB DNL (1/4LSB INITIAL DNL)
Straight R-2R	±0.0015%	±0.00076%	±0.127ppm/°C	±0.063ppm/°C
Segmented 4 Bits + 12 Bits	±0.024%	±0.012%	±2ppm/°C	±1ppm/°C

Table 1. Resistor Matching Requirements for 16-Bit DAC

is used as a voltage reference to feed a 12-bit R-2R type D/A converter operating in the voltage switching mode (Reference 1). From Figure 2 the reference voltage is the voltage between V_X and V_Y and is always equal to one voltage segment. The output of the D/A converter may be expressed as follows:

$$V_{OUT} = V_Y + D(V_X - V_Y)$$

where D is the lower 12-bit digital code, V_X is the higher segment voltage and V_Y is the lower segment voltage. The 12-bit D/A converter reference inputs, V_X and V_Y, are connected to the two resistor chain nodes which define the segment of interest and the 12-bit D/A converter interpolates between these two points.

Thus the 65,536 output levels available from the 16-bit DAC are composed of 16 groups of 4,096 steps each. Since the major carry of the 12-bit DAC is repeated in each of the 16 segments it requires sixteen times lower initial resistor accuracy and tracking to maintain a given differential nonlinearity over temperature. The resistors that determine monotonicity are in the 12-bit DAC. The truth table for the switch decoder is shown in Table 2.

DB15	DB14	DB13	DB12	Segment Switches	Output Switches
1	1	1	1	S15, S16	S18, S20
1	1	1	0	S14, S15	S17, S19
1	1	0	1	S13, S14	S18, S20
1	1	0	0	S12, S13	S17, S19
1	0	1	1	S11, S12	S18, S20
1	0	1	0	S10, S11	S17, S19
1	0	0	1	S9, S10	S18, S20
1	0	0	0	S8, S9	S17, S19
0	1	1	1	S7, S8	S18, S20
0	1	1	0	S6, S7	S17, S19
0	1	0	1	S5, S6	S18, S20
0	1	0	0	S4, S5	S17, S19
0	0	1	1	S3, S4	S18, S20
0	0	1	0	S2, S3	S17, S19
0	0	0	1	S1, S2	S18, S20
0	0	0	0	S0, S1	S17, S19

Table 2. Truth Table for Switch Decoder

Since the input impedance of the D/A converter is low and varies with code, two external amplifiers are used to buffer the selected reference segment from the D/A converter. The buffer amplifiers, A1, A2, could give rise to differential nonlinearity if connected directly to V_X and V_Y and stepped up the ladder. For example consider A1 and A2 to have input offset voltages V_{OS1} and V_{OS2} respectively, then the first major carry from segment 0 to segment 1 occurs as follows:

Segment 0: $V_X = V_1 + V_{OS1}$, $V_Y = V_0 + V_{OS2}$

$$V_{OUT} = V_0 + V_{OS2} + (1 - 1/2^{12})\,[(V_1 + V_{OS1}) - (V_0 + V_{OS2})]$$

$$V_{OUT} = V_1 + V_{OS1} - \frac{(V_1 - V_0)}{2^{12}} - \frac{(V_{OS1} - V_{OS2})}{2^{12}}$$

Segment 1: $V_X = V_2 + V_{OS1}$, $V_Y = V_1 + V_{OS2}$

$$V_{OUT} = V_1 + V_{OS2}$$

The error term generated by this segment change is:

$$V_{OS2} - V_{OS1} + \frac{(V_{OS1} - V_{OS2})}{2^{12}}$$

It can be seen that V_{OS1} and V_{OS2} must match to within one LSB to guarantee monotonic behavior at this transition.

To overcome this problem the AD7546 circuit interchanges the amplifiers at each segment transition and, as a result, differential nonlinearity can be guaranteed for a very large range of V_{OS}. Switching inside the feedback loop of the op amp is used to remove the effect of switch R_{ON}. With this technique the first major carry from segment 0 to segment 1 now occurs as follows:

Segment 0: $V_X = V_1 + V_{OS1}$, $V_Y = V_0 + V_{OS2}$

$$V_{OUT} = V_1 + V_{OS1} - \frac{(V_1 - V_0)}{2^{12}} - \frac{(V_{OS1} - V_{OS2})}{2^{12}}$$

Segment 1: Interchange amplifiers

$V_X = V_2 + V_{OS2}$, $V_Y = V_1 + V_{OS1}$

$$V_{OUT} = V_1 + V_{OS1}$$

The error term at the transition from one segment to another is now $(V_{OS1} - V_{OS2})/4096$ which gives very good differential nonlinearity for reasonable offsets. At the next segment transition, $V_X = V_3 + V_{OS1}$, $V_Y = V_2 + V_{OS2}$ and so on through each segment. The amplifiers are interchanged via output switches S17 - S20, see Table 2.

In the segmented DAC the precision of the resistor chain determines integral nonlinearity only. If the resistor chain is trimmed for perfect matching such that $Vn + 1 = Vn = Vn - 1 =$ Vsegment, then the resulting nonlinearity due to amplifier offset voltage corresponds to a gain error in adjacent segments of $V_{OS1} - V_{OS2}$, see Figure 3. This term may be nulled to zero with offset adjustment of one op amp.

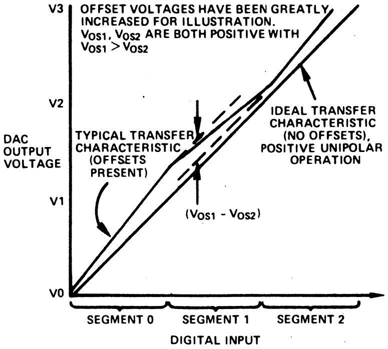


Figure 3. Positive Unipolar Transfer Characteristic ($V_{REF}^- = 0V$, $V_{REF}^+ = +4V$) Exaggerated to Show the Effect of Amplifier Offset Voltages

Furthermore, if offsets are equal in magnitude and sign, the result is a constant offset shift in the D/A transfer function and the device will have true 16-bit linearity.

(Reference 1. Analog Dialogue, Volume 14, Number 1 P16-17.)

OP-AMP SELECTION

Amplifiers A1 and A2 determine the overall performance of the AD7546. Since these are external to the converter, the user can choose amplifiers which will tailor the system performance to the required accuracy. Input bias current, open-loop gain and offset voltage of the amplifiers affect relative accuracy. Differential nonlinearity is affected by input bias current. (The offset voltage contribution to linearity has already been dealt with on previous pages.) The following two expressions deal with the relationship between device linearity and input bias current.

For Differential Nonlinearity:

$$\text{MAX DNL (in LSBs)} = \frac{14}{16} \cdot \frac{(I_{BIAS})(R)}{1LSB}$$

For Relative Accuracy:

$$\text{MAX NL (in LSBs)} = \frac{15}{2} \cdot \frac{(I_{BIAS})(R)}{1LSB}$$

Where I_{BIAS} = Input bias current for the noninverting input terminal of A1 or A2

$$1LSB = \frac{V_{REF}^+ - V_{REF}^-}{2^N}$$

N is determined by the required system resolution up to N = 16.

R = R segment, typically 2kΩ

Low bias current op amps, BIFET or Super-Beta types, should be used such as the AD542K, AD544K, AD517K, TL071, TL081. Table 3 lists some important parameters against various op amps. Note that the AD7546 output settling time is dependent upon the op amps used. The figures in column two give the additional offset voltage contribution to nonlinearity of A1 and A2.

A1, A2	Maximum Additional Nonlinearity	Settling Time (µs) to ±1/2LSB 14 Bits	16 Bits
2 X AD544KH	±0.01%	15	35
1 X TL072BCP (Dual)	±0.05%	5	10
2 X AD517JH	±0.003%	90	100
1 X AD644JH (Dual AD544)	±0.01%	15	35
2 X LF256	±0.05%	5	10

Settling time measurements were made with a similar op amp to buffer V_{OUT} (A4 in Figure 6)

Table 3. AD7546 Performance vs A1, A2

DATA LOADING AND DEGLITCH SWITCH

The AD7546 timing specifications are included on specifications page and illustrated here in Figure 4. Signals $\overline{CS}$ and $\overline{WR}$ have the same interpretation as in normal microprocessor systems. When both $\overline{CS}$ and $\overline{WR}$ are low the input latches are transparent and the DAC output voltage follows the input data. With $\overline{CS}$ low, the input data is latched on the rising edge of $\overline{WR}$.

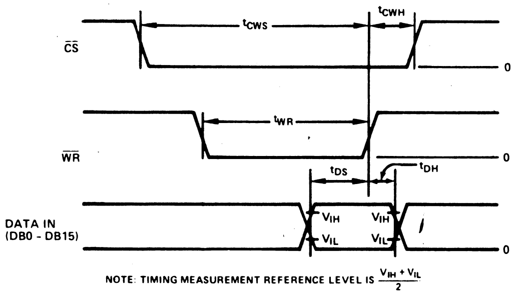


Figure 4. AD7546 Timing Waveforms

Included on the chip is an SPST switch intended for use in a Track/Hold circuit to remove glitches from the DAC output and simplify low-pass filtering of the reconstructed output voltage. The switch is synchronized with the latch loading signals, being open when both $\overline{CS}$ and $\overline{WR}$ inputs are low. The internal logic of the AD7546 ensures that the switch opens before data to the latches can change. To function as a Track/Hold the switch is placed in series with the DAC output as shown in Figure 5. Pin 23 is a no-connect pin which should be grounded to minimize any feedthrough resulting from stray capacitances at the two switch terminals. The switch should be used with pin 24 as the input and pin 22 as the output. When the switch is open the Hold capacitor stores the previous output voltage of the DAC. The $\overline{WR}$ pulse should be of sufficient duration to allow the DAC to settle to its new analog output and for all glitches to have settled out. Driving the $\overline{WR}$ input from a one-shot will ensure sufficient settling time.

When $\overline{WR}$ returns high the switch is closed, updating the output voltage on the capacitor. Typical output waveforms using the circuit of Figure 5 are shown below.

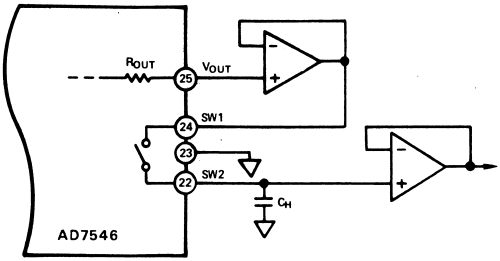
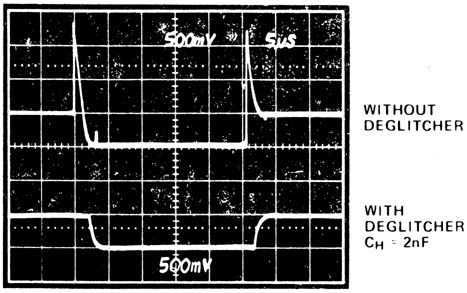


Figure 5. Track/Hold Circuit



UNIPOLAR AND BIPOLAR OPERATION

The reference voltage $V_{REF}^+ - V_{REF}^-$ is divided into sixteen equal voltage segments by the resistor chain. The top four input data bits (DB15 - DB12) are used to select one of these voltage segments for the 12-bit DAC to interpolate between. By suitable choice of V_{REF}^+ and V_{REF}^- the AD7546 transfer characteristic can be shifted such that any segment start will coincide with the zero crossing of the transfer characteristic. With an input code of all 0s the DAC output is V_{REF}^-. For an all 1s input code the DAC output is 1LSB less than V_{REF}^+. The maximum positive reference voltage, V_{REF}^+, must be less than or equal to +5V; the maximum negative reference voltage, V_{REF}^-, should be less than or equal to -5V.

A typical circuit configuration for the AD7546 is shown in Figure 6. Unipolar (single quadrant) operation is obtained when one end of the resistor chain is tied to ground i.e. when $V_{REF}^+ = +V_{REF}$ and $V_{REF}^- = 0V$ or when $V_{REF}^+ = 0V$ and $V_{REF}^- = -V_{REF}$. A Unipolar transfer characteristic with a positive reference is shown in Figure 7. The negative supply voltage V_{SS} must be at least as negative as the most negative reference voltage used, V_{REF}^-. For positive unipolar applications V_{SS} may be set to 0V and the AD7546 operated as a single supply device.

Bipolar (two quadrant) operation with a symmetrical transfer function around 0V is achieved with $|V_{REF}^+| = |V_{REF}^-|$. The zero crossing now occurs when DB15 = 1 and DB14 to DB0 all 0s. A Bipolar transfer characteristic is shown in Figure 8.

Note that V_{REF}^+ must always be more positive than V_{REF}^-; operation is confined to two quadrants (1st and 3rd).

Two equal trimmed resistors, R1 and R2, are included on the AD7546 to allow one reference to be generated from the other with the addition of an external amplifier (A3 in Figure 6).

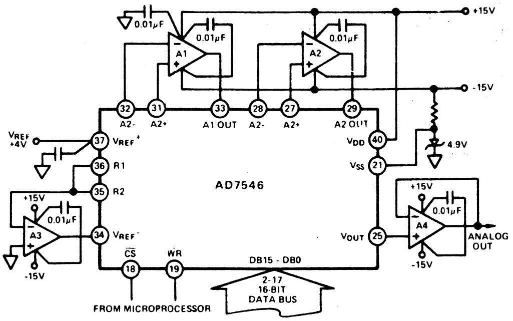


Figure 6. Typical Circuit Configuration for the AD7546

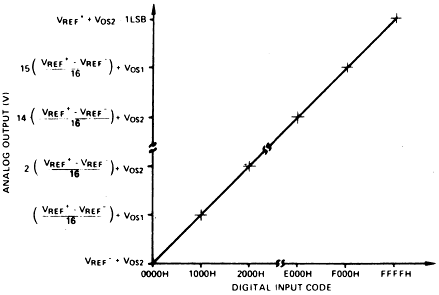


Figure 7. Unipolar Transfer Characteristic (Positive Reference)

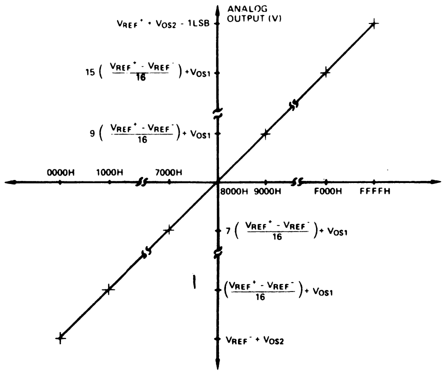


Figure 8. Bipolar Transfer Characteristic, $|V_{REF}^+| = |V_{REF}^-|$

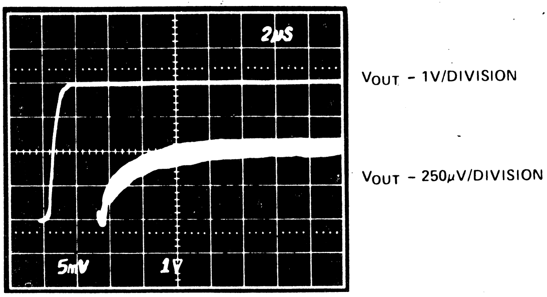


Figure 9. Typical Settling Characteristics of Figure 6 Using TL071 for Full Scale Code Change

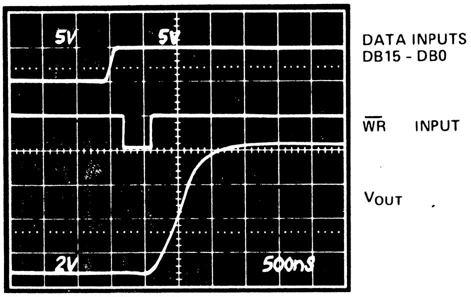


Figure 10. Typical Loading Waveforms with $\overline{CS}$ = 0V

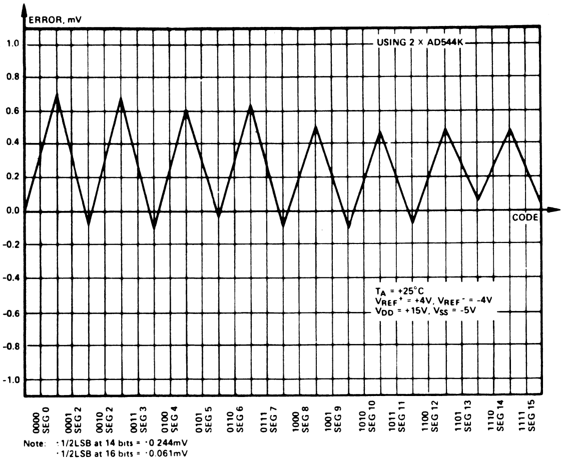


Figure 11a. Typical Error vs Input Code with A1 = A2 = AD544K

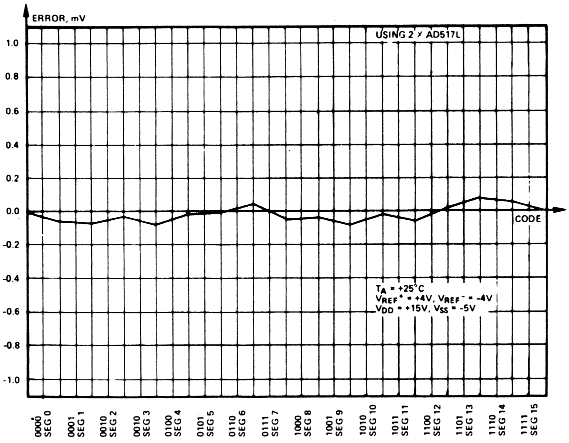


Figure 11b. Typical Error vs Input Code with A1 = A2 = AD517L

ANALOG DEVICES

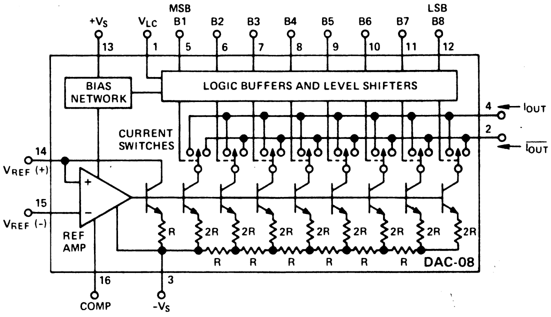
8-Bit Monolithic High Speed Multiplying D/A Converter

AD DAC-08

FEATURES

Exact Replacement for Industry Standard DAC-08
Fast (85ns typical) Settling Time
Linearity Error ±1/4LSB (±0.1%) Guaranteed Over Full Temperature Range
Wide Output Voltage Compliance: -10V to +18V
Single Chip Monolithic Construction
16-Pin Ceramic DIP Packaging
Low Cost
MIL-STD-883 Processing Available

AD DAC-08 FUNCTIONAL BLOCK DIAGRAM



TO-116

PRODUCT DESCRIPTION

The AD DAC-08 is a low-cost, 8-bit monolithic multiplying digital-to-analog converter featuring typical settling times of 85ns. The chip contains 8 matched bipolar current steering switches, a precision resistor network, and high-speed control amplifier, thus integrating all important circuit functions on a single chip.

The AD DAC-08 provides matching of full-scale output current to the reference current within 1LSB. Analog Devices' precision linear processing makes this matching possible without the use of laser trimming. Diffused resistors are used rather than thin-film resistors in order to provide specified performance at low cost.

The AD DAC-08 is recommended for use in applications requiring 8-bit accuracy and fast settling times coupled with ease of use. The AD DAC-08 also provides an alternate source for designs already using the standard DAC-08.

The AD DAC-08 is available in 5 performance grades: the AD DAC-08A and AD DAC-08 are rated for the full -55°C to +125°C military temperature range; and the AD DAC-08H, E, and C grades are specified for the 0 to +70°C commercial temperature range. All models are guaranteed monotonic over their full temperature range, and all are packaged in a hermetically-sealed 16-pin ceramic dual-in-line package.

PRODUCT HIGHLIGHTS

1. The AD DAC-08 is a true second-source equivalent to the industry standard DAC-08.
2. The versatile current-in, current-out design, choice of fixed or variable reference, and CMOS or TTL compatible inputs offer the user greater flexibility in applying the device.
3. The fast settling time allows the AD DAC-08 to be used in applications such as CRT displays, waveform generators, and high-speed analog-to-digital converters.
4. The high impedance current output can drive a resistor directly, or be used with an external op amp to produce a low impedance output voltage.
5. The AD DAC-08 is available in chip form for use in hybrid microcircuits. Consult the chip section for available grades and application details.
6. The AD DAC-08 and AD DAC-08A are available screened to MIL-STD-883, Method 5004 Class B.

SPECIFICATIONS

The AD DAC-08 and AD DAC-08A specifications apply for $V_S = \pm15V$, $I_{REF} = 2.0mA$, $T_A = -55°C$ to $+125°C$ unless otherwise noted.

MODEL CHARACTERISTIC	SYMBOL	CONDITIONS	AD DAC-08 MIN	 TYP	 MAX	AD DAC-08A MIN	 TYP	 MAX	UNITS
RESOLUTION					8			8	Bits
MONOTONICITY		$T_A = -55°C$ to $+125°C$		GUARANTEED			GUARANTEED		
NONLINEARITY		$T_A = -55°C$ to $+125°C$			±0.19			±0.1	% FS
SETTLING TIME	t_s	Full Scale Step to ±1/2LSB		85	135		85	135	ns
PROPAGATION DELAY	t_{PLH}, t_{PHL}	All Bits Switched		35	60		35	60	ns
FULL SCALE TEMPCO	TC I_{FS}			±10	±50		±10	±50	ppm/°C
OUTPUT VOLTAGE COMPLIANCE	V_{OC}	$\Delta I_{FS} < 1/2LSB$; $R_{OUT} > 20M\Omega$ typ	-10		+18	-10		+18	V dc
FULL SCALE CURRENT	I_{FS4}	$V_{REF} = 10.000V$; R_{14}, R_{15} = 5.000kΩ; $T_A = 25°C$	1.94	1.99	2.04	1.984	1.992	2.000	mA
FULL SCALE SYMMETRY	I_{FSS}	$(I_{FS4} - I_{FS2})$		±1.0	±8.0		±0.5	±4.0	μA
ZERO SCALE CURRENT	I_{ZS}			0.2	2.0		0.1	1.0	μA
OUTPUT CURRENT RANGE	I_{FSR}	$V- = -5.0V$	0	2.0	2.1	0	2.0	2.1	mA
		$V- = -7.0$ to $-18V$	0	2.0	4.2	0	2.0	4.2	mA
LOGIC INPUT LEVELS									
Logic "0"	V_{IL}	$V_{LC} = 0V$			0.8			0.8	V
Logic "1"	V_{IH}	$V_{LC} = 0V$	2.0			2.0			V
LOGIC INPUT CURRENTS		$V_{LC} = 0V$							
Logic "0"	I_{IL}	$-10V < V_{IN} < +0.8V$		-2.0	-10		-2.0	-10	μA
Logic "1"	I_{IH}	$2.0V < V_{IN} < 18V$		0.002	10		0.002	10	μA
LOGIC INPUT SWING	V_{IS}	$V- = -15V$	-10		+18	-10		+18	V
LOGIC THRESHOLD RANGE	V_{THR}	$V_S = \pm15V$	-10		+13.5	-10		+13.5	V
REFERENCE BIAS CURRENT	I_{REF}		+0.1	-1.0	-3.0	+0.1	-1.0	-3.0	μA
REFERENCE INPUT SLEW RATE	dI/dt		4.0	8.0		4.0	8.0		mA/μs
POWER SUPPLY SENSITIVITY	$PSSI_{FS+}$	$V+ = 4.5V$ to $18V$		+0.0003	±0.01		±0.0003	±0.01	%/%
	$PSSI_{FS-}$	$V- = 4.5V$ to $-18V$ $I_{REF} = 1.0mA$		±0.002	±0.01		±0.002	±0.01	%/%
POWER SUPPLY CURRENT									
From $+V_S$	I+		0.4	2.3	3.8	0.4	2.3	3.8	mA
From $-V_S$	I-		-0.8	-6.4	-7.8	-0.8	-6.4	-7.8	mA
POWER DISSIPATION	P_D	±5V, $I_{REF} = 1.0mA$		33	48		33	48	mW
		+5V, -15V, $I_{REF} = 2.0mA$		108	136		108	136	mW
		±15V, $I_{REF} = 2.0mA$		135	174		135	174	mW
PACKAGE STYLE[1] "D" (Q16A)				AD DAC-08D			AD DAC-08AD		

Specifications subject to change without notice.

[1] See Section 20 for package outline information.

ABSOLUTE MAXIMUM RATINGS

Operating Temperature	
AD DAC-08, DAC-08A	-55°C to +125°C
AD DAC-08E, C, H	0 to +70°C
Storage Temperature	-65°C to +150°C
Power Dissipation	500mW
Above 100°C Derate by	10mW/°C
Lead Soldering Temperature	300°C (60sec)
$-V_S$ Supply to $+V_S$ Supply	36V
Logic Inputs	$-V_S$ to $(-V_S + 36V)$
V_{LC}	$-V_S$ to $+V_S$
Reference Inputs (V_{14}, V_{15})	$-V_S$ to $+V_S$
Reference Input Differential	
Voltage (V_{14} to V_{15})	±18V
Reference Input Current (I_{14})	5.0mA

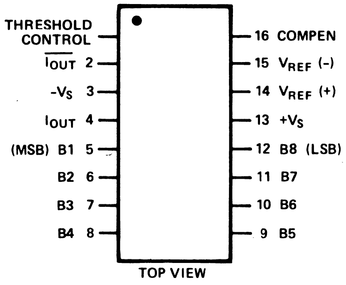
SPECIFICATIONS

The AD DAC-08C, E, and H specifications apply for $V_S = \pm 15V$, $I_{REF} = 2.0mA$, $T_A = 0$ to $+70°C$ unless otherwise noted.

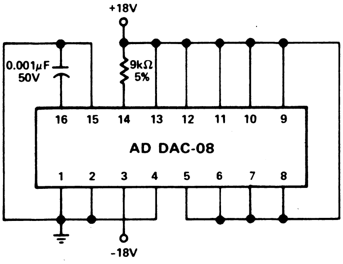
MODEL			AD DAC-08C			AD DAC-08E			AD DAC-08H			
CHARACTERISTIC	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
RESOLUTION					8			8			8	Bits
MONOTONICITY		$T_A = 0$ to $+70°C$		GUARANTEED			GUARANTEED			GUARANTEED		
NONLINEARITY		$T_A = 0$ to $+70°C$			±0.39			±0.19			±0.1	% FS
SETTLING TIME	t_s	Full Scale Step to ±1/2LSB		85	150		85	150		85	135	ns
PROPAGATION DELAY	t_{PLH}, t_{PHL}	All Bits Switched		35	60		35	60		35	60	ns
FULL SCALE TEMPCO	$TC\ I_{FS}$			±10	±80		±10	±50		±10	±50	ppm/°C
OUTPUT VOLTAGE COMPLIANCE	V_{OC}	$\Delta I_{FS} < 1/2LSB$; $R_{OUT} > 20M\Omega$	-10		+18	-10		+18	-10		+18	V dc
FULL SCALE CURRENT	I_{FS4}	$V_{REF} = 10.000V$; R_{14}, $R_{15} = 5.000k\Omega$; $T_A = 25°C$	1.94	1.99	2.04	1.94	1.99	2.04	1.984	1.992	2.000	mA
FULL SCALE SYMMETRY	I_{FSS}	$(I_{FS4} - I_{FS2})$		±2.0	±16		±1.0	±8.0		±0.5	±4.0	μA
ZERO SCALE CURRENT	I_{ZS}			0.2	4.0		0.2	2.0		0.1	1.0	μA
OUTPUT CURRENT RANGE	I_{FSR}	$V- = -5.0V$	0	2.0	2.1	0	2.0	2.1	0	2.0	2.1	mA
		$V- = -7.0$ to $-18V$	0	2.0	4.2	0	2.0	4.2	0	2.0	4.2	mA
LOGIC INPUT LEVELS												
Logic "0"	V_{IL}	$V_{LC} = 0V$			0.8			0.8			0.8	V
Logic "1"	V_{IH}	$V_{LC} = 0V$	2.0			2.0			2.0			V
LOGIC INPUT CURRENTS		$V_{LC} = 0V$										
Logic "0"	I_{IL}	$-10V < V_{IN} < +0.8V$		-2.0	-10		-2.0	-10		-2.0	-10	μA
Logic "1"	I_{IH}	$2.0V < V_{IN} < 18V$		0.002	10		0.002	10		0.002	10	μA
LOGIC INPUT SWING	V_{IS}	$V- = -15V$	-10		+18	-10		+18	-10		+18	V
LOGIC THRESHOLD RANGE	V_{THL}	$V_S = \pm 15V$	-10		+13.5	-10		+13.5	-10		+13.5	V
REFERENCE BIAS CURRENT	I_{REF}		+0.1	-1.0	-3.0	+0.1	-1.0	-3.0	+0.1	-1.0	-3.0	μA
REFERENCE INPUT SLEW RATE	dI/dt		4.0	8.0		4.0	8.0		4.0	8.0		mA/μs
POWER SUPPLY SENSITIVITY	$PSSI_{FS+}$	$V+ = 4.5V$ to $18V$		+0.0003	±0.01		±0.0003	±0.01		±0.0003	±0.01	%/%
	$PSSI_{FS-}$	$V- = -4.5V$ to $-18V$ $I_{REF} = 1.0mA$		±0.002	±0.01		±0.002	±0.01		±0.002	±0.01	%/%
POWER SUPPLY CURRENT	I+	From $+V_S$	0.4	2.3	3.8	0.4	2.3	3.8	0.4	2.3	3.8	mA
	I-	From $-V_S$	-0.8	-6.4	-7.8	-0.8	-6.4	-7.8	-0.8	-6.4	-7.8	mA
POWER DISSIPATION	P_D	±5V, $I_{REF} = 1.0mA$		33	48		33	48		33	48	mW
		+5V, -15V, $I_{REF} = 2.0mA$		108	136		108	136		108	136	mW
		±15V, $I_{REF} = 2.0mA$		135	174		135	174		135	174	mW
PACKAGE STYLE[1] "D" (Q16A)				AD DAC-08CD			AD DAC-08ED			AD DAC-08HD		

Specifications subject to change without notice.

[1] See Section 20 for package outline information.



Pin Connections



Burn-In Circuit

APPLYING THE AD DAC-08

Reference Connections

Figure 1 shows the block diagram of the AD DAC-08 circuit. A reference current (equal to the desired full-scale output current) is applied to pin 14. The reference amplifier adjusts the base voltage of the NPN current source transistors. The collector currents are binarily weighted, and their sum is equal to 255/256 times the reference current. The binary weighting is accomplished by the diffused resistor R-2R ladder network. The individual collector currents are steered into either the I_{OUT} or $\overline{I_{OUT}}$ lines by the current switches. These switches are driven by level shifters which can accept TTL or CMOS logic levels directly. The I_{OUT} and $\overline{I_{OUT}}$ lines can drive an op amp summing junction or can drive resistive loads directly due to the wide range of output compliance voltage.

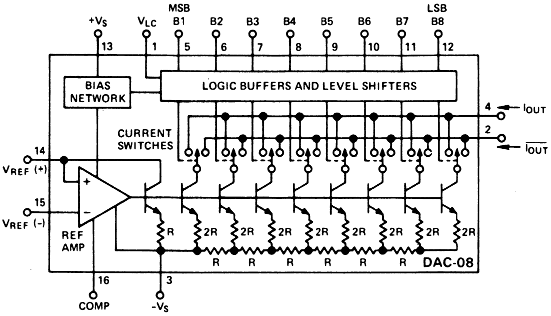


Figure 1. AD DAC-08 Block Diagram

Figure 2 illustrates the connections for positive and negative references. When a positive reference is used (Figure 2a), resistor R14 (equal to V_{REF} divided by the desired I_{FS}) establishes the reference current into pin 14. Reference amplifier bias current errors are minimized by connecting R15 (equal to R14) from pin 15 to ground. Adjustment of the output scale can be done by trimming R14, although in most applications the tight initial matching between reference current and output current will be adequate.

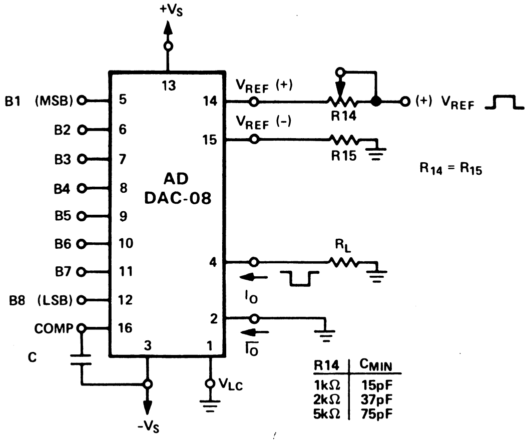


Figure 2a. Connections for Use with Positive Reference

Figure 2b shows the connections for a negative reference. Note that the reference current flows from ground into pin 14 through R14, which should be a low TC resistor as in the positive reference configuration. Resistor R15 serves the purpose of bias current cancellation only and need not be a precision resistor. Note that the input impedance for a negative reference is very high, while a positive reference sees an impedance equal to R14.

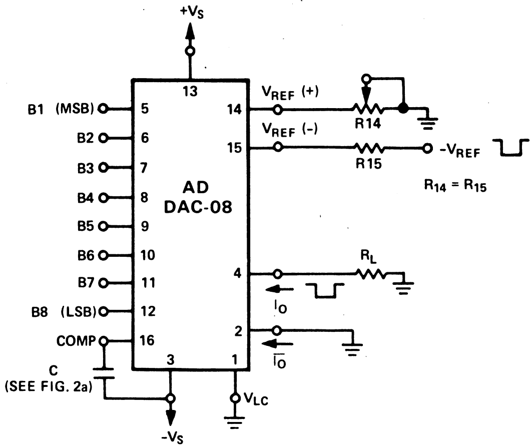


Figure 2b. Connections for Use with Negative Reference

When a dc reference is used, a 0.01µF reference bypass capacitor is recommended. The reference should be a low-drift, well-regulated and filtered type, such as the AD581 10V reference IC. Other values of reference voltage may be used, provided that R14 is chosen for a reference current between 0.2mA and 4.0mA.

MULTIPLYING MODE PERFORMANCE

The AD DAC-08 can be used to perform two-quadrant digital-analog multiplication by applying an ac reference signal. When an ac reference is used, pin 15 must be offset to insure that pin 14 is always at a higher potential than pin 15.

The reference amplifier must be properly compensated in ac applications to insure stability. The value of the capacitor from pin 16 to $-V_S$ depends on the value of R14. Minimum values of compensation capacitor for R14 values of 1, 2 and 5kΩ are 15, 37 and 75pF respectively.

For fastest response to a pulsed reference, low values of R14 should be used, allowing smaller values of compensation capacitor. It is possible to lower the equivalent resistance at pin 14 by connecting a shunt resistor to ground. Figure 3 shows the performance with equivalent resistance of 200Ω and no compensation capacitor. Slew rate is approximately 15mA/µs under these conditions.

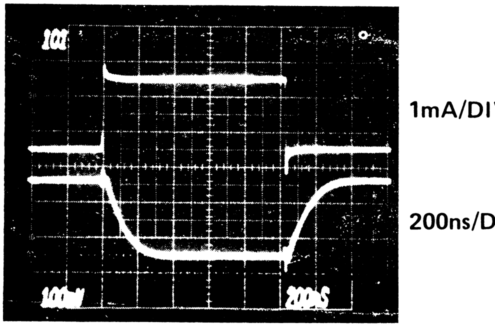


Figure 3. Fast Pulsed Reference Operation

The photographs on this page demonstrate the dynamic performance of the AD DAC-08. The AD DAC-08 is capable of extremely fast settling time, typically 85 nanoseconds for a full-scale step with I_{REF} = 2.0mA. As with any high speed circuitry, component layout must be optimized for minimum parasitic capacitances if full speed is to be realized.

Figure 4 below shows the output settling characteristic for a full-scale step. The vertical scale is 1LSB per division. Note that the zero-to-full scale settling time (Figure 4a) to within 1/2LSB is approximately 70 nanoseconds.

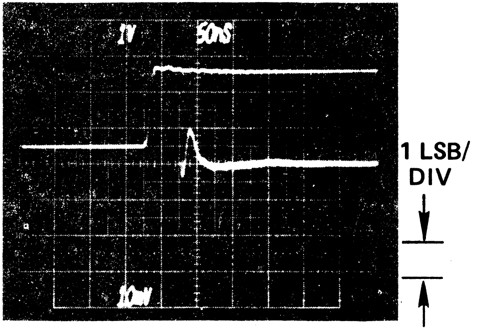


Figure 4a. Zero to Full-Scale Settling

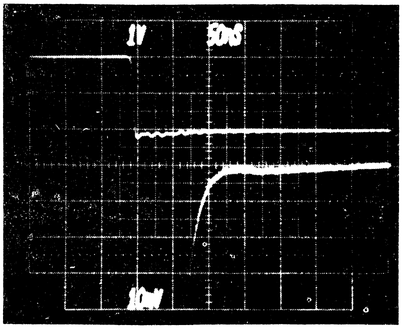


Figure 4b. Full-Scale to Zero Settling

Since the settling time of a DAC circuit includes propagation delay, slewing time, and final settling, switching time is best measured when only the LSB is switched. This minimizes the slewing time necessary. The LSB switching characteristic is shown in Figure 5.

SETTLING TIME MEASUREMENT

It should be noted that settling time measurement is not a simple matter. Since 1/2LSB of a 2.0mA full scale is only 4μA, a 1kΩ load resistance is needed to provide adequate drive for most oscilloscopes. However, any stray capacitance can cause the settling time of the fixture to be longer than the DAC settling time. For example, 15pF stray capacitance can cause a settling time to 1/2LSB of nearly 100 nanoseconds in the test fixture alone. The circuit of Figure 6 reduces the capacitance at the measurement node to less than 5pF, allowing more accurate determination of settling time.

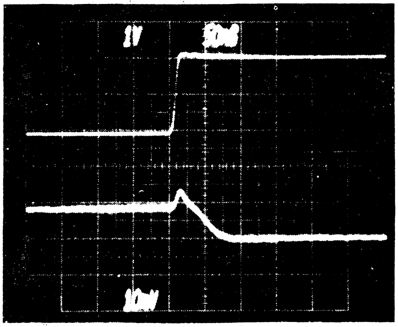
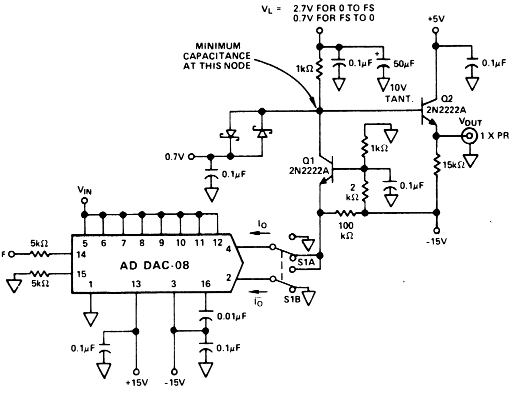


Figure 5. LSB Switching



BANDWIDTH OF OSCILLOSCOPE USED FOR MEASUREMENT SHOULD BE 50MHz MINIMUM; SATURATION OF PREAMP MUST BE AVOIDED.

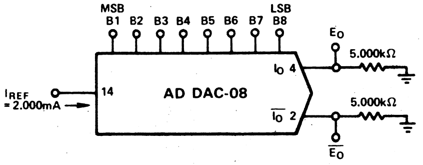
Figure 6. Settling Time Test Circuit

LOGIC INPUT CIRCUIT

The AD DAC-08 digital inputs will accommodate all popular logic families. The switching threshold is adjustable by applying a voltage to the logic threshold control pin (pin 1). The threshold is nominally 1.4 volts above V_{LC} at room temperature. For TTL/DTL interface, pin 1 is simply grounded. The logic inputs will tolerate wide voltage swings; for example, for $-V_S$ = -15V, the inputs may swing between -10V and +18V.

OUTPUT CONNECTIONS

The I_O and $\overline{I_O}$ outputs provide the user with several possible output configurations. Current is steered into the I_O terminal when a bit is at Logic "1", and into $\overline{I_O}$ when the bit is at Logic "0". Either output may be used, or both may be used simultaneously. If only one output is used, the unused output must still be connected to ground or some other point capable of sourcing I_{FS}.



	B1	B2	B3	B4	B5	B6	B7	B8	I_OmA	$\overline{I_O}$mA	E_O	$\overline{E_O}$
FULL SCALE	1	1	1	1	1	1	1	1	1.992	0.000	-9.960	0.000
FULL SCALE -LSB	1	1	1	1	1	1	1	0	1.984	0.008	-9.920	-0.040
HALF SCALE + LSB	1	0	0	0	0	0	0	1	1.008	0.984	-5.040	-4.920
HALF SCALE	1	0	0	0	0	0	0	0	1.000	0.992	-5.000	-4.960
HALF SCALE -LSB	0	1	1	1	1	1	1	1	0.992	1.000	-4.960	-5.000
ZERO SCALE +LSB	0	0	0	0	0	0	0	1	0.008	1.984	-0.040	-9.920
ZERO SCALE	0	0	0	0	0	0	0	0	0.000	1.992	0.000	-9.960

Figure 7. High Impedance Voltage Output

The wide output compliance range permits the AD DAC-08 to drive a resistive load directly. For example, with I_{REF} = 2.0mA, and a 5kΩ resistor from pin 4 to ground, the voltage at pin 4 varies from 0V with all bits OFF to -9.960V with all bits ON. While this is the simplest current-to-voltage conversion, it presents a 5kΩ output impedance, which adversely affects settling time and requires buffering.

An operational amplifier configured as a current-to-voltage converter will lower the output impedance and provide a voltage inversion. An output range of zero to +9.960V is then produced with a 5kΩ feedback resistor as shown in Figure 8.

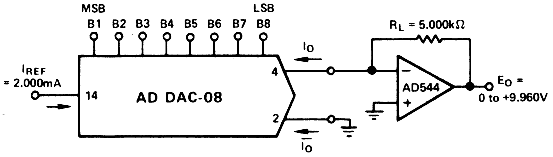
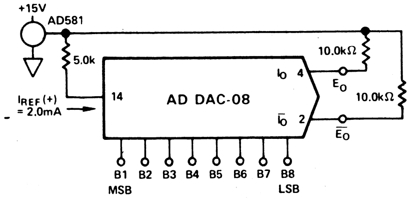


Figure 8. Low Impedance Voltage Output

Bipolar output voltage ranges are also possible. Figure 9 demonstrates the simplest scheme, providing a -9.92 to +10.00 volt scale in 80 millivolt steps. The voltage output has a high impedance as shown and should be buffered with an amplifier connected as a voltage follower.



	B1	B2	B3	B4	B5	B6	B7	B8	E_O	$\overline{E_O}$
POS FULL SCALE	1	1	1	1	1	1	1	1	- 9.920	+10.000
POS FULL SCALE -LSB	1	1	1	1	1	1	1	0	- 9.840	+ 9.920
ZERO SCALE +LSB	1	0	0	0	0	0	0	1	- 0.080	+ 0.160
ZERO SCALE	1	0	0	0	0	0	0	0	0.000	+ 0.080
ZERO SCALE -LSB	0	1	1	1	1	1	1	1	+ 0.080	0.000
NEG FULL SCALE +LSB	0	0	0	0	0	0	0	1	+ 9.920	- 9.840
NEG FULL SCALE	0	0	0	0	0	0	0	0	+10.000	- 9.920

Figure 9. Bipolar Voltage Output

ANALOG DEVICES

High Resolution 16-Bit D/A Converter

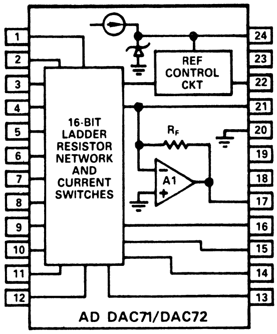
AD DAC71/ AD DAC72

ADVANCE TECHNICAL DATA

FEATURES

16-Bit Resolution
±0.003% Maximum Nonlinearity
Low Gain Drift ±5ppm/°C
0 to +70°C Operation (AD DAC71, AD DAC72C)
−25°C to +85°C Operation (AD DAC72)
Current and Voltage Models Available
Improved Second-Source
Low Cost

AD DAC71/AD DAC72 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD DAC71 and AD DAC72 are high resolution 16-bit hybrid IC digital-to-analog converters including reference, scaling resistors and output amplifier (V models).

The devices offer outstanding accuracy, including maximum linearity of 0.003% at room temperature and maximum gain drifts of 15ppm/°C (AD DAC71, AD DAC72C) and 5ppm/°C (AD DAC72). This performance is possible due to the innovative design, using proprietary monolithic D/A converter chips. Laser-trimmed thin film resistors provide the linearity and wide temperature range for guaranteed monotonicity.

The AD DAC71 and AD DAC72 digital inputs are TTL-compatible. Coding is complementary straight binary (CSB) for unipolar output versions and complementary offset binary (COB) for bipolar output versions.

All versions are packaged in a 24-pin ceramic DIP. The AD DAC72 and AD DAC72C are specified for operation from 0 to +70°C, and the AD DAC72 is specified from −25°C to +85°C. The AD DAC71 and AD DAC72 are intended to serve as improved second sources to DAC71 and DAC72 devices from other manufacturers.

PRODUCT HIGHLIGHTS

1. The AD DAC71 and AD DAC72 provide 16-bit resolution with 0.003% linearity.
2. The proprietary chips used in the hybrid design provide excellent stability over temperature and improved reliability.
3. Unipolar and bipolar current and voltage output versions are available to fill a wide range of system requirements.
4. The AD DAC71 and AD DAC72 are improved second source replacements for DAC71 and DAC72 devices from other manufacturers.

SPECIFICATIONS (T_A @ +25°C, rated power supplies unless otherwise noted)

	AD DAC71/72C			AD DAC72			
MODEL	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
DIGITAL INPUTS							
Resolution		16			16		Bits
Logic Levels (TTL-Compatible)[1]							
Logical "1" (at +40μA)	+2.4		+5.5	+2.4		+5.5	V dc
Logical "0" (at −1.0μA)	+0		+0.4	+0		+0.4	V dc
ACCURACY							
Linearity Error at 25°C			±0.003			±0.003	% of FSR[2]
Gain Error[3], Voltage		±0.01	±0.05		±0.01	±0.05	%
Current		±0.05	±0.25		±0.05	±0.25	%
Offset Error[3], Voltage, Unipolar		±0.1	±1		±0.1	±1	mV
Voltage, Bipolar			±2			±2	mV
Current, Unipolar			±1			±1	μA
Current, Bipolar			±5			±5	μA
Monotonicity Temp. Range (14-Bits)	0		+50	0		+70	°C
DRIFT (Over Specified Temp Range)							
Total Bipolar Drift (include gain, offset, and linearity drift), Voltage		±7	±15		±5	±8	ppm of FSR/°C
Current		±15	±50		±10	±40	ppm of FSR/°C
Total Error over Temp Range[4]							
Voltage, Unipolar			±0.083			±0.045	% of FSR
Bipolar			±0.071			±0.05	% of FSR
Current, Unipolar			±0.23			±0.24	% of FSR
Bipolar			±0.23			±0.24	% of FSR
Gain, Voltage			±15			±5	ppm/°C
Current			±45			±35	ppm/°C
Offset							
Voltage, Unipolar		±1	±2		±1	±2	ppm of FSR/°C
Bipolar			±10			±5	ppm of FSR/°C
Current, Unipolar			±1			±1	ppm of FSR/°C
Bipolar			±40			±35	ppm of FSR/°C
Differential Linearity over Temperature			±2			±1	ppm of FSR/°C
Linearity Error over Temperature			±2			±1	ppm of FSR/°C
SETTLING TIME							
Voltage Models (to ±0.003% of FSR)							
Output: 20V Step		5	10		5	10	μs
1LSB Step[5]		3	5		3	5	μs
Slew Rate		20			20		V/μs
Current Models (to ±0.003% of FSR)							
Output: 2mA step 10Ω to 100Ω Load			1			1	μs
1kΩ Load			3			3	μs
Switching Transient		500			500		mV
ANALOG OUTPUT							
Voltage Models							
Ranges – CSB		0 to +10			0 to +10		V
COB		±10			±10		V
Output Current	±5			±5			mA
Output Impedance (dc)		0.05			0.05		Ω
Short Circuit Duration		Indefinite to Common			Indefinite to Common		
Current Models							
Ranges – CSB		0 to −2			0 to −2		mA
COB		±1			±1		mA
Output Impedance – Unipolar		15			15		kΩ
Bipolar		4.4			4.4		kΩ
Compliance			±2.5			±2.5	V
INTERNAL REFERENCE VOLTAGE	6.0	6.3	6.6	6.0	6.3	6.6	V
Maximum External Current[6]			±5			±5	mA
Temp. Coeff. of Drift			±10			±5	ppm/°C
POWER SUPPLY SENSITIVITY							
Unipolar Offset							
±15V dc		±0.0001			±0.0001		% of FSR/% V_S
+5V dc		±0.0001			±0.0001		% of FSR/% V_S
Bipolar Offset							
±15V dc		±0.0004			±0.0004		% of FSR/% V_S
+5V dc		±0.0001			±0.0001		% of FSR/% V_S
Gain							
±15V dc		±0.001			±0.001		% of FSR/% V_S
+5V dc		±0.0005			±0.0005		% of FSR/% V_S
POWER SUPPLY REQUIREMENTS							
DAC71/72	±14.5, +4.75	±15.0, +5	±15.5, +5.25	±14.5, +4.75	±15.0, +5	±15.5, +5.25	V dc
Supply Drain, ±15V dc (no load)		±25	±35		±25	±35	mA
+5V dc (logic supply)		20	30		20	30	mA
TEMPERATURE RANGE							
Specification	0		+70	−25		+85	°C
Operating (double above Drift Specs)	−25		+85	−55		+100	°C
Storage	−55		+100	−55		+110	°C

NOTES

[1] Adding external CMOS hex buffers CD4009A will provide 15V dc CMOS input compatability.

[2] FSR means Full Scale Range and is 20V for ± 10V range, 10V for ± 5V range, etc.

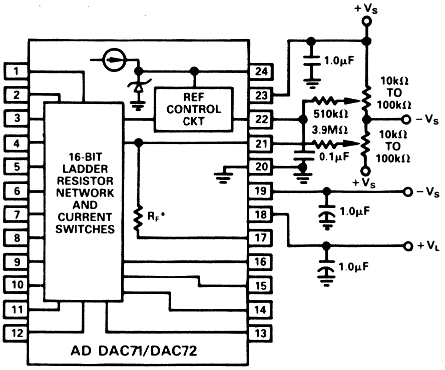
[3] Adjustable to zero with external trim potentiometer.

[4] With gain and offset errors adjusted to zero at 25°C.

[5] LSB is for 14-bit resolution.

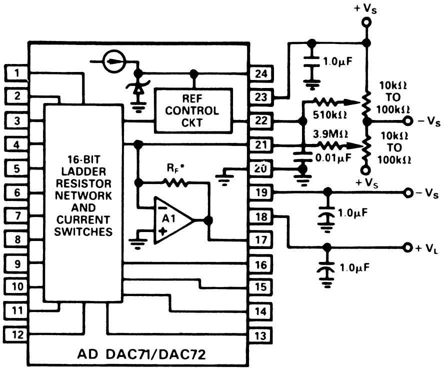
[6] Maximum with no degradation of specification.

Specifications subject to change without notice.



*R_F = 5kΩ (CSB), 10kΩ (COB)

Figure 1. External Adjustment and Voltage Supply Connection Diagram, Current Model



*R_F = 5kΩ (CSB), 10kΩ (COB)

Figure 2. External Adjustment and Voltage Supply Connection Diagram, Voltage Model

PIN CONFIGURATION

24 LEAD DUAL IN-LINE PACKAGE

	I Models	Pin #	V Models
(MSB)	Bit 1	1	Bit 1 (MSB)
	Bit 2	2	Bit 2
	Bit 3	3	Bit 3
	Bit 4	4	Bit4
	Bit 5	5	Bit 5
	Bit 6	6	Bit 6
	Bit 7	7	Bit 7
	Bit 8	8	Bit 8
	Bit 9	9	Bit 9
	Bit 10	10	Bit 10
	Bit 11	11	Bit 11
	Bit 12	12	Bit 12
	Bit 13	13	Bit 13
	Bit 14	14	Bit 14
	Bit 15	15	Bit 15
(LSB)	Bit 16	16	Bit 16 (LSB)
	R_F	17	V_{OUT}
	+5V dc	18	+5V dc
	−15V dc	19	−15V dc
	Common	20	Common
	I_{OUT}	21	Summing Junction
	Gain Adjust	22	Gain Adjust
	+15V dc	23	+15V dc
	6.3V_{REF} Out	24	6.3V_{REF} Out

ORDERING GUIDE

Model	Output	Input Code	Temp Range	Package Seal	Package Option[1]
AD DAC71–COB–I	Current	Comp. Offset Binary	0 to +70°C	Polymer	HY24B
AD DAC71–CSB–I	Current	Comp. Straight Binary	0 to +70°C	Polymer	HY24B
AD DAC72C–COB–I	Current	Comp. Offset Binary	0 to +70°C	Hermetic	HY24B
AD DAC72C–CSB–I	Current	Comp. Straight Binary	0 to +70°C	Hermetic	HY24B
AD DAC72-COB-I	Current	Comp. Offset Binary	−25°C to +85°C	Hermetic	HY24B
AD DAC72-CSB-I	Current	Comp. Straight Binary	−25°C to +85°C	Hermetic	HY24B
AD DAC71–COB–V	Voltage	Comp. Offset Binary	0 to +70°C	Polymer	HY24B
AD DAC71–CSB–V	Voltage	Comp. Straight Binary	0 to +70°C	Polymer	HY24B
AD DAC72C–COB–V	Voltage	Comp. Offset Binary	0 to +70°C	Hermetic	HY24B
AD DAC72C–CSB-V	Voltage	Comp. Straight Binary	0 to +70°C	Hermetic	HY24B
AD DAC72-COB-V	Voltage	Comp. Offset Binary	−25°C to +85°C	Hermetic	HY24B
AD DAC72-CSB-V	Voltage	Comp. Straight Binary	−25°C to +85°C	Hermetic	HY24B

[1] See Section 20 for package outline information.

DISCUSSION OF SPECIFICATIONS

Digital Input Codes

The AD DAC71 and AD DAC72 accept complementary digital input codes in a binary format. The CSB (complementary straight binary) versions provide unipolar outputs proportional to the binary input code. The COB (complementary offset binary) versions deliver a bipolar analog output in response to the offset binary digital input code. The COB versions can also be used with CTS (complementary two's complement) coding by inverting the most significant bit. Table I shows the relationship between the digital inputs and analog outputs.

		CSB Compl. Straight Binary	**COB Compl. Offset Binary**	**CTS Compl. Two's Compl.**
All Bits On	0000 . . . 0000	+ Full Scale	+ Full Scale	- 1LSB
Mid-Scale	0111 . . . 1111	+ 1/2 Full Scale	Zero	- Full Scale
All Bits Off	1111 . . . 1111	Zero	- Full Scale	Zero
	1000 . . . 0000	Mid-Scale - 1LSB	- 1LSB	+ Full Scale

Table I. Digital Input Codes

ACCURACY

Linearity Error

Linearity error is the most important accuracy specification in a digital-to-analog converter, since it cannot be externally trimmed or adjusted. Linearity is defined as the deviation of the DAC's actual analog output from a straight line drawn between the endpoints. The AD DAC71 and AD DAC72 feature guaranteed maximum linearity error of 0.003% of full scale.

Differential Linearity Error

Differential linearity error is the deviation from an ideal 1LSB output change when the digital input changes 1LSB. A differential linearity error specification of ± ½LSB means that the output changes at least ± ½LSB and at most ± ½LSB for a 1LSB increment in digital input code.

Monotonicity

Monotonicity indicates that the output of the DAC in question will always increase (or stay the same) for an increasing digital input code. Converters generally specify the maximum resolution for which monotonicity is guaranteed over a particular temperature range. The AD DAC71 and AD DAC72C are guaranteed monotonic at 14-bit resolution for 0 to +50°C, while the AD DAC72 is guaranteed 14-bit monotonic from 0 to +70°C.

Drift

Gain drift is a measure of the change in full scale output range as a function of temperature, expressed in parts per million (ppm) per °C. Gain drift is computed by testing the full scale range at +25°C and the endpoints of the applicable temperature range. The resulting change is divided by the temperature change and converted to ppm/°C.

Offset drift is a measure of the actual change in output with all "1"s on the digital inputs as a result of changes in temperature. For COB versions, the bipolar offset drift is measured with an input code of 011111111111.

SETTLING TIME

Settling time is defined as the total time required for the analog output to settle to within a particular error band around its final value after a change in the digital input code. In the case of the AD DAC71 and AD DAC72, the error band is specified as 0.003% of full scale. The specification for a 1LSB change is measured at the major carry (1000 . . . 00 to 0111 . . . 11) with the LSB defined as the 14-bit LSB.

Current output versions are specified for settling into two different resistive loads: 10Ω to 100Ω and 1000Ω.

OUTPUT COMPLIANCE VOLTAGE

Compliance voltage is the maximum voltage swing allowed on the output of the current models while maintaining specified accuracy. The AD DAC71 and AD DAC72 are specified for a compliance range of 2.5 volts and maximum safe voltage swing permitted without damage is 5 volts.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of change in either the positive, negative, or logic supplies about the nominal power supply voltages.

REFERENCE SUPPLY

All AD DAC71 and AD DAC72 models are supplied with an internal +6.3V reference voltage supply. This reference voltage (pin 24) has a tolerance of 5% and is connected internally for specified operation. The zener is selected for a gain drift of typically 3ppm/°C and is burned-in for a total of 168 hours for guaranteed reliability. This reference may also be used externally but the current drain is limited to 5mA. An external buffer amplifier is recommended if the AD DAC71/72 internal reference is used externally in order to provide a constant load to the reference supply output.

ANALOG DEVICES

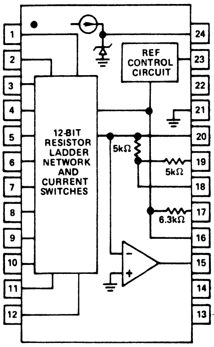
Low Cost 12-Bit IC D/A Converter

AD DAC80*

FEATURES

Low Cost
Improved Replacement for Standard DAC80
3 Chip, High Reliability Construction
Low Power Dissipation
Laser-Trimmed to High Accuracy:
±½LSB Max Nonlinearity, 0 to +70°C
Guaranteed Monotonicity, 0 to +70°C
High Stability, High Current Output
Buried Zener Reference
On-Board Output Amplifier (V Models)
24 Lead Side Brazed Ceramic DIP

AD DAC80 FUNCTIONAL BLOCK DIAGRAM



24-PIN DIP

PRODUCT DESCRIPTION

The AD DAC80 is a low cost 12-bit digital-to-analog converter, consisting of matched bipolar switches, a precision resistor network, a low-drift high-stability voltage reference and an optional output amplifier. Options include TTL compatible complementary 12-bit binary (CBI) or 3 digit BCD (CCD) input codes, as well as current or voltage output modes. The AD DAC80 offers output voltage ranges of ±2.5, ±5, ±10, 0 to +5, or 0 to +10 volts (V models); output current ranges (I models) are either ±1mA or 0 to -2mA.

Advanced circuit design and precision processing techniques result in significant performance advantages over conventional, larger, standard DAC80 devices. An innovative 3-chip construction improves reliability by a factor of two. The AD DAC80 incorporates a fully differential, nonsaturating precision current switching cell structure which provides greatly increased immunity to supply voltage variation. This same structure also reduces nonlinearities due to thermal transients as the various bits are switched; nearly all critical components operate at constant power dissipation. High stability, SiCr thin film resistors are trimmed with a fine resolution laser, resulting in lower differential nonlinearity errors. A low noise,, high stability subsurface zener diode is used to produce a reference voltage with excellent long term stability, high external current capability and temperature cycle characteristics which challenge the best discrete zener references.

The AD DAC80 is recommended for all low cost 12-bit D/A converter applications where reliability and cost are of paramount importance. The AD DAC80 is also ideal for use in constructing A/D conversion systems and as a building block for higher resolution D/A systems.

PRODUCT HIGHLIGHTS

1. The AD DAC80 directly replaces other devices of this type with significant increases in performance.
2. 3-Chip IC construction makes the AD DAC80 the optimum choice for applications where low cost and high reliability are major considerations.
3. System performance upgrading is possible without redesign.
4. The AD DAC80 offers a maximum nonlinearity error of ±0.012%, ±30ppm/°C maximum gain drift, and a total accuracy drift in the bipolar configuration of ±20ppm/°C maximum.
5. The low T.C. Binary ladder guarantees that all AD DAC80 units will be monotonic over the specified temperature range.
6. Reduced power consumption requirements result in improved stability and shorter warm-up time.
7. The precision buried zener reference can supply up to 2.5mA for use elsewhere in the application.
8. Voltage or current output modes are available in either of the BCD or binary input formats.

***Covered by Patent Nos.: 3,978,473; RE28,633; 4,020,486; 3,747,088; 3,803,590; 3,961,326.**

SPECIFICATIONS (T_A = +25°C, rated power supplies unless otherwise noted)

MODEL	DAC80-CBI	DAC80-CCD
DIGITAL INPUT		
Resolution	12 Bits max	3 Digits max
Logic Levels (TTL/Compatible)		
Logical "1" (at +1μA)	+2V dc min, +5.5V dc max	*
Logical "0" (at -100μA)	0V dc min, +0.8V dc max	*
ACCURACY		
Linearity Error 0 to +70°C	±1/4LSB typ, ±1/2LSB[1] max	±1/8LSB typ, ±1/4LSB max
Differential Linearity Error 0 to +70°C	±1/2LSB typ, ±3/4LSB max	±1/4LSB typ, ±1/2LSB max
Gain Error[2]	±0.1% typ, ±0.3% max	*
Offset Error[2]	±0.05% FSR typ, ±0.15% FSR[3] max	*
Monotonicity Temp. Range	0 to +70°C	*
DRIFT[4] (0 to +70°C)		
Total Bipolar Drift (Includes Gain, Offset, and Linearity Drifts)[5]	±20ppm FSR/°C max	*
Total Error Over 0 to +70°C[6]		
Unipolar	±0.08% FSR typ, ±0.15% FSR max	*
Bipolar	±0.06% FSR typ, ±0.10% FSR max	*
Gain	±15ppm/°C typ, ±30ppm/°C max	*
Exclusive of Internal Reference	±5ppm/°C typ, ±7ppm/°C max	*
Unipolar Offset	±1ppm FSR/°C typ, ±3ppm FSR/°C max	*
Bipolar Offset	±5ppm FSR/°C typ, ±10ppm FSR/°C max	*
CONVERSION SPEED/V Models		
Settling Time to ±0.01% of FSR		
For FSR Change		
with 10kΩ Feedback[7]	5μs typ	*
with 5kΩ Feedback	3μs typ	*
For 1LSB Change	1.5μs typ	*
Slew Rate	10V/μs min, 15V/μs typ	*
CONVERSION SPEED/I Models		
Settling Time to ±0.01% of FSR		
For FSR Change		
10 to 100Ω Load	300ns typ	*
1kΩ Load	1μs typ	*
ANALOG OUTPUT/V Models		
Ranges[7]	±2.5V, ±5V, ±10V, 0 to +5V, 0 to +10V	0 to +10V
Output Current	±5mA min	*
Output Impedance (dc)	0.05Ω typ	*
Short Circuit Duration	Indefinite to Common	*
ANALOG OUTPUT/I Models		
Ranges	±1mA, 0 to -2mA typ	0 to -2mA typ
Output Impedance - Bipolar	3.2kΩ typ	*
Output Impedance - Unipolar	6.6kΩ typ	*
Compliance	+10V, -1.5V	*
INTERNAL REFERENCE VOLTAGE	+6.3V ±2%max	*
Tempco of Drift	±10ppm/°C typ, ±20ppm/°C max	*
External - Use Current[8]	+2.5mA max	*
Output Impedance	1.5Ω typ	*
POWER SUPPLY SENSITIVITY		
+15V Supply	±0.002% FSR/% V_S	*
-15V and +5V Supplies	±0.002% FSR/% V_S	*
POWER SUPPLY REQUIREMENTS		
DAC80	±14V dc, +4.75V dc min	*
	±15V dc, +5V dc typ	*
	±16V dc, +16V dc max	*
DAC80Z[7]	±11.4V dc, +4.75V dc min	*
	±12V dc, +5V dc typ	*
	±16V dc, +16V dc max	*
Supply Drain		
+15/+12V (Including 5mA Load)	10mA typ, 20mA max	*
-15/-12V (Including 5mA Load)	-20mA typ, -35mA max	*
+5V (Logic Supply)	8mA typ, 20mA max	
TEMPERATURE RANGE		
Specification	0 to +70°C max	*
Operating	-25°C to +85°C max	*
Storage	-55°C to +100°C	*

NOTES

[1] Least Significant Bit (LSB).

[2] Adjustable to zero with external trim potentiometer.

[3] FSR means "Full Scale Range" and is 20V for ±10V range, 10V for ±5V range, etc.

[4] To maintain drift spec internal feedback resistors must be used for current output models.

[5] See discussion on Performance Over Temperature.

[6] With gain and offset errors adjusted to zero at +25°C.

[7] DAC80Z supply range is ±12.0V min to ±16.0V max for ±5V and 0 to +5V outputs.

[8] Maximum with no degradation of specifications with constant load.

Specifications subject to change without notice.

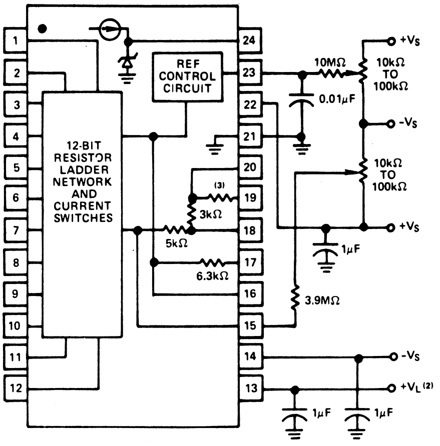


Figure 1. External Adjustment and Voltage Supply Connection Diagram, Current Model

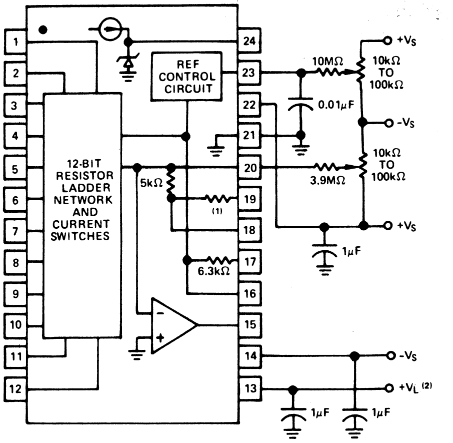


Figure 2. External Adjustment and Voltage Supply Connection Diagram, Voltage Model

NOTES:

1. 3kΩ for CCD models. 5kΩ for CBI models.
2. If connected to +V_S which is permissible, power dissipation increases 200mW.
3. CBI model, 2kΩ; CCD model, 0Ω and pin 20 has no internal connection.

PIN CONFIGURATION

24 LEAD DUAL IN-LINE PACKAGE

I Models	Pin #	V Models
(MSB) Bit 1	1	Bit 1(MSB)
Bit 2	2	Bit 2
Bit 3	3	Bit 3
Bit 4	4	Bit 4
Bit 5	5	Bit 5
Bit 6	6	Bit 6
Bit 7	7	Bit 7
Bit 8	8	Bit 8
Bit 9	9	Bit 9
Bit 10	10	Bit 10
Bit 11	11	Bit 11
(LSB) Bit 12	12	Bit 12 (LSB)

I Models	Pin #	V Models
Logic Supply	13	Logic Supply
$-V_S$	14	$-V_S$
I_{OUT}	15	V_{OUT}
Ref Input	16	Ref Input
Bipolar Offset	17	Bipolar Offset
Scaling Network	18	10V Range
Scaling Network	19	20V Range
Scaling Network	20	Summing Junction
Common	21	Common
$+V_S$	22	$+V_S$
Gain Adjust	23	Gain Adjust
$6.3V_{REF}$ Out	24	$6.3V_{REF}$ Out

AD DAC80 ORDERING GUIDE

MODEL	INPUT CODE	OUTPUT MODE	SUPPLY RANGE	PACKAGE OPTION[1]
AD DAC80-CBI-V	Binary	Voltage	Normal	HY24A
AD DAC80-CBI-I	Binary	Current	Normal	HY24A
AD DAC80-CCD-V	Binary Coded Decimal	Voltage	Normal	HY24A
AD DAC80-CCD-I	Binary Coded Decimal	Current	Normal	HY24A
AD DAC80Z-CBI-V	Binary	Voltage	Extended	HY24A
AD DAC80Z-CBI-I	Binary	Current	Extended	HY24A
AD DAC80Z-CCD-V	Binary Coded Decimal	Voltage	Extended	HY24A
AD DAC80Z-CCD-I	Binary Coded Decimal	Current	Extended	HY24A

[1] See Section 20 for package outline information.

DIGITAL INPUT CODES

The AD DAC80 accepts complementary digital input codes in either binary (CBI) or decimal (CCD) format. The CBI model may be connected by the user for any one of three complementary codes: CSB, COB or CTC.

	DIGITAL INPUT	ANALOG OUTPUT		
CBI Models	MSB LSB	CSB Compl. Straight Binary	COB Compl. Offset Binary	CTC* Compl. Two's Compl.
	000000000000	+Full Scale	+Full Scale	-LSB
	011111111111	+½ Full Scale	Zero	-Full Scale
	100000000000	Mid-scale -1LSB	-1 LSB	+Full Scale
	111111111111	Zero	-Full Scale	Zero
CCD Models	MSB LSB	CCD Complementary Coded Decimal - 3 Digits		
	0110 0110 0110	+Full Scale		
	1111 1111 1111	Zero		

*Invert the MSB of the COB code with an external inverter to obtain CTC code.

Table I. Digital Input Codes

ACCURACY

Accuracy error of a D/A converter is the difference between the analog output that is expected when a given digital code is applied and the output that is actually measured with that code applied to the converter. Accuracy error can be caused by gain error, zero error, linearity error, or any combination of the three. Of these three specifications, the linearity error specification is the most important since it can not be corrected for. The linearity error of the AD DAC80 is specified over its entire temperature range. This means that the analog output will not vary by more than ±1/2LSB, maximum, from an ideal straight line drawn between the end points (inputs all "1"s and all "0"s) over the specified temperature range of 0 to +70°C.

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output voltage step sizes can range from 1/2LSB to 3/2LSB when the input changes from one adjacent input state to the next. Monotonicity over the 0 to +70°C range is guaranteed in the AD DAC80 to ensure that the analog output will not decrease with increasing input digital codes.

DRIFT

Gain Drift is a measure of the change in the full scale range output over temperature expressed in parts per million per °C (ppm/°C). Gain drift is established by: 1) testing the end point differences for each AD DAC80 model at 0°C; +25°C and +70°C; 2) calculating the gain error with respect to the +25°C value and; 3) dividing by the temperature change.

Offset Drift is a measure of the actual change in output with all "1"s on the input over the specified temperature range. The offset is measured at 0°C, +25°C and +70°C. The maximum change in offset is referenced to the offset at 25°C and is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

SETTLING TIME

Settling time for each AD DAC80 model is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 3).

Voltage Output Models. Three settling times are specified to ±0.01% of full scale range (FSR); two for maximum full scale range changes of 20V, 10V and one for a 1LSB change. The 1LSB change is measured at the major carry (0 1 1 1 ... 1 1 to 1 0 0 0 ... 0 0), the point at which the worst case settling time occurs.

Current Output Models. Two settling times are specified to ±0.01% of FSR. Each is given for current models connected with two different resistive loads: 10 to 100 ohms and 1000 to 1875 ohms. Internal resistors are provided for connecting nominal load resistance of approximately 1000 to 1800 ohms for output voltage range of ±1V and 0 to -2V (see Table IV).

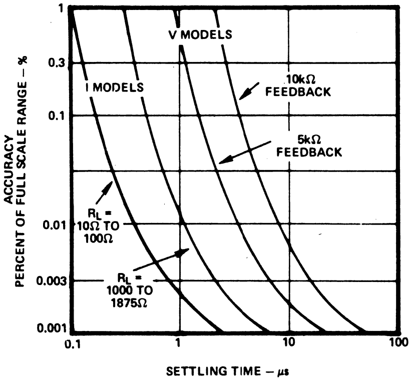


Figure 3. Full Scale Range Settling Time vs. Accuracy

COMPLIANCE

Compliance voltage is the maximum voltage swing allowed on the current output node in order to maintain specified accuracy.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a per cent of FSR per per cent of change in either the positive, negative, or logic supplies about the nominal power supply voltages.

REFERENCE SUPPLY

All AD DAC80 models are supplied with an internal 6.3 volt reference voltage supply. This voltage (pin 24) is accurate to ±2% and must be connected to the Reference Input (pin 16) for specified operation. This reference may also be used externally with external current drain limited to 2.5mA. An external buffer amplifier is recommended if this reference is to be used to drive other system components. Otherwise, variations in the load driven off of the reference will result in gain variations of the AD DAC80. All gain adjustments should be made under constant load conditions.

ANALYZING DEVICE ACCURACY OVER THE TEMPERATURE RANGE

For the purposes of temperature drift analysis, the major device components are shown in Figure 4. The reference element and buffer amplifier drifts are combined to give the total reference temperature coefficient, which is specified as ±20ppm/°C max. The input reference current to the DAC, I_{REF}, is developed from the internal reference and will show the same drift rate as the reference voltage. The DAC output current, I_{DAC}, which is a function of the digital input code, is designed to track I_{REF}; if there is a slight mismatch in these currents over temperature, it will contribute to the gain T.C. The bipolar offset resistor, R_{BP}, and gain setting resistor, R_{GAIN}, also have temperature coefficients which contribute to system drift errors. The input offset voltage drift of the output amplifier, OA, also contributes a small error.

There are three types of drift errors over temperature: offset, gain, and linearity. Offset drift causes a vertical translation of the entire transfer curve; gain drift is a change in the slope of the curve; and linearity drift represents a change in the shape of the curve. The combination of these three drifts results in the complete specification for total error over temperature.

Total error is defined as the deviation from a true straight line transfer characteristic from exactly zero at a digital input which calls for zero output to a point which is defined as full scale. A specification for total error over temperature assumes that both the zero and full scale points have been trimmed for zero error at +25°C. Total error is normally expressed a percentage of the full scale range. In the bipolar situation, this means the total range from $-V_{FS}$ to $+V_{FS}$.

Several new design concepts not previously used in DAC80-type devices contribute to a reduction in all the error factors over temperature. The incorporation of low temperature coefficient silicon-chromium thin-film resistors deposited on a single chip, a patented, fully differential, emitter weighted, precision current steering cell structure, and a T.C. trimmed buried zener diode reference element results in superior wide temperature range performance. The full scale gain settling resistors and bipolar offset resistor are also fabricated on the chip with the same SiCr material as the ladder network, resulting in low gain and offset drift.

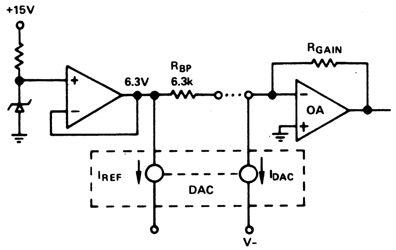


Figure 4. Bipolar Configuration

MONOTONICITY AND LINEARITY

The initial linearity error of ±1/2LSB max and the differential linearity error of ±3/4LSB max guarantee monotonic performance over the range of 0 to +70°C. It can therefore be assumed that linearity errors are insignificant in computation of total temperature errors.

UNIPOLAR ERRORS

Temperature error analysis in the unipolar mode is straightforward: there is an offset drift and a gain drift. The offset drift of 3ppm/°C max (which comes from leakage currents and drift in the output amplifier (OA)) causes a linear shift in the transfer curve as shown in Figure 5. The gain drift causes a change in the slope of the curve and results from reference drift, DAC drift, and drift in R_{GAIN} relative to the DAC resistors for a total of 30ppm/°C max. Total absolute error due to all of these effects is guaranteed to be less than ±0.15% of full scale from 0 to +70°C.

BIPOLAR RANGE ERRORS

The analysis is slightly more complex in the bipolar mode. In this mode R_{BP} is connected to the summing node of the output amplifier (see Figure 5) to generate a current which, exactly balances the current of the MSB so that the output voltage is zero with only the MSB on.

Note that if the DAC and application resistors track perfectly, the bipolar offset drift will be zero even if the reference drifts. A change in the reference voltage, which causes a shift in the bipolar offset, will also cause an equivalent change in I_{REF} and thus I_{DAC}, so that I_{DAC} will always be exactly balanced by I_{BP} with the MSB turned on. This effect is shown in Figure 5. The net effect of the reference drift then is simply to cause a rotation in the transfer around bipolar zero. However, consideration of second order effects (which are often overlooked) reveals the errors in the bipolar mode. The unipolar offset drifts discussed before will have the same effect on the bipolar offset. A mismatch of R_{BP} to the DAC resistors is usually the largest component of bipolar drift, but in the AD DAC80 this error is held to 10ppm/°C max. Gain drift in the DAC also contributes to bipolar offset drift, as well as full scale drift, but again is held to 7ppm/°C max. The total of all these errors is held to ±0.1% of full scale from 0 to +70°C. Note that, in the bipolar ranges, full scale is defined as the total range from $-V_{FS}$ to $+V_{FS}$.

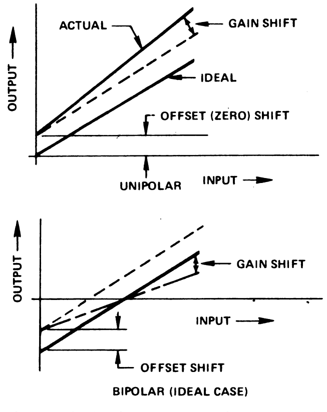


Figure 5. Unipolar and Bipolar Drifts

Using the AD DAC80

±12 VOLT SUPPLY OPERATION

The Z models will operate with supply voltages as low as ±11.4V. It is recommended that output voltage ranges -10V to +10V and 0V to +10V not be used with the Z model if the supply voltages are ever less than the recommended ±12V. The output amplifier may saturate if $|V_{SUPPLY}| - |V_{OUT}\ max| < 2.0V$. This applies to units with both CBI and CCD input codes. Except for operation at lower supply voltages, the AD DAC80Z and AD DAC80 operation is identical.

POWER SUPPLY CONNECTIONS

For optimum performance power supply decoupling capacitors should be added as shown in the connection diagrams (Figures 1 and 2). These capacitors (1µF electrolytic recommended) should be located close to the AD DAC80. Electrolytic capacapacitors, if used, should be paralleled with 0.01µF ceramic capacitors for optimum high frequency performance.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external OFFSET and GAIN potentiometers. These potentiometers should be connected as shown in the block diagrams and adjusted as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 10MΩ resistors (20% carbon or better) should be located close to the AD DAC 80 to prevent noise pick-up. If it is not convenient to use these high-value resistors, a functionally equivalent "T" network, as shown in Figure 6 may be substituted in each case. The gain adjust (pin 23) is a high impedance point and a 0.01µF ceramic capacitor should be connected from this pin to common to prevent noise pick-up. Figures 7 and 8 show the relationship of the OFFSET and GAIN adjustments to the unipolar and bipolar D/A converters.

Offset Adjustment. For unipolar (CSB, CCD) configurations, apply the digital input code that should produce zero potential output and adjust the OFFSET potentiometer for zero output. For bipolar (COD, CTC) configurations, apply the digital input code that should produce the maximum negative output voltage. Example: If the FULL SCALE RANGE is connected for 20 volts, the maximum negative output voltage is -10V. See Table II for corresponding codes and the block diagrams for offset adjustment connections.

Gain Adjustment. For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output. Adjust the GAIN potentiometer for this positive full scale voltage. See Table II for positive full scale voltages and the block diagrams for gain adjustment connections.

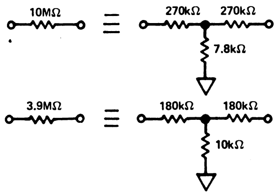


Figure 6. Equivalent Resistances

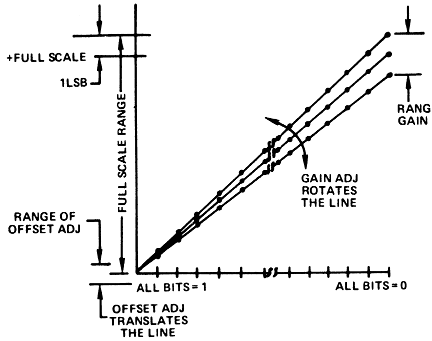


Figure 7. Relationship of OFFSET and GAIN Adjustments for a UNIPOLAR D/A Converter (Input, Horizontal; Output, Vertical)

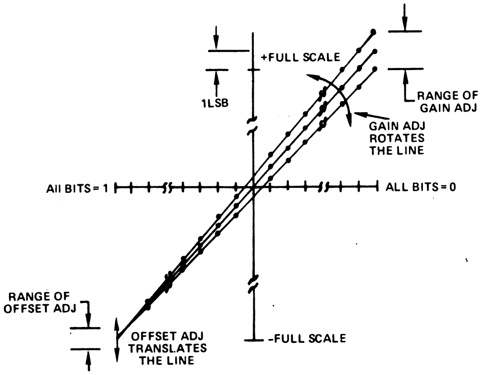


Figure 8. Relationship of OFFSET and GAIN Adjustments for a BIPOLAR D/A CONVERTER (Input, Horizontal; Output, Vertical)

	DIGITAL INPUT	ANALOG OUTPUT			
	12 Bit Resolution	VOLTAGE*		CURRENT	
CBI Models	MSB LSB	0 to +10V	±10V	0 to -2mA	±1mA
	000000000000	+9.9976V	+9.9951V	-1.9995mA	-0.9995mA
	011111111111	+5.0000V	0.0000V	-1.0000mA	0.0000mA
	100000000000	+4.9976V	-0.0049V	-0.9995mA	+0.0005mA
	111111111111	0.0000V	-10.0000V	0.0000mA	0.488µV
	1LSB	2.44mV	4.88mV	0.488mA	+1.000mA
CCD Models	3 Digital Resolution				
	MSB LSB				
	0110 0110 0110	+9.990V**	N/A	-1.249mA	N/A
	0110 0110 1111	+9.900V	N/A	-1.238mA	N/A
	0110 1111 1111	+9.000V	N/A	-1.125mA	N/A
	1111 1111 1111	0.000V	N/A	0.000mA	N/A
	1LSB	10.00mV	N/A	1.25µA	N/A

*To obtain values for other binary (CBI) ranges: 0 to +5V range: divide 0 to +10V range values by 2; ±5V range: divide ±10V range values by 2; ±2.5V range; divide ±10V range values by 4.

**Normal full scale range with correct codes; output can go higher if illegal codes are applied.

Table II. Digital Input/Analog Output

VOLTAGE OUPUT MODELS

Internal scaling resistors provided in the DAC80 may be connected to produce bipolar output voltage ranges of ±10, ±5 or ±2.5V or unipolar output voltage ranges of 0 to +5 or 0 to +10V (see Figure 9).

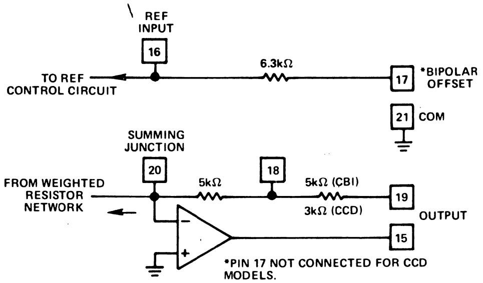


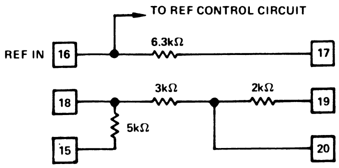
Figure 9. Output Amplifier Voltage Range Scaling Circuit

Gain and offset drift are minimized in the DAC80 because of the thermal tracking of the scaling resistors with other device components. Connections for various output voltage ranges are shown in Table III. Settling time is specified for a full scale range change: 5 microseconds for 8kΩ or 10kΩ feedback resistors; 3 microseconds for a 5kΩ feedback resistor.

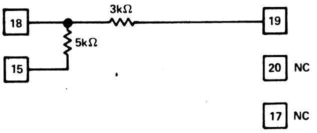
Output Range	Digital Input Codes	Connect Pin 15 to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10V	COB or CTC	19	20	15	24
±5V	COB or CTC	18	20	N.C.	24
±2.5V	COB or CTC	18	20	20	24
0 to +10V	CSB	18	21	N.C.	24
0 to +5V	CSB	18	21	20	24
0 to +10V	CCD	19	N.C.	15	24

Table III. Output Voltage Range Connections-Voltage Model AD DAC80

The equivalent resistive scaling network and output circuit of the current model are shown in Figures 10 and 11. External R_{LS} or R_{LP} resistors are required to produce exactly 0 to -2V or ±1V output. TCR of these resistors should be ±100ppm/°C or less to maintain the AD DAC80 output specifications. If exact output ranges are not required, the external resistors are not needed.



a) AD DAC80-CBI-I



b) AD DAC80-CCD-I

Figure 10. Internal Scaling Resistors

Internal resistors are provided to scale an external op amp or to configure a resistive load to offer two output voltage ranges of ±1V or 0 to -2V. These resistors (R_{LI}) are an integral part of the AD DAC80 and maintain gain and bipolar offset drift specifications. If the internal resistors are not used, external R_L (or R_F) resistors should have a TCR of ±25ppm/°C or less to minimize drift. This will typically add ±50ppm/°C + the TCR of R_L (or R_F) to the total drift.

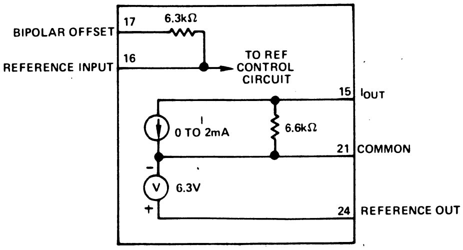


Figure 11. AD DAC80 Current Model Equivalent Output Circuit

Digital Input Codes	Output Range	Internal Resistance R_{LI}	1% Metal Film External Resistance R_{LS}	R_{LP}	R_{LI} Connections			Reference	Bipolar Offset		
					Connect Pin 15 to	Connect Pin 18 to	Connect Pin 20 to	Connect Pin 16 to	Connect Pin 17 to	R_{LS}	R_{LP}
CSB	0 to -2V	0.968kΩ	210Ω	N/A	20	19 & R_{LS}	15	24	Com (21)	Between Pin 18 & Com (21)	N/A
CCD	0 to -2V	3kΩ	N/A	3.57kΩ	N.C.	Com (21)	N.C.	24	N.C.	N/A	Between Pin 15 & 21
COB or CTC	±1V	1.2kΩ	249Ω	N/A	18	19	R_{LS}	24	15	Between Pin 20 & Com (21)	N/A

Table IV. Current Model/Resistive Load Connections

DRIVING A RESISTIVE LOAD UNIPOLAR

A load resistance, $R_L = R_{LI} + R_{LS}$, connected as shown in Figure 12 will generate a voltage range, V_{OUT}, determined by:

$$V_{OUT} = -2mA \left(\frac{6.6k \times R_L}{6.6k + R_L}\right)$$

Where R_L max = 1.54kΩ

and V_{OUT} max = -2.5V

To achieve specified drift, connect the internal scaling resistor (R_{LI}) as shown in Table IV to an external metal film trim resistor (R_{LS}) to provide full scale output voltage range of 0 to -2V. With $R_{LS} = 0$, $V_{OUT} = -1.69V$.

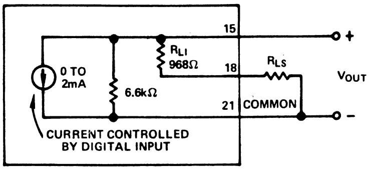


Figure 12 Equivalent Circuit AD DAC80-CBI-I Connected for Unipolar Voltage Output with Resistive Load

CCD Input Code: Connect the internal scaling resistors as shown in Table V and add an external metal film resistor (R_{LP}) in parallel as shown in Figure 13 to obtain a 0 to -2 volt full scale output voltage range for CCD input codes.

$$\text{With } R_L = \frac{R_{LI} \times R_{LP}}{R_{LI} + R_{LP}},$$

$$V_{OUT} = -1.25mA \left(\frac{6.9k \times R_L}{6.9k + R_L}\right)$$

If $R_{LP} = \infty$, $V_{OUT} = -3.62V$

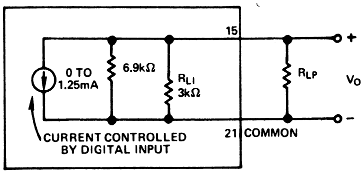


Figure 13. AD DAC80-CCD-I Connected for Voltage Output with Resistive Load

DRIVING A RESISTOR LOAD BIPOLAR

The equivalent output circuit for a bipolar output voltage range is shown in Figure 14, $R_L = R_{LI} + R_{LS}$. V_{OUT} is determined by:

$$V_{OUT} = \pm 1mA \left(\frac{R_L \times 3.22k}{R_L + 3.22k}\right)$$

Where R_L max = 11.18kΩ

V_{OUT} max = ±2.5V

To achieve specified drift, connect the internal scaling resistors (R_{LI}) as shown in Table IV for the COB or CTC codes and add an external metal film resistor (R_{LS}) in series to obtain a full scale output range of ±1V. In this configuration, with R_{LS} equal to zero, the full scale range will be ±0.874V.

DRIVING AN EXTERNAL OP AMP

The current model AD DAC80 will drive the summing junction of an op amp used as a current to voltage converter to produce an output voltage. As seen in Figure 15.

$$V_{OUT} = I_{OUT} \times R_F$$

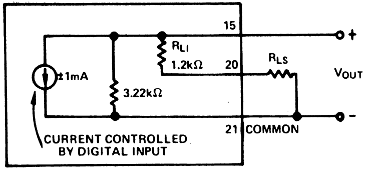
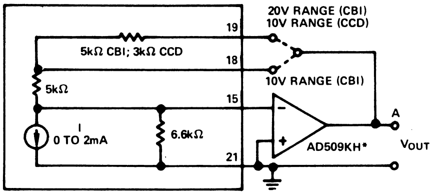


Figure 14. AD DAC80-CBI-I Connected for Bipolar Output Voltage with Resistive Load

where I_{OUT} is the AD DAC80 output current and R_F is the feedback resistor. Using the internal feedback resistors of the current model AD DAC80 provides output voltage ranges the same as the voltage model AD DAC80. To obtain the desired output voltage range when connecting an external op amp, refer to Table V and Figure 15.

Output Range	Digital Input Codes	Connect A to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10V	COB or CTC	19	15	A	24
±5V	COB or CTC	18	15	N.C.	24
±2.5V	COB or CTC	18	15	15	24
0 to +10V	CSB	18	21	N.C.	24
0 to +5V	CSB	18	21	15	24
0 to +10V	CCD	19	N.C.	A	24

Table V. Voltage Range of Current Output AD DAC80



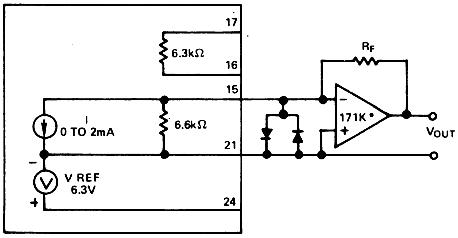
*FOR FAST SETTLING TIMES

Figure 15. External Op Amp – Using Internal Feedback Resistors

OUTPUT LARGER THAN 20V RANGE

For output voltage ranges larger than ±10 volts, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} values of ±1mA for bipolar voltage ranges and -2mA for unipolar voltage ranges (see Figure 16). Use protection diodes when a high voltage op amp is used.

The feedback resistor, R_F, should have a temperature coefficient as low as possible. Using an external feedback resistor, overall drift of the circuit increases due to the lack of temperature tracking between R_F and the internal scaling resistor network. This will typically add 50ppm/°C + R_F drift to total drift.



*FOR OUTPUT VOLTAGE SWINGS UP TO 140V p-p.

Figure 16. External Op Amp – Using External Feedback Resistors

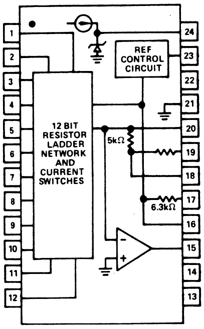
ANALOG DEVICES

High Performance 12-Bit IC D/A Converter

AD DAC85*

FEATURES
Improved Replacement for Standard DAC85
3 Chip, High Reliability Construction
Low Power Dissipation
Laser-Trimmed to High Accuracy:
  ±3/4LSB Max Nonlinearity, -55°C to +125°C
  (AD DAC85 MIL)
High Stability, High Current Output
  Buried Zener Reference
On-Board Output Amplifier (V Models)
24 Lead Side Brazed Ceramic DIP

AD DAC85 FUNCTIONAL BLOCK DIAGRAM



24-PIN DIP

PRODUCT DESCRIPTION

The AD DAC85 is a high performance 12-bit digital-to-analog converter, consisting of matched bipolar switches, a precision resistor network, a low-drift high-stability voltage reference and and an optional output amplifier. Options include TTL compatible complementary 12-bit binary (CBI) or 3 digit BCD (CCD) input codes, as well as current or voltage output modes. The AD DAC85 offers output voltage ranges of ±2.5, ±5, ±10, 0 to +5, or 0 to +10 volts (V models); output current ranges (I models) are either ±1mA or 0 to -2mA.

Advanced circuit design and precision processing techniques result in significant performance advantages over conventional, larger, standard DAC85 devices. An innovative 3-chip construction improves reliability by a factor of five.[1] The AD DAC85 incorporates a fully differential, non-saturating precision current switching cell structure which provides greatly increased immunity to supply voltage variation. This same structure also reduces nonlinearities due to thermal transients as the various bits are switched; nearly all critical components operate at constant power dissipation. High stability, SiCr thin film resistors are trimmed with a fine resolution laser, resulting in low differential nonlinearity errors. A low noise, high stability subsurface zener diode is used to produce a reference voltage with excellent long term stability, high external current capability and temperature cycle characteristics which challenge the best discrete zener references.

The AD DAC85 is recommended for all 12-bit D/A converter applications where reliability and performance over temperature are of paramount importance.

PRODUCT HIGHLIGHTS

1. The AD DAC85 directly replaces other devices of this type with significant increases in performance.
2. 3-Chip IC construction makes the AD DAC85 the optimum choice for applications where performance and reliability are major considerations.
3. System performance upgrading is possible without redesign.
4. The AD DAC85 offers a maximum nonlinearity error of ±0.012%, ±20ppm/°C maximum gain drift, and a total accuracy drift in the bipolar configuration of ±10ppm/°C maximum.
5. The low T.C. Binary ladder guarantees that all AD DAC85 units will be monotonic over the specified temperature range.
6. Reduced power consumption requirements result in improved stability and shorter warm-up time.
7. The precision buried zener reference can supply up to 2.5mA for use elsewhere in the application.
8. Voltage or current output modes are available in either of the BCD or binary input formats.

***Covered by Patent Nos. 3,978,473; RE 28,633; 4,020,486; 3,747,088; 3,803,590; 3,961,326.**

[1] For details of calculations see Application Note, "AD DAC85 Reliability Predictions".

SPECIFICATIONS (Typical @ +25°C unless otherwise specified)

MODEL	AD DAC85C	AD DAC85C	AD DAC85	AD DAC85	AD DAC85LD	AD DAC85MIL	UNITS
	CBI	CCD	CBI	CCD	CBI	CBI	
DIGITAL INPUT							
Resolution	12		12		12	12	Bits
		3		3			Digits
Logic Levels (TTL Compatible)							
Logic "1" (at +1μA)	+2V dc min, +5.5V dc max	*	*	*	*	*	V
Logic "0" (at -100μA)	0V dc min, +0.8V dc max	*	*	*	*	*	V
TRANSFER CHARACTERISTICS							
ACCURACY							
Linearity Error @ 25°C (max)	±1/2	±1/4	±1/2	±1/4	±1/2	±1/2	LSB
0 to +70°C (max)	±1/2	±1/2					LSB
-25°C to +85°C (max)			±1/2	±1/2	±1/2	±1/2	LSB
-55°C to +125°C (max)						±3/4	LSB
Differential Linearity Error	±1/2	*	*	*	*	*	LSB
Gain Error[1]	±0.1	*	*	*	*	*	%
Offset Error[1]	±0.05	*	*	*	*	*	% of FSR[2]
Minimum Temperature Range for Guaranteed Monotonicity	0 to +70	0 to +70	-25 to +85	-25 to +85	-25 to +85	-55 to +125	°C
DRIFT[3]							
Gain 0 to +70°C (max)	±20	±20	±20	±20	±10	±20	ppm/°C
-25°C to +85°C (max)	–	–	±20	±20	±10	±20	ppm/°C
-55°C to +125°C (max)	–	–	–	–	–	±20	ppm/°C
Offset							
Unipolar 0 to +70°C	+1	+1					ppm of FSR/°C
-25°C to +85°C			±1	±1	±1	±1	ppm of FSR/°C
-55°C to +125°C						±2	ppm of FSR/°C
Bipolar 0 to +70°C (max)	±10						ppm of FSR/°C
-25°C to +85°C (max)			±10		±5	±10	ppm of FSR/°C
-55°C to +125°C (max)						±10	ppm of FSR/°C
CONVERSION SPEED							
Voltage Models							
Settling Time to ±0.01% of FSR							
for FSR change							
with 10kΩ Feedback	5	*	*	*	*	*	μs
with 5kΩ Feedback	3	*	*	*	*	*	μs
for 1LSB change	1.5	*	*	*	*	*	μs
Slew Rate	20	*	*	*	*	*	V/μs
Current Models							
Settling Time to ±0.01% of FSR							
for FSR change 10 to 100Ω load	300	*	*	*	*	*	ns
1kΩ load	1	*	*	*	*	*	μs
ANALOG OUTPUT							
Voltage Models Ranges – CBI Units	±2.5, ±5, ±10, +5, +10	*	*	*	*	*	V
CCD Units	+10	*	*	*	*	*	V
Output Current (min)	±5	*	*	*	*	*	mA
Output Impedance (dc)	0.05	*	*	*	*	*	Ω
Current Models							
Ranges	±1, -2	*	*	*	*	*	mA
Output Impedance - Bipolar	3.2	*	*	*	*	*	kΩ
Unipolar	6.65	*	*	*	*	*	kΩ
Compliance	-2.5, +10.5	*	*	*	*	*	V
Internal Reference Voltage (V_r)	6.3	*	*	*	*	*	V
Output Impedance	1.5	*	*	*	*	*	Ω
Max. External Current[4]	2.5	*	*	*	*	*	mA
Max Reference Error	±2	*	*	*	*	*	%
Tempco of Drift	±10 typ, ±20 max	*	*	*	*	*	ppm of V_r/°C
POWER SUPPLY SENSITIVITY							
+15V Supply	±0.002	*	*	*	*	*	% of FSR/% V_S
-15 and +5V Supplies	±0.002	*	*	*	*	*	% of FSR/% V_S
POWER SUPPLY REQUIREMENTS							
Rated Voltage	±15 and +5	*	*	*	*	*	V
Range	±14.5 to ±15.5 and +4.50 to +15.5	*	*	*	*	*	V
Supply Drain							
+15V (including 5mA load)	15 typ, 20 max	*	*	*	*	*	mA
+5V	15 typ, 20 max	*	*	*	*	*	mA
-15V	25 typ, 30 max	*	*	*	*	*	mA
TEMPERATURE RANGE							
Specification	0 to +70	*	-25 to +85	-25 to +85	-25 to +85	-55 to +125	°C
Operating	-25 to +85	*	-55 to +125	-55 to +125	-55 to +125	-55 to +125	°C
Storage	-55 to +125	*	*	*	*	*	°C

NOTES

*Specifications same as AD DAC85C CBI.

[1] Adjustable to zero with external trim potentiometer.

[2] FSR means "full scale range" and is 20V for ±10V range, 10V for ±5V range, etc.

[3] To maintain drift spec internal feedback resistors must be used for current output models; the buried zener reference drift is a nonlinear function of temperature: all devices are tested to insure that actual drift at any temperature within the specified operating range is less than guaranteed maximum.

[4] With no degradation of specifications under constant load.

Specifications subject to change without notice.

MIL-STD-883B

The rigors of the military/aerospace environment (temperature extremes, humidity, mechanical stress, etc.), demand the utmost in electronic circuits. The AD DAC85 with the inherent reliability of integrated circuit construction, was designed with these applications in mind. To further insure reliability, the AD DAC85 is offered with 100% screening to MIL-STD-883, method 5008.

The quality assurance section details the test procedures of MIL-STD-883. All AD DAC85 models with 883B suffix have been processed in accordance with these tests on a 100% basis; AD DAC85 MIL-CBI-V-883B is an example of 883 Level B designation.

AD DAC85 ORDERING GUIDE

MODEL	INPUT CODE	OUTPUT MODE	TEMPERATURE RANGE	PACKAGE OPTION[1]
AD DAC85C-CBI-V	Binary	Voltage	0°C to +70°C	HY24A
AD DAC85C-CBI-I	Binary	Current	0°C to +70°C	HY24A
AD DAC85-CBI-V	Binary	Voltage	-25°C to +85°C	HY24A
AD DAC85-CBI-I	Binary	Current	-25°C to +85°C	HY24A
AD DAC85LD-CBI-V	Binary	Voltage	-25°C to +85°C	HY24A
AD DAC85LD-CBI-I	Binary	Current	-25°C to +85°C	HY24A
AD DAC85MIL-CBI-V	Binary	Voltage	-55°C to +125°C	HY24A
AD DAC85MIL-CBI-I	Binary	Current	-55°C to +125°C	HY24A
AD DAC85C-CCD-V	Binary Coded Decimal	Voltage	0°C to +70°C	HY24A
AD DAC85C-CCD-I	Binary Coded Decimal	Current	0°C to +70°C	HY24A
AD DAC85-CCD-V	Binary Coded Decimal	Voltage	-25°C to +85°C	HY24A
AD DAC85-CCD-I	Binary Coded Decimal	Current	-25°C to +85°C	HY24A

[1] See Section 20 for package outline information.

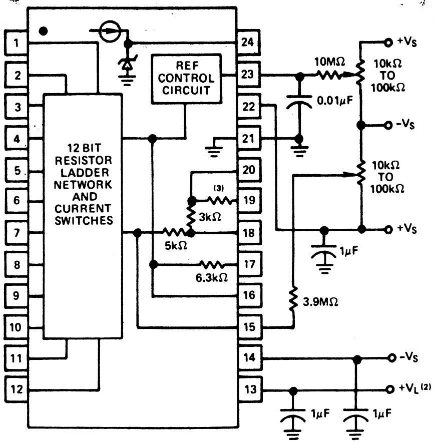


Figure 1. External Adjustment and Voltage Supply Connection Diagram, Current Model

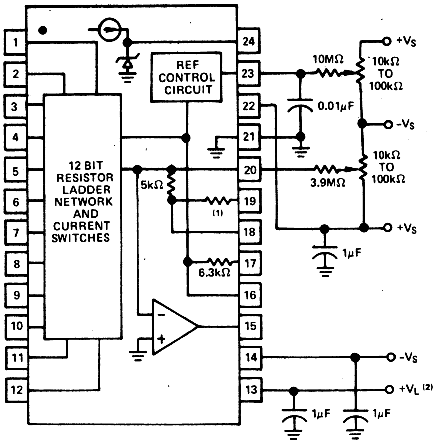


Figure 2. External Adjustment and Voltage Supply Connection Diagram, Voltage Model

NOTES:

1. 3kΩ for CCD models. 5kΩ for CBI models.
2. If connected to $+V_S$ which is permissible, power dissipation increases 200mW.
3. CBI model, 2kΩ; CCD model, 0Ω and pin 20 has no internal connection.

PIN CONFIGURATION

24 LEAD DUAL IN-LINE PACKAGE

I Models	Pin #	V Models
(MSB) Bit 1	1	Bit 1(MSB)
Bit 2	2	Bit 2
Bit 3	3	Bit 3
Bit 4	4	Bit 4
Bit 5	5	Bit 5
Bit 6	6	Bit 6
Bit 7	7	Bit 7
Bit 8	8	Bit 8
Bit 9	9	Bit 9
Bit 10	10	Bit 10
Bit 11	11	Bit 11
(LSB) Bit 12	12	Bit 12 (LSB)

I Models	Pin #	V Models
Logic Supply	13	Logic Supply
$-V_S$	14	$-V_S$
I_{OUT}	15	V_{OUT}
Ref Input	16	Ref Input
Bipolar Offset	17	Bipolar Offset
Scaling Network	18	10V Range
Scaling Network	19	20V Range
Scaling Network	20	Summing Junction
Common	21	Common
$+V_S$	22	$+V_S$
Gain Adjust	23	Gain Adjust
6.3V_{REF} Out	24	6.3V_{REF} Out

DIGITAL INPUT CODES

The AD DAC85 accepts complementary digital input codes in either binary (CBI) or decimal (CCD) format. The CBI model may be connected by the user for any one of three complementary codes: CSB, COB or CTC.

	DIGITAL INPUT	ANALOG OUTPUT		
CBI Models	MSB LSB	CSB Compl. Straight Binary	COB Compl. Offset Binary	CTC* Compl. Two's Compl.
	000000000000	+Full Scale	+Full Scale	-LSB
	011111111111	+½ Full Scale	Zero	-Full Scale
	100000000000	Mid-scale -1LSB	-1 LSB	+Full Scale
	111111111111	Zero	-Full Scale	Zero
CCD Models	MSB LSB	CCD Complementary Coded Decimal - 3 Digits		
	0110 0110 0110	+Full Scale		
	1111 1111 1111	Zero		

*Invert the MSB of the COB code with an external inverter to obtain CTC code.

Table I. Digital Input Codes

ACCURACY

Accuracy error of a D/A converter is the difference between the analog output that is expected when a given digital code is applied and the output that is actually measured with that code applied to the converter. Accuracy error can be caused by gain error, zero error, linearity error, or any combination of the three. Of these three specifications, the linearity error specification is the most important since it can not be corrected for. The linearity error of the AD DAC85 is specified over its entire temperature range. This means that the analog output will not vary by more than ±1/2LSB, maximum, from an ideal straight line drawn between the end points (inputs all "1"s and all "0"s) over the specified temperature range of -25°C to +85°C.

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output voltage step sizes can range from 1/2LSB to 3/2LSB when the input changes from one adjacent input state to the next. Monotonicity over the -25°C to +85°C range is guaranteed in the AD DAC85 to insure that the analog output will not decrease with increasing input digital codes.

DRIFT

Gain Drift is a measure of the change in the full scale range output over temperature expressed in parts per million per °C (ppm/°C). Gain drift is established by: 1) testing the end point differences for each AD DAC85 model at the lowest operating temperature, +25°C and the highest operating temperature; 2) calculating the gain error with respect to the +25°C value and; 3) dividing by the temperature change.

Offset Drift is a measure of the actual change in output with all "1"s on the input over the specified temperature range. For example, the offset for the "C" version is measured at 0°C, +25°C and +70°C. The maximum change in offset is referenced to the offset at 25°C and is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

SETTLING TIME

Settling time for each AD DAC85 model is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 3).

Voltage Output Models. Three settling times are specified to ±0.01% of full scale range (FSR); two for maximum full scale range changes of 20V, 10V and one for a 1LSB change. The 1LSB change is measured at the major carry (0 1 1 1 ... 1 1 to 1 0 0 0 ... 0 0), the point at which the worst case settling time occurs.

Current Output Models. Two settling times are specified to ±0.01% of FSR. Each is given for current models connected with two different resistive loads: 10 to 100 ohms and 1000 to 1875 ohms. Internal resistors are provided for connecting nominal load resistances of approximately 1000 to 1800 ohms for output voltage range of ±1V and 0 to -2V(see Table IV).

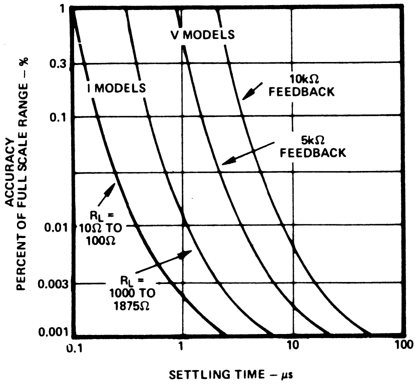


Figure 3. Full Scale Range Settling Time vs. Accuracy

COMPLIANCE

Compliance voltage is the maximum voltage swing allowed on the current output node in order to maintain specified accuracy.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a per cent of FSR per per cent of change in either the positive, negative, or logic supplies about the nominal power supply voltages.

REFERENCE SUPPLY

All AD DAC85 models are supplied with an internal 6.3 volt reference voltage supply. This voltage (pin 24) is accurate to ±2% and must be connected to the Reference Input (pin 16) for specified operation. This reference may also be used externally with external current drain limited to 2.5mA. An external buffer amplifier is recommended if this reference is to be used to drive other system components. Otherwise, variations in the load driven off of the reference will result in gain variations of the AD DAC85. All gain adjustments should be made under constant load conditions.

Using the AD DAC85

POWER SUPPLY CONNECTIONS

For optimum performance power supply decoupling capacitors should be added as shown in the connection diagrams (Figures 1 and 2). These capacitors (1μF electrolytic recommended) should be located close to the AD DAC85. Electrolytic capacitors, if used, should be paralleled with 0.01μF ceramic capacitors for optimum high frequency performance.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external OFFSET and GAIN potentiometers. These potentiometers should be connected as shown in the block diagrams in Figures 1 and 2 and adjusted as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩand 10MΩ resistors (20% carbon or better) should be located close to the AD DAC85 to prevent noise pick-up. If it is not convenient to use these high-value resistors, a functionally equivalent "T" network, as shown in Figure 4 may be substituted in each case. The gain adjust (pin 23) is a high impedance point and a 0.01μF ceramic capacitor should be connected from this pin to common to prevent noise pick-up. Figures 5 and 6 show the relationship of the OFFSET and GAIN adjustments to the unipolar and bipolar D/A converters.

Offset Adjustment. For unipolar (CSB, CCD) configurations, apply the digital input code that should produce zero potential output and adjust the OFFSET potentiometer for zero output. For bipolar (COD, CTC) configurations, apply the digital input code that should produce the maximum negative output voltage. Example: If the FULL SCALE RANGE is connected for 20 volts, the maximum negative output voltage is -10V. See Table II for corresponding codes and the block diagrams in Figures 1 and 2 for offset adjustment connections.

Gain Adjustment. For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output. Adjust the GAIN potentiometer for this positive full scale voltage. See Table II for positive full scale voltages and the block diagrams for gain adjustment connections.

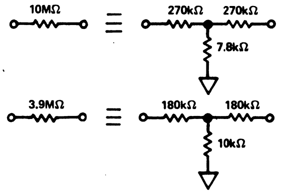


Figure 4. Equivalent Resistances

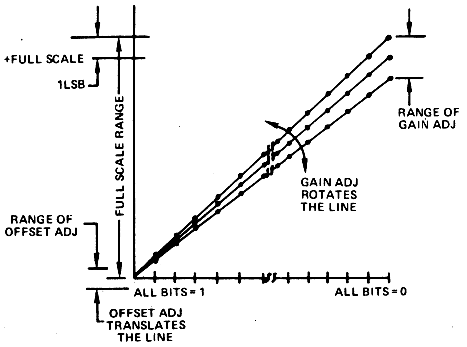


Figure 5. Relationship of OFFSET and GAIN Adjustments for a UNIPOLAR D/A Converter (Input, Horizontal; Output, Vertical)

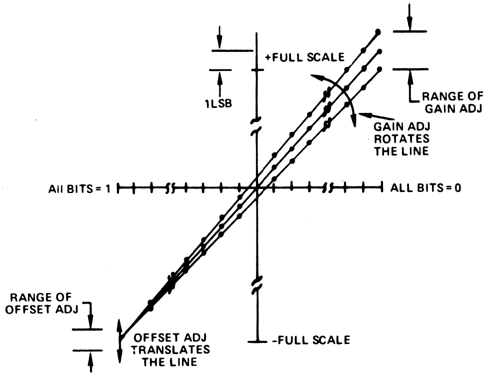


Figure 6. Relationship of OFFSET and GAIN Adjustments for a BIPOLAR D/A CONVERTER (Input, Horizontal; Output, Vertical)

	DIGITAL INPUT	ANALOG OUTPUT			
	12 Bit Resolution	VOLTAGE*		CURRENT	
CBI Models	MSB LSB	0 to +10V	±10V	0 to -2mA	±1mA
	000000000000	+9.9976V	+9.9951V	-1.9995mA	-0.9995mA
	011111111111	+5.0000V	0.0000V	-1.0000mA	0.0000mA
	100000000000	+4.9976V	-0.0049V	-0.9995mA	+0.0005mA
	111111111111	0.0000V	-10.0000V	0.0000mA	0.488μV
	1LSB	2.44mV	4.88mV	0.488mA	+1.000mA
CCD Models	3 Digital Resolution				
	MSB LSB				
	0110 0110 0110	+9.990V**	N/A	-1.249mA	N/A
	0110 0110 1111	+9.900V	N/A	-1.238mA	N/A
	0110 1111 1111	+9.000V	N/A	-1.125mA	N/A
	1111 1111 1111	0.000V	N/A	0.000mA	N/A
	1LSB	10.00mV	N/A	1.25μA	N/A

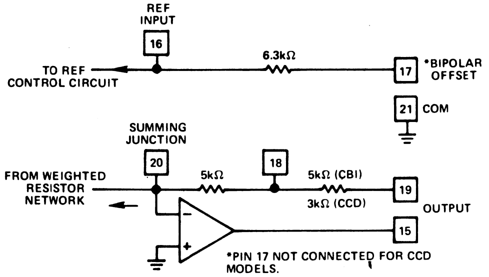
*To obtain values for other binary (CBI) ranges: 0 to +5V range: divide 0 to +10V range values by 2; ±5V range: divide ±10V range values by 2; ±2.5V range; divide ±10V range values by 4.

**Normal full scale range with correct codes; output can go higher if illegal codes are applied.

Table II. Digital Input/Analog Output

VOLTAGE OUTPUT MODELS

Internal scaling resistors provided in the AD DAC85 may be connected to produce bipolar output voltage ranges of ±10, ±5 or ±2.5V or unipolar output voltage ranges of 0 to +5V or 0 to +10V (see Figure 7).



*PIN 17 NOT CONNECTED FOR CCD MODELS.

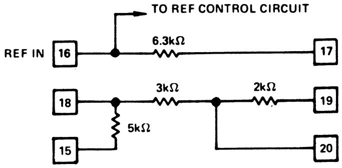
Figure 7. Output Amplifier Voltage Range Scaling Circuit

Gain and offset drift are minimized in the AD DAC85 because of the thermal tracking of the scaling resistors with other device components. Connections for various output voltage ranges are shown in Table III. Settling time is specified for a full scale range change: 5 microseconds for 8kΩ or 10kΩ feedback resistors; 3 microseconds for a 5kΩ feedback resistor.

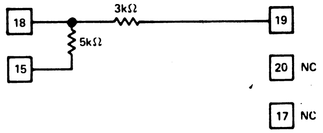
Output Range	Digital Input Codes	Connect Pin 15 to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10V	COB or CTC	19	20	15	24
±5V	COB or CTC	18	20	N.C.	24
±2.5V	COB or CTC	18	20	20	24
0 to +10V	CSB	18	21	N.C.	24
0 to +5V	CSB	18	21	20	24
0 to +10V	CCD	19	N.C.	15	24

Table III. Output Voltage Range Connections-Voltage Model AD DAC85

The equivalent resistive scaling network and output circuit of the current model are shown in Figures 8 and 9. External R_{LS} or R_{LP} resistors are required to produce exactly 0 to -2V or ±1V output. TCR of these resistors should be ±100ppm/°C or less to maintain the AD DAC85 output specifications. If exact output ranges are not required, the external resistors are not needed.



a) AD DAC85-CBI-I



b) AD DAC85-CCD-I

Figure 8. Internal Scaling Resistors

Internal resistors are provided to scale an external op amp or to configure a resistive load to offer two output voltage ranges of ±1V or 0 to -2V. These resistors (R_{LI}) are an integral part of the AD DAC85 and maintain gain and bipolar offset drift specifications. If the internal resistors are not used, external R_L (or R_F) resistors should have a TCR of ±25ppm/°C or less to minimize drift. This will typically add ±50ppm/°C + the TCR of R_L (or R_F) to the total drift.

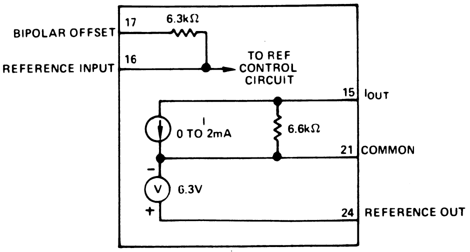


Figure 9. AD DAC85 Current Model Equivalent Output Circuit

Digital Input Codes	Output Range	Internal Resistance R_{LI}	1% Metal Film External Resistance R_{LS}	1% Metal Film External Resistance R_{LP}	R_{LI} Connections: Connect Pin 15 to	R_{LI} Connections: Connect Pin 18 to	R_{LI} Connections: Connect Pin 20 to	Reference: Connect Pin 16 to	Bipolar Offset: Connect Pin 17 to	Bipolar Offset: R_{LS}	Bipolar Offset: R_{LP}
CSB	0 to -2V	0.968kΩ	210Ω	N/A	20	19 & R_{LS}	15	24	Com (21)	Between Pin 18 & Com (21)	N/A
CCD	0 to -2V	3kΩ	N/A	3.57kΩ	N.C.	Com (21)	N.C.	24	N.C.	N/A	Between Pin 15 & 21
COB or CTC	±1V	1.2kΩ	249Ω	N/A	18	19	R_{LS}	24	15	Between Pin 20 & Com (21)	N/A

Table IV. Current Model/Resistive Load Connections

DRIVING A RESISTIVE LOAD UNIPOLAR

A load resistance, $R_L = R_{LI} + R_{LS}$, connected as shown in Figure 10 will generate a voltage range, V_{OUT}, determined by:

$$V_{OUT} = -2\text{mA} \left(\frac{6.6\text{k} \times R_L}{6.6\text{k} + R_L} \right)$$

Where R_L max = 1.54kΩ

and V_{OUT} max = −2.5V

To achieve specified drift, connect the internal scaling resistor (R_{LI}) as shown in Table IV to an external metal film trim resistor (R_{LS}) to provide full scale output voltage range of 0 to −2V. With $R_{LS} = 0$, $V_{OUT} = -1.69\text{V}$.

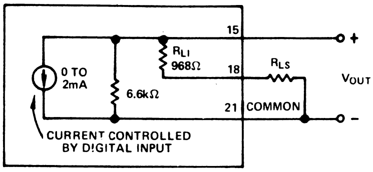


Figure 10. Equivalent Circuit AD DAC85-CBI-I Connected for Unipolar Voltage Output with Resistive Load

CCD Input Code: Connect the internal scaling resistors as shown in Table V and add an external metal film resistor (R_{LP}) in parallel as shown in Figure 11 to obtain a 0 to −2 volt full scale output voltage range for CCD input codes.

$$\text{With } R_L = \frac{R_{LI} \times R_{LP}}{R_{LI} + R_{LP}},$$

$$V_{OUT} = -1.25\text{mA} \left(\frac{6.9\text{k} \times R_L}{6.9\text{k} + R_L} \right)$$

If $R_{LP} = \infty$, $V_{OUT} = -3.62\text{V}$

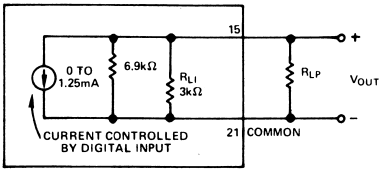


Figure 11. AD DAC85-CCD-I Connected for Voltage Output with Resistive Load

DRIVING A RESISTOR LOAD BIPOLAR

The equivalent output circuit for a bipolar output voltage range is shown in Figure 12, $R_L = R_{LI} + R_{LS}$. V_{OUT} is determined by:

$$V_{OUT} = \pm 1\text{mA} \left(\frac{R_L \times 3.22\text{k}}{R_L + 3.22\text{k}} \right)$$

Where R_L max = 11.18kΩ

V_{OUT} max = ±2.5V

To achieve specified drift, connect the internal scaling resistors (R_{LI}) as shown in Table IV for the COB or CTC codes and add an external metal film resistor (R_{LS}) in series to obtain a full scale output range of ±1V. In this configuration, with R_{LS} equal to zero, the full scale range will be ±0.874V.

DRIVING AN EXTERNAL OP AMP

The current model AD DAC85 will drive the summing junction of an op amp used as a current to voltage converter to produce an output voltage. As seen in Figure 13.

$$V_{OUT} = I_{OUT} \times R_F$$

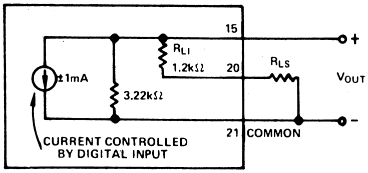
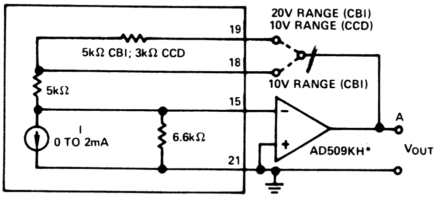


Figure 12. AD DAC85-CBI-I Connected for Bipolar Output Voltage with Resistive Load

where I_{OUT} is the AD DAC85 output current and R_F is the feedback resistor. Using the internal feedback resistors of the current model AD DAC85 provides output voltage ranges the same as the voltage model AD DAC85. To obtain the desired output voltage range when connecting an external op amp, refer to Table V and Figure 13.

Output Range	Digital Input Codes	Connect A to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10V	COB or CTC	19	15	A	24
±5V	COB or CTC	18	15	N.C.	24
±2.5V	COB or CTC	18	15	15	24
0 to +10V	CSB	18	21	N.C.	24
0 to +5V	CSB	18	21	15	24
0 to +10V	CCD	19	N.C.	A	24

Table V. Voltage Range of Current Output AD DAC85



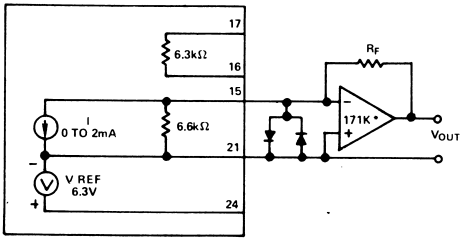
*FOR FAST SETTLING TIMES

Figure 13. External Op Amp – Using Internal Feedback Resistors

OUTPUT LARGER THAN 20V RANGE

For output voltage ranges larger than ±10 volts, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} values of ±1mA for bipolar voltage ranges and −2mA for unipolar voltage ranges (see Figure 14). Use protection diodes when a high voltage op amp is used.

The feedback resistor, R_F, should have a temperature coefficient as low as possible. Using an external feedback resistor, overall drift of the circuit increases due to the lack of temperature tracking between R_F and the internal scaling resistor network. This will typically add 50ppm/°C + R_F drift to total drift.



*FOR OUTPUT VOLTAGE SWINGS UP TO 140V p-p.

Figure 14. External Op Amp – Using External Feedback Resistors

ANALOG DEVICES

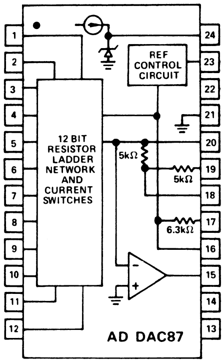
Wide Temperature Range 12-Bit IC D/A Converter

AD DAC87*

FEATURES

Wide Temperature Range: -55°C to +125°C
Pin-Compatible with AD DAC80 and AD DAC85
3 Chip, High Reliability Construction
Low Power Dissipation
Laser-Trimmed to High Accuracy:
±3/4LSB Max Nonlinearity, -55°C to +125°C
High Stability, High Current Output
Buried Zener Reference
On-Board Output Amplifier (V Models)
24 Lead Side Brazed Hermetically-Sealed Ceramic DIP
MIL-STD-883 Processing Available

AD DAC87 FUNCTIONAL BLOCK DIAGRAM



24-PIN DIP

PRODUCT DESCRIPTION

The AD DAC87 is a high performance 12-bit digital-to-analog converter, consisting of matched bipolar switches, a precision resistor network, a low-drift high-stability voltage reference and an optional output amplifier. The digital inputs are TTL compatible with complementary binary (CBI) input coding. The AD DAC87 offers output voltage ranges of ±2.5, ±5, ±10, 0 to +5, or 0 to +10 volts (V models); output current ranges (I models) are either ±1mA or 0 to -2mA.

Advanced circuit design and precision processing techniques result in significant performance advantages over conventional, larger, standard DAC87 devices. An innovative 3-chip construction improves reliability by a factor of five.[1] The AD DAC87 incorporates a fully differential, non-saturating precision current switching cell structure which provides greatly increased immunity to supply voltage variation. This same structure also reduces nonlinearities due to thermal transients as the various bits are switched; nearly all critical components operate at constant power dissipation. High stability SiCr thin film resistors are trimmed with a fine resolution laser, resulting in low differential linearity errors. A low noise, high stability subsurface zener diode is used to produce a reference voltage with excellent long term stability, high external current capability and temperature drift characteristics which challenge the best discrete zener references.

The AD DAC87 is recommended for all 12-bit D/A converter applications where reliability and performance over temperature are of paramount importance.

PRODUCT HIGHLIGHTS

1. The AD DAC87 directly replaces other devices of this type with significant increases in performance.
2. 3-Chip IC construction makes the AD DAC87 the optimum choice for applications where performance and reliability are major considerations.
3. System performance upgrading is possible without redesign.
4. The AD DAC87 offers a maximum nonlinearity of ±0.012%, ±25ppm/°C maximum gain drift, and a total accuracy drift in the bipolar configuration of ±0.24% of FSR maximum over the -55°C to +125°C temperature range.
5. The low T.C. Binary ladder guarantees that all AD DAC87 units will be monotonic over the specified temperature range.
6. Reduced power consumption requirements result in improved stability and shorter warm-up time.
7. The precision buried zener reference can supply up to 2.5mA for use elsewhere in the application.
8. Voltage or current output models are available.
9. The solder-sealed ceramic package provides a reliable hermetic metal-to-metal seal.
10. All accuracy and drift parameters are 100% tested at -55°C and +125°C to insure high performance over the full temperature range.
11. Both voltage and current output models are available processed to the requirements of MIL-STD-883, method 5008, class B.

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*Covered by Patent Nos. 3,978,473; RE 28,633; 4,020,486; 3,747,088; 3,803,590; 3,961,326.

[1] For details of calculations see Application Note, "AD DAC87 Reliability Predictions".

SPECIFICATIONS (T_A = +25°C, rated power supplies unless otherwise noted)

MODEL	AD DAC87-CBI			
	MIN	TYP	MAX	UNITS
DIGITAL INPUT				
Resolution			12	Bits
Logic Levels (TTL Compatible)				
Logic "1" (at +1μA)	+2		+5.5	V
Logic "0" (at -100μA)	0		+0.8	V
TRANSFER CHARACTERISTICS				
ACCURACY				
Linearity Error @ +25°C		±1/4	±1/2	LSB
-55°C to +125°C			±3/4	LSB
Differential Linearity Error at +25°C		±1/2	±3/4	LSB
-55°C to +125°C			±1	LSB
Gain Error[1]		±0.1	±0.2	%
Offset Error[1]		±0.05	±0.1	%FSR[2]
Temperature Range for Guaranteed Monotonicity	-55		+125	°C
DRIFT[3] (-55°C to +125°C)				
Total Bipolar Drift, max (includes gain, offset, and linearity drifts)		±15	±30	ppm of FSR/°C
Total Error (-55°C to +125°C)[4]				
Unipolar		±0.13	±0.3	% of FSR
Bipolar		±0.12	±0.24	% of FSR
Gain				
Including Internal Reference		±10	±25	ppm/°C
Excluding Internal Reference		±5	±10	ppm/°C
Unipolar Offset		±1	±3	ppm of FSR/°C
Bipolar Offset		±5	±10	ppm of FSR/°C
CONVERSION SPEED				
Voltage Model (AD DAC87-CBI-V)				
Settling Time to ±0.01% of FSR				
for FSR change				
with 10kΩ Feedback		5		μs
with 5kΩ Feedback		3		μs
for 1LSB change		1.5		μs
Slew Rate	10	20		V/μs
Current Model (AD DAC87-CBI-I)				
Settling Time to ±0.01% of FSR				
for FSR Change 10 to 100Ω Load		300		ns
1kΩ Load		1		μs
ANALOG OUTPUT				
Voltage Models				
Ranges		±2.5, ±5, ±10, 0 to +5, 0 to +10		V
Output Current	±5			mA
Output Impedance (dc)		0.05		Ω
Short Circuit Duration		INDEFINITE TO COMMON		
Current Models				
Ranges		±1, 0 to -2		mA
Output Impedance – Bipolar	2.5	3.3	4.1	kΩ
– Unipolar	5.0	6.6	8.2	kΩ
Compliance	-1.5		+10.5	V
Internal Reference Voltage (V_R)	+6.17	+6.3	+6.43	V
Output Impedance		1.5		Ω
Max. External Current[5]			2.5	mA
Tempco of Drift		±5	±10	ppm of V_R/°C
POWER SUPPLY SENSITIVITY				
+15V Supply		±0.002	±0.003	% of FSR/%V_S
-15V and +5V Supplies		±0.002	±0.003	% of FSR/%V_S
POWER SUPPLY REQUIREMENTS				
Rated Voltages		±15, +5		V
Range	±13.5, +4.5		±16.5, +16.5	V
Supply Drain				
+15V (Including 5mA Load)		10	20	mA
+5V		10	20	mA
-15V		20	30	mA
TEMPERATURE RANGE				
Specification	-55		+125	°C
Storage	-65		+150	°C
PACKAGE OPTION[6]		HY24A		

NOTES

[1] Adjustable to zero with external trim potentiometer.

[2] FSR means "full scale range" and is 20V for ±10V range, 10V for ±5V range, etc.

[3] To maintain drift spec internal feedback resistors must be used for current output models; the buried zener reference drift is a nonlinear function of temperature: all devices are tested to insure that actual drift at any temperature within the specified operating range is less than guaranteed maximum.

[4] With gain and offset errors adjusted to zero at +25°C.

[5] With no degradation of specifications under constant load.

[6] See Section 20 for package outline information.

Specifications subject to change without notice.

MIL-STD-883

The rigors of the military/aerospace environment (temperature extremes, humidity, mechanical stress, etc.), demand the utmost in electronic circuits. The AD DAC87, with the inherent reliability of integrated circuit construction, was designed with these applications in mind. To further insure reliability, the AD DAC87 is available with 100% screening to MIL-STD-883, method 5008.

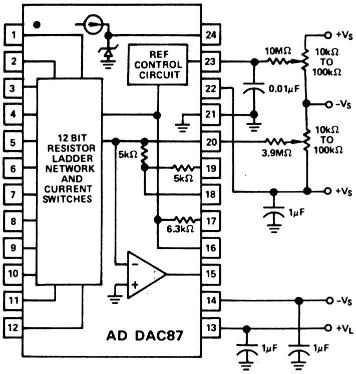


Figure 1. External Adjustment and Voltage Supply Connection Diagram, Voltage Model

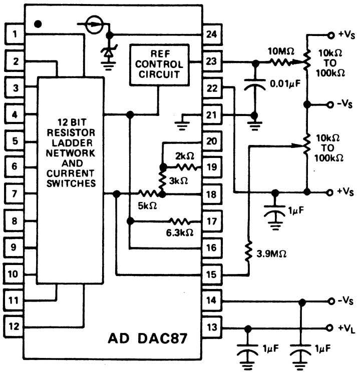


Figure 2. External Adjustment and Voltage Supply Connection Diagram, Current Model

PIN CONFIGURATION
24 LEAD DUAL IN-LINE PACKAGE

I Models	Pin #	V Models
(MSB) Bit 1	1	Bit 1(MSB)
Bit 2	2	Bit 2
Bit 3	3	Bit 3
Bit 4	4	Bit 4
Bit 5	5	Bit 5
Bit 6	6	Bit 6
Bit 7	7	Bit 7
Bit 8	8	Bit 8
Bit 9	9	Bit 9
Bit 10	10	Bit 10
Bit 11	11	Bit 11
(LSB) Bit 12	12	Bit 12 (LSB)
Logic Supply	13	Logic Supply
$-V_S$	14	$-V_S$
I_{OUT}	15	V_{OUT}
Ref Input	16	Ref Input
Bipolar Offset	17	Bipolar Offset
Scaling Network	18	10V Range
Scaling Network	19	20V Range
Scaling Network	20	Summing Junction
Common	21	Common
$+V_S$	22	$+V_S$
Gain Adjust	23	Gain Adjust
$6.3V_{REF}$ Out	24	$6.3V_{REF}$ Out

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external OFFSET and GAIN potentiometers, as shown in the block diagrams on the previous page. TCR of the potentiometers should be 100ppm/°C or less. If it is not convenient to use the 3.9MΩ and 33MΩ resistors shown, a functionally equivalent "T" network, as shown in Figure 3 may be substituted in each case.

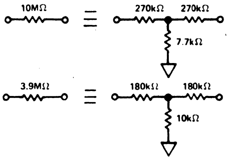


Figure 3. Equivalent Resistances

Offset Adjustment. For unipolar configurations, apply the digital input code that should produce zero potential output and adjust the OFFSET potentiometer for zero output. For bipolar configurations, apply the digital input code that should produce the maximum negative output voltage. Example: If the FULL SCALE RANGE is connected for 20 volts, the maximum negative output voltage is -10V. See Table I for corresponding codes and the block diagrams on the previous page for offset adjustment connections.

Gain Adjustment. For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output. Adjust the GAIN potentiometer for this positive full scale voltage. See Table I for positive full scale voltages and the block diagrams for gain adjustment connections.

DIGITAL INPUT	ANALOG OUTPUT			
12 Bit Resolution	VOLTAGE		CURRENT	
MSB LSB	0 to +10V	±10V	0 to -2mA	±1mA
000000000000	+9.9976V	+9.9951V	-1.9995mA	-0.9995mA
011111111111	+5.0000V	0.0000V	-1.0000mA	0.0000mA
100000000000	+4.9976V	-0.0049V	-0.9995mA	+0.0005mA
111111111111	0.0000V	-10.0000V	0.0000mA	+1.000mA
1LSB	2.44mV	4.88mV	0.488μA	0.488μA

Table I. Digital Input/Analog Output

VOLTAGE OUTPUT MODELS

Internal scaling resistors provided in the AD DAC87 may be connected to produce bipolar output voltage ranges of ±10, ±5 or ±2.5V or unipolar output voltage ranges of 0 to +5V or 0 to +10V (see Figure 4).

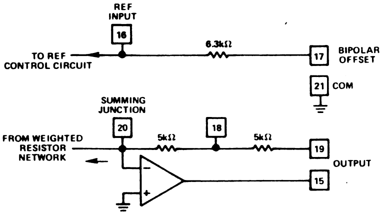


Figure 4. Output Amplifier Voltage Range Scaling Circuit

Gain and offset drift are minimized in the AD DAC87 because of the thermal tracking of the scaling resistors with other device components. Connections for various output voltage ranges are shown in Table II.

Output Range	Digital Input Codes	Connect Pin 15 to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10V	COB or CTC	19	20	15	24
±5V	COB or CTC	18	20	N.C.	24
±2.5V	COB or CTC	18	20	20	24
0 to +10V	CSB	18	21	N.C.	24
0 to +5V	CSB	18	21	20	24

Table II. Output Voltage Range Connections AD DAC87-CBI-V

CURRENT OUTPUT MODELS

The current output model of the AD DAC87 can be used to drive a resistive load directly to produce a voltage output. Recommended output ranges and pin connections are shown in Table III.

Digital Input Codes	Output Range	External Resistance R_{LS}	Connect Pin 15 to	Connect Pin 18 to	Connect Pin 20 to	Connect Pin 16 to	Connect Pin 17 to	R_{LS}
CSB	0 to -2V	210Ω	20	19 & R_{LS}	15	24	Com (21)	Between Pin 18 & Com (21)
COB or CTC	±1V	249Ω	18	19	R_{LS}	24	15	Between Pin 20 & Com (21)

Table III. AD DAC87-CBI-I Resistive Load Connections

DRIVING A RESISTIVE LOAD UNIPOLAR

A load resistance, $R_L = R_{LI} + R_{LS}$, connected as shown in Figure 5a will generate a voltage range, V_{OUT}, determined by:

$$V_{OUT} = -2\text{mA} \left(\frac{6.6\text{k} \times R_L}{6.6\text{k} + R_L}\right)$$

Where R_L max = 1.54kΩ

and V_{OUT} max = -2.5V

To achieve specified drift connect the internal scaling resistor (R_{LI}) as shown in Table III to an external metal film trim resistor (R_{LS}) to provide full scale output voltage range of 0 to -2V. With R_{LS} = 0, V_{OUT} = -1.69V.

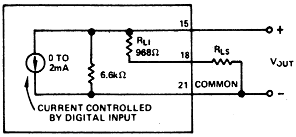


Figure 5a. Unipolar Voltage Output

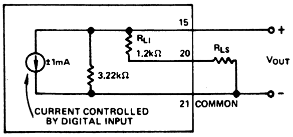


Figure 5b. Bipolar Voltage Output

Figure 5. AD DAC87-CBI-I Equivalent Circuit Driving Resistive Loads

DRIVING A RESISTIVE LOAD BIPOLAR

The equivalent output circuit for a bipolar output voltage range is shown in Figure 5b, $R_L = R_{LI} + R_{LS}$. V_{OUT} is determined by:

$$V_{OUT} = \pm 1\text{mA} \left(\frac{R_L \times 3.22\text{k}}{R_L + 3.22\text{k}}\right)$$

Where R_L max = 11.18kΩ

V_{OUT} max = ±2.5V

To achieve specified drift, connect the internal scaling resistors (R_{LI}) for the COB or CTC codes and add an external metal film resistor (R_{LS}) in series to obtain a full scale output range of ±1V. In this configuration, with R_{LS} equal to zero, the full scale range will be ±0.874V.

ANALOG DEVICES

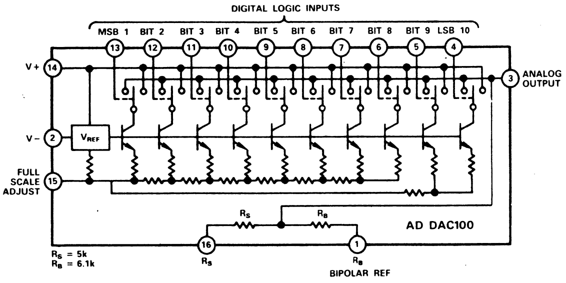
10-Bit Monolithic D/A Converter

AD DAC100

FEATURES

Complete Current Output Converter
High Stability Buried Zener Reference
Single Chip Monolithic Construction
Wide Supply Range ±6V to ±18V
Trimmed Output Application Resistors
Fast Settling – 225ns (8 Bits), 375ns (10 Bits)
Guaranteed Monotonicity Over Full Operating Temperature Range
TTL and DTL Compatible Logic Inputs
MIL-STD-883B Processed Models Available
Hermetically-Sealed 16-Pin Ceramic DIP (All Grades)

AD DAC100 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD DAC100 is a 10-bit digital-to-analog converter with a high stability voltage reference fabricated on a single monolithic chip. Using 10 precision high-speed current-steering switches, a control amplifier, voltage reference, and laser-trimmed thin-film SiCr resistor network, the device produces a fast, accurate analog output current. Laser trimmed output application resistors are also included to facilitate accurate, stable current-to-voltage conversion.

The AD DAC100 also incorporates a low noise, high stability subsurface zener diode to produce a reference voltage with excellent long term stability and temperature cycle characteristics which challenge the best discrete zener references. A temperature compensation circuit is laser-trimmed to allow correction of the temperature coefficient of each device. This results in a maximum full-scale temperature coefficient of 15ppm/°C for the L and U versions, 30ppm/°C max for the K and T versions, 60ppm/°C max for the J and S versions.

All grades are packaged in a 16-pin hermetically-sealed ceramic dual-in-line package. The J, K, L versions are specified for operation over the –25°C to +85°C temperature range, the AD DAC100S, T and U for operation over the full military temperature range from –55°C to +125°C. MIL-STD-883B processing is available on all grades.

PRODUCT HIGHLIGHTS

1. The AD DAC100 is a true second-source equivalent to the industry standard DAC100.
2. The high impedance current output can be used with an external op amp and the internal applications resistors to produce a low impedance output voltage.
3. The AD DAC100 is available with a 10 volt output; or 5 volt version, consult factory.
4. The AD DAC100 is available in chip form for use in hybrid microcircuits.
5. MIL-STD-883 processing to method 5004, Class B is available on all grades and temperatures ranges, both industrial (–25°C to +85°C) and military (–55°C to +125°C).

SPECIFICATIONS (V_S = ±15V, −25°C≤T_A≤+85°C for J, K, L devices; −55°C≤T_A≤+125°C for S, T, U devices unless otherwise specified)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Resolution			10	10	10	Bits
Nonlinearity	N_L	K, L, T, U (±½LSB – 10 Bits)	–	–	±0.05	% FS
	N_L	J, S (±½LSB – 9 Bits)	–	–	±0.1	% FS
Full Scale Tempco	T_C	L, U	–	–	±15	ppm/°C
	T_C	K, T	–	–	±30	ppm/°C
	T_C	J, S	–	–	±60	ppm/°C
Settling Time T_A = ±25°C	t_S	to ±0.05% FS	–	–	375	ns
	t_S	to ±0.1% FS	–	–	300	ns
	t_S	to ±0.2% FS	–	–	225	ns
	t_S	to ±0.4% FS	–	–	150	ns
	t_S	to ±0.8% FS	–	–	100	ns
Full Range Output Voltage* Adjustable to 10.0V with External 200Ω Trimmer	V_{FR}	Connect FS Adjust to V –	10	–	11.1	V
Zero Scale Output Voltage	V_{ZS}	V_{IN} = 2.1V	–	–	0.013	% FS
Logic Inputs: High	V_{INH}	Measured with Respect to Output Pin	2.1	–	–	V
Logic Inputs: Low	V_{INL}	Measured with Respect to Output Pin	–	–	0.7	V
Logic Input Current, Each Input	I_{IN}	V_{IN} = 0 to +6V	–	–	5	µA
Logic Input Resistance	R_{IN}	V_{IN} = 0 to +6V	–	3	–	MΩ
Logic Input Capacitance	C_{IN}		–	2	–	pF
Output Resistance	R_O		–	500	–	kΩ
Output Capacitance	C_O		–	13	–	pF
Applied Power Supplies: V +		Linearity within Specification	+6	–	+18	V
Applied Power Supplies: V –		Linearity within Specification	–6	–	–18	V
Power Supply Sensitivity	P_{SS}	V_S + ±6V to ±18V	–	–	±0.10	% per volt
Power Consumption	P_D	V_S = ±15V	–	200	250	mW
Positive Supply Current	I +	V_S = +15V	–	–	8.33	mA
Negative Supply Current	I –	V_S = –15V	–	–	–8.33	mA

*Using external op amp for I/V conversion (see Figure 3).

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

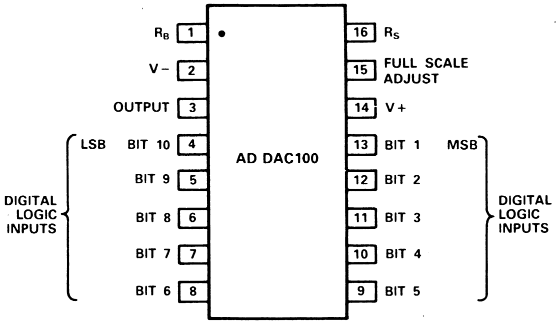
V+ Supply to V – Supply	0 to +36V
V+ Supply to Output	0 to +18V
V – Supply to Output	0 to –18V
Logic Inputs to Output	–1V to +6V
Power Dissipation[1]	500mW

Operating Temperature Range	
AD DAC100J, K, L	–25°C to +85°C
AD DAC100S, T, U	–55°C to +125°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering)	+300°C (60 sec)

NOTE:

[1] Rating applies to ambient temperature of 100°C. Above 100°C, derate at 10mW/°C.

PIN CONFIGURATION TOP VIEW



AD DAC100 ORDERING GUIDE

Model	Temperature Range	Maximum Linearity Error %	Max T.C. ppm/°C	Package Type
AD DAC100JD	– 25°C to + 85°C	0.1	60	D16A
AD DAC100JD/883B	– 25°C to + 85°C	0.1	60	D16A
AD DAC100KD	– 25°C to + 85°C	0.05	30	D16A
AD DAC100KD/883B	– 25°C to + 85°C	0.05	30	D16A
AD DAC100LD	– 25°C to + 85°C	0.05	15	D16A
AD DAC100LD/883B	– 25°C to + 85°C	0.05	15	D16A
AD DAC100SD/883B	– 55°C to + 125°C	0.10	60	D16A
AD DAC100TD/883B	– 55°C to + 125°C	0.05	30	D16A
AD DAC100UD/883B	– 55°C to + 125°C	0.05	15	D16A

CROSS REFERENCE

Analog Devices	Precision Monolithics Inc.
AD DAC100JD	DAC-100 BCQ1, BCQ3, CCQ1, CCQ3, DDQ1, DDQ3
AD DAC100JD/883B	DAC-100 BCQ7, CCQ7, DDQ7
AD DAC100KD	DAC-100 ABQ1, ACQ1, ACQ3, BBQ1, BBQ3
AD DAC100KD/883B	DAC-100 ABQ7, ACQ7, BBQ7
AD DAC100LD	DAC-100 AAQ1
AD DAC100LD/883B	DAC-100 AAQ7
AD DAC100SD/883B	DAC-100 BCQ5, CCQ5, DDQ5
AD DAC100TD/883B	DAC-100 ABQ5, ACQ5, BBQ5
AD DAC100UD/883B	DAC-100 AAQ5, BAQ5

Applying the AD DAC100

DIGITAL INPUT CODES

The AD DAC100 accepts complementary digital input codes in either binary, offset binary or two's complement (see Table 1).

DIGITAL INPUT	ANALOG OUTPUT		
MSB LSB	Compl. Straight Binary	Compl. Offset Binary	Compl.* Two's Compl.
0000000000	+ Full Scale	+ Full Scale	− LSB
0111111111	+ ½ Full Scale	Zero	− Full Scale
1000000000	Mid-scale − LSB	− LSB	+ Full Scale
1111111111	Zero	− Full Scale	Zero

*Invert the MSB of the COB code with an external inverter to obtain CTC code.

Table 1. Digital Input Codes

ACCURACY

Accuracy error of a D/A converter is the difference between the analog output that is expected when a given digital code is applied and the output that is actually measured with that code applied to the converter. Accuracy error can be caused by gain error, zero error, linearity error, or any combination of the three. Of these three specifications, the linearity error specification is the most important since it cannot be corrected for. The linearity error of the AD DAC100 is specified over its entire temperature range. This means that the analog output will not vary by more than ± ½LSB, maximum, from an ideal straight line drawn between the end points (inputs all "1"s and all "0"s) over the specified temperature range (see Figures 1 and 2).

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ± 1LSB means that the output voltage step sizes can range from 0LSB to 2LSB when the input changes from one adjacent input state to the next. Monotonicity over the full temperature range is guaranteed in the AD DAC100 to insure that the analog output will not decrease with increasing input digital codes.

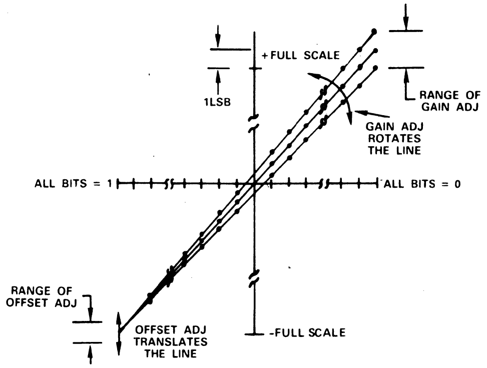


Figure 1. Relationship of OFFSET and GAIN Adjustments for a BIPOLAR D/A Converter (Input, Horizontal; Output, Vertical)

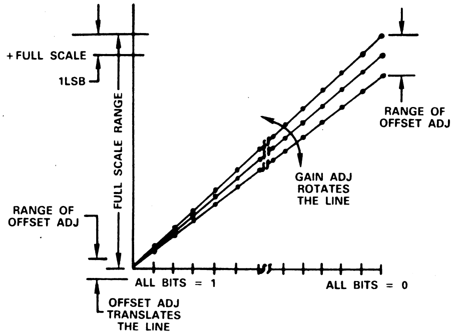
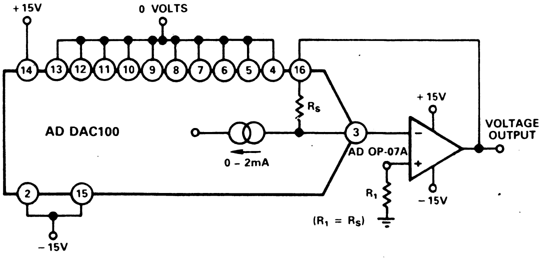


Figure 2. Relationship of OFFSET and GAIN Adjustments for a UNIPOLAR D/A Converter (Input, Horizontal; Output, Vertical)



NOTE:
FULL SCALE TEMPCO IS DEFINED AS THE CHANGE IN OUTPUT VOLTAGE MEASURED IN THE CIRCUIT ABOVE AND IS EXPRESSED IN PPM BETWEEN EITHER TEMPERATURE EXTREME DIVIDED BY THE CORRESPONDING TEMPERATURE CHANGE.

Figure 3. Full Scale Test Circuit

CONNECTING THE AD DAC100 FOR BUFFERED VOLTAGE OUTPUT

The standard current-to-voltage conversion connections using an operational amplifier are shown here with the preferred trimming techniques. If a low offset operational amplifier (AD544, AD547, AD509, AD510, AD741L) is used, excellent performance can be obtained in many situations without trimming. (A 5mV op amp offset is equivalent to ½LSB on a 10 volt scale).

The AD509 is recommended for buffered voltage-output applications which require a settling time to ± ½LSB of one microsecond. The feedback capacitor is shown with the optimum value for each application; this capacitor is required to compensate for the 13 picofarad DAC output capacitance.

FIGURE 4. UNIPOLAR CONFIGURATION

This configuration will provide a unipolar 0 to + 10 volt output range.

STEP I . . . ZERO ADJUST

Turn all bits HIGH and adjust op amp trimmer, R4, until the output reads 0.000 volts (1LSB = 9.76mV).

STEP II . . . GAIN ADJUST

Turn all bits LOW and adjust 200Ω gain trimmer, R2, until the output is 9.990 volts (Full scale is adjusted to 1LSB less than nominal full scale of 10.000 volts.)

FIGURE 5. BIPOLAR CONFIGURATION

This configuration will provide a bipolar output voltage from − 5.000 to + 4.990 volts, with positive full scale occurring with all bits LOW (all 0's).

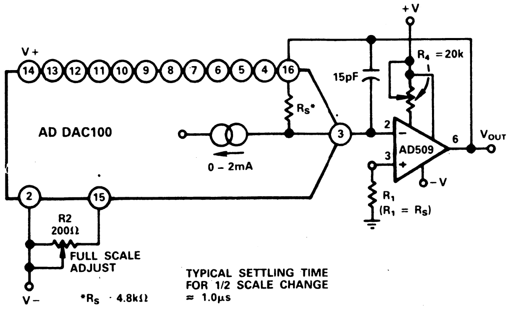
STEP I . . . OFFSET ADJUST

Turn all bits HIGH, adjust 200Ω gain trimmer to give a reading of − 5.000 volts.

STEP II . . . GAIN ADJUST

Turn LOW MSB only, turn all other bits HIGH. Adjust 500Ω trimmer R3, to give 0.000 output volts.

Please note that it is not necessary to trim the op amp to obtain full accuracy at room temperature. In most bipolar situations, the op amp trimmer is unnecessary unless the untrimmed offset drift of the op amp is excessive.



TYPICAL SETTLING TIME FOR 1/2 SCALE CHANGE ≈ 1.0μs

Figure 4. Unipolar Voltage Output Circuit

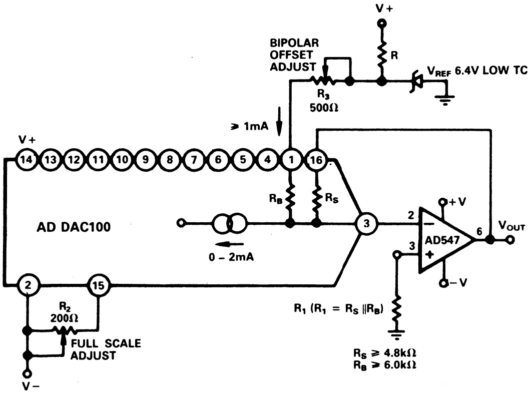


Figure 5. ±5V Bipolar Voltage Output Circuit

COMPLIANCE

Compliance voltage is the maximum voltage swing allowed on the current output node in order to maintain specified accuracy.

The AD DAC100 is designed to be operated with the output voltage near zero. Output voltage swings can affect linearity by causing improper switching of bits. Potentially damaging large voltage swings can be avoided by clamping the output within ±0.7 volts using a pair of back to back silicon diodes between the output and ground as shown in Figure 6.

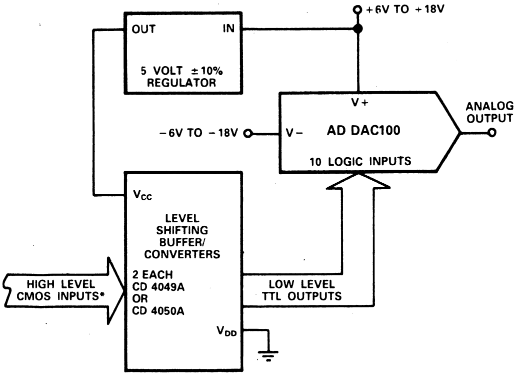
INTERFACING WITH CMOS LOGIC

CMOS inputs may be used directly as long as the logic input voltages do not exceed 6.5V or V+ (the lesser of the two). If a +6 (±5%)V input supply is used, no interfacing components are required.

For CMOS levels between 6.5V and +15V, a method of interfacing is shown in Figure 7. The high level inputs are stepped down to TTL level inputs not exceeding 5V by using CMOS Hex buffer/converters. These buffer/converters not only provide level shifting but allow input coding flexibility since they are available as inverting (CD4049A) or noninverting (CD4050A) devices. The user can then choose betwen negative true and positive true binary coding.

REDUCED RESOLUTION APPLICATIONS

For applications requiring less than 10 bits of resolution, all unused logic inputs must be tied high for proper operation (see Figure 8).



*MUST BE CURRENT LIMITED TO AVOID DAMAGING THE LEVEL SHIFTING BUFFER.

Figure 7. CMOS to AD DAC100 Interface

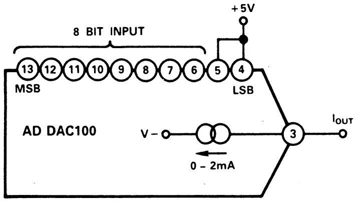


Figure 8. Reduced Resolution Application

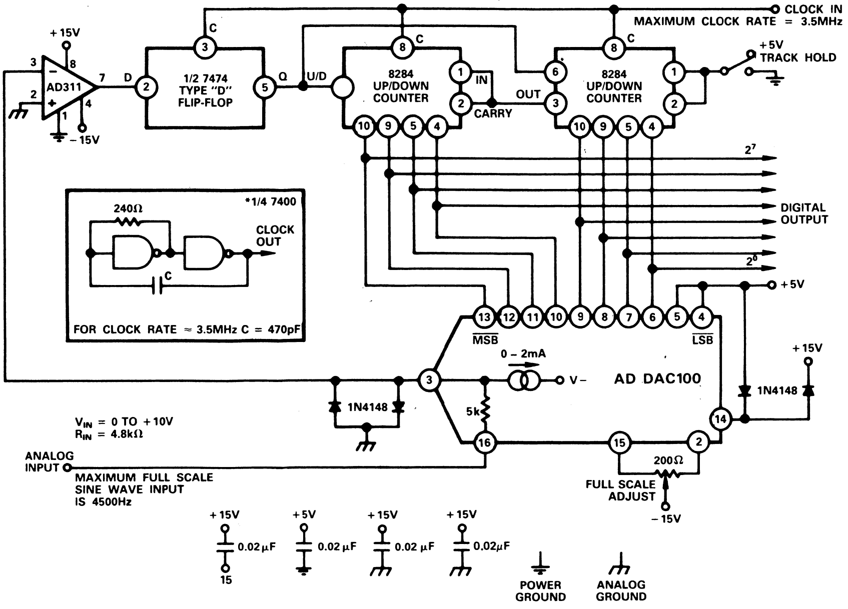


Figure 6. Tracking (Servo Type) A/D Converter

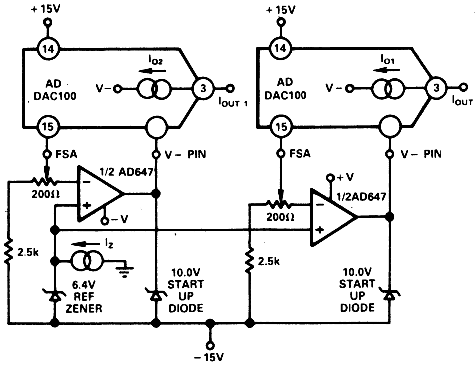


Figure 9. External Reference Connection

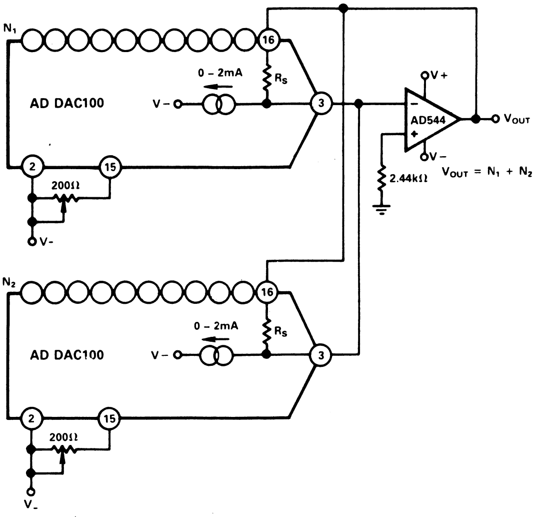


Figure 10. Analog Sum of Two Digital Numbers

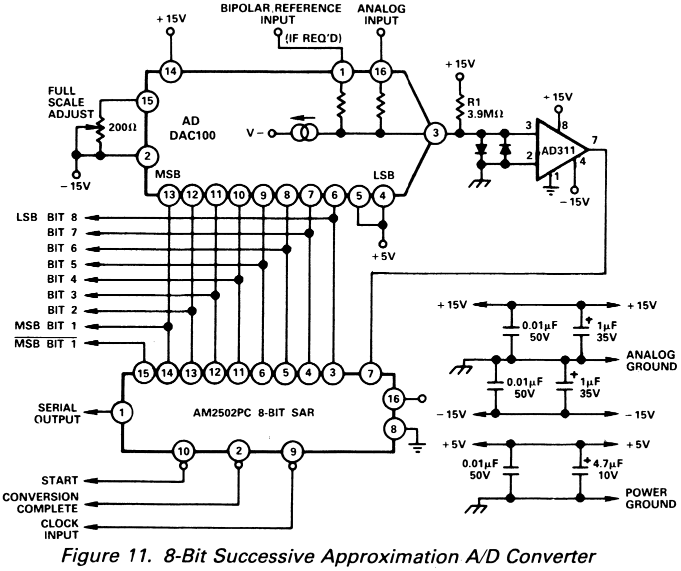


Figure 11. 8-Bit Successive Approximation A/D Converter

ANALOG DEVICES

High Resolution 16- and 18-Bit Digital to Analog Converters

DAC1136/1138

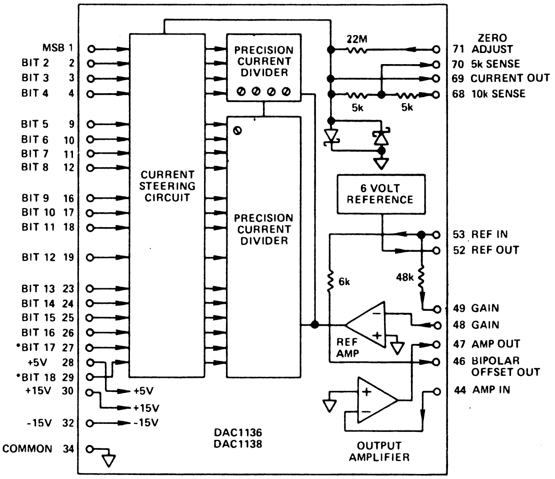
FEATURES

DAC1138
- **18-Bit Resolution and Accuracy (38μV, 1 Part in 262,144)**
- **Nonlinearity 1/2LSB max (DAC1138K)**
- **Excellent Stability**
- **Settling to 1/2LSB (0.0002%) in 10μs**
- **Hermetically-Sealed Semiconductors**

DAC1136
- **16-Bit Resolution and Accuracy (152μV, 1 Part in 65,536)**
- **Low Cost**
- **Nonlinearity 1/2LSB Max (DAC1136K, L)**
- **Settling to 1/2LSB (0.0008%) in 6μs**

DEGLITCHER IV
- **Eliminates DAC Glitches**
- **Available on DAC1136/1138 Card-Mounted Assembly**

DAC1136/38 FUNCTIONAL BLOCK DIAGRAM



*DAC1138 ONLY

GENERAL DESCRIPTION

The DAC1136/1138 are complete self-contained current or voltage output modular digital to analog converters with resolutions and accuracies of 16 and 18 bits.

The DAC1136/1138 combine precision current sources with state-of-the-art steering switches to produce a very linear output. Inputs to these converters are compatible with TTL levels. The converters have a current output of -2mA full scale. A voltage output can be obtained by connecting the internal amplifier to the current output by means of jumpers. By using additional jumpers, the user can select any one of the following output ranges: 0 to +5V, 0 to +10V, ±5V, or ±10V.

The DAC1136/1138 are available on Card-Mounted Assemblies. In this configuration, selectable options include: input codes, output amplifiers, and a high speed transient-suppressing Deglitcher Module, Deglitcher IV.

WHERE TO USE HIGH RESOLUTION DACS

The DAC1136/1138 deliver exceptional accuracy for a broad range of display, test and instrumentation applications. The DAC1136, with a resolution of 16 bits or 1 part in 65,536, and the DAC1138 with a resolution of 18 bits or 1 part in 262,144 are ideally suited for applications requiring wide dynamic range measurement and control. Applications include data acquisition systems, high resolution CRT displays, automatic semiconductor testing, photo-typesetting, frequency synthesis and nuclear reactor control.

CERTIFICATE OF CALIBRATION

Each DAC1138 has been calibrated with equipment and methods that are traceable to the National Bureau of Standards (NBS). A Certificate of Performance is sent with each unit, which includes 1000 hour stability data for the reference zener and linearity test data.

This two-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be found in Volume II, page 10-15.

SPECIFICATIONS (typical @ +25°C, rated power supplies unless otherwise noted; specifications for mounting card with amplifier/deglitcher options same as module unless otherwise noted)

	DAC1136 Module			DAC1138 Module	
	J	K	L	J	K
RESOLUTION, BITS	16			18	
ACCURACY					
Integral Nonlinearity	± 1LSB max	± 1/2LSB max	± 1/2LSB max	± 1LSB max	± 1/2LSB max
Differential Nonlinearity	± 1LSB max	± 1/2LSB max	± 1/2LSB max	± 1LSB max	± 1/2LSB max
Gain and Offset Error (Externally Adjustable)	± 1LSB			± 1LSB	
ANALOG OUTPUT					
Unipolar Mode	– 2mA to 0mA			– 2mA to 0mA	
Bipolar Mode	– 1mA to + 1mA			– 1mA to + 1mA	
Voltage Output Range (Pin Selectable)	0 to + 5V, 0 to + 10V, ± 5V, ± 10V			0 to + 5V, 0 to + 10V, ± 5V, ± 10V	
DIGITAL INPUTS	TTL/CMOS			TTL/CMOS	
INPUT CODES					
Unipolar Mode	Complementary Binary (COMP BIN)			Complementary Binary (COMP BIN)	
Bipolar Mode	Complementary Offset Binary (COMP OBIN)			Complementary Offset Binary (COMP OBIN)	
DYNAMIC CHARACTERISTICS					
Settling Time to 1/2LSB					
Current					
Full Scale Step	8μs			10μs	
LSB Step	6μs			8μs	
Voltage					
Unipolar (10V Step)	90μs			175μs	
Bipolar (20V Step)	250μs			140μs	
LSB Step	8μs			18μs	
Slew Rate	1V/μs			2V/μs	
TEMPERATURE COEFFICIENTS (ppm of FSR/°C)[1]					
Integral Nonlinearity	± 1	± 1	± 1.5 max	± 0.3	
Differential Nonlinearity	± 1	± 1	± 1.5 max	± 0.4	
Gain (Excluding V_{REF})	± 5	± 5	± 8 max	± 0.8	
Offset					
Unipolar Mode	± 0.5			± 0.5	
Bipolar Mode	± 5			± 1	
STABILITY, LONG TERM (ppm of FSR/1,000 hrs.)[2]					
Gain (Excluding V_{REF})	± 5			± 2	
Offset	± 6			± 2	
NOISE (Include V_{REF}; Double for Bipolar Mode)					
Output Current (BW = 100kHz)	0.5nA rms			0.5nA rms	
Output Voltage (BW = 0.1–10Hz)					
@ 0V (All 1's Code; "ZERO")	4μV pk-pk			4μV pk-pk	
@ 5V (MSB = 0 Code; "Half Scale")	6μV pk-pk			6μV pk-pk	
@ 10V (All 0's Code; "Full Scale")	9μV pk-pk			9μV pk-pk	
Output Voltage (BW = 100kHz)	30μV rms			30μV rms	
VOLTAGE COMPLIANCE (Amplifier Offset, E_{OS})					
Max E_{OS} Allowed for Rated Accuracy	± 2mV max			± 200μV max	
Initial E_{OS} (Factory Adj.)	± 100μV			± 100μV	
E_{OS} Drift	± 10μV/°C			± 10μV/°C	
Current Output (pin 69)					
Voltage Protection	via Internal Schottky Diodes			via Internal Schottky Diodes	
Source Resistance					
Unipolar Mode	>33kΩ			>33kΩ	
Bipolar Mode	>5kΩ			>5kΩ	
Source Capacitance	150pF			150pF	
REFERENCE VOLTAGE (V_{REF})					
Voltage ($Z_{OUT} \approx 200\Omega$)	+ 6.000V (Maximum Error, ± 0.024V)			+ 6.000V (Maximum Error, ± 0.024V)	
Noise (BW = 0.1–10Hz)	3μV pk-pk			3μV pk-pk	
Tempco	5ppm/°C			5ppm/°C	
POWER SUPPLY REQUIREMENTS[3]					
+ 5V dc, ± 5%	9mA			9mA	
± 15V dc, ± 5%	± 30mA			± 30mA	
POWER SUPPLY REJECTION (± 15V dc)					
Gain or Offset vs. FSR	80dB			80dB	
Differential Nonlinearity	± 1/4LSB per Volt ΔV_S			± 1/4LSB per Volt ΔV_S	
ENVIRONMENTAL					
Operating Temperature	0 to + 70°C			0 to + 70°C	
Storage Temperature	– 55°C to + 85°C			– 55°C to + 85°C	
Humidity	5% to 95%, Noncondensing			5% to 95%, Noncondensing	

NOTES:

[1] Temperature coefficients guaranteed maximum from 15°C to 35°C, typical from 0 to + 70°C.

[2] Recommended DNL calibration check: 6 months.

[3] Recommended Power Supply: Analog Devices Model 923.

Specifications subject to change without notice.

ANALOG DEVICES

4-20mA, 8- and 10-Bit Digital-to-Analog Converters

DAC1420, DAC1422

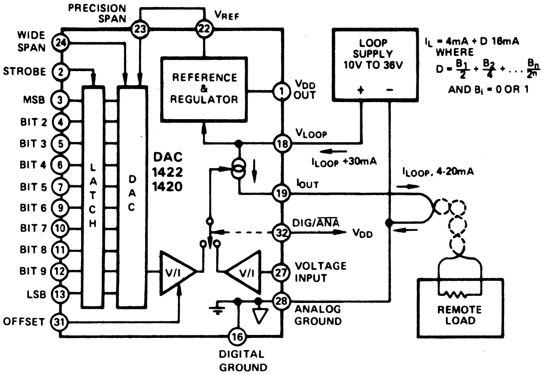
FEATURES

- ISA S50.1 Type 3 Class U Output
- Guaranteed Monotonic 0 to +70°C
- Totally Powered From Loop Supply
- Wide Supply Range +10V to +36V
- Self-Contained Data Latch
- Auxiliary Analog Input
- No Minimum Load Requirement

APPLICATIONS

- Direct Digital Controllers
- Computer Based Process Control Systems
- Digital Pressure Transducers

DAC1422 FUNCTIONAL BLOCK DIAGRAM



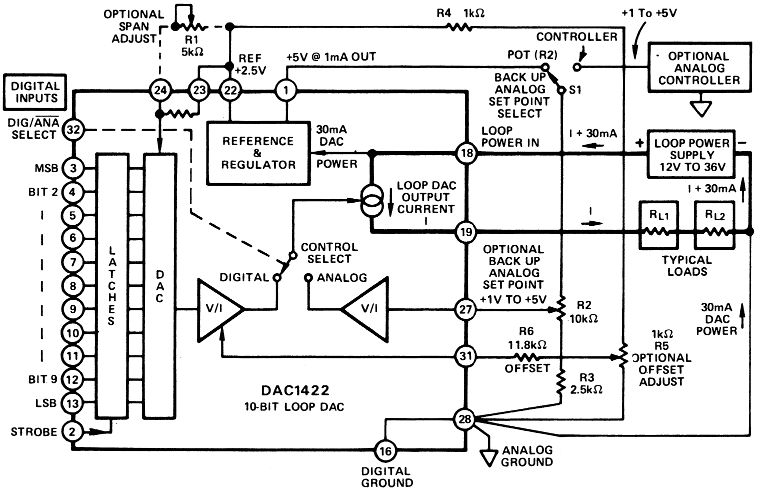
GENERAL DESCRIPTION

Models DAC1420/1422 are 8/10-bit D/A converters with analog output in the form of a 4-to-20mA current source. Specifically designed for the process-control industry, and requiring but a single +10V to +36V power supply, they meet the requirements of ISA standard S50.1 for Type 3 Class U (3-wire nonisolated) output. Included in the 2" X 2" X 0.4" module are a set of CMOS latches, an 8/10-bit CMOS DAC, two analog-to-current converters—one reflecting the translated output from the DAC, the other an auxiliary backup analog input—a current amplifier, and a regulator & reference. The

DAC1422 Block Diagram shows the basic connections and operation of the devices with an external loop supply and a remote load, R_L, supplied via a twisted pair.

HOW LOOP DACS WORK

The Loop DAC Block Diagram is a more-detalied version of the DAC1422 Block Diagram, showing some of the options available to the user in applying the DAC1420/1422. The basic digital-to-analog conversion is performed by a circuit employing an Analog Devices CMOS integrated-circuit multiplying DAC. Its output is a voltage, which is converted to a 4-to-20mA output current by a V-to-I converter circuit.



LOOP DAC FUNCTIONAL BLOCK DIAGRAM

This two-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be found in Volume II, page 10-23.

SPECIFICATIONS

(typical @ +25° C, V_{LOOP} = +24 volts unless otherwise specified)

MODEL	DAC1420	DAC1422
DIGITAL INPUTS		
Resolution	8 Bits	10 Bits
Levels		
(Except “$\overline{\text{ANA}}$/DIG”)	CMOS V_{DD} =5V	*
	“1” = >3.3V @ 1µA	*
	“0” = <1.7V @ 1µA	*
$\overline{\text{ANA}}$/DIG Input		
Impedance	12kΩ	*
“1”	“1” = >2.4V @ 140µA	*
“0”	“0” = <0.7V @ 0µA	*
Latch Strobe	Rising Edge Sensitive	*
T_{DH} (Data Hold)	0ns (min)	*
T_{DS} (Data Set-Up)	50ns (min)	*
ANALOG OUTPUT		
Type	ISA S50.1 Type 3 Meets and Exceeds Class U	*
Nominal Range	4-20mA	*
Compliance	V_{LOOP} -6V	*
Output Impedance	>4MΩ @ dc	*
Minimum Load	0Ω	*
STABILITY AND ACCURACY		
Monotonicity	Guaranteed, 0 to +70°C	*
Integral Nonlinearity	±1/2LSB	*
Differential Nonlinearity	±1/2LSB	*
Temperature Stability		
Offset	25ppm FSR/°C	*
Span	50ppm FSR/°C	*
Adjustability	±10% each, Offset and Span	*
Initial Error, Untrimmed[1]	±2LSB's each, Offset and Span	*
Power Supply Rejection	20ppm FSR/V	*
Noise, 10Hz to 100Hz[2]	4mV p-p	*
ANALOG BACKUP INPUT		
Range[3]	1 - 5V	*
Gain	4mA/Volt (1-5V produces 4-20mA)	*
Accuracy	±3%	*
Stability	±100ppm FSR/°C	*
Input Impedance	10^8 Ω	*
POWER		
Loop Supply, minimum	+10V	*
maximum	+36V	*
Supply Current	I_{OUT} +30mA	*
ENVIRONMENTAL		
Operating Temperature	0 to +70°C	*
Storage Temperature	-25°C to +85°C	*
SIZE	2" X 2" X 0.4"	*

NOTES

[1] Both offset and span error are adjustable to zero.

[2] Load = 750Ω ‖ 1,000pF.

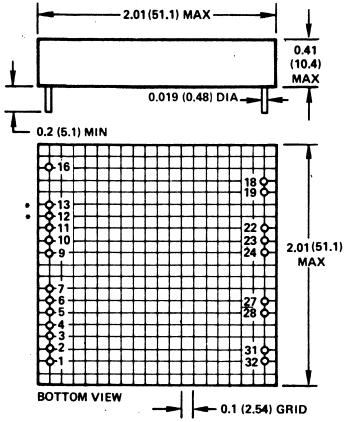
[3] This input should not exceed +5.5V and should be grounded if not used.

*Specifications same as DAC1420.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



NOTE:
Module Weight: 1.6 ounces
(45 G)

*Pins 12 & 13 appear on DAC1422 only.

DIGITAL INPUT	NOMINAL CURRENT OUTPUT
Binary Code	
1 1 1 1 1 1 1 1 1 1	+19.984mA
0 0 0 0 0 0 0 0 0 1	+ 4.016mA
0 0 0 0 0 0 0 0 0 0	+ 4.000mA

Table 1. Nominal Input-Output Relationships

DAC1423: ISO-DAC™

For applications in hostile environments, where ground loop elimination is required, consider Analog Devices model DAC1423. This isolated 10-bit 4-20mA DAC offers the following:

- High Voltage Protection (1500V dc)
- 8- and 10-bit Bus Compatibility
- Fail Safe Design
- Increment/Decrement Back-Up
- Bumpless Transfer

ANALOG DEVICES

4-20mA, 10-Bit, Isolated Digital-to-Analog Converter

DAC1423

FEATURES

- 3-Port Galvanic Isolation
- Guaranteed Monotonic 0 to +70°C
- Microprocessor Compatible Interface
- Increment/Decrement Backup Control
- May be Powered from Loop Supply
- Low Power: 450mW typ
- Output Will Drive 0Ω Loads
- Bumpless Transfer, Auto to Manual

APPLICATIONS

- Direct Digital Controllers
- Ground Loop Elimination in Industrial and Process Control
- High Voltage Protected Data Acquisition Systems
- Digital Pressure Transducers
- Driving Analog Recorders

GENERAL DESCRIPTION

Analog Devices' ISO-DAC™ (ISOlated Digital-to-Analog Converter) model DAC1423 is a low power 10-bit DAC with 4-20mA current output, designed specifically for the process and industrial control industry. Its advanced features and excellent performance make for easy application within new and existing control systems. The DAC1423 contains a CMOS holding register, allowing direct interface with microprocessors, CMOS digital-to-analog converter, voltage-to-voltage isolator and a voltage-to-loop current converter. The small size and low profile (2" X 4" X 0.4") allows much greater functional density than previously available solutions.

DESIGN FEATURES AND USER BENEFITS

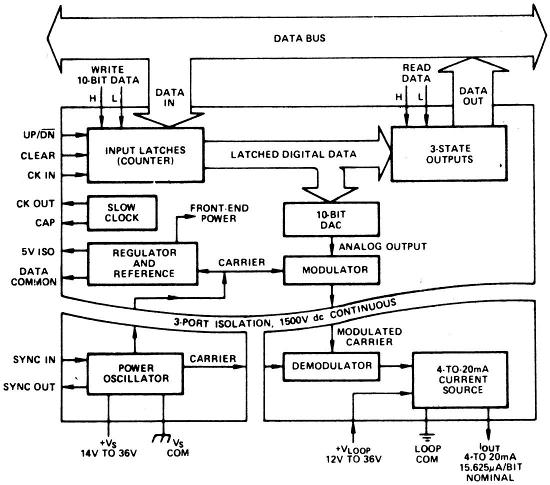
Microcomputer Interface: The parallel digital interface is a 5V CMOS design with independently controllable input latches and Tri-State* buffers, split into upper and lower sections (an 8-bit and a 2-bit byte) so that 8- or 16-bit bus compatibility may be achieved.

True 3-Port Isolation: The output connections and power connections are galvanically isolated, both from each other and from the digital section. Each will accommodate a wide range of power supply voltages and may be operated from the same supply, if desired.

Increment/Decrement: Increment/decrement control is achieved via the input latch/counter. An internal slow speed clock is supplied for this operation. Overflow/underflow lockout circuitry is used to prevent full scale "bumps" from occurring.

This two-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be found in Volume II, page 10-27.

DAC1423 FUNCTIONAL BLOCK DIAGRAM



Adjustable Offset and Span: The ISO-DAC has offset and span accuracies of ±2LSB's (±0.2% FSR) each. However, if the user desires adjustable offset and span, there are provisions for ±10% adjustment range for each.

High CMV Isolation: The isolation barriers will withstand 1.5kV dc continuously, or 1kV rms @ 60Hz for 60 seconds. The ISO-DAC is designed to meet the IEEE Standard for Transient Voltage Protection (472-1974: Surge Withstand Capability). Common Mode Rejection is excellent; typically, 103dB @ 60Hz for a 250Ω load.

Synchronized: The ISO-DAC may be synchronized to an external system clock, multiple DAC1423's may be on synchronized to one another. In the event of loss of external sync, the DAC1423 will "free run" on its own oscillator.

Isolated Power Out: An internally derived +5V supply is brought out so that the user may power a small amount of application circuitry from the DAC1423's power supply.

ISA-S50.1: The three terminal output structure conforms to the Instrument Society of America Standard ISA-S50.1, "Compatibility of Analog Signals for Electronic Industrial Process Instruments."

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*Tri-State is a trademark of National Semiconductor Corporation.

SPECIFICATIONS (typical @ +25°C, V_{LOOP} = +24 volts unless otherwise specified)

MODEL	DAC1423
DIGITAL INPUTS	
Resolution	10 Bits
Levels, CMOS V_{DD} = 5V	"1" = >3.3V @ 1μA "0" = <1.7V @ 1μA
Strobe	Level Sensitive
ANALOG OUTPUTS	
Type	ISA S50.1 Type 3 Meets or Exceeds Class U
Nominal Range	4-20mA
Compliance	V_{LOOP} -6V
Output Impedance	>4MΩ @ dc
Minimum Load	0Ω
Maximum Load	(V_{LOOP} -6V/I_{OUT})
Maximum Capacitive Load	Unlimited
STABILITY AND ACCURACY	
Monotonicity	Guaranteed, 0 to +70°C
Integral Nonlinearity	±1/2LSB
Differential Nonlinearity	±1/2LSB
Temperature Stability	
Offset	50ppm FSR/°C
Span	50ppm FSR/°C
Adjustability	±10% each, Offset and Span
Initial Error, Untrimmed[1]	±2LSB's each, Offset and Span
Power Supply Rejection	20ppm FSR/V
Noise, 10Hz to 100Hz[2]	0.1LSB
Warm Up Time to Rated Accuracy	5 minutes
Warm Up Drift	0.5LSB
ISOLATION	
Max CMV, Inputs to Outputs	
ac, 60Hz, 1 minute	1000V rms
dc, Continuous	1500V dc
CMR, Inputs to Outputs, 60Hz, R_L = 250Ω	103dB
POWER	
Loop Supply Range	12–36V dc
Loop Supply Current	I_{OUT} + 5mA
Power Supply Range[3]	14–36V dc
Power Supply Current[3]	20mA
ENVIRONMENTAL	
Operating Temperature	0 to +70°C
Storage Temperature	-25°C to +85°C

NOTES:

[1] Both offset and span error are adjustable to zero.

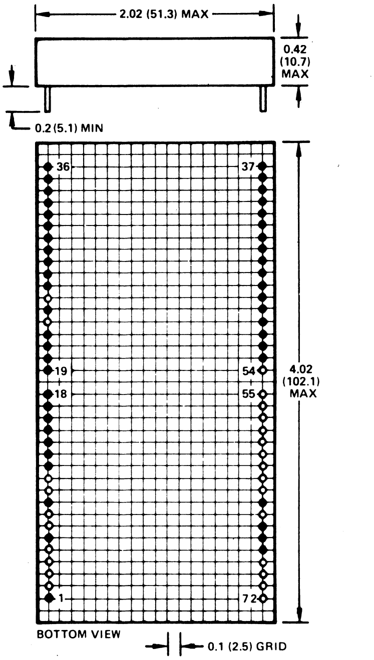
[2] Load = 750Ω‖1,000pF and slow clock disabled.

[3] The DAC1423 can be entirely powered from the loop supply.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



NOTE:
TERMINAL PINS INSTALLED ONLY IN SHADED HOLE LOCATIONS.
MODULE WEIGHT: 60.8G

PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	I_{OUT}	72	NC
2	NC	71	NC
3	NC	70	NC
4	NC	69	NC
5	NC	68	SYNC IN
6	$+V_{LOOP}$	67	+V POWER
7	NC	66	SYNC OUT
8	NC	65	NC
9	COMMON	64	PWR COMMON
10	NC	63	NC
11	NC	62	NC
12	NC	61	NC
13	WIDE SPAN	60	NC
14	PRECISION SPAN	59	NC
15	$+V_{REF}$	58	NC
16	WIDE OFFSET	57	NC
17	PRECISION OFFSET	56	NC
18	SPAN COMMON	55	NC
19	DIGITAL COMMON[1]	54	NC
20	$+5V_{OUT}$	53	DIGITAL COMMON[1]
21	LOAD HIGH	52	CLOCK IN
22	LOAD LOW	51	LSB OUT
23	NC	50	BIT 9 OUT
24	LSB IN	49	BIT 8 OUT
25	NC	48	BIT 7 OUT
26	BIT 9 IN	47	BIT 6 OUT
27	BIT 8 IN	46	BIT 5 OUT
28	UP/$\overline{DN}$	45	READ HIGH
29	BIT 7 IN	44	READ LOW
30	BIT 6 IN	43	BIT 4 OUT
31	BIT 5 IN	42	BIT 3 OUT
32	BIT 4 IN	41	BIT 2 OUT
33	BIT 3 IN	40	MSB OUT
34	BIT 2 IN	39	CLOCK OUT
35	MSB IN	38	C_T
36	CLEAR	37	DIGITAL COMMON[1]

[1] PINS 19, 37 and 53 ARE INTERNALLY CONNECTED.

ANALOG DEVICES

Hybrid Video Low Glitch D/A Converter

HDD Series

FEATURES

- Ultra Fast 10ns Settling Time to 0.2% (HDD-0810)
  15ns Settling Time to 0.1% (HDD-1015)
- Internal Monolithic Reference
- Low 200pV-sec Glitch Energy
- Single -5.2V Power Supply
- Available Screened to MIL-STD-883
- Designed for General Output Compatibility with EIA Standards RS-170 and RS-343, including 10% Brightness
- Complete Composite Inputs (HDD-0810C, HDD-1015C)

APPLICATIONS

- Raster Scan and Vector Graphic Displays
- TV Video Reconstruction
- Ultra Fast Current or Voltage Output DAC for Use in Analytical Instrumentation
- Digital VCOs

GENERAL DESCRIPTION

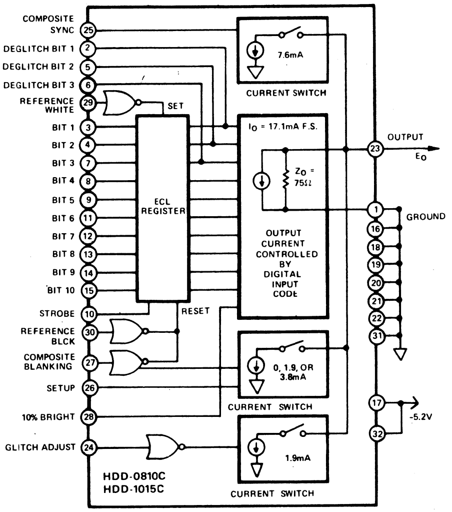
The HDD-0810 and HDD-1015 combine state-of-the-art technology with the latest active laser trimming techniques to achieve the world's fastest 8- and 10-bit voltage output digital-to-analog converters of their type.

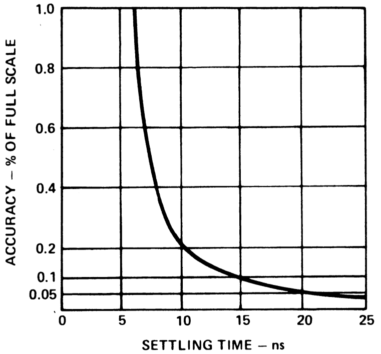
Containing input registers and an ultra stable monolithic internal reference, the HDD-0810 8-bit D/A converter settles to within 0.2% in 10ns, while the 10-bit version HDD-1015 settles to within 0.1% in only 15ns. They are compatible with standard ECL logic levels. The 75Ω output impedance allows them to drive 75Ω cables or filters directly, without costly external output drivers. This feature assures that a full one volt is available at the load, since the D/A output is a minimum of 27mA (HDD-1015). Additionally, these D/As are monotonic over the full operating temperature range of -25°C to +85°C (metal case versions), or 0 to +70°C for the commercial style glass-ceramic package, and require only a single -5.2V supply for operation.

The HDD-0810C and HDD-1015C combine all of the above features with full composite input capability, which allows operation directly with raster scan/output video display systems. These controls include Composite Sync, Blanking, Setup and a 10% Brightness input which gives the user digital control of the picture's intensity. Further, the HDD Series D/A converters contain provisions for external adjustments to optimize differential phase and gain, critical considerations in composite color video applications.

The industry standard 32-pin dual in-line packages are available in either ceramic/glass cases for commercial applications or hermetically sealed metal cases for military type applications. They are available screened to MIL-STD-883.

HDD-0810C, HDD-1015C FUNCTIONAL BLOCK DIAGRAM





TIME IS MEASURED FROM 50% TRANSITION POINT OF THE STROBE WITH INPUT DATA LINES DESKEWED AND 75Ω LOAD. VOLTAGE OUTPUT. INHERENT DELAY OF INTERNAL REGISTER (3ns) HAS BEEN DISREGARDED.

HDD Series D/A Converters Accuracy vs. Settling Time

SPECIFICATIONS (typical @ +25°C with nominal power supplies and 75Ω output load unless otherwise noted)

MODEL	UNITS	HDD-0810	HDD-0810C	HDD-1015	HDD-1015C
RESOLUTION FS = FULL SCALE	Bits	8	8	10	10
LSB WEIGHT (Current)	μA	106	67	27	17
LSB WEIGHT (Voltage)	mV	4	2.5	1	0.625
ACCURACY[1]	±% of FS	0.1		0.05	
	±% of GS		0.1		0.05
Linearity	±μA	26.5	17	13	8.5
Monotonicity		Guaranteed	*	*	*
Zero Offset (Initial)	mV	-1.4	*	*	*
TEMPERATURE COEFFICIENTS					
Linearity	ppm/°C	5	*	*	*
Zero Offset	ppm/°C	1	*	*	*
Gain	ppm/°C	80	*	*	*
STROBE INPUT					
Logic Compatibility		ECL	*	*	*
Logic Voltage Levels "1" =	V	-0.9	*	*	*
(Positive Logic) "0" =	V	-1.7	*	*	*
Logic Loading		50pF and 5kΩ to -5.2V	*	*	*
Set-Up Time (Data)	ns	2.5 min	*	*	*
Hold Time (Data)	ns	1.5 min	*	*	*
Propagation Delay	ns	3	*	*	*
REFERENCE BLACK AND REFERENCE WHITE INPUTS[2]		See Note 2	*	*	*
Logic Compatibility		ECL	*	*	*
Logic Voltage Levels "1" =	V	-0.9	*	*	*
"0" =	V	-1.7	*	*	*
Logic Loading		50pF and 5kΩ to -5.2V	5pF and 50kΩ *	50pF and 5kΩ *	5pF and 50kΩ *
DATA INPUTS					
Logic Compatibility		ECL	*	*	*
Logic Voltage Levels "1" =	V	-0.9	*	*	*
(Positive Logic) "0" =	V	-1.7	*	*	*
Logic Loading (Each Bit)		5pF and 50kΩ to -5.2V	*	*	*
Coding (See Table)		Complementary Binary (CBN)	*	*	*
COMPOSITE SYNC INPUT					
Logic Compatibility		N/A	ECL	N/A	ECL
Logic Voltage Levels "1" =	V	N/A	-0.9	N/A	-0.9
"0" =	V	N/A	-1.7	N/A	-1.7
Logic Loading for Logic "1"		N/A	5pF, +7.6mA	N/A	5pF, +7.6mA
Logic "0"		N/A	5pF, -50μA	N/A	5pF, -50μA
COMPOSITE BLANKING AND 10% BRIGHT INPUTS					
Logic Compatibility		N/A	ECL	N/A	ECL
Logic Voltage Levels "1"	V	N/A	-0.9	N/A	-0.9
"0"	V	N/A	-1.7	N/A	-1.7
Logic Loading		N/A	5pF and 50kΩ to -5.2V	N/A	5pF and 50kΩ to -5.2V
SETUP CONTROL					
Ground	mV	0 (0 IRE Units)	*	*	*
Open	mV	71 (10 IRE Units)	*	*	*
-5.2V	mV	142 (20 IRE Units)	*	*	*
OUTPUT[3]					
Current	mA	0 to -27.2	0 to -17	0 to -27.3	0 to -17.05
Voltage[4]	V (±1%)	0 to -1.020	0 to -0.6375	0 to -1.023	0 to -0.639375
Compliance	V	+1.1 to -1.1	*	*	*
Internal Impedance	Ω (±5%)	75	*	*	*
OUTPUT – COMPOSITE SYNC					
Current	mA (±5%)	N/A	0 or -7.6	N/A	0 or -7.6
Voltage	mV (±5%)	N/A	0 or -286	N/A	0 or -286
OUTPUT – 10% BRIGHT					
Current	mA (±5%)	N/A	0 or -1.9	N/A	0 or -1.9
Voltage	mV (±5%)	N/A	0 or -71	N/A	0 or -7.1
OUTPUT – COMPOSITE BLANKING[5]					
Current	mA (±1%)	N/A	0, -17.0, -18.9, or -20.8	N/A	0, -17.05, -18.95, or -20.85
Voltage	mV (±1%)	N/A	0, -637.5, -708.75 or -780	N/A	0, -639.4, -710.6, or -781.9

MODEL	UNITS	HDD-0810	HDD-0810C	HDD-1015	HDD-1015C
SPEED PERFORMANCE – FULL SCALE OR GRAY SCALE OUTPUT					
Settling Time (Voltage)[6]	ns (to % FS)	10 (0.2)		15 (0.1)	
	or (to % GS)		10 (0.2)		15 (0.1)
Slew Rate	V/μs	200	*	*	*
Update Rate[7]	MHz	100	100	67	67
Rise Time	ns	4	*	*	*
Glitch Energy[8]	pV-s	200	*	*	*
SPEED PERFORMANCE – CONTROL INPUTS					
Settling Time to 10% of Final Value for:					
Composite Sync	ns	N/A	10	N/A	10
Composite Blanking	ns	N/A	10	N/A	10
Reference White	ns	N/A	10	N/A	10
Reference Black	ns	N/A	10	N/A	10
10% Bright	ns	N/A	10	N/A	10
POWER REQUIREMENTS					
-5.2V ±0.25V	mA	380	390	450	450
Power Supply Rejection Ratio	%/%	0.04	*	*	*
Reference		Monolithic, Internal	*	*	*
TEMPERATURE RANGE					
Operating, Glass Case	°C Case	0 to +70	*	*	*
Operating, Metal Case ("M")	°C Case	-25 to +85	*	*	*
Storage	°C	-55 to +125	*	*	*
MTBF[9]					
Mean Time Between Failure	hours	>300,000			
PACKAGE OPTIONS[10]	HY32A (glass package)		HY32C (metal package)		

NOTES:

[1] Accuracy is relative to full scale (FS) for binary versions. or relative to gray scale (GS) for Composite ("C") versions, and includes linearity.

[2] Reference White on models HDD-0810, -1015 a logic "1" on Pin 30 Reference Black will produce all "0" code 0 volts output; a logic "1" on Pin 29 Reference White will produce all "1" code -1 volt output.
On models HDD-0810C, 1015C a logic "0" on Pin 30 Reference Black will drive the output to reference black level of -643mV; a logic "0" on Pin 29 Reference White will drive the output to reference white level of 0 volts absolute.

[3] The output is shown for full scale (FS) for binary versions, and for full gray scale (GS) for Composite ("C") versions.

[4] The difference between the full-scale output of 637.5mV and 643mV shown elsewhere herein is due to the fact that we selected an LSB value of 2.5mV for ease of calibration. These differences are well within the output and EIA standard RS-170 tolerances.

[5] The three currents and voltages correspond to the three set-up levels of 0, 10, and 20 IRE units as externally selected.

[6] Worst case settling time includes FS and most significant bit (MSB) transitions. The inherent 3ns proposition delay through the input registers (50% point of Strobe to 50% point of register output) has been disregarded. Settling time to a percentage of FS is given for straight versions, and settling time to a percentage of maximum gray scale (GS) is given for composite video output ("C") versions.

[7] The update rates shown are limited by a full scale settling time that is useable for the number of bits of resolution. Both DACs may be operated up to 125MHz with settling time degradation. This is the limit of the logic switching speed.

[8] Reducible to less than 100pV-s with appropriate deskewing of digital inputs. See Applications Section.

[9] Calculated for HDD-1015CMB using MIL Handbook 217. Ground: Fixed Temperature Case = 60°C.

[10] See Section 20 for package outline information.

*Specifications same as for HDD-0810.

Specifications subject to change without notice.

ORDERING NOTES

1. To order devices with hermetically sealed metal cases, add "M" suffix to part number.
2. To order devices screened to MIL-883B requirements, add "MB" suffix to part number.

   Example: HDD-0810CMB

PIN DESIGNATIONS

PIN	FUNCTION
1	GROUND
2	DEGLITCH BIT 1
3	BIT 1 (MSB)
4	BIT 2
5	DEGLITCH BIT 2
6	DEGLITCH BIT 3
7	BIT 3
8	BIT 4
9	BIT 5
10	STROBE
11	BIT 6
12	BIT 7
13	BIT 8
14	BIT 9
15	BIT 10 (LSB)
16	GROUND
17	-5.2V
18	GROUND
19	GROUND
20	GROUND
21	GROUND
22	GROUND
23	OUTPUT
24	GLITCH ADJUST
25	COMPOSITE SYNC
26	SETUP
27	COMPOSITE BLANKING
28	10% BRIGHT
29	REFERENCE WHITE
30	REFERENCE BLACK
31	GROUND
32	-5.2V

ON THE HDD-0810 AND HDD-0810C, PINS 14 AND 15 ARE NOT USED, AND PIN 13 IS THE LSB. ON THE HDD-0810 AND HDD-1015, PINS 25, 27, AND 28 ARE NOT USED. ALL GROUND PINS (1, 16, 18-22, 31) ARE CONNECTED INTERNALLY.

APPLICATIONS INFORMATION

HIGH-SPEED LOW-GLITCH OPERATION SUGGESTIONS

The HDD Series D/As offer the highest available speed. However, with this speed performance, certain precautions and operation conditions should be considered.

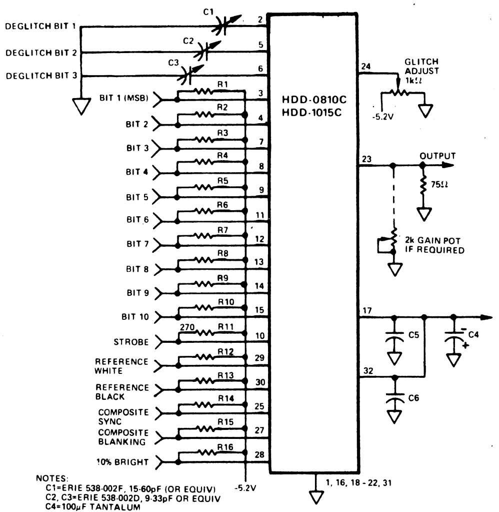
1. The D/A converter should be provided with a very low impedance grounding system to very high frequencies. A large ground plane is a must.
2. Low frequency bypassing should be provided with a 1μF (or larger) tantalum capacitor mounted between the -5.2V supply line and ground near the D/A.
3. High frequency bypassing should be provided by ceramic capacitors of 0.1μF or larger mounted within 0.25 inches of Pins 17 and 32 to ground (see Figure 1).
4. The threshold of the internal current switches can be optimized for low glitch energy by the addition of an external potentiometer connected to Pin 24 of the D/A (see Figure 1). This potentiometer is adjusted for minimum glitch energy as shown in Photo 2.

   If required, variable capacitors can be added to "deskew" the most significant bits for lowest glitch—although this is not usually required in many applications. These capacitors are added as shown in Figure 1 (C1-3). They are adjusted in conjunction with the glitch adjust pot for minimum glitch energy as shown in Photo 2.

   In composite television applications, C1-3 are adjusted for best differential phase performance, and the glitch adjust is adjusted for best differential gain performance. These may tend to interact, so going back and forth between adjustments may be required.
5. Standard 32-pin sockets should be avoided. Individual "pin sockets" are most suited for evaluating devices, as lead inductance is reduced. In final designs, the D/As should be soldered directly into the printed circuit board without sockets.

GAIN ADJUSTMENT

The HDD Series D/As are actively laser-trimmed to provide a voltage into exactly 75Ω which is an even binary multiple; i.e., the HDD-0810 has an LSB of 4mV and the HDD-1015 has an LSB of 1mV. This makes the full-scale output slightly greater than one volt. If an output of exactly one volt is required—such as for TV reconstruction—a 2k potentiometer may be placed across the output of the D/A for gain adjustment. For a one volt output, the adjusted value of this pot will be about 1500Ω (see Figures 1 and 5).



NOTES:
C1=ERIE 538-002F, 15-60pF (OR EQUIV)
C2, C3=ERIE 538-002D, 9-33pF OR EQUIV
C4=100μF TANTALUM
C5, C6=0.1μF CERAMIC
R1-R10, R12-R16=2K 1/4W, 5%

Figure 1. HDD-0810, HDD-1015C Typical Hook-Up Circuit

ULTRA-LOW GLITCH OPERATION

For extremely low glitch requirements (<50 - 100pV-s), an HTS-0025 Track-and-Hold is recommended as a deglitcher (see Figure 2). The duration of the HDD Series D/A glitch is approximately 10ns. The hold time of the HTS-0025 should be at least 15ns to "mask out" the glitch. The minimum acquisition time of the HTS-0025 for 0.1% accuracy is 30ns. This implies that the circuit of Figure 2 can be operated up to 22MHz and still maintain 10-bit accuracy. For 0.2% accuracy, the acquisition time for the T&H can be reduced to 25ns, allowing the circuit to operate to 25MHz. This discussion assumes that the D/A will be required to slew full scale (one volt) between adjacent samples. In practice, the sample-to-sample variation is less than full scale depending on the amount of oversampling. In a practical situation, therefore, 10-bit accuracy should be achievable at 25MHz update rates.

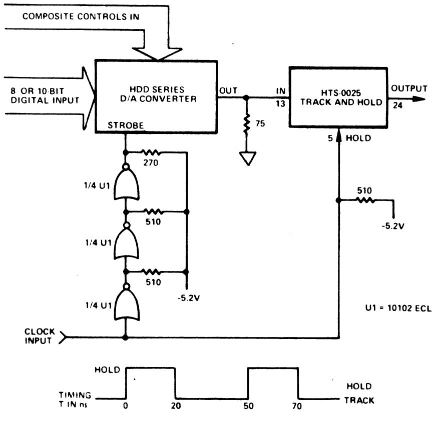


Figure 2. HTS-0025 Track and Hold Used as a Deglitcher (Update ≈ 20MHz)

CHARACTERISTICS OF HDD-1015C [0810C] VIDEO DACS

COMPOSITE VIDEO SIGNAL
1024 [256] gray levels plus blanking and sync levels

STEP SIZE
0.625mV [2.5mV]

GRAY SCALE RANGE
0.643V Peak to Peak

SETUP CONTROL
User programmable in three levels

	mV	IRE Units
1. Input Grounded	0	0
2. Input Open	71	10
3. Input @ -5.2V	142	20

REFERENCE WHITE LEVEL
0V Absolute
100 IRE Units (+0.714V relative to blanking level with standard setup; +0.643V relative to Reference Black)

DIGITAL INPUT FOR WHITE LEVEL
All ones (1111111111)

REFERENCE WHITE/BLACK CONTROLS[1]
Overrides Video Input Word
A logic 0 on Pin 30 (reference Black) will drive the output to reference black level of –643mV.
A logic 0 on Pin 29 (Reference White) will drive the output to reference white level of 0 volts absolute.

REFERENCE BLACK LEVEL
-0.643V Absolute; +71mV (10 IRE Units)
Relative to blanking level with standard setup.

DIGITAL INPUT FOR REFERENCE BLACK
All zeroes (0000000000)

COMPOSITE BLANKING LEVEL
-0.714V Absolute, (0 IRE Units) with standard setup.

COMPOSITE BLANKING INPUT - PIN 27[1]
Logic 0 on Pin 27 resets input register to 0000000000, and causes output voltage to go negative by the amount of setup voltage with respect to the all "0" output voltage.

COMPOSITE SYNC LEVEL
-1.0V Absolute with standard setup.
-0.286V (-40 IRE Units) relative to blanking level (Back Porch).

COMPOSITE SYNC INPUT - PIN 25
Logic 0 resets input register to 0000000000, and the output voltage goes negative by 0.286V.

10% BRIGHT - PIN 28
Logic "0" causes output voltage to go positive by 71mV.

STROBE - PIN 10
Logic "0" to Logic "1" transition clocks input register.

DEFINITION OF VIDEO TERMS

BLANKING LEVEL
The level separating the SYNC portion from the Video portion of the waveform. Usually referred to as the Front Porch of Back Porch. At 0 IRE Units, it is the level which will shut off the picture tube, resulting in the blackest possible picture.

COLOR VIDEO (RGB)
This usually refers to the technique of combining the three primary colors of Red, Green, and Blue to produce color pictures within the usual spectrum. In RGB monitors, three HDD "C" Series DACs would be required, one for each color.

COMPOSITE SYNC SIGNAL (SYNC)
The position of the composite video signal which synchronizes the scanning process.

COMPOSITE VIDEO SIGNAL
The video signal with or without setup, plus the composite SYNC signal.

GRAY SCALE
The discrete levels of video signal between Reference Black and Reference White levels. A 10-bit DAC contains 1,024 different levels, while an 8-bit DAC contains 256.

RASTER SCAN
The most basic method of sweeping a CRT one line at a time to generate and display images. This method is used in commercial television in the USA.

REFERENCE BLACK LEVEL
The maximum negative polarity amplitude of the video signal.

REFERENCE WHITE LEVEL
The maximum positive polarity amplitude of the video signal.

SETUP
The difference between the Reference Black level and the blanking level. This should not be confused with setup as used with digital logic.

SYNC LEVEL
The peak level of the composite SYNC signal.

VIDEO SIGNAL
That portion of the composite video signal which varies in gray scale levels between Reference White and Reference Black. Also referred to as the picture signal, this is the portion which may be visually observed.

NOTES:

[1] Reference White (Pin 29) should not be activated at the same time as composite blanking (Pin 27) or Reference Black (Pin 30).

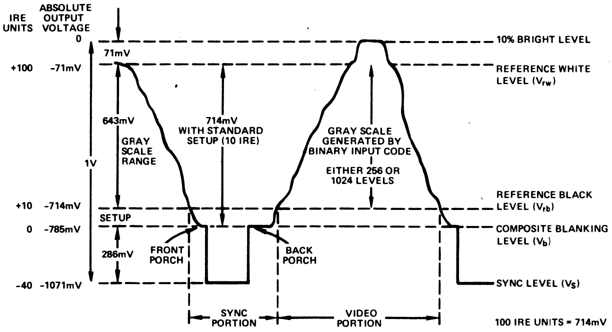


Figure 3. HDD-0810C, HDD-1015C Output Waveforms

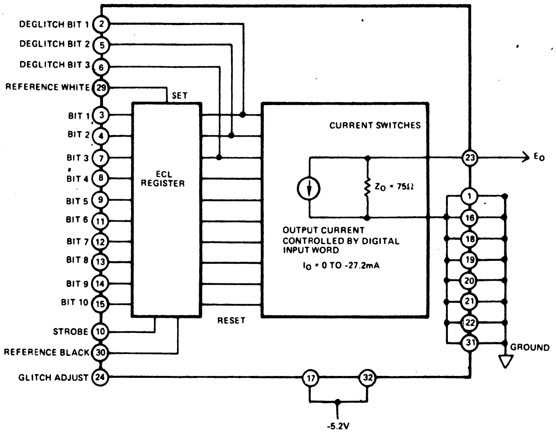


Figure 4. HDD-0810; HDD-1015 Block Diagram

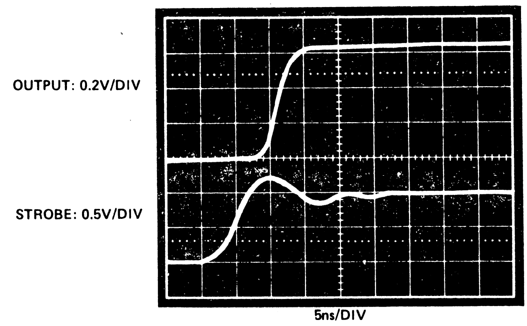
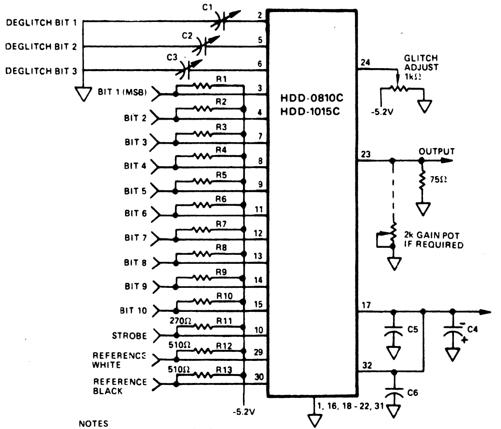


Photo 1. Full Scale Rise Time vs. Strobe



NOTES
C1 = ERIE 538-002F, 15-60pF
C2, C3 = ERIE 538-002D, 9-35pF
C4 = 100μF TANTALUM
C5, C6 = 0.1μF CERAMIC
R1-R10 = 2k
OMIT R12 & R13 IF REFERENCE WHITE AND REFERENCE BLACK ARE NOT USED

Figure 5. HDD-0810, HDD-1015 Typical Hook-Up Circuit

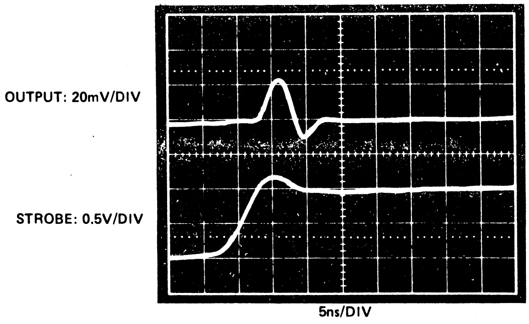


Photo 2. Midscale Glitch

HDD-0810C, HDD-1015C Output Waveform

ANALOG OUTPUT WITH 75Ω LOAD

Digital Input	HDD-0810	HDD-0810C	HDD-1015	HDD-1015C
111 . . . 111	0	0	0	0
111 . . . 110	-4mV	-2.5mV	-1mV	-0.625mV
110 . . . 000	-252mV	-157.5mV	-255mV	-159.375mV
101 . . . 111	-256mV	-160mV	-256mV	-160mV
100 . . . 111	-508mV	-317.5mV	-511mV	-319.375mV
011 . . . 111	-512mV	-320mV	-512mV	-320mV
010 . . . 000	-764mV	-477.5mV	-767mV	-479.375mV
001 . . . 111	-768mV	-480mV	-768mV	-480mV
000 . . . 001	-1016mV	-635mV	-1022mV	-638.75mV
000 . . . 000	-1020mV	-637.5mV	-1023mV	-639.375mV

Coding Table

ANALOG DEVICES

12-Bit Deglitched Voltage Out D/A Converter

HDD-1206

FEATURES
- Registers, D/A, Amplifier in Single Hybrid
- Deglitched Voltage Output
- 6MHz Update Rate
- Available with 883 Screening

APPLICATIONS
- Vector Scan Displays
- Analytical Instrumentation
- Digital VCOs
- Military Systems

GENERAL DESCRIPTION
The Analog Devices HDD-1206 D/A converter combines innovative design techniques with remarkable hybrid construction to achieve deglitched voltage outputs at digital update rates as high as 6MHz.

Despite its small size and low power, the HDD-1206 provides the user with a complete solution to demanding applications which require the conversion of high-speed digital inputs into deglitched analog output voltages.

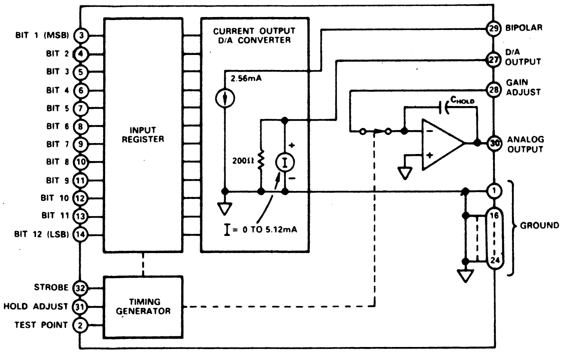
The unit is housed in an industry standard 32-pin hybrid and contains all the necessary circuit components to provide analog outputs at high update rates without the need for designing external circuits. Input registers, current-output D/A, deglitching circuits, and an output amplifier are all included inside the HDD-1206.

With the deglitching problem solved in a single package, the user of the HDD-1206 is able to incorporate the solution into his system with a minimum of design effort. User involvement is limited to the simple task of establishing the "hold" time for an optimum value by selecting the correct resistor value.

After that step is accomplished, the addition of a low-pass filter at the output of the D/A assures a "clean" voltage representation of the 12 bits of digital information applied to the inputs at video update rates.

The HDD–1206 is available in 32-pin dual in-line packages in either glass or metal. For applications which require military processing of hybrids, the HDD-1206 D/A converter can be specified with processing per MIL-STD-883, Method 5008.

HDD-1206 FUNCTIONAL BLOCK DIAGRAM



PIN DESIGNATIONS HDD-1206

PIN	FUNCTION	PIN	FUNCTION
1	GROUND	17	GROUND
2	TEST POINT	18	GROUND
3	BIT 1 (MSB)	19	GROUND
4	BIT 2	20	GROUND
5	BIT 3	21	GROUND
6	BIT 4	22	GROUND
7	BIT 5	23	GROUND
8	BIT 6	24	GROUND
9	BIT 7	25	+15V
10	BIT 8	26	−15V
11	BIT 9	27	D/A OUTPUT
12	BIT 10	28	GAIN ADJUST
13	BIT 11	29	BIPOLAR
14	BIT 12 (LSB)	30	OUTPUT
15	+5V	31	HOLD ADJUST
16	GROUND	32	STROBE

SPECIFICATIONS (typical @ +25°C with nominal power supplies and 1kΩ output load unless otherwise noted).

Model		HDD-1206JW			HDD-1206SM		
Parameter	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
RESOLUTION		12			*		Bits
LSB WEIGHT (FS = 10.24V)		2.5			*		mV
ACCURACY (Including Linearity)		±0.0125			*		%FS
Linearity		±1.25			*		mV
Zero Offset[1] (Initial)		±35	±50		*	*	mV
Monotonicity		Guaranteed			*		
TEMPERATURE COEFFICIENTS							
Linearity		5			*		ppm/°C
Gain		40			*		ppm/°C
Offset		100			*		ppm/°C
DYNAMIC CHARACTERISTICS[2]							
Settling Time to ½LSB							
±5.12V FS Change		2			*		µs
1LSB Change		60			*		ns
Internal Current D/A		50			*		ns
Slew Rate		25			*		V/µs
Small Signal Bandwidth (3dB)		1.5			*		MHz
Gain		Adjustable			*		V/V
DIGITAL DATA INPUTS							
Logic Compatibility		TTL			*		
Logic Levels							
"1"	+2.4		+5	*		*	V
"0"	0		+0.4	*		*	V
Load (each bit)		One Standard			*		TTL Load
Coding (see Table on last page)		Complementary Binary (CBN); Offset Binary (OBN)			* *		
STROBE INPUT							
Logic Compatiblity		TTL			*		
Logic Levels							
"1"	+2.4		+5	*		*	V
"0"	0		+0.4	*		*	V
Load		One Standard			*		TTL Load
Risetime/Falltime (10%–90%)			15			*	ns
Width	50		.65/word rate	*		*	ns
Frequency			6			*	MHz
OUTPUT (see Table on last page)							
R_{FB} = 1,000Ω							
Bipolar Voltage[3]		±2.56			*		V
Unipolar Voltage		0 to −5.12			*		V
Current	8			*			mA
R_{FB} = 2,000Ω							
Bipolar Voltage		±5.12			*		V
Current	8		100	*		*	mA
Residual Glitch		50			*	*	mV
Output Impedance		0.1	1		*	*	Ω
Capacitive Loading		1,000			*		pF
POWER REQUIREMENTS							
+15V ± 3% Current		55	60		*	*	mA
−15V ± 3% Current		30	35		*	*	mA
+5V ± 5% Current		85	95		*	*	mA
Power Supply Rejection Ratio		2			*		mV/V
Power Dissipation		1.7	1.9		*	*	W
TEMPERATURE RANGE							
Operating[4]	0		+70	−55		+125	°C
Storage	−55		+125	*		*	°C
THERMAL RESISTANCE[5]							
Junction to Air, θja (free air)		38			34		°C/W
Junction to Case, θjc		18			14		°C/W
MTBF[6]							
Mean Time Between Failures				3.015 × 10^5			Hours

FOR APPLICATIONS HELP, CALL (919) 292-6427

NOTES:

[1] Adjustable to zero.

[2] All dynamic characteristics are based on FS = ±5.12V; R_{FB} = 2,000Ω.

[3] With R_{FB} = 1k, analog output voltages are half those shown in Table on last page.

[4] Case Temperature.

[5] Maximum junction temperature is 150°C.

[6] Calculated per MIL-HDBK 217, Ground; Fixed Case Temperature = 60°C.

*Specifications same as HDD-1206JW
Specifications subject to change without notice.

See Figures HY32A (glass) and HY32C (metal) for complete outline and mechanical information.

THEORY OF OPERATION

Refer to the equivalent circuit for the HDD-1206 D/A converter.

The unit consists of input registers, fast-settling current output D/A, output amplifier, timing generator, and associated circuits.

The purpose of the input register circuits is to de-skew the input bits and assure their simultaneous arrival at the input of the current D/A. This is critical because time skew on the input data bits is a major contributor to discontinuities, or "glitches," in the analog output of a D/A.

The Timing Generator includes a Track & Hold circuit and generates the required internal pulses for operation whenever it receives a Strobe input pulse. See Figure 1, the HDD-1206 timing diagram.

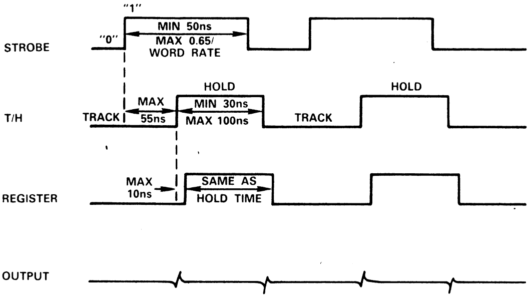


Figure 1. HDD-1206 Timing Diagram (Digital Inputs not Changing)

As shown, the Strobe pulse is a positive-going TTL pulse supplied by the user of the HDD-1206. Internal timing circuits establish the maximum 55ns delay from the leading edge of the Strobe pulse to the leading edge of the T/H (Track/Hold) pulse; and the maximum 10ns delay from the leading edge of the T/H pulse to the leading edge of the Register pulse. The data from the input registers are strobed into the current D/A at the end of this 65ns interval, so they must be valid by that time.

The user determines the width of the T/H pulse (and the Register pulse) by selecting the value of the R_{HOLD} resistor. See Figures 2 and 4. As shown, the width of the Hold pulse can vary from approximately 30ns to approximately 100ns by using resistor values from 1k to 5k, respectively.

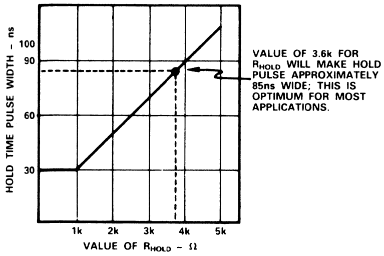


Figure 2. Hold Time vs. R_{HOLD}

For most applications, a value of 3.6kΩ and a pulse width of approximately 85ns is the optimum choice. This pulse width will "hold" the analog output of the HDD-1206 D/A until the "glitch" resulting from the most recent update has passed, without infringing on the word rate capabilities of the HDD–1206.

CURRENT-OUTPUT D/A CONVERTERS

A brief review of the salient characteristics of current D/A converters may be a useful approach to understanding the operation of the HDD-1206 unit.

Current-switching D/A converters are inherently faster than voltage-output types because of the absence of an output amplifier. This means current-switching converters have no slew rate limitation which can slow settling; nor are they subject to the overshoot and ringing problems often associated with feedback amplifiers.

Current-switching and voltage-output converters display a discontinuity, or "glitch," in their analog outputs because of the basic characteristic of saturated logic (TTL is an example) which causes the propagation delay to be less for negative-going inputs than it is for positive-going inputs.

This difference in propogation delay manifests itself as a "worst case glitch" at the major carry point, or mid-scale, of the output range of the current converter. This is the point at which nearly equal and opposite currents are being switched within the converter.

The "glitch" at mid-scale, the switching point of the Most Significant Bit (MSB), will be halved at the ¼ and ¾ points; halved again at the ⅛ and ⅞ points, etc. The amplitude of the "glitch," therefore, is a function of signal dynamics and cannot be eliminated with filtering.

The variations in glitch amplitude caused by signal dynamics create a multitude of intermodulation (IM) products, some of which fall into the video pass-band as spurious signals, and increased noise level. These IM products are also relatively immune to elimination by filtering.

The amplitude of the glitch can be reduced by de-skewing the input bits; but no amount of de-skewing or filtering can negate the physics of saturated logic which cause the glitch to be generated initially.

The best solution, then, is to cause the glitch to remain a constant across the entire output range of the converter. The efficiencies of the circuit will be enhanced if the solution can also permit using the full drive capabilities of the current-output D/A in either unipolar or bipolar modes of operation.

The design approach used in the Analog Devices HDD-1206 D/A converter accomplishes these desired goals and provides voltage outputs at high update rates.

NOTES ON DEGLITCHING

Refer again to the equivalent circuit for the HDD-1206. The data bits are applied through the input register to the current-output D/A converter, which is capable of supplying up to 5.12mA of output current.

The output of the current D/A, in turn, is applied to the input of the output amplifier via strapping external to the HDD-1206. The Timing Generator supplies the necessary pulses and timing to apply signals to the current D/A and output amplifier after the initial glitch caused by the digital inputs has subsided.

The digital "1" (Hold) level of the T/H pulse causes the switch at the input of the amplifier to open, holding the last value of the current D/A converter. During this hold interval, the switching transients caused by updating digital inputs are masked from the amplifier, thereby avoiding HDD-1206 output discontinuities whose amplitude would be a function of signal dynamics.

Ten nanoseconds after the T/H pulse goes to the digital "1" level, the register pulse also changes state from "0" to "1".

This transition moves the output of the current D/A to the new value established by the most recent digital inputs applied to the HDD-1206.

Any change in the current D/A output has stablized by the time the T/H pulse returns to the digital "0" (Track) level. Re-establishing the track mode closes the switch at the input of the amplifier and the output of the HDD-1206 moves to the new analog value dictated by the digital input word.

As shown in Figure 1, the output of the HDD-1206 will contain switching transients associated with the T/H pulse. But these "glitches" will be constant in amplitude and duration and will occur at the update rate, since they are a function of the strobe pulse applied by the user.

These switching transients will settle out in approximately 500ns, and will have uniform amplitude over the complete analog output range of the D/A. For strobe rates of 2MHz and above, the settling interval switching from "hold" to "track", and vice versa, will produce a constant dc offset on the output. The HDD-1206 is not intended to get rid of all glitches per se; it is designed to provide a constant-amplitude glitch.

When the area under the transient curve is held constant, the frequency spectrum of the glitch is a fine line, i.e., a single-line spectrum at the sample rate frequencies, and harmonics of the sample frequency.

The HDD–1206 effectively eliminates the IM products discussed above. When it does, the signal-to-noise (S/N) ratio approaches that of an ideally-quantized signal, where the rms noise is $q/\sqrt{12}$, when frequencies above Nyquist are filtered out.

GLITCH VS. PEDESTAL

In addition to the "glitch" which is a characteristic of current D/As, the track & hold used in the HDD-1206 also contributes an anomaly to the output signal.

Refer to Figure 3. This diagram compares the "glitch" created by the HDD-1206 to the pedestal created by the internal T/H circuits.

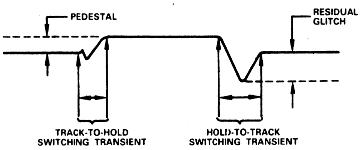

PEDESTAL
RESIDUAL GLITCH
TRACK-TO-HOLD SWITCHING TRANSIENT
HOLD-TO-TRACK SWITCHING TRANSIENT

Figure 3. Pedestal/Glitch Relationship

As shown, the "glitch" is a transient signal which remains constant in width and amplitude over the entire output range, at all update rates. The pedestal, on the other hand, is an offset signal whose amplitude can vary (because of switching transient settling) as a function of hold time and word rate.

This pedestal is caused by charge transfer associated with the hold capacitor; the transfer occurs when the HDD-1206 circuits are switched from a "track" to "hold" condition. The pedestal is basically an offset error in the HDD-1206 output and can be compensated with the Offset Adjust when the unit is installed in the user's system.

Figure 3 is not drawn to scale; there is no attempt to imply the identified elements have precisely that relationship to one another. They are exaggerated for illustrative purposes.

Applications

Bipolar connections for the HDD-1206 D/A converter are shown in Figure 4. As indicated, a unipolar negative output is accomplished by connecting Bipolar Pin 29 to ground, instead of to Pins 27 and 28.

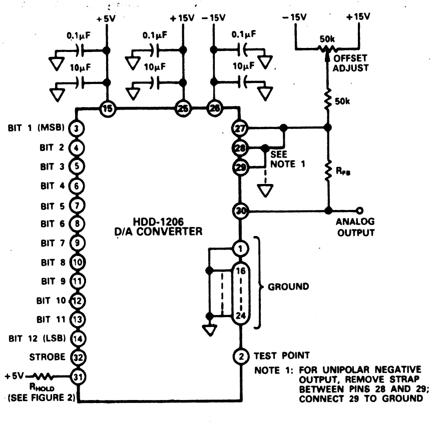


Figure 4. HDD-1206 Bipolar Connections

The output voltage swing is established by the value of feedback resistor R_{FB}. The table below indicates output levels for both unipolar and bipolar operation, with feedback resistors of either 1,000Ω or 2,000Ω.

Hold resistor R_{HOLD} connected between the +5V supply and Pin 31 sets the width of the Hold mode of the T/H pulse. Test Point Pin 2 is used for observing the pulse.

The Offset Adjust potentiometer is used to set the desired analog output of the HDD-1206 and can be used to help assure correct voltages are present when the D/A is installed in the system.

When operated in a unipolar mode with digital "0" applied to all inputs but no continuous strobe pulses applied, the Offset Adjust is set for an analog output of either −5.12V or −10.24V, depending on the value of R_{FB}. (NOTE: At least one strobe pulse needs to be applied to latch the input data into the registers.)

If the HDD-1206 is installed in a system and the strobe pulse is applied continuously, the Offset Adjust is calibrated for the desired output value with a digital "0" applied to all input pins.

HDD-1206 ANALOG OUTPUT WITH 1kΩ LOAD

Digital Inputs	Offset Binary (OBN) Bipolar Output $R_{FB} = 2k$	Complementary Binary (CBN) Unipolar Negative Output $R_{FB} = 1k$
111...111	+5.175(+FS − 1LSB)	0.0000(0)
111...110	+5.1150	− 0.0125(+1LSB)
110...000	+2.5600(+1/2FS)	− 1.27875
101...111	+2.5575	− 1.28(1/4)
100...000	0.0000(0)	− 2.55875
011...111	−0.0025(−1LSB)	− 2.56(1/2)
010...000	−2.5600(−1/2FS)	− 3.83875
001...111	−2.5625	− 3.84(3/4)
000...001	−5.1175	− 5.1175
000...000	−5.1200(−FS)	− 5.11875(FS − 1LSB)

ORDERING INFORMATION

Model HDD-1206JW D/A converter is housed in a glass package, the model HDD-1206SM is a metal version; outline dimensions of both are shown elsewhere. For metal case version processed per MIL-STD-883, Method 5008, specify model HDD-1206SM/883.

Mating individual pin sockets are available from AMP. Part number 6-330808-0 are knockout end type; 6-330808-3 are open end type.

ANALOG DEVICES

Hybrid Video Digital-to-Analog Converters

HDG SERIES

FEATURES

- Ultra Fast 7ns Settling Time to 0.4% (8ns Max)
- Low 50 pV-s Max Glitch Energy
- Operates from Single -5.2V Power Supply
- Complete Composite Inputs
- Designed for General Output Compatibility with EIA Standards RS-170 and RS-343, Including 10% Brightness
- Available Screened to MIL-STD-883
- Low Price

APPLICATIONS

- Raster Scan Graphics Displays
- TV Video Reconstruction
- Ultra Fast Current or Voltage Output DAC for Analytical Instrumentation
- Digital VCOs

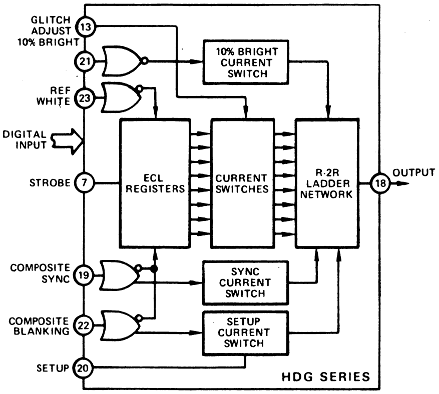
GENERAL DESCRIPTION

The HDG series digital-to-analog converters are the fastest D/As with full composite capabilities presently available. The units are available in three resolutions (levels) of Gray Scale. The HDG-0805 has 8 bits of resolution (256 levels) and typically settles in 7ns (8 max). The HDG-0605 has 6-bit resolution (64 levels) and typically settles in 5ns (6 max), while the HDG-0405 features 4-bit resolution (16 levels) and typically settles in less than 3ns (4 max). All three units are packaged in 24-pin metal hybrids and require only a single -5.2V power supply for operation.

All three units have complete composite controls including self-contained, digitally-controlled sync, blanking, and 10% bright, a unique feature not found on most composite D/A converters. A reference white control input is also provided, thus assuring compatibility with EIA Standards RS-170, RS-330, and RS-343A.

Absolute accuracies of the HDG-0805, HDG-0605 and HDG-0405 are ±0.19, 0.8, and 3.2% respectively. The output impedance is 75Ω and the full scale output current of -17mA is sufficient to develop 1V across a 75Ω video load. Operation of all three units is specified over the case temperature range of -25°C to +85°C. Monotonicity is guaranteed.

HDG SERIES FUNCTIONAL BLOCK DIAGRAM



The HDG series D/A converters represent the most cost-effective high performance system solution for 8-bit raster scan D/A converter requirements. Older modular technology offers similar electrical performance but at much larger size and at a higher price. Monolithic technology has produced DACs at comparable speeds but without composite capabilities, thereby requiring external registers, sync and blanking circuits, and references for compatibility.

Because of the units ultra-fast speed and low cost, and their ability to be screened to the requirements of MIL-STD-883, the HDG series DACs can be used in military D/A applications as well.

Model	Resolution	% of Gray Scale	Settling Time (max)
HDG-0805	8 Bits	0.4%	8ns
HDG-0605	6 Bits	1.6%	6ns
HDG-0405	4 Bits	6.4%	4ns

Table 1. Accuracy vs. Settling Time

SPECIFICATIONS (typical @ +25°C with nominal power supplies and 75Ω output load unless otherwise noted)

Model	Units	HDG-0405	HDG-0605	HDG-0805
RESOLUTION FS = FULL SCALE	Bits	4	6	8
LSB WEIGHT (Current)	μA	1072	268	67
LSB WEIGHT (Voltage)	mV	40	10	2.5
ACCURACY[1]				
Absolute	±% of GS	3.2	0.8	0.19
Linearity	±% of GS	3.2	0.8	0.19
Monotonicity		Guaranteed	*	*
Zero Offset (Initial)	mV	0.9	*	*
SPEED PERFORMANCE – GRAY SCALE OUTPUT				
Settling Time (Voltage) Max[2]	ns (to % GS)	4(6.4)	6(1.6)	8(0.4)
Slew Rate	V/μs	200	*	*
Update Rate[3]	MHz	100	*	*
Rise Time	ns	3	*	*
Glitch Energy[4]	pV-s	50	*	*
TEMPERATURE COEFFICIENTS				
Linearity	ppm/°C	16.0	*	*
Zero Offset	ppm/°C	6.0	*	*
Gain	ppm/°C	17.0	*	*
STROBE INPUT				
Logic Compatibility		ECL	*	*
Logic Voltage Levels "1"	V	-0.9	*	*
Positive Logic) "0"	V	-1.7	*	*
Logic Loading		50pF and 5kΩ to -5.2V	*	*
Set-Up Time (Data)	ns	2.5 min	*	*
Hold Time (Data)	ns	1.5 min	*	*
Propagation Delay	ns	3	*	*
REFERENCE WHITE INPUT[5]				
Logic Compatibility		ECL	*	*
Logic Voltage Levels "1"	V	-0.9	*	*
"0"	V	-1.7	*	*
Logic Loading		5pF and 50kΩ to -5.2V	*	*
DATA INPUTS				
Logic Compatibility		ECL	*	*
Logic Voltage Levels "1"	V	-0.9	*	*
(Positive Logic) "0"	V	-1.7	*	*
Logic Loading (Each Bit)		5pF and 50kΩ to -5.2V	*	*
Coding (See Table)		Complementary Binary (CBN)	*	*
COMPOSITE SYNC INPUT				
Logic Compatibility		ECL	*	*
Logic Voltage Levels "1"	V	-0.9	*	*
"0"	V	-1.7	*	*
Logic Loading		5pF and 50kΩ to -5.2V	*	*
COMPOSITE BLANKING AND 10% BRIGHT, INPUTS				
Logic Compatibility		ECL	*	*
Logic Voltage Levels "1"	V	-0.9	*	*
"0"	V	-1.7	*	*
Logic Loading		5pF and 50kΩ to -5.2V	*	*
SETUP CONTROL				
Ground	mV	0 (0 IRE Units)	*	*
Open	mV	71 (10 IRE Units)	*	*
-5.2V	mV	142 (20 IRE Units)	*	*
OUTPUT				
Current	mA	0 to -17	*	*
Voltage[6]	V (±1%)	0 to -0.600	0 to -0.630	0 to -0.6375
Compliance	V	+1.1 to -1.1	*	*
Internal Impedance	Ω (±5%)	75	*	*

Model	Units	HDG-0405	HDG-0605	HDG-0805
OUTPUT – COMPOSITE SYNC				
Current	mA (±5%)	0 or -7.6	*	*
Voltage	mV (±5%)	0 or -286	*	*
OUTPUT – 10% BRIGHT				
Current	mA (±5%)	0 or -1.9	*	*
Voltage	mV (±5%)	0 or -71	*	*
OUTPUT – COMPOSITE BLANKING[7]				
Current	mA (±1%)	0, -17.0, -18.9, or -20.8	*	*
Voltage	mV (±1%)	0, -637.5, -708.75 or -780	*	*
SPEED PERFORMANCE – CONTROL INPUTS				
Settling Time to 10% of Final Value for:				
Composite Sync	ns	8	*	*
Composite Blanking	ns	8	*	*
Reference White	ns	8	*	*
Reference Black	ns	8	*	*
10% Bright	ns	8	*	*
POWER REQUIREMENTS				
-5.2V ±0.25V[8]	mA	200	260	320
TEMPERATURE RANGE				
Operating, Metal Case	°C Case	-25 to +85	*	*
Storage	°C	-55 to +125	*	*
MTBF[9]				
Mean Time Between Failure	hours			195,434
PACKAGE OPTION[10]	HY24G (metal package)			

NOTES

[1] Accuracy is relative to Gray Scale and includes linearity.

[2] Worst case settling to a percentage of maximum Gray Scale is given, and includes FS and MSB transitions. The inherent 3ns propagation delay through the input registers (50% points) has been disregarded.

[3] The update rates shown are limited by a full-scale settling time that is useable for the number of bits of resolution. The DACs may be updated to a maximum of 125MHz with some settling time degradation.

[4] Reducible to less than 25pV-s with glitch adjustment.

[5] A Logic "0" on Pin 29, Reference White will drive the output to the Reference White level regardless of digital input.

[6] The difference between the full-scale output of 637.5mV and 643mV shown elsewhere herein (HDG-0805) is due to the fact that we selected an LSB value of 2.5mV for ease of calibration. These differences are well within the output and EIA Standard RS-170 tolerances.

[7] The three currents and voltages correspond to the three set-up levels of 0, 10, and 20 IRE units as externally selected.

[8] Power Supply must have less than 5mV p-p ripple. Sensitivity is 1:1.

[9] Calculated for HDG-0805 using MIL Handbook 217. Ground: fixed; Ambient Temperature: 50°C.

[10] See Section 20 for package outline information.

*Specifications same as for HDG-0405.

Specifications subject to change without notice.

PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	GROUND	13	GLITCH ADJUST
2	-5.2V	14	GROUND
3	BIT 1 (MSB)	15	GROUND
4	BIT 2	16	GROUND
5	BIT 3	17	GROUND
6	BIT 4	18	ANALOG OUTPUT
7	CLOCK	19	COMPOSITE SYNC
8	BIT 5	20	SETUP
9	BIT 6	21	10% BRIGHT
10	BIT 7	22	COMPOSITE BLANKING
11	BIT 8 (LSB)	23	REFERENCE WHITE
12	GROUND	24	-5.2V

NOTES: FOR HDG-0605 PIN 9 IS LSB AND PINS 10 AND 11 ARE PRESENT BUT NOT USED.
FOR HDG-0405 PIN 6 IS LSB AND PINS 8, 9, 10 AND 11 ARE PRESENT BUT NOT USED.

Typical Applications

A typical raster scan graphics display system is depicted in Figure 1. The system consists of a MOS RAM memory buffer for storing the data to be displayed, one or more memory controllers for display updating and CRT refresh, and a programmable μP for graphics generation and image manipulation. The system acts as an intelligent peripheral to the host CPU, and drives standard television monitors via the built-in DAC circuitry.

The D/A converter controls the Z axis of the CRT modulating the brightness of the raster scan beam. A typical raster scan system requires resolution anywhere from 4 to 8 bits, which represents 16 to 256 levels of Gray Scale. For color displays three DACs are required—one each for the red, green, and blue color guns.

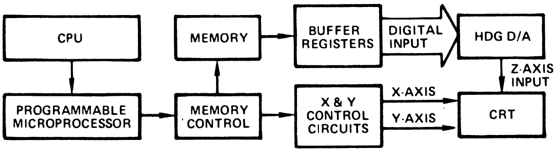
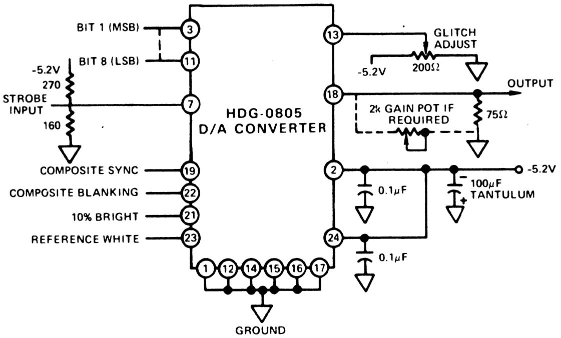


Figure 1. Typical Raster Scan Display System

APPLICATIONS INFORMATION

The HDG series D/A converters feature the fastest 8-bit settling times presently available. To insure maximum performance at these speeds the following guidelines should be followed:

1. The D/A converter should be provided with a very low impedance grounding system to very high frequencies. A large ground plane is a must.
2. Low frequency bypassing should be provided with a 1μF (or larger) tantalum capacitor mounted between the -5.2V supply line and ground near the D/A.
3. High frequency bypassing should be provided by ceramic capacitors of 0.1μF or larger mounted within 0.25 inches of Pins 2 and 24 to ground (see Figure 2).



NOTES: ALL DIGITAL INPUTS TERMINATED TO -5.2V THROUGH 2kΩ EXCEPT STROBE WHICH IS 270 FOR HDG-0605 PIN 9 IS LSB, FOR HDG-0405 PIN 6 IS LSB

Figure 2. HDG-0805 Typical Connection Diagram

4. The threshold of the internal current switches can be optimized for low glitch energy by the addition of an external potentiometer connected to Pin 13 of the D/A (see Figure 2). This potentiometer is adjusted for minimum glitch energy as shown in Photo 2.
5. Standard 24 pin sockets should be avoided. Individual "pin sockets" are most suited for evaluating devices, as lead inductance is reduced. In final designs, the D/As should be soldered directly into the printed circuit board without sockets.
6. Microstrip techniques are recommended for routing digital and strobe inputs to the DAC for distances greater than 1" (2.54mm).

Power Supply Sensitivity

Precision -5.2V Supply

The power supply sensitivity of the HDG series DACs is given as 1:1. This means that 1mV change in the power supply voltage will produce a 1mV change at the output. For the HDG-0605 and HDG-0405 this presents no problems, since even 5mV of ripple is less than 1/2LSB. If regulation is desired, use a LM120 or equivalent 3 terminal negative regulator. When applying the HDG-0805, it may be desirable to supply a highly regulated -5.2V supply to counteract the effects of time and temperature.

A circuit to supply a precise -5.2V supply is shown in Figure 3. This uses AD584 and AD OP-07 to achieve an ultra stable -5.2V input to the DAC.

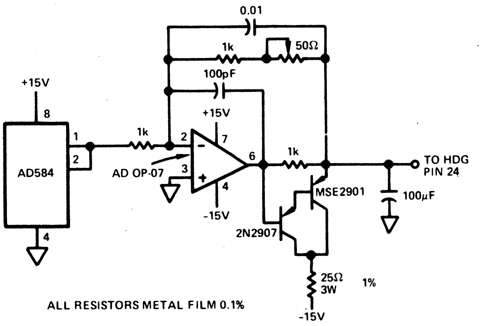


Figure 3. Precision -5.2V Supply

TESTING THE HDG SERIES DACs

Settling Time

Measuring the full-scale settling time of an 8ns DAC presents a significant challenge even under perfect conditions. The only practical solution using oscilloscopes is to extrapolate the settling time from a rise-time measurement. This is because the vertical amplifier of the scope will undoubtedly be overdriven when the required gain is achieved.

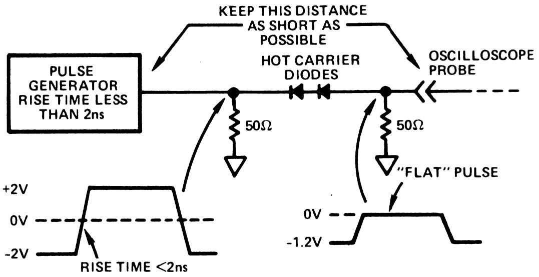


Figure 4. Flat Pulse Generator

Using the circuit of Figure 4, a pulse generator with rise times of less than 2ns is a must. The scope proble is calibrated using the resistor/diode scheme shown, which results in a "flat pulse." The rise time (10% to 90%) of the all "0s" to all "1s" transition, t_r, is measured using a sampling oscilloscope having a bandwidth of 500MHz minimum. The associated time constant, τ, is related to t_r by the following:

$$t_r = 2.2\tau$$

Assuming an exponential function, the D/A output, V, is given by:

$$V = (1 - e^{-t/\tau})\, V_O$$

The settling time required, t_s, to reach a percentage of the final output, V_O is given by the following table:

Resolution	% of Full Scale	Settling Time
8	0.4	$2.5\ t_r$
7	0.5	$2.2\ t_r$
6	1.6	$1.9\ t_r$
5	3.2	$1.5\ t_r$
4	6.4	$1.2\ t_r$

It can then be seen that using the HDG rise time of 3ns results in settling times of 3.6, 5.7, and 7.5ns for the HDG-0405, 0605, and 0805 respectively.

Photo 1 shows an actual full-scale output signal measured using the above procedure indicating a rise time of 2.5ns. The corresponding settling time to 8-bit accuracy would thus be 6.3ns.

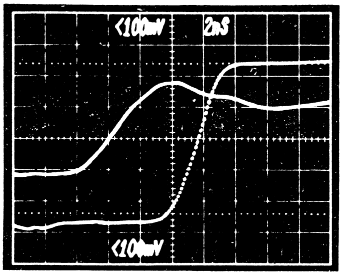


Photo 1. Full Scale Output — Rise Time

Glitch Energy

The glitch amplitude of the HDG series DACs at the major carry point is typically less than 100mV. This allows the user to measure it directly since there is little danger of overdriving the oscilloscope's vertical amplifier. Distances from the DAC output to the scope input should be minimal (no more than a few inches). Photo 2 shows an actual HDG-0805 mid-scale glitch measured using the 50Ω input of the sampling scope as termination for the D/A. The D/A test set output was connected directly to the scope using the appropriate BNC fittings. Positive and negative glitch energy in the photo is less than 30 picovolt-seconds. Net glitch energy is approximately zero. Note that glitch settling is less than 6ns.

In the rare case that positive and negative glitch excursions are unequal the glitch adjust input (Pin 13) may be used as shown in Figure 2 to minimize the net glitch energy.

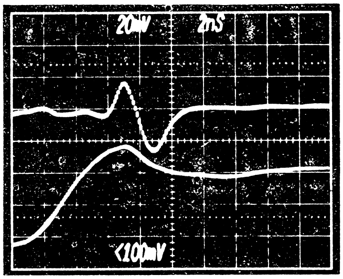


Photo 2. Midscale Glitch

CHARACTERISTICS OF HDG-0805, [-0605], [-0405] VIDEO DACs

COMPOSITE VIDEO SIGNAL

256 gray levels plus blanking and sync levels [64] [16]

STEP SIZE

2.5 [10] [40] mV

GRAY SCALE RANGE

0.643V Peak to Peak

SETUP CONTROL

User programmable in three levels

	mV	IRE Units
1. Input Grounded	0	0
2. Input Open	71	10
3. Input 0 -5.2V	142	20

REFERENCE WHITE LEVEL

0V Absolute

100 IRE Units (+0.714V relative to blanking level with standard setup; +0.643V relative to Reference Black)

DIGITAL INPUT FOR WHITE LEVEL

All ones (11111111)

REFERENCE WHITE CONTROLS[1]

Overrides Video Input Word

A Logic "0" on Pin 23 will drive the output to the Reference White Level.

REFERENCE BLACK LEVEL

-0.643V Absolute; +71mV (10 IRE Units)

Relative to blanking level with standard setup.

DIGITAL INPUT FOR REFERENCE BLACK

All zeroes (00000000)

COMPOSITE BLANKING LEVEL

-0.714V absolute, (0 IRE Units) with standard setup.

COMPOSITE BLANKING INPUT – PIN 22

Logic "0" on Pin 22 resets input register to 00000000, and causes output voltage to go negative by the amount of setup voltage with respect to the all "0" output voltage.

COMPOSITE SYNC LEVEL

-1.0V absolute with standard setup.

-0.286V (–40 IRE Units) relative to blanking level (Back Porch).

COMPOSITE SYNC INPUT – PIN 19

Logic "0" resets input register to 00000000, and the output voltage goes negative by 0.286V.

10% BRIGHT – PIN 21

Logic "0" causes output to go positive by 71mV. Note: The most positive output voltage is still 0 volts absolute. All other levels are shifted down by 71mv; i.e., Sync Level (-40 IRE) becomes -1.071V.

STROBE – PIN 7

Logic "0" to Logic "1" transition clocks input register.

DEFINITION OF VIDEO TERMS

BLANKING LEVEL

The level separating the SYNC portion from the Video portion of the waveform. Usually referred to as the Front Porch or Back Porch. At 0 IRE Units, it is the level which will shut off the picture tube, resulting in the blackest possible picture.

COLOR VIDEO (RGB)

This usually refers to the technique of combining the three primary colors of Red, Green, and Blue to produce color pictures within the usual spectrum. In RGB monitors, three HDG "C" Series DACs would be required, one for each color.

COMPOSITE SYNC SIGNAL (SYNC)

The portion of the composite video signal which synchronizes the scanning process.

COMPOSITE VIDEO SIGNAL

The video signal with or without setup, plus the composite SYNC signal.

GRAY SCALE

The discrete levels of video signal between Reference Black and Reference White levels. A 10-bit DAC contains 1,024 different levels, while an 8-bit DAC contains 256 (2^N).

RASTER SCAN

The most basic method of sweeping a CRT one line at a time to generate and display images. This method is used in commercial television in the USA.

REFERENCE BLACK LEVEL

The maximum negative polarity amplitude of the video signal.

REFERENCE WHITE LEVEL

The maximum positive polarity amplitude of the video signal.

SETUP

The difference between the Reference Black level and the blanking level. This should not be confused with setup as used with digital logic.

SYNC LEVEL

The peak level of the composite SYNC signal.

VIDEO SIGNAL

That portion of the composite video signal which varies in gray scale levels between Reference White and Reference Black. Also referred to as the picture signal, this is the portion which may be visually observed.

NOTE:

[1] Reference White (Pin 23) should not be activated at the same time as composite blanking (Pin 22).

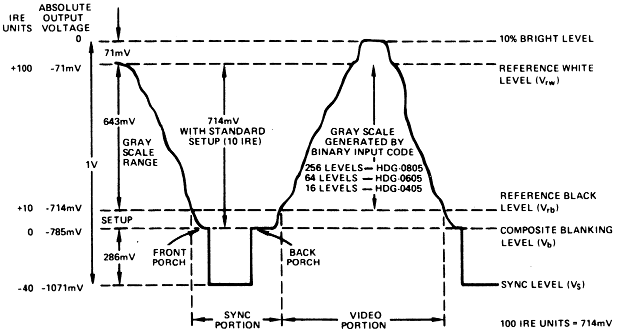


Figure 5. HDG-0805 Composite Output Waveform

ORDERING GUIDE

Model	Resolution	Settling Time (max)
HDG-0805 HDG-0805/883[1]	8 Bits	8ns
HDG-0605 HDG-0605/883[1]	6 Bits	6ns
HDG-0405 HDG-0405/883[1]	4 Bits	4ns

[1] Denotes processing to MIL-STD 883; per method 5008. Consult factory for availability.

ANALOG DEVICES

8-, 10-, 12-Bit Video Speed Hybrid Current & Voltage Out D/A Converter

HDS-0820, -1025, -1250/HDH-0802, -1003, -1205

FEATURES

- 25ns Current Settling to 0.1% (HDS)
- 200ns Voltage Settling to 0.1% (HDH)
- 10mA Current Out (HDS)
- Guaranteed Monotonicity Over Temperature
- No External Parts Required
- Reliable Hybrid Construction

APPLICATIONS

- CRT Vector Displays
- TV Video Reconstruction
- Military Equipment (MIL-STD-883)
- Analytical and Medical Instruments

GENERAL DESCRIPTION

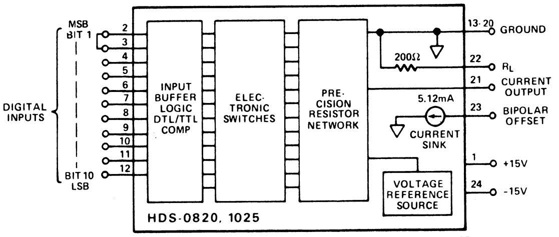
The HDS/HDH series of digital to analog converters represent the fastest precision settling current and voltage DAC's available. Capable of processing to MIL-STD-883 and guaranteed monotonicity over their operating temperature range; their quiescent power is 1/2 that of competitive units. The current output models provide 10mA full scale allowing direct drive of capacitive loads and transmission lines. All versions have a precision reference and are active laser trimmed to specified accuracy, thus no external adjustment pots or other components are required.

Other general specifications that apply to all devices include TTL logic; glass or hermetic metal package; unipolar or bipolar operation with internal offsetting reference.

The HDH voltage output devices provide access to the op amp summing point so that reduced full scale output voltage swing can be provided. Such operation with an external resistor shunting the internal 1k resistor will reduce the already low op amp offset drift.

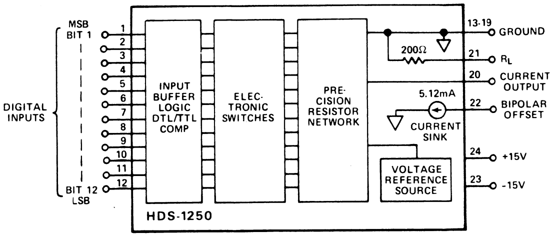
With 6 available units engineering trade-offs can be made between resolution, speed, current or voltage output, and of course price. To facilitate this comparison major specifications are summarized in Table 1.

HDS-0820, HDS-1025 FUNCTIONAL BLOCK DIAGRAM

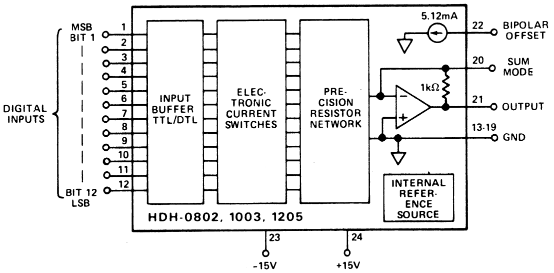


NOTE: ON 8-BIT VERSIONS, PINS 11 AND 12 ARE NOT CONNECTED INTERNALLY, AND PIN 10 IS LSB.

HDS-1250 FUNCTIONAL BLOCK DIAGRAM



HDH-0802, HDH-1003 AND HDH-1205 FUNCTIONAL BLOCK DIAGRAM



NOTE: ON HDH-0802 DEVICES, GROUND PINS 9, 10, 11 AND 12.
ON HDH-1003 DEVICES, GROUND PINS 11 AND 12.

Model	Resolution	Full Scale Step Settling Time
Current Output		10mA Step
HDS-0820	8 Bits	20ns to 0.4%
HDS-1025	10 Bits	25ns to 0.1%
HDS-1250	12 Bits	35ns to 0.025%
Voltage Output		10V Step
HDH-0802	8 Bits	200ns to 0.4%
HDH-1003	10 Bits	300ns to 0.1%
HDH-1205	12 Bits	500ns to 0.125%

Table 1.

For detailed information, contact factory.

SPECIFICATIONS (typical @ +25°C with nominal power supply voltages unless otherwise noted)

		CURRENT OUT			VOLTAGE OUT		
MODEL	UNITS	HDS-0820	HDS-1025	HDS-1250	HDH-0802	HDH-1003	HDH-1205
RESOLUTION FS = Full Scale	Bits	8	10	12	8	10	12
LSB WEIGHT		40μA	10μA	2.5μA	40mV	10mV	2.5mV
ACCURACY (Relative to FS Including Linearity)	±% FS	0.1	0.05	0.0125	0.1	0.05	0.0125
Linearity		±10μA	±5μA	±1.25μA	±10mV	±5mV	±1.25mV
	LSB	±1/4	±1/2	±1/2	±1/4	±1/2	±1/2
Monotonicity		Guaranteed Over Operating Temperature Range					
Zero Offset (Initial)		15nA max	*	*	10mV typ 50mV max	*	*
TEMPERATURE COEFFICIENTS							
Linearity	ppm/°C	3	*	*	*	*	*
Gain	ppm/°C	30	*	*	*	*	*
Unipolar Offset	ppm/°C	3	*	*	*	*	*
Bipolar Offset	ppm/°C	15	*	*	*	*	*
DATA INPUTS							
Logic Compatibility		TTL and 5V CMOS					
Logic Voltage Levels Positive Logic "1" =	V	+2 to +7	*	*	*	*	*
"0" =	V	0 to +0.8	*	*	*	*	*
Logic Loading (Each Bit) "1" =	μA	40	*	*	*	*	*
"0" =	mA	-2.6	*	*	*	*	*
Codes		BIN, OBN			BIN,OBN		
OUTPUT							
Current Range FS							
Unipolar	mA	+10.24	*	+10.24 ±0.05%	±25 max	**	**
Bipolar	mA	±5.12	*	±5.12 ±0.025%	±25 max	**	**
Voltage Out FS[1, 2]							
Unipolar HDS with 200Ω Internal Connected R_L	V	+1.024	*	+1.024 ±0.05%	-10.24 ±0.1%	**	**
Bipolar	V	±0.512	*	±0.512 ±0.025%	∓5.12 ±0.05%	**	**
Compliance	V	+1.5, -2	*	*	N/A	**	**
Impedance, Internal (See Figure 1)	Ω	200	*	*	0.1 max	**	**
SETTLING TIME							
Current	ns to % FS	20 to 0.4	25 to 0.1	35 to 0.025	N/A	N/A	N/A
Voltage[2]							
Unipolar or Bipolar Out, 75Ω Load, 0.56V p-p	ns to % FS	30 to 0.4	35 to 0.1	50 to 0.025	N/A	N/A	N/A
Unipolar or Bipolar Out, Internal 200Ω Load, 1.024V p-p	ns to % FS	45 to 0.4	50 to 0.1	60 to 0.025	N/A	N/A	N/A
10V Output Step	ns to % FS	N/A	N/A	N/A	200 to 0.4	300 to 0.1	500 to 0.025
5V Output Step	ns to % FS	N/A	N/A	N/A	150 to 0.4	200 to 0.1	350 to 0.025
POWER REQUIREMENTS							
+14.5V to +15.5V	mA max	42	*	50	70	**	**
-12V to -16V	mA max	14	*	15	40	**	**
Power Supply Rejection Ratio	%/V	0.2	*	*	*	*	*
TEMPERATURE RANGE							
Operating – Glass Package	°C	0 to +70	*	*	*	*	*
Operating – "M" Metal Case[3]	°C	-55 to +125	*	*	*	*	*
Storage	°C	-55 to +125	*	*	*	*	*
PACKAGE OPTIONS[4]	HY24E (glass package)			HY24G (metal package)			

NOTES:

[1] Other voltages may be obtained with external resistor.

[2] For HDS series, $V_{OUT} = I_{OUT} \times R_{equivalent}$ which is the value of the 200Ω internal impedance in parallel with the external load resistance. Thus, by correct selection of external R1 V_{OUT} can be any magnitude up to the + or – compliance voltage. See Figures 1 and 2.

[3] Contact factory or local Analog Devices sales office for "M" Metal Case device specifications and prices.

[4] See Section 20 for package outline information.

*Specifications same as HDS-0820.

**Specifications same as HDH-0802.

Specifications subject to change without notice.

PIN DESIGNATIONS
HDS-0820, HDS-1025

PIN	FUNCTION
1	+15V
2, 3	BIT 1 (MSB)
4	BIT 2
5	BIT 3
6	BIT 4
7	BIT 5
8	BIT 6
9	BIT 7
10	BIT 8
11	BIT 9 (HDS-1025)
12	BIT 10
13-20	GND
21	OUTPUT
22	R_L 200Ω
23	BIPOLAR OFFSET
24	-15V

PIN DESIGNATIONS
HDS-1250

PIN	FUNCTION
1	BIT 1 (MSB)
2	BIT 2
3	BIT 3
4	BIT 4
5	BIT 5
6	BIT 6
7	BIT 7
8	BIT 8
9	BIT 9
10	BIT 10
11	BIT 11
12	BIT 12
13-19	GND
20	OUTPUT
21	R_L 200Ω
22	BIPOLAR OFFSET
23	-15V
24	+15V

PIN DESIGNATIONS
HDH SERIES

PIN	FUNCTION
1	BIT 1 (MSB)
2	BIT 2
3	BIT 3
4	BIT 4
5	BIT 5
6	BIT 6
7	BIT 7
8	BIT 8
9	BIT 9
10	BIT 10
11	BIT 11
12	BIT 12
13-19	GROUND
20	SUM NODE
21	OUTPUT
22	BIPOLAR OFFSET
23	-15V
24	+15V

ON HDH-0802 DEVICES, GROUND PINS 9, 10, 11 AND 12.
ON HDH-1003 DEVICES, GROUND PINS 11 AND 12.

Analog Output, ±5.12mA	Offset Binary
+5.11mA (1LSB)	111......1
+2.56mA	110......0
0mA	100......0
-2.56mA	010......0
-5.12mA	000......0
Analog Output, 0 to +10.24mA	**Straight Binary**
+10.23mA	111......1
+7.68mA	110......0
+5.12mA	100......0
+2.56mA	010......0
0mA	000......0

Table 2. Coding HDS Series

Analog Output, ±5.12V	Complement Offset Binary
-5.1175V	111......1
-2.56V	110......0
0V	100......0
+2.56V	010......0
+5.12V	000......0
Analog Output, 0 to +10.24V	**Complement Binary**
-10.2375V	111......1
-7.68V	110......0
-5.12V	100......0
-2.56V	010......0
0V	000......0

Table 3. Coding HDH Series

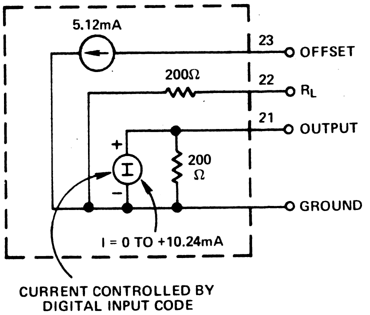


Figure 1. HDS Current Equivalent Circuit

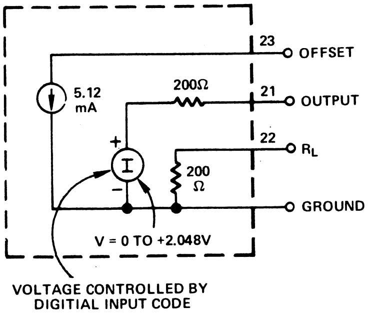


Figure 2. HDS Voltage Equivalent Circuit

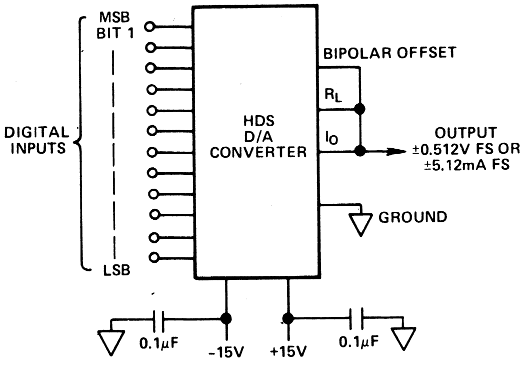


Figure 3. Bipolar Current Output

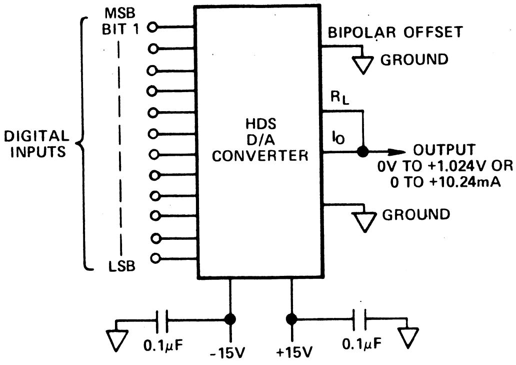
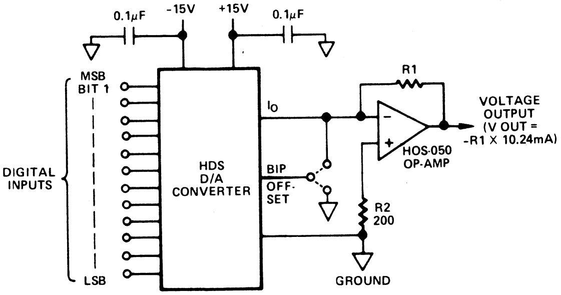


Figure 4. Unipolar Current Output



CIRCUIT PROVIDES UNIPOLAR NEGATIVE OUTPUT WITH COMPLEMENT BINARY CODING (BIPOLAR OFFSET GROUNDED) OR BIPOLAR OUTPUT WITH COMPLEMENTARY OFFSET BINARY CODING (BIPOLAR OFFSET TO I_O).

SETTLING TIME FOR 10.24V OUTPUT (R1 = 1k) IS APPROXIMATELY 150ns.

Figure 5. Inverting Unipolar or Bipolar Voltage Output

ORDERING INFORMATION

Order model number HDS-0820, HDS-1025, HDS-1250, HDH-0802, HDH-1003, HDH-1205. Models with extended operating temperature range, hermetically-sealed metal-case construction (M versions) and MIL-STD-883 processing are also available. Consult factory or local Analog Devices sales office for further information.

ANALOG DEVICES

Ultra High-Speed ECL Hybrid D/A Converter

HDS-0810E - HDS-1015E

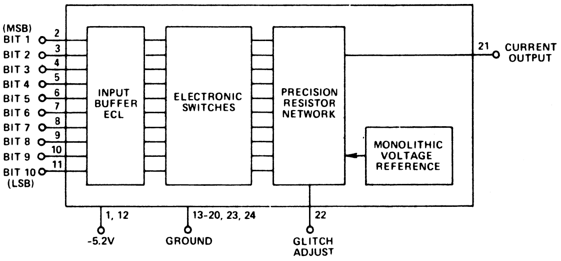
FEATURES

- Settling Times to 10ns
- Low Glitch Energy – 200pV-sec.
- 100MHz Update Rates
- 8- & 10-Bit Versions Available
- Low Power < 1 Watt
- Available Screened to MIL-STD-883

APPLICATIONS

- Raster Scan & Vector Graphic Displays
- TV Video Reconstruction
- Digital VCO's
- High-Frequency Waveform Generators
- Analytical & Medical Instrumentation

HDS-0810E, HDS-1015E FUNCTIONAL BLOCK DIAGRAM



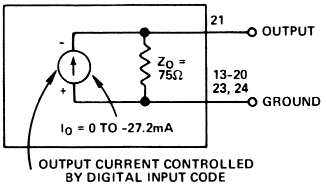
ON THE HDS-0810E, PINS 10 AND 11 ARE NOT CONNECTED INTERNALLY

PRODUCT DESCRIPTION

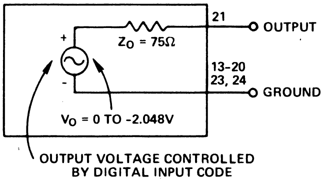
The HDS-0810E and HDS-1015E represent the latest state-of-the-art in ultra-high-speed hybrid D/A converters. They are designed to be input compatible with standard ECL logic families, and feature internal high-precision monolithic voltage reference, active laser-trimmed resistor network, and 75Ω output impedance – allowing them to be used to drive 75Ω cable directly without external driver amplifiers. This feature assures that a full 1 volt is available at the load, since the D/A output is a full 27mA. In addition, these D/A's are monotonic over the full operating temperature range and require only one power supply (-5.2V) for operation.

The HDS-E D/A's are ideally suited for use in a wide variety of applications, including graphic CRT displays, since they feature very low glitch energy and extremely fast settling time.

Packaged in an industry standard size 24-pin double width dual in-line case, the HDS-E Series D/A's are available in either ceramic/glass cases (commercial) or hermetically sealed metal cases (military). They are also available screened to MIL-STD-883.



Current Equivalent Circuit



Voltage Equivalent Circuit

For detailed information, contact factory.

SPECIFICATIONS (typical @25°C with nominal power supplies and with 75Ω output load unless otherwise noted)

MODEL	UNITS	HDS-0810E	HDS-1015E
RESOLUTION FS = Full Scale	Bits	8	10
LSB WEIGHT (Current)	μA	106	27
LSB WEIGHT (Voltage)	mV	4	1
ACCURACY[1]	±% FS	0.1	0.05
Linearity	±μA	26.5	13
Monotonicity		Guaranteed	*
Zero Offset (Initial)	μA	5	*
TEMPERATURE COEFFICIENTS			
Linearity	ppm/°C	5	*
Zero Offset	ppm/°C	1	*
Gain	ppm/°C	80	*
DATA INPUTS			
Logic Compatibility		ECL	*
Logic Voltage Levels "1" =	V	-0.9	*
(Positive Logic) "0" =	V	-1.7	*
Logic Loading "1" =	mA	+13.6	*
(Each Bit) "0" =	μA	-50	*
Coding (See Coding Table)		BIN	*
OUTPUT			
Current Range (Unipolar) FS	mA	0 to -27.2	0 to -27.3
Voltage with 75Ω Ext. Load	V (±1%)	0 to -1.020	0 to -1.023
Compliance	V	-1.1 to +1.1	*
Impedance, Internal	Ω (±5%)	75	*
SPEED PERFORMANCE			
Settling Time (Voltage)[2]	ns (to % FS)	10 (0.2)	15 (0.1)
Slew Rate	V/μs	200	*
Update Rate[3]	MHz	100	67
Rise Time	ns	4	4
Glitch Energy[4]	pV-sec	200	*
POWER REQUIREMENTS			
-5.2V ±0.25V	mA	155	180
Power Supply Rejection Ratio	%/%	0.04	*
Reference		Monolithic, Internal	*
TEMPERATURE RANGE			
Operating; Glass Case	°C	0 to +70	*
Operating; "M" Metal Case	°C	-55 to +125	*
Storage	°C	-55 to +125	*
PACKAGE OPTIONS[5]	HY24E (glass package) HY24G (metal package)		

NOTES:

[1] Relative to FS, including linearity.

[2] Worst case settling time. Includes FS and MSB transitions.

[3] Limited only by D/A settling time.

[4] Reducible to less than 100pV-sec with appropriate deskewing of digital inputs.

[5] See Section 20 for package outline information.

*Specifications same as HDS-0810E.

Specifications subject to change without notice.

PIN DESIGNATIONS

PIN	FUNCTION
1, 12	-5.2V
2	BIT 1 (MSB)
3	BIT 2
4	BIT 3
5	BIT 4
6	BIT 5
7	BIT 6
8	BIT 7
9	BIT 8
10	BIT 9
11	BIT 10 (LSB)
13-20	GROUND
21	OUTPUT
22	GLITCH ADJUST
23, 24	GROUND

ON THE HDS-0810E, PINS 10 AND 11 ARE NOT CONNECTED INTERNALLY, AND PIN 9 IS THE LSB. ALL GROUND PINS ARE CONNECTED TOGETHER INTERNALLY.

ORDERING INFORMATION

For commercial environment applications (0 to +70°C), order models HDS-0810E or HDS-1015E for 8- or 10-bit operation, respectively.

For extreme environment applications (-55°C to +125°C), order metal cased models HDS-0810EM or HDS-1015EM for 8- or 10-bit operation, respectively.

These devices are also available screened to MIL-STD-883. Consult the factory.

ANALOG
DEVICES

Ultra High Speed ECL Hybrid D/A Converter

HDS-1240E

FEATURES

12-Bit Settling Time to 40ns
Low Glitch Energy
ECL Compatible
Replacement for ADH-030, DA-4000, DAC397

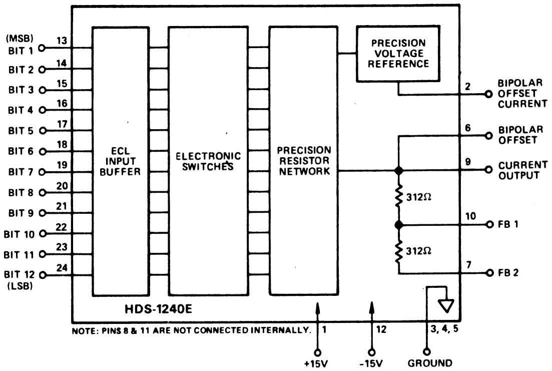
APPLICATIONS

Graphic Displays - Random Scan
Digital VCO's
Waveform Generation
ECM-EW Military
High-Speed ADC's

GENERAL

The HDS-1240E is a 12-bit high current output hybrid IC D/A converter which has an output settling time of 40ns. Its inputs are compatible with standard ECL (emitter coupled logic), and it features an actively trimmed resistor ladder network for high accuracy. The HDS-1240E can be operated in either the unipolar or bipolar mode by external pin interconnection. For voltage output applications, the feedback resistors required for use with an external op-amp are built-in to allow various voltage ranges without the need for external components. Additionally, the HDS-1240E features practically glitch-free operation without the need for external adjustments, and it operates on standard ±15 volt power supplies.

HDS-1240E FUNCTIONAL BLOCK DIAGRAM



PIN	FUNCTION	PIN	FUNCTION
1	+15 VOLTS	13	BIT 1 (MSB) INPUT
2	BIPOLAR OFFSET CURRENT	14	BIT 2 INPUT
3	GROUND	15	BIT 3 INPUT
4	GROUND	16	BIT 4 INPUT
5	GROUND	17	BIT 5 INPUT
6	BIPOLAR OFFSET	18	BIT 6 INPUT
7	FB 2	19	BIT 7 INPUT
8	N.C.	20	BIT 8 INPUT
9	OUTPUT	21	BIT 9 INPUT
10	FB 1	22	BIT 10 INPUT
11	N.C.	23	BIT 11 INPUT
12	-15 VOLTS	24	BIT 12 (LSB) INPUT

PIN DESIGNATIONS
HDS-1240E

SPECIFICATIONS (typical @ +25°C with nominal power supply voltages unless otherwise noted)

Model	Units	HDS-1240E
RESOLUTION FS = Full Scale	Bits	12
LSB WEIGHT	µA	3.9
ACCURACY (Relative to FS)		
Linearity	% FS	±0.0125 max
Differential Linearity	% FS	±0.0125 max
Gain	% FS	±0.05 max
Zero Offset - Unipolar	µA	1
Zero Offset - Bipolar	µA	4
Monotonicity		Guaranteed
TEMPERATURE COEFFICIENTS		
Linearity	ppm/°C	±3 typ; ±5 max
Differential Linearity	ppm/°C	±3 typ; ±5 max
Gain	ppm/°C	25
Zero Offset	ppm/°C	10
DATA INPUTS		
Logic Compatibility		
Logic "1"		
Voltage Range (Operating)	V	-0.81 to -0.96
Voltage Range (Absolute max)	V	0
Current	mA	10 max
Logic "0"		
Voltage Range (Operating)	V	-1.65 to -1.85
Voltage Range (Absolute min)	V	-6
Current	µA	1 max
Coding		Complementary Binary (CBN) for Unipolar; Complementary Offset Binary (COB) for Unipolar
OUTPUT		
Current - Unipolar	mA	0 to -16
Current - Bipolar	mA	±8
Compliance	V	+0.5V to -1.1V
Impedance	Ω	200
Capacitance	pF	25
SPEED PERFORMANCE		
Settling Time[1]		
For FS Input Change		
to 1% of FS	ns	20 typ; 30 max
to 0.1% of FS	ns	35 typ; 50 max
to 0.0125% of FS	ns	40 typ
For 1LSB Change from		
011...11 to 100...00 to 0.0125%	ns	30 typ; 35 max
Internal Skewing Time	ps	400 typ; 800 max
Output Time Constant	ps	3 into 100Ω load
Glitch Energy (with 100Ω Load)	pV-s	150
	mA-ns	2.5
POWER REQUIREMENTS		
Voltage - Operating	V	+15 ±10%: -15 ±10%
Voltage - Absolute Limit	V	+18, -18
Current	mA	20 typ; 30 max: 60 typ; 80 max
Rejection Ratio	%/V	0.02 max
TEMPERATURE RANGE (Case)		
Operating		
HDS-1240E	°C	0 to +70
HDS-1240EM, HDS-1240EMB	°C	-55 to +100
Storage	°C	-55 to +125
THERMAL RESISTANCE[2]		
Junction to Air, θja (free air)		
HDS-1240E	°C/W	65 max
HDS-1240EM, HDS-1240EMB	°C/W	65 max
Junction to Case, θjc	°C/W	7 max
MTBF[3]		
Mean Time Between Failure	hours	>1.356 X 10^6
PACKAGE OPTIONS[4]	HY24E (glass package) HY24G (metal package)	

NOTES:

[1] Measured with output loaded with 100Ω.

[2] Maximum junction temperature is 150°C.

[3] HDS-1240EMB calculated using MIL Handbook-217 Ground: Fixed Temperature Case = 60°C.

[4] See Section 20 for package outline information.

Specifications subject to change without notice.

APPLICATIONS

The HDS-1240E is a current output D/A converter which is input compatible with standard ECL (emitter coupled logic). Each digital input controls an internal switch, which through a precision binary weighted resistor network, sets the output current of the device. Starting with the most significant bit (MSB) and proceeding toward the least significant bit (LSB), each lesser bit controls one-half the current value of the preceeding bit. Therefore, the MSB (Bit 1) controls 8mA, Bit 2 controls 4mA, and so on until the LSB is reached which has a weight of 3.9μA. Thus, the output of the D/A varies from 0 with all digital inputs at a logic "1" state to -16mA with all inputs at a logic "0" state. This operating condition is called unipolar. For bipolar operation, an 8mA current source is provided. When this current source is connected to the output, it will then swing from -8mA to +8mA. See Figures 1 and 2 for this hook-up.

Transfer Characteristics

With the DAC hooked-up as shown in Figure 1, the output will be 0 to -16mA. Since the output compliance is +0.5V to -1.1V, care must be taken not to let the output voltage exceed these limits. The input/output relationships are shown in the table below.

Analog Output		Digital Input Code
Unipolar	**Bipolar**	
0	+FS	111...11
-1/2LSB	+FS -1LSB	111...10
-1/4FS	+1/2 FS	100...00
-1/2 FS +1LSB	+1LSB	100...00
-1/2FS	0	011...11
-1/2 FS -1LSB	-1LSB	011...10
-3/4 FS	-1/2LSB	001...11
-FS +1LSB	-FS -1LSB	000...00

Table 1. Coding Table

ANALOG OUTPUT

A. Normal Operation Without Amplification

The HDS-1240E is a current output D/A converter. However, the wide voltage compliance of +0.5V to -1.1V allows it to be used to generate an output voltage within this range which is proportional to the digital input code and the load impedance. When the DAC is operated in this mode the following formulae apply:

$$V_O = -0.016\ [R_t]$$

$$R_t = \frac{R_i \times R_L}{R_i - R_L} = \frac{200R_L}{200 - R_L}$$

Where: R_i = the internal resistance of the DAC (200Ω)
R_L = the external load resistance loading the DAC
R_t = the total resistance seen by the DAC output current, i.e., R_i in parallel with R_L.

In general, the output voltage of DAC is limited to 1V p-p. In this instance, from the above formulae, it can be determined that the maximum external load resistance will be about 90Ω. Since the bipolar offsetting provision is a true current source, this calculation does not differ even when the DAC is used in the bipolar mode. Full-scale gain may be adjusted by varying R_L (see Figure 4).

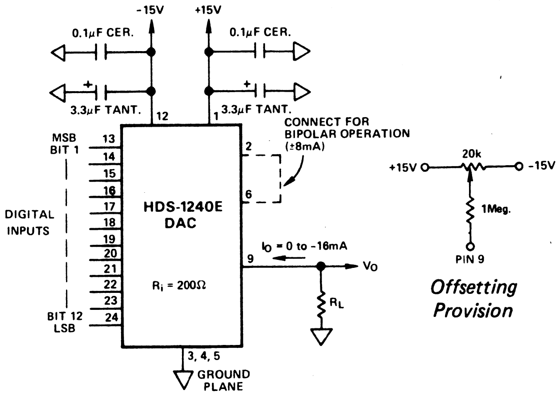


Figure 1. Current Output Operation

B. Operation with Voltage Amplification

There are certain applications that require more than the 1V p-p that is directly obtainable with the DAC output. In these circumstances, the use of an ultra-high speed operational amplifier is required. Figure 2 shows such an application utilizing the ADI Model HOS-050 op amp. The HDS-1240E DAC has built-in feedback resistors which are actively laser trimmed, and which eliminate the need for extra components. A variety of connections of these resistors allows various output voltages as shown in the table below. Care should be taken to keep all leads as short as possible, as the bandwidths encountered in these type circuits are quite high, and parasitics can be a very real problem. The power supply bypassing arrangement shown in Figure 1 should be used.

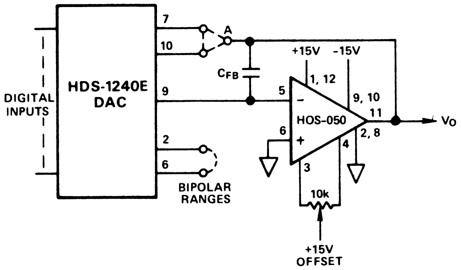


Figure 2. Voltage Output Operation

Voltage Range	Jumper Connections
±1.25V	7 to 9, 10 to A, 2 to 6
±2.5V	10 to A, 2 to 6
±5V	7 to A, 2 to 6
0 to +2.5V	7 to 9, 10 to A
0 to +5V	10 to A
0 to +10V	7 to A

Table 2. Output Voltage Connections

NOTE: The value of Cfb should be optimized for best settling time without overshoot. If absolute accuracy of gain is required, a large value of resistance can be introduced in parallel with Pins 7 and 9 of the DAC.

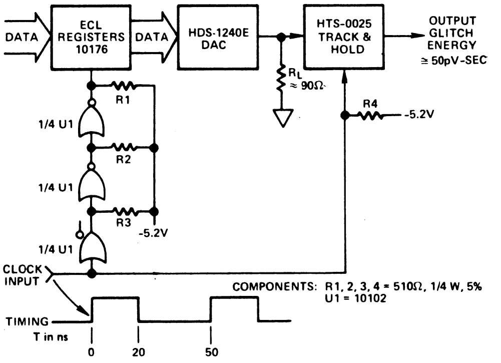
High-Speed Low-Glitch Operation Suggestions

The HDS-1240E D/A offers the highest available speed. However, with this speed performance, certain precautions and operating conditions should be considered. You are now in the RF world.

1. The D/A converter should be provided with a very low impedance grounding system to very high frequencies. A large ground plane is a must.
2. Low frequency bypassing should be provided with 1μF (or larger) tantalum capacitors mounted between the ±15V supply lines and ground near the D/A (see Figure 1).
3. High frequency bypassing should be provided by ceramic capacitors of 0.1μF or larger mounted within 0.25 inches of Pins 1 and 12 to ground (see Figure 1).
4. The D/A converter should be driven with ECL registers as physically close to the D/A as possible. The 10176 HEX "D" Master-slave flip-flop is recommended. The six most significant bits should come from the same package as shown in Figure 4. The six least significant bits should come from a second package.
5. Each digital input should be terminated with a 510Ω resistor connected between the input and -5.2V (see Figure 4).
6. If required, variable capacitors can be added to "deskew" the most significant bits for lowest glitch—although this is not usually required in many applications. These capacitors are added as shown in Figure 4 (C1-4), and are adjusted for minimum glitch energy.
7. Standard 24-pin sockets should be avoided. Individual "pin sockets" are most suited for evaluating devices, as lead inductance is reduced. In final designs, the D/A's should be soldered directly into the printed circuit board without sockets.

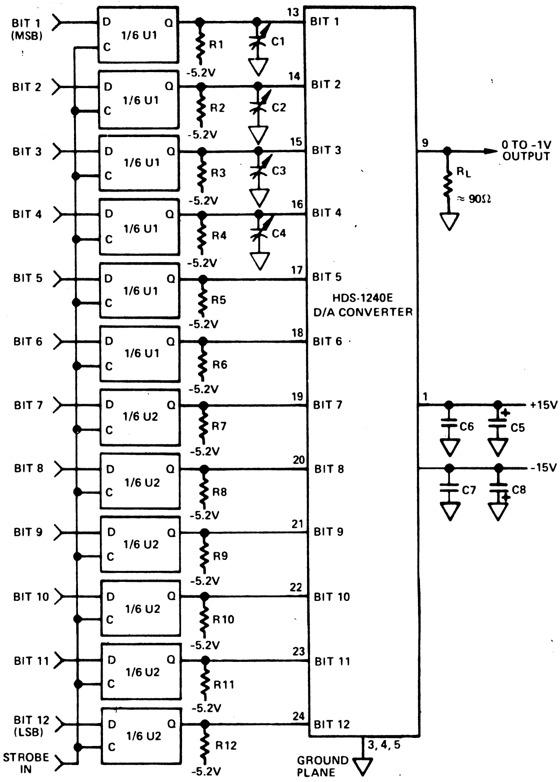
ULTRA-LOW GLITCH OPERATION

For extremely low glitch requirements (<50 - 100pV-s), an HTS-0025 Track-and-Hold is recommended as a deglitcher (see Figure 3). The duration of the HDS-1240E D/A glitch is approximately 10ns. The hold time of the HTS-0025 should be at least 15ns to "mask out" the glitch.



COMPONENTS: R1, 2, 3, 4 = 510Ω, 1/4 W, 5%
U1 = 10102

Figure 3. HTS-0025 Track & Hold Used with HDS-1240E D/A as Deglitcher @ 20MHz Update Rate



NOTES:
1. R1-1 = 510Ω, 1/4 W, 5%; R1 = OUTPUT LOAD; ADI P/N 79PR1K; C1 - ERIE 538-002F, 15-60pF, OR EQUIVALENT; C2, 3, 4 = ERIE 538-002D, 9-35pF, OR EQUIVALENT; C5, 8 = 3.3μF TANTALUM; C6, 7 = 0.1μF CERAMIC; U1, 2 = 10176, 10K ECL TYP "D" F-F.
2. THE FIRST SIX MOST SIGNIFICANT BITS (BITS 1-6) SHOULD ALWAYS BE ROUTED THROUGH ONE 10176 FOR CONSISTENCY IN TIMING AND REDUCED DATA SKEW.
3. R_L IS ADJUSTED FOR ABSOLUTE GAIN (FULL-SCALE) ACCURACY.

Figure 4. HDS-1240E – Typical Hook-Up and Test Circuit

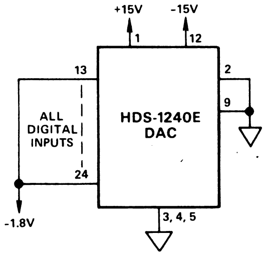


Figure 5. Recommended Burn-In Circuit

ORDERING INFORMATION

For commercial environment applications (0 to +70°C), order HDS-1240E. For extreme environment applications (-55°C to +100°C), order HDS-1240EM. For devices screened to MIL-STD-883, order HDS-1240EMB.

ANALOG
DEVICES

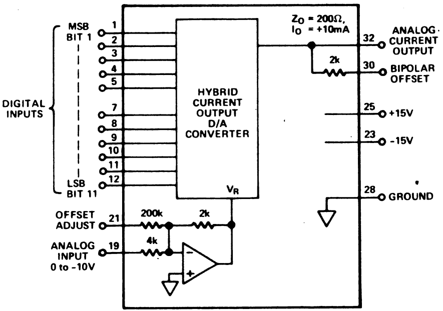
Ultra High Speed Multiplying D/A Converter

MDMS SERIES

FEATURES
- Small Size: 2" X 2" X 0.4"
- Highest Speed Available
- High Multiplying Accuracy: Maintains Monotonicity and Linearity for any Analog Input within the Specified Range
- High Current Output: 10mA Full Scale
- High Reliability, Hybrid Microcircuit Construction
- Guaranteed Operation: -30°C to +85°C

APPLICATIONS
- CRT Displays
- Waveform Generation
- Vector Generation
- Fast Digital Attenuator

MDMS SERIES FUNCTIONAL BLOCK DIAGRAM



BIPOLAR OPERATION IS ACCOMPLISHED BY CONNECTING PIN 30 to -10V, OR IF ADJUSTMENT IS REQUIRED, PIN 30 MAY BE CONNECTED THROUGH A 1.5k ADJUSTMENT POTENTIOMETER TO -15V.

GENERAL DESCRIPTION

The MDMS series is an ultra-high speed, one or two-quadrant, multiplying D/A converter capable of 10MHz operation and 11-bit precision. The settling time for both analog and digital inputs is 100ns, and the large signal bandwidth of the analog input is in excess of 10MHz. The module is designed for the needs of the graphic display field and other applications requiring high-accuracy, high-speed multiplying operation.

The current output of the MDMS series D/A is precisely proportional to the analog input signal multiplied by the digital input code. The analog input signal may be any voltage between 0V and -10V, and can be a sine wave, triangle wave, sawtooth, or other waveform. The D/A output is an accurate scaled version of the input waveform, the scale factor being the digital input code. Alternatively, the analog input voltage may be used to scale a digitally generated signal. Various offsetting provisions are made so that the analog signal, digital signal, and output may be made bipolar or unipolar in order to accommodate various uses requiring one or two-quadrant operation.

The output impedance of the D/A is 200 ohms so that a two-volt output swing is possible with no load. Loading the output with 200 ohms results in a 1 volt p-p output. If an external operational amplifier such as the Analog Devices' HOS-050 Op Amp is connected to the output of the D/A, output voltages up to 20V p-p are obtainable at a small sacrifice in speed.

ORDERING INFORMATION

Order Model Number MDMS-0801, MDMS-1001, or MDMS-1101. Ruggedized versions with extended burn-in are also available. Consult the factory.

This two-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be found in Volume II, page 10–37.

SPECIFICATIONS (typical @ +25°C and nominal power supply voltages unless otherwise noted)

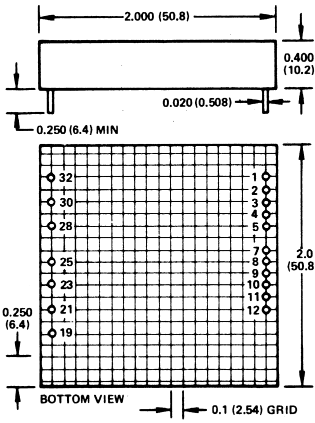
MODEL	MDMS-0801	MDMS-1001	MDMS-1101
RESOLUTION	8 Bits	10 Bits	11 Bits
LSB Weight	40μA	10μA	5μA
ACCURACY (ADJUSTABLE TO)	±0.2%	±0.05%	±0.025%
Monotonicity	Guaranteed	*	*
Linearity	20μA, ±1/2LSB	5μA, ±1/2LSB	2.5μA, ±1/2LSB
ANALOG INPUT			
Voltage Range	0 to -10V	*	*
Impedance	4kΩ ±2%	*	*
Transfer Function (inverting)	0V input scales D/A output to minimum output; -10V input scales D/A output to maximum output.		
DIGITAL INPUT (TTL)			
Positive Logic, "1" =	+2.4V to +5.0V	*	*
"0" =	0V to 0.4V	*	*
Loading, 2 Std. TTL Loads			
"0" =	-5mA	*	*
"1" =	50μA	*	*
CODING (PARALLEL INPUT DATA)			
Unipolar	BIN	*	*
Bipolar	OBN	*	*
All "1's" Input		Maximum Positive Output	
All "0's" Input		Maximum Negative Output	
OUTPUT (CURRENT)			
Unipolar	0 to +10mA	*	*
Bipolar	±5mA	*	*
Compliance Voltage	+1.5V, -2V	*	*
Impedance	200Ω, ±1%	*	*
Loading		200Ω for 0 to 1V p-p Out 0Ω for 0 to 2V p-p Out	
Zero Offset (max)	50nA	*	*
DYNAMIC CHARACTERISTICS			
Settling Time (digital & analog)	90ns to 0.2% F.S.	100ns to 0.1% F.S.	130ns to 0.05% F.S.
Bandwidth (analog in)	10MHz	*	*
TEMPERATURE COEFFICIENTS			
Linearity	2ppm/°C	*	*
Monotonicity		Guaranteed -30°C to +85°C	
POWER REQUIREMENTS			
+15V ±10%	60mA	*	*
-15V ±10%	20mA	*	*
Power Supply Rejection Ratio	0.005%/V	*	*
TEMPERATURE RANGE			
Operating		-30°C to +85°C	
Storage		-55°C to +125°C	
PHYSICAL CHARACTERISTICS			
Case		Diallyl Phthalate per MIL-M-14 Type SDG-F	

*Specifications same as MDMS-0801

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



NOTE: DOT ON TOP INDICATES POSITION OF PIN 1

WEIGHT: 1.6 OZ, 45.3 G

PINS ARE GOLD PLATED PER MIL-G-5204 TYPE II

MATING SOCKET MSA-1

PIN DESIGNATIONS

PIN	FUNCTION
1	BIT 1 INPUT (MSB)
2	BIT 2 INPUT
3	BIT 3 INPUT
4	BIT 4 INPUT
5	BIT 5 INPUT
7	BIT 6 INPUT
8	BIT 7 INPUT
9	BIT 8 INPUT
10	BIT 9 INPUT
11	BIT 10 INPUT
12	BIT 11 INPUT LSB
19	ANALOG INPUT
21	OFFSET ADJ
23	-15V POWER INPUT
25	+15V POWER INPUT
28	GROUND
30	BIPOLAR OFFSET
32	ANALOG OUTPUT

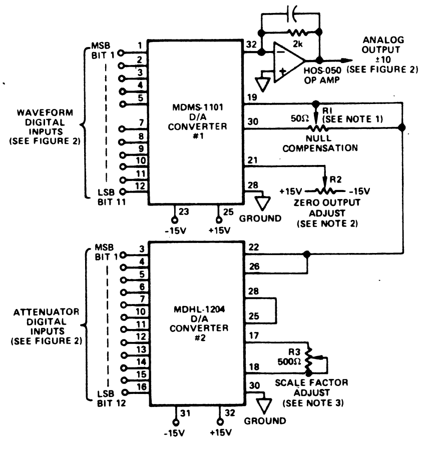
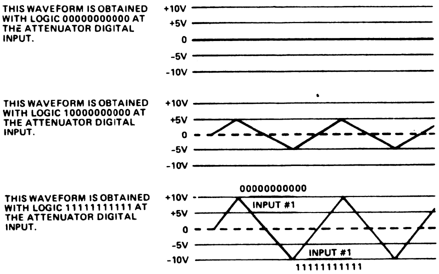

MSB BIT 1
1
2
3
4
5
7
8
9
10
11
12
LSB BIT 11
WAVEFORM DIGITAL INPUTS (SEE FIGURE 2)
MDMS-1101 D/A CONVERTER #1
32
2k
ANALOG OUTPUT ±10 (SEE FIGURE 2)
HOS-050 OP AMP
19
30
50Ω
R1 (SEE NOTE 1)
NULL COMPENSATION
21
R2
28
+15V
-15V
ZERO OUTPUT ADJUST (SEE NOTE 2)
23
25
-15V
+15V
GROUND
MSB BIT 1
3
4
5
6
7
10
11
12
13
14
15
16
LSB BIT 12
ATTENUATOR DIGITAL INPUTS (SEE FIGURE 2)
MDHL-1204 D/A CONVERTER #2
22
26
28
25
17
R3 500Ω
18
SCALE FACTOR ADJUST (SEE NOTE 3)
30
31
32
-15V
+15V
GROUND

Figure 1. The MDMS-1101 Multiplying D/A Used as a Digital Waveform Generator with Digital Attenuator Control



NOTES
1. R1 MAY BE OMITTED IF 0.5% DC SHIFT IS PERMISSIBLE BETWEEN MINIMUM & MAXIMUM ATTENUATION.
2. ADJUST R2 FOR 0V OUTPUT WITH ATTENUATOR INPUT SET FOR 00000000000 AND WAVEFORM INPUT ACTIVE.
3. ADJUST R3 TO OBTAIN ±10V OUTPUT WITH ATTENUATOR INPUT SET FOR 11111111111 AND WAVEFORM INPUT ACTIVE.

THE ABOVE WAVEFORMS DEPICT THE ANALOG OUTPUT FOR VARIOUS VALUES OF ATTENUATOR DIGITAL INPUTS TO D/A #2 WITH A DIGITAL TRIANGLE BEING APPLIED TO THE WAVEFORM DIGITAL INPUT OF D/A #1.

PEAK POSITIVE LEVEL = 00000000000 DIGITAL INPUT
PEAK NEGATIVE LEVEL = 11111111111 DIGITAL INPUT

(THE OUTPUT OP AMP INVERTS THE SENSE OF THE INPUT BITS)

Figure 2. Operation of Multiplying D/A Circuit

Analog-to-Digital Converters

Contents

	Page
Selection Guide	11-3
Factors in Choosing an A/D Converter	11-4
Specifications & Terms	11-6
AD570 Low-Cost Complete Monolithic IC 8-Bit ADCs	11-11
AD571 Complete Monolithic IC 10-Bit ADCs	11-15
AD572 Complete Hybrid IC 12-Bit Successive-Approximation ADCs	11-23
•AD573J/K/S Fast, Complete 10-Bit A/D Converter with Microprocessor Interface	11-31
•AD574A/AJ/AK/AL Fast Complete 12-Bit A/D Converter with Microprocessor Interface	11-39
AD578 Fast Complete Hybrid IC 12-Bit ADCs	11-47
•AD579JN/KN/BD/TD Very Fast, Complete 10-Bit A/D Converter	11-53
•AD673J/S Fast, Complete, 8-Bit A/D Converter with Microprocessor Interface	11-59
AD5200 Hybrid IC 12-Bit Successive-Approximation ADCs	11-63
•AD5210 Series 12-Bit Successive-Approximation High-Accuracy A/D Converter	11-67
•AD5240KD/SD Very Fast, Complete 12-Bit A/D Converter	11-73
AD7550 CMOS IC Quad-Slope Bus-Compatible 13-Bit ADC	11-81
•AD7552 CMOS 12-Bit Plus Sign Monolithic A/D Converter	11-89
AD7555 CMOS IC 4 1/2 Digit 20,000-Count ADC Subsystem	11-101
AD7574 CMOS Microprocessor-Compatible 8-Bit ADCs	11-113
•AD7581 CMOS μP Compatible 8-Bit 8-Channel DAS	11-121
AD ADC80 Hybrid IC 10- and 12-Bit ADCs with Improved Performance and Reliability	11-129
•AD ADC84/85C Fast, Complete 12-Bit A/D Converter	11-137
ADC1130/ADC1131 14-Bit High-Speed A/D Converter	11-145
•ADC1140 Low Cost 16-Bit Analog-to-Digital Converter	11-147
HAS Hybrid 8-, 10-, and 12-Bit Ultra-Fast ADCs	11-149
MAH Ultra-High-Speed 8- and 10-Bit A/D Converter	11-153
MAS Ultra-High-Speed 8-, 10- and 12-Bit A/D Converter	11-155
MATV Video 8-Bit ADCs with Built-In Track-Hold	11-157
MOD-1005 10-Bit 5MHz Video ADC with Built-In Track-Hold	11-159
MOD-1020 10-Bit 20MHz Video ADC with Built-In Track-Hold	11-161
MOD-1205 12-Bit 5MHz Video ADC with Built-In Track-Hold	11-163

•New product since the *1980 Data-Acquisition Components and Subsystems Catalog.*

Selection Guide
Analog-to-Digital Converters

HIGH PERFORMANCE/HIGH RESOLUTION FEATURE SELECTION CHART

		GENERAL PURPOSE				µP BUS COMPATIBLE		MULTI-CHAN	HIGH PERFORMANCE				µP BUS COMPATIBLE			HIGH RESOLUTION	
		AD570	AD571	AD ADC80	AD673	AD573	AD7574	AD7581	AD5200	AD5210	AD572	AD574A	AD7550	AD7552	AD7555	ADC1130/ ADC1131	ADC1140
Resolution	8 Bits	●			●		●	●									
	10 Bits		●			●											
	12 Bits			●					●	●	●	●					
	13 Bits												●	●			
	14 Bits															●	
	16 Bits																●
	4 1/2 Digits														●		
	5 1/2 Digits														●		
Conversion Time	1800ms														●		
	50ms												●	●			
	66.6µs/ch							●									
	50µs								●								●
	25µs	●	●	●	●	●					●	●				●	
	15µs						●			●						●	
Internal Reference		●	●	●	●	●			●	●	●	●				●	●
Ratiometric Capability							●	●	●	●			●	●	●		
Low Power							●	●					●	●	●		
Second Source				●					●	●							
Logic Compatibility	TTL	●	●	●	●	●		●	●	●	●	●	●	●		●	●
	CMOS		●				●	●					●	●	●		
Operating Temperature Ranges	C = 0 to +70°C	●	●		●	●	●	●				●			●	●	●
	I = -25°C to +85°C			●			●	●	●	●	●		●	●	●		●
	M = -55°C to +125°C	●	●		●	●	●		●	●	●	●					
Dice Availability		●	●			●											
Volume I Page		11-11	11-15	11-129	11-59	11-31	11-113	11-121	11-63	11-67	11-23	11-39	11-81	11-89	11-101	11-145	11-147
Volume II Page		–	–	–	–	–	–	–	–	–	–	–	–	–	–	11-11	11-15

HIGH/SPEED VIDEO FEATURE SELECTION CHART

		HIGH SPEED										VIDEO					
		AD579	AD578	AD ADC84/85[1]	AD5240[1]	HAS-0802	HAS-1002	HAS-1202	MAH-0801	MAH-1001	MAS-1202	MATV-0811[2]	MATV-0816[2]	MATV-0820	MOD-1005[2]	MOD-1020[2]	MOD-1205[2]
Resolution	8 Bits					●			●			●	●	●			
	10 Bits	●		●			●			●					●	●	
	12 Bits		●	●	●			●			●						●
Conversion Time	≤8µs		●	●	●	●	●		●	●	●						
	≤3µs	●	●			●	●	●	●	●	●						
	≤1.1µs								●	●							
Word Rate	≥5MHz											●			●		●
	≥16MHz												●	●		●	
Internal Reference		●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●
Logic Compatibility	TTL	●	●	●	●	●	●	●	●	●	●	●	●	●	●		●
	ECL															●	
Operating Temperature Ranges	C = 0 to +70°C	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●
	I = -25°C to +85°C			●		●	●	●									
	M = -55°C to +125°C	●	●	●	●												
Volume I Page		11-53	11-47	11-137	11-73	11-149	11-149	11-149	11-153	11-153	11-155	11-157	11-157	11-157	11-159	11-161	11-163
Volume II Page		–	–	–	–	–	–	–	11-19	11-19	11-23	11-27	11-27	11-27	11-31	11-35	11-39

[1] Second Source
[2] Complete with Track and Hold.

Orientation
Analog-to-Digital Converters

FACTORS IN CHOOSING AN A/D CONVERTER

In the two volumes of this catalog, there are listed some 27 different families of analog-to-digital converters (ADCs). If one were to consider all the variations, there would be considerably more than 50 different types to choose among. The reason for so many different types is the number of degrees of freedom in selection—technological, functional, performance, and package. Complete information on converters may be found in the 246-page book, *Analog-Digital Conversion Notes*, published by Analog Devices and available for $5.95 from P.O. Box 796, Norwood, MA 02062.

FUNCTIONAL CHARACTERISTICS

Block diagrams illustrating the various conversion techniques appear on individual data sheets.

The moderate-speed converters described in this catalog (<1MHz) employ two fundamental techniques—*successive approximations*, for moderate-to-high resolution at moderate-to-high speed, and *integration*, for high resolution at modest speeds. The AD ADC80 and ADC1131 are examples of the former, the AD7550 and AD7583, the latter.

Like a chemist's balance with binary weights (1/2, 1/4, 1/8, etc.), the *successive-approximation* converter compares the unknown input with sums of accurately-known binary fractions of full scale, starting with the largest (2^{-1}), and rejecting any that change the comparator's state ("tip the scale"). At the end of conversion (EOC), the output of the converter is a digital word, representing the ratio of the input to full scale by a fractional-binary code.

Integrating types count pulses for a period proportional to the input. Most-frequently used are *dual slope* types, which count off the period required for the integral of the reference to become equal to the average value of the input (over a fixed period). Integrating types can be made insensitive to drift by storing errors during an error-correcting cycle and subtracting them during the input-measuring cycle. This correction can be performed in analog fashion, using capacitance for storage, or digitally—using the information stored in a counter for correction (AD7550).

The video converters described here (MATV, MOD-1205, etc.) employ two basic encoding techniques: simultaneous, or *flash* conversion, and serial-Gray-Code conversion. High resolution and high speed are obtained by *subranging*, i.e., by performing an n-bit conversion in two steps; Analog Devices has perfected a form of subranging, known as DSC—*digitally corrected subranging*—which permits accurate resolutions of 12 bits and more.*

In *flash* conversion, the analog signal is compared against $2^n - 1$ graded voltage levels, using as many comparators, and the comparator output logic levels are processed by a priority encoder, which converts the "thermometer" output to a binary (or Gray) code. Since the whole conversion occurs essentially simultaneously, it is the fastest means of conversion, but it requires many accurate comparators and large numbers of gates.

In *serial*-analog-parallel-digital conversion, there are a number of cascaded stages, each having a gain of +2 for signals less than one-half the reference, and a gain of −2 for signals between one-half the reference and full scale. At each stage, a decision is made as to whether the signal is larger (1) or smaller (0) than one-half the reference; the stage's analog output becomes the input to the next stage. The complete time for one conversion is determined by the propagation delay of the analog signal through all stages; however, since the decision of each stage can be latched as soon as the stage has settled (and a new conversion can, in principle, be started as soon as the first bit has been latched), the rate at which conversions come out of the pipeline is considerably faster than the time for one sample to go through the conversion process. Though fast, this process is difficult to implement accurately for more than a few bits, because of the compounding of gain (hence errors).

A *subranging* converter digitizes to a group of more-significant bits, and stores them in a latch. A fast, very-high-accuracy D/A converter converts them to an analog signal, which is then subtracted from the input. The difference, or residue, is amplified and digitized, and (in DCS) the result is combined digitally in such a way as to correct for mid-scale conversion errors.

Whatever the technique, these A/D converters comprise several essential functions: an analog section, a digital data-generating section, data outputs, and digital controls.

Analog Section

This section requires a reference, one or more high-gain comparators, and either a D/A converter (successive approximations) or a controllable integrator. The reference may be internal or external, fixed or variable, and of a specified polarity/sense in relation to the analog input. In ratiometric conversion, the reference is usually external and variable.

In successive-approximation converters the comparator is generally used in the *current-summing* mode; that is, the current output of the DAC is summed with the current developed in the DAC's "feedback resistor" by the input voltage (of opposite polarity), and the balancing action of the converter tends to bring the summing junction towards a voltage null (much like that of an op amp) at the end of conversion. The typical DAC feedback options, when applied in an ADC, provide input-scaling choices. When the bipolar-offset connection is jumpered to the summing point, input signals of both polarities can be handled. The current-switching action of the DAC, at the typically fast clock-rates used in successive-approximation converters, can disturb the output of the analog signal source, especially if it is a slow high-precision op amp. In such cases, buffering may be necessary.

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*A considerable amount of useful information about the differences between video conversion and moderate-speed conversion can be found in the article "Very High Speed Data Acquisition," by Ed Graves, in *Analog Dialogue* 13-2, available upon request.

In integrating types, absolute-value and polarity-sensing circuitry may be required at the front end to handle both polarities of input. Outputs are usually sign-magnitude BCD. However, the AD7550, which uses an offset-reference scheme, requires none of the above; and it has a two's-complement binary output. The AD7555 provides the quadslope control logic, counters, and analog switching, but require external integrators and comparators.

Digital Data-Generating Section

In successive-approximation types, this section consists of a discrete or integrated successive-approximations register (SAR), its controls, and inputs from the comparator and clock (which is on-board, but in many cases permits external clock pulses, frequency adjustment, and/or control). In integrating types, this section consists of the clock-pulse generator, the counter(s), the input from the comparator, and the associated controls. Often, provisions are made for the pulse-train to be jumpered to the counter externally, so that the pulse train can be operated on externally, or can transmit its train of pulses to a remote counter. In a few types there are no on-board counters or registers; the pulse train, magnitude, overrange, and control terminals are intended to communicate with external counters and registers.

Data Outputs

Factors to consider here include coding, resolution, overrange information, levels, format, validity, and timing. *Coding* is usually binary, including jumper-connected offset-binary and/or two's complement for bipolar input signals. For some types, BCD is available, with sign-magnitude for bipolar inputs. Output coding specs should always be checked for digital polarity (positive- or negative-true) of both magnitude and sign information. The *resolution* (number of output bits) must be sufficient for the application; in addition, the specifications must be checked to ascertain that not only will all 2^n (binary) output codes be present (no missing codes), but they must all be present at any temperature in the operating range and related to the input with sufficient accuracy. Integrating types generally have no problems with missing codes (except sometimes at zero, with sign-magnitude coding); nevertheless, nonlinear integration can cause the conversion relationship to become nonlinear. Successive-approximation types have no way of determining *overrange;* they simply fill up. However, counter types roll over and put out a carry flag to signal overrange

The *data levels* available at the converter output must be checked (TTL, low-voltage CMOS, high-voltage CMOS, ECL), as must the load-driving capability and fanout, and the supply conditions under which appropriate output levels will be furnished. The available choice of output *formats* must also be as desired—parallel, serial, byte-serial, and/or pulse-train. If the converter is intended to communicate directly with an 8-bit data bus, the output should have three-state capability, and parallel outputs must be enabled in bytes of 8 or fewer lines (AD573, AD574A). If the output is serial, it is usually NRZ (non-return-to-zero) and should be accompanied by a set of synchronized clock-pulses.

A *status* (or *busy* or *EOC*) output changes state to indicate when the data becomes *valid.* The exact nature of this transition should be specified—polarity, timing, levels, etc. For serial data, the exact relationship between the data and the synchronizing clock should be specified, to indicate when each bit becomes valid, and for how long. In general, the *timing* of the whole conversion process must be clearly understood, especially if high speeds are necessary, either for conversion, or for communication with a processor (or both). The timing diagrams on specification sheets are usually accompanied by adequate descriptions of the conversion process and specifications of the critical interface parameters.

Controls

The functions, action (levels or edges), polarity, and timing of all control inputs and outputs should be clearly understood, as well as their loading characteristics and dependence on the supply. In addition to the essential *start-conversion-command* input and a *status* output, various control commands may be available, such as *clock inhibit, high (low)-byte enable, status enable*, and—for speeding up conversion at the cost of resolution in successive-approximation converters—*short-cycle.*

Power Supplies

Appropriate power supplies should be made available, considering the logic levels and analog input signals to be employed in the system. The appropriate degree of power-supply stability to meet the accuracy specifications should be provided. Any recommended external protection circuitry should be planned for. In many cases, separate analog and digital grounds are required; ground wiring should follow best practice to minimize digital interference with high-accuracy analog signals, while ensuring that a connection between grounds can always exist at one point, even if the "mecca" point is inadvertently unplugged from the system.

Application Checklist

The designer will generally require specific information in the following categories, before proceeding to the selection process:

- Accurate description of input and output
    1. analog signal range and source or load impedance
    2. digital code needed – binary, offset binary, 2's complement, BCD, etc.
    3. logic level system, i.e., TTL/DTL compatible
- What is the needed data throughput rate?
- What are the control interface details?
- What does the system error budget allow for the converter?
- What are environmental conditions – temperature range, time, supply voltage – over which the converter should operate to the desired accuracy?

For A/D converters, the following considerations are typical.

- What is the analog input voltage range, and to what resolution must the signal be measured?

- What is the requirement for linearity error (or relative accuracy error)?
- To what extent must the various sources of error be minimized as environmental temperature changes?
- How much time can be allowed in the system for each complete conversion? What aperture uncertainty and acquisition time are needed for the sample-hold?
- How stable is the system power supply? What errors will result from power supply terminal voltage variations of this order?
- Can the system tolerate missed codes under any conditions?
- What is the character of the input signal? Is it noisy, sampled, filtered, rapidly-varying, slowly-varying? What kind of pre-processing is to be (or can be) done that will affect the choice (and cost) of the converter? Is aliasing a potential problem?

SPECIFICATIONS & TERMS

Definitions of performance specifications, and related information, are to be found on the following pages, in alphabetical order.*

Accuracy, Absolute

The error of an A/D converter at a given output code is the difference between the theoretical and the actual analog input voltages required to produce that code. Since the code can be produced by any analog voltage in a finite band (see Quantizing Uncertainty), the "input required to produce that code" is defined as the midpoint of the band of inputs that will produce the code. For example, if 5 volts (±1.2mV) will theoretically produce a 12-bit half-scale code of 100000000000, then a converter for which any voltage from 4.997V to 4.999V will produce that code will have absolute error of
$1/2(4.997 + 4.999) - 5 \text{ volts} = -2\text{mV}$.

Absolute error comprises gain error, zero error, and nonlinearity, together with noise, Absolute-accuracy measurements should be made under a set of standard conditions with sources and meters traceable to an internationally accepted standard.

Accuracy, Relative

Relative accuracy error, expressed in %, ppm, or fractions of an LSB, is the deviation of the analog value at any code (relative to the full analog range of the device transfer characteristic) from its theoretical value (relative to the same range), after the full-scale range (FSR) has been calibrated.

Since the discrete points on the theoretical transfer characteristic lie on a straight line, this deviation can also be interpreted as a measure of nonlinearity (see Linearity).

The "discrete points" of an A/D transfer characteristic are the midpoints of the quantization bands at each code (see Accuracy, Absolute).

Aperture Time

This is the interval between the application of the *hold* command to a sample/track-hold and the actual opening of the switch. The aperture time consists of a delay (which depends on the logic and the switching device—50ns for SHA1144) and an uncertainty (due to jitter—20ps max rms for HTS-0025). When a sample-hold is used in an application where timing is critical, the timing of the hold command can be advanced to compensate for the known component of aperture delay. The jitter, however, imposes the ultimate limitation on timing accuracy. When a sample-hold is used with an ADC, the timing uncertainty of the conversion process is reduced by the ratio of aperture jitter to the conversion time, i.e., the maximum frequency which can be handled with less than 1LSB error due to timing is $2^{-n}/(\pi\,\tau_{au})$ instead of $2^{-n}/(\pi\,\tau_c)$, where τ_{au} is the aperture uncertainty and τ_c is the conversion time.

Common Mode Rejection (CMR)

The ability of a device to reject the effect of voltage applied to both input terminals simultaneously. Usually expressed as the log of a "common-mode rejection ratio," e.g., 1,000,000:1 (CMRR) or 120dB (CMR). A CMRR of 1,000,000 to 1 means that a 1V common-mode voltage passes through the amplifier as through it were a differential signal of one microvolt at the input.

Conversion Time and Conversion Rate

The time required for a complete measurement by an ADC is called *conversion time*. For most converters (assuming no significant additional systemic delays), this is identical to the inverse of *conversion rate*. However, in some high-speed converters, because of pipelining, new conversions are initiated before the results of prior conversions have been determined; thus, for example, the MOD-1205 can provide 12-bit output data at a 5MHz word rate (200ns/conversion), even though the time for any one conversion, from start to finish, is two clock periods plus 275ns, or 675ns, at 5MHz.

Dual-Slope Converter

An integrating analog-to-digital converter in which the unknown signal is converted to a proportional time interval, which is then measured digitally. This is done by integrating the unknown for a predetermined time. Then a reference input is switched to the integrator, and integrates "down" from the level determined by the unknown until a "zero" level is reached. The time for the second integration process is proportional to the average of the unknown signal level over the predetermined integrating period. A digital time-interval meter (i.e., counter) is generally used as the output indicator.

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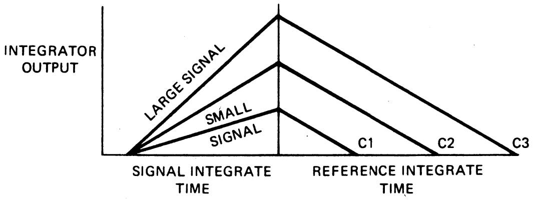
*For video converters, there are a number of additional application-oriented specifications pertaining to the device's use in a system (e.g., *noise power ratio, differential phase, differential gain, signal-to-noise ratio*). Some useful references for understanding such specifications can be found in the following publications, available from Analog Devices, Computer Labs Division, 505 Edwardia Drive, Greensboro, NC 27409.

Kester, W. A., "PCM Signal Codecs for Video Applications", *SMPTE Journal*, Volume 88, November 1979, pp 770-778.

Pratt, W. J., "Test A/D Converters Digitally", *Electronic Design*, December 6, 1975

Smith, B.F. and Pratt, W.J., "Understanding High-Speed A/D Converter Specifications", Computer Labs, 1974



Feedthrough

Undesirable signal-coupling around switches or other devices that are supposed to be turned off or provide isolation, e.g., *feedthrough error* in a multiplexer. It is variously specified in %, ppm, fractions of 1 LSB, or fractions of 1 volt, with a given set of inputs, at a specified frequency.

"Flash" Converter

A converter in which all the bit choices are made at the same time. It requires $2^n - 1$ voltage-divider taps and comparators, and a comparable amount of priority encoding logic. An extremely fast scheme, it requires large numbers of precision components. Flash converters are often used for partial conversions in *subranging converters*.

Gain Adjustment

The "gain" of a converter is that analog scale factor setting that provides the nominal conversion relationship, e.g., 10V full scale, in a fixed-reference converter, or 100% of full-scale in a ratiometric converter. Gain- and zero-adjustment principles are discussed under *zero*.

Least Significant Bit (LSB)

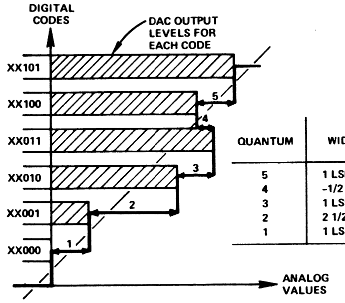
In a system in which a numerical magnitude is represented by a series of binary (i.e., two-valued) digits, the "least significant bit" is that digit (or "bit") that carries the smallest value or weight. For example, in the natural binary number 1101 (decimal 13, or $2^3 + 2^2 + 0 + 2^0$), the rightmost "1" is the LSB. Its analog weight, relative to full scale, is 2^{-n}, where n is the number of binary digits. It represents the smallest change that can be resolved by an n-bit converter.

Linearity Error

Linearity error of a converter, expressed in percent or parts-per-million of full-scale range, or fractions of a least-significant bit, is the deviation of the analog values from a straight line, in a plot of the measured conversion relationship. The straight line can be either a "best straight line," determined empirically by manipulation of the gain and/or offset to equalize maximum positive and negative deviations of the actual transfer characteristic from this straight line; or, it can be a straight line passing through the end points of the transfer characteristic after they have been calibrated. Sometimes referred to as "end-point" nonlinearity, the latter is both a more conservative measure and is much easier to verify in actual practice. "End-point" nonlinearity is similar to relative accuracy error (see Accuracy, Relative). Linearity has two components—*differential* and *integral* nonlinearity.

Linearity, Differential and Integral

A digital output code should correspond to a quantum of analog input values exactly 1 LSB in width (2^{-n} of full scale, for an n-bit converter). Any deviation of the measured "step" from the ideal width is called Differential Nonlinearity. It is an important specification, because a differential nonlinearity error greater than 1 LSB can lead to nonmonotonic behavior of of a D/A converter, and missed codes in an A/D converter employing such a DAC. A flagrant example of differential nonlinearity is shown here.



QUANTUM	WIDTH	DIFFERENTIAL LINEARITY ERROR
5	1 LSB	0
4	-1/2 LSB	-1 1/2 LSB
3	1 LSB	0
2	2 1/2 LSB	+1 1/2 LSB
1	1 LSB	0

In the illustration, the horizontal bars represent the measured DAC output values corresponding to 6 adjacent digital codes. The DAC is nonlinear, in that the next-least-significant bit (XX010) is 1½ LSB too large. Thus, instead of the five quanta, or steps, being all equal (= 1 LSB), quantum 2 is 2½ LSB and quantum 4 is –½ LSB. The differential linearity error, the difference between the actual quantum width and the ideal 1 LSB, is +1½ LSB for quantum 2 and –1½ LSB for quantum 4.

When this DAC is used in successive-approximations conversion, it will lead to a missed code. Analog inputs slightly larger than the value of XX100 will be converted to XX100, and analog inputs slightly less than the value of XX100 will be converted to XX010. The code XX011 will not exist; it will be a *missed code*.

Often, instead of a maximum differential nonlinearity specification, there will be a simple specification of "no missed codes", which implies a differential nonlinearity less than 1 LSB.

While differential nonlinearity deals with errors in step size, *integral nonlinearity* has to do with deviations of the overall shape of the conversion response. Even converters that are not subject to differential linearity errors (e.g., integrating types) have integral linearity (sometimes just "linearity") errors.

Power-Supply Sensitivity

The sensitivity of a converter to dc changes in power-supply voltages is normally expressed in terms of percentage change in analog input value (or fractions of the analog equivalent of 1 LSB), corresponding to a given code, for a 1% dc change in the power supply, e.g., 0.05%/%ΔV_S). Power-supply sensitivity may also be expressed in relation to a specified dc shift of the supply voltage. High-accuracy ADCs intended for battery operation require excellent rejection of large supply-variations.

Quad-Slope Converter
This is an integrating analog-to-digital converter that goes through two cycles of *dual-slope* conversion, once with zero input and once with the analog input being measured. The errors determined during the first cycle are subtracted digitally from the result in the second cycle. The scheme results in an extremely accurate converter. For example, the 13-bit single-chip AD7550 is a CMOS quad-slope A/D converter with typical tempcos (gain and zero temperature coefficients) of 1ppm/°C.

Quantizing Uncertainty (or "Error")
The analog continuum is partitioned into 2^n discrete ranges for n-bit conversion. All analog values within a given range are represented by the same digital code, usually assigned to the nominal midrange value. There is, therefore, an inherent quantization uncertainty of ±½ LSB, in addition to the actual conversion errors. In integrating converters, this "error" is often expressed as "±1 count."

Ratiometric Converter
The output of an A/D converter is a digital number proportional to the ratio of (some measure of) the input to a reference. Most requirements for conversions call for an absolute measurement, i.e., against a fixed reference. In some cases, where the measurement is affected by a changing reference voltage (e.g., the voltage applied to a bridge), it is advantageous to use that same reference as the reference for the conversion, to eliminate the effect of variation. Ratiometric conversion can also serve as a substitute for analog signal division (where the denominator changes but little during the conversion).

Stability
Stability of a converter, usually applies to the insensitivity of its characteristics with time, temperature, etc. All measurements of stability are difficult and time consuming, but stability vs. temperature is sufficiently critical in most applications to warrant universal inclusion in tables of specifications (see "Temperature Coefficients").

Subranging Converters
In this type of converter, an extremely fast conversion produces the most-significant portion of the output word. This portion is converted back to analog with a fast high-accuracy D/A converter and subtracted from the input. The resulting residue is converted to digital at high speed and combined with the results of the earlier conversion to form the output word. In *digitally corrected subranging* (DCS), the two bytes are combined in a manner that corrects for the error of the LSB of the most-significant byte. For example, using 8-bit and 5-bit conversion, and this proprietary technique, a full-accuracy high-speed 12-bit converter can be built.

Successive Approximations
Successive approximations is a high speed method of comparing an unknown against a group of weighted references. The operation of a successive approximations A/D converter is generally similar to the orderly weighing of an unknown quantity on a precision chemical balance, using a set of weights such as: 1 gram, 1/2 gram, 1/4 gram, 1/8 gram, 1/16 gram, etc. The weights are tried in order, starting with the largest. Any weight that tips the scale is removed. At the end of the process, the sum of the weights remaining on the scale will be within one LSB of the actual weight (±½ LSB, if the scale is properly biased – see *zero*).

Temperature Coefficients
In general, temperature instabilities are expressed in %/°C, ppm/°C, as fractions of 1 LSB/°C, or as a change in a parameter over a specified temperature range. Measurements are usually made at room temperature and at the extremes of the specified range, and the temperature coefficient (tempco, T.C.) is defined as the change in the parameter, divided by the corresponding temperature change. Parameters of interest include *gain, linearity, offset* (bipolar), and *zero*. The last three are expressed in % or ppm of full-scale range per Celsius degree.

Gain Tempco: Two factors principally affect converter gain instability with temperature:

a) In fixed-reference converters, the reference source will vary with temperature. For example, the tempco of an AD581L is typically 5ppm/°C.

b) The ratiometric circuitry has a sensitivity to temperature.

Linearity Tempco: Sensitivity of linearity to temperature over the specified range. To avoid missed codes, it is sufficient that the differential nonlinearity error be less than 1 LSB at any temperature in the range of interest. The *differential nonlinearity temperature coefficient* may be expressed as a ratio, as a maximum change over a specified temperature range, and/or implied by a statement that there are no missed codes when operating within a specified temperature range.

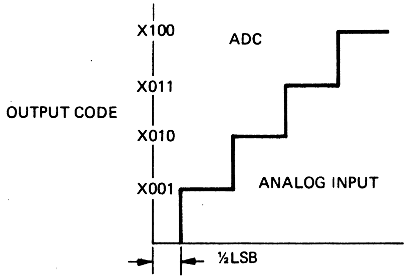
Offset Tempco The temperature coefficient of the all-DAC-switches-off (minus full-scale) point, of a bipolar successive-approximations converter, is dependent on three variables:

1) The tempco of the reference source
2) The voltage stability of the input buffer and the comparator
3) The tracking capability of the bipolar-offset resistors and the gain resistors.

Unipolar Zero The zero tempco of an ADC is dependent only on the zero stability of the integrator and/or the input buffer and the comparator. It may be expressed in μV/°C, or in percent or ppm of full-scale per degree C.

Zero- and Gain-Adjustment Principles

The zero adjustment of a unipolar ADC is set so that the transition from all-bits-off to LSB-on occurs at $\frac{1}{2} \times 2^{-n}$ of nominal full-scale. The gain is set for the final transition to all-bits-on to occur at F.S. (1 - $\frac{3}{2} \times 2^{-n}$). The "zero" of an offset-binary bipolar ADC is set so that the first transition occurs at -F.S. (1 - 2^{-n}) and the last transition at +F.S. (1 − 3 x 2^{-n}). The data sheet instructions should be followed.



ANALOG DEVICES

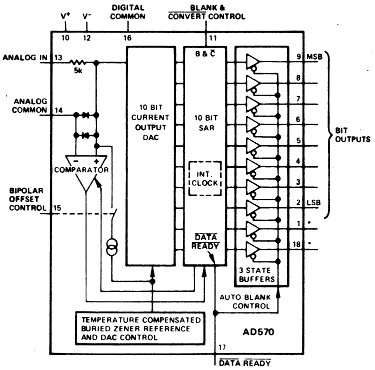
Low Cost, Complete IC 8-Bit A to D Converter

AD570*

FEATURES

Complete A/D Converter with Reference and Clock
Fast Successive Approximation Conversion – 25µs
No Missing Codes Over Temperature
0 to +70°C – AD570J
-55°C to +125°C – AD570S
Digital Multiplexing – 3 State Outputs
18-Pin DIP
Low Cost Monolithic Construction

AD570 FUNCTIONAL BLOCK DIAGRAM



18-PIN DUAL IN LINE PACKAGE

PRODUCT DESCRIPTION

The AD570 is an 8-bit successive approximation A/D converter consisting of a DAC, voltage reference, clock, comparator, successive approximation register and output buffers – all fabricated on a single chip. No external components are required to perform a full accuracy 8-bit conversion in 25µs.

The AD570 incorporates the most advanced integrated circuit design and processing technology available today. I^2L (integrated injection logic) processing in the fabrication of the SAR function along with laser trimming of the high stability SiCr thin film resistor ladder network at the wafer stage (LWT) and a temperature compensated, subsurface Zener reference insures full 8-bit accuracy at low cost.

Operating on supplies of +5V and -15V, the AD570 will accept analog inputs of 0 to +10V unipolar or ±5V bipolar, externally selectable. As the BLANK and $\overline{\text{CONVERT}}$ input is driven low, the three state outputs will be open and a conversion will commence. Upon completion of the conversion, the $\overline{\text{DATA READY}}$ line will go low and the data will appear at the output. Pulling the BLANK and $\overline{\text{CONVERT}}$ input high blanks the outputs and readies the device for the next conversion. The AD570 executes a true 8-bit conversion with no missing codes in approximately 25µs.

The AD570 is available in two versions; the AD570J is specified for the 0 to 70°C temperature range, the AD570S for -55°C to +125°C. Both guarantee full 8-bit accuracy and no missing codes over their respective temperature ranges. The AD570J is also offered in an 18-pin plastic DIP.

PRODUCT HIGHLIGHTS

1. The AD570 is a complete 8-bit A/D converter. No external components are required to perform a conversion. Full scale calibration accuracy of ±0.8% (2LSB of 8 bits) is achieved without external trims.
2. The AD570 is a single chip device employing the most advanced IC processing techniques. Thus, the user has at his disposal a truly precision component with the reliability and low cost inherent in monolithic construction.
3. The AD570 accepts either unipolar (0 to +10V) or bipolar (-5V to +5V) analog inputs by simply grounding or opening a single pin.
4. The device offers true 8-bit accuracy and exhibits no missing codes over its entire operating temperature range.
5. Operation is guaranteed with -15V and +5V supplies. The device will also operate with a -12V supply.
6. The AD570S is also available with processing to MIL-STD-883, Class B. The single chip construction and functional completeness make the AD570 especially attractive for high reliability applications.

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*Protected by Patent Nos. 3940760, 4213806 and 4136349.

SPECIFICATIONS

(typical @ +25°C with V+ = +5V, V- = -15V, all voltages measured with respect to digital common, unless otherwise indicated)

MODEL	AD570J	AD570S[1]
RESOLUTION[2]	8 Bits	*
RELATIVE ACCURACY @ 25°C[2,3,4]	±1/2LSB max	*
T_{min} to T_{max}	±1/2LSB max	*
FULL SCALE CALIBRATION[4,5] (With 15Ω Resistor In Series With Analog Input	±2LSB (typ)	*
UNIPOLAR OFFSET (max)[4]	±1/2LSB	*
BIPOLAR OFFSET (max)[4]	±1/2LSB	*
DIFFERENTIAL NONLINEARITY (Resolution for Which no Missing Codes are Guaranteed)		
+25°C	8 Bits	*
T_{min} to T_{max}	8 Bits	*
TEMPERATURE RANGE	0 to +70°C	-55°C to +125°C
TEMPERATURE COEFFICIENTS[4]		
Guaranteed max Change		
T_{min} to T_{max}		
Unipolar Offset	±1LSB (88ppm/°C)	±1LSB (40ppm/°C)
Bipolar Offset	±1LSB (88ppm/°C)	±1LSB (40ppm/°C)
Full Scale Calibration[6] (With 15Ω Fixed Resistor or 200Ω Trimmer)	±2LSB (176ppm/°C)	±2LSB (80ppm/°C)
POWER SUPPLY REJECTION[4]		
Max Change In Full Scale Calibration		
TTL Positive Supply		
$+4.5V \leqslant V+ \leqslant +5.5V$	±2LSB max	*
Negative Supply		
$-16.0V \leqslant V- \leqslant -13.5V$	±2LSB max	*
ANALOG INPUT RESISTANCE	3kΩ min	*
	5kΩ typ	*
	7kΩ max	*
ANALOG INPUT RANGES		
(Analog Input to Analog Common)		
Unipolar	0 to +10V	*
Bipolar	-5V to +5V	*
OUTPUT CODING		
Unipolar	Positive True Binary	*
Bipolar	Positive True Offset Binary	*
LOGIC OUTPUT		
Bit Outputs and $\overline{\text{Data Ready}}$		
Output Sink Current	3.2mA min	*
(V_{OUT} = 0.4V max, T_{min} to T_{max})	(2TTL Loads)	*
Output Source Current (Bit Outputs)[7]		
(V_{OUT} = 2.4V min, T_{min} to T_{max})	0.5mA min	*
Output Leakage When Blanked	±40μA max	*
LOGIC INPUT		
Blank and Convert Input		
$0 \leqslant V_{in} \leqslant V+$	±40μA max	*
Blank – Logic "1"	2.0V min	*
Convert – Logic "0"	0.8V max	*
CONVERSION TIME	15μs min	*
	25μs typ	*
	40μs max	*

ALL MODELS	
POWER SUPPLY	
Absolute Maximum	
V+	+7V
V-	-16.5V
Specified Operating – Rated Performance	
V+	+5V
V-	-15V
Operating Range	
V+	+4.5V to +5.5V
V-	-12.0V to -16.5V
Operating Current	
Blank Mode	
V+ = +5V	2mA typ (10mA max)
V- = -15V	9mA typ (15mA max)
Convert Mode	
V+ = +5V	5mA
V- = -15V	10mA

*Specifications same as AD570J

Specifications subject to change without notice.

NOTES

[1] The AD570S is available processed and screened to the requirements of MIL-STD-883B, Class B. When ordering, specify the AD570SD/883B.

[2] The AD570 is a selected version of the AD571 10-bit A to D converter. As such, some devices may exhibit 9 or 10 bits of relative accuracy or resolution, but that is neither tested nor guaranteed. Only TTL logic inputs should be connected to pins 1 and 18 (or no connection made) or damage may result.

[3] Relative accuracy is defined as the deviation of the code transition points from the ideal transfer point on a straight line from the zero to the full scale of the device.

[4] Specifications given in LSB's refer to the weight of a least significant bit at the 8-bit level, which is 0.39% of full-scale.

[5] Full scale calibration is guaranteed trimmable to zero with an external 200Ω potentiometer in place of the 15Ω fixed resistor. Full scale is defined as 10 volts minus 1 LSB, or 9.961 volts.

[6] Full Scale Calibration Temperature Coefficient includes effects of unipolar offset drift as well as gain drift.

[7] The Data output lines have active pull-ups to source 0.5mA. The $\overline{\text{DATA READY}}$ line is open collector with a nominal 6kΩ internal pull-up resistor.

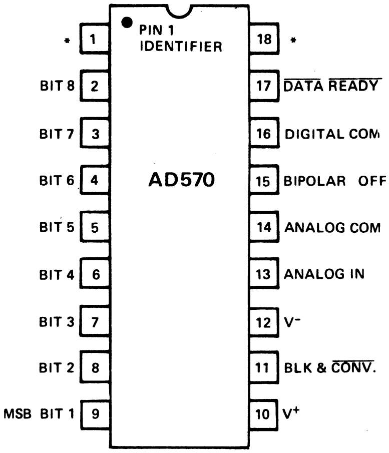
ABSOLUTE MAXIMUM RATINGS

V+ to Digital Common	0 to +7V
V- to Digital Common	0 to -16.5V
Analog Common to Digital Common	±1V
Analog Input to Analog Common	±15V
Control Inputs	0 to V+
Digital Outputs (Blank Mode)	0 to V+
Power Dissipation	800mW

AD570 ORDERING GUIDE

Model	Package Number[1]	Temperature Range
AD570JN	18-Pin Plastic DIP (N18A)[2]	0 to +70°C
AD570JD	18-Pin Ceramic DIP (D28A)	0 to +70°C
AD570SD	18-Pin Ceramic DIP (D18A)	-55°C to +125°C
AD570SD/883B	18-Pin Ceramic DIP (D18A)	-55°C to +125°C

[1] See Section 20 for package outline information.
[2] To be available June 1982.



*SEE NOTE 2, SPEC TABLE

Figure 1. AD570 Pin Connections

CONNECTING THE AD570 FOR STANDARD OPERATION

The AD570 contains all the active components required to perform a complete A/D conversion. Thus, for most situations, all that is necessary is connection of the power supply (+5 and -15), the analog input, and the conversion start pulse. But, there are some features and special connections which should be considered for achieving optimum performance. The functional pin-out is shown in Figure 1.

FULL SCALE CALIBRATION

The 5kΩ thin film input resistor is laser trimmed to produce a current which matches the full scale current of the internal DAC—plus about 0.3%—when a full scale analog input voltage of 9.961 volts (10 volts – 1LSB) is applied at the input. The input resistor is trimmed in this way so that if a fine trimming potentiometer is inserted in series with the input signal, the input current at the full scale input voltage can be trimmed down to match the DAC full scale current as precisely as desired. However, for many applications the nominal 9.961 volt full scale can be achieved to sufficient accuracy by simply inserting a 15Ω resistor in series with the analog input to pin 14. Typical full scale calibration error will then be about ±2LSB or ±0.8%. If a more precise calibration is desired a 200Ω trimmer should be used instead. Set the analog input at 9.961 volts, and set the trimmer so that the output code is just at the transition between 11111110 and 11111111. Each LSB will then have a weight of 39.06mV. If a nominal full scale of 10.24 volts is desired (which makes the LSB have weight of exactly 40.00mV), a 50Ω resistor in series with a 200Ω trimmer (or a 500Ω trimmer with good resolution) should be used. Of course, larger full scale ranges can be arranged by using a larger input resistor, but linearity and full scale temperature coefficient may be compromised if the external resistor becomes a sizeable percentage of 5kΩ.

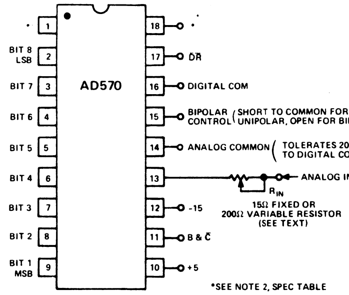

AD570
1 •
BIT 8 LSB 2
BIT 7 3
BIT 6 4
BIT 5 5
BIT 4 6
BIT 3 7
BIT 2 8
BIT 1 MSB 9
18 •
17 DR
16 DIGITAL COM
15 BIPOLAR CONTROL (SHORT TO COMMON FOR UNIPOLAR, OPEN FOR BIPOLAR)
14 ANALOG COMMON (TOLERATES 200mV TO DIGITAL COMMON)
13
ANALOG IN
R_IN
15Ω FIXED OR 200Ω VARIABLE RESISTOR (SEE TEXT)
12 -15
11 B & C
10 +5
•SEE NOTE 2, SPEC TABLE

Figure 2. Standard AD570 Connections

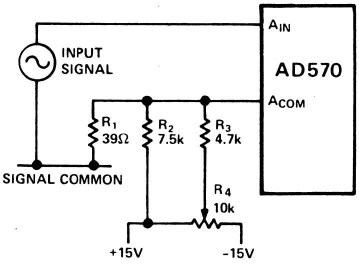
BIPOLAR OPERATION

The standard unipolar 0 to +10V range is obtained by shorting the bipolar offset control pin to digital common. If the pin is left open, the bipolar offset current will be switched into the comparator summing node, giving a -5V to +5V range with an offset binary output code. (-5.00 volts in will give a 8-bit code of 00000000; an input of 0.00 volts results in an output code of 10000000 and 4.96 volts at the input yields the 11111111 code.)

ZERO OFFSET

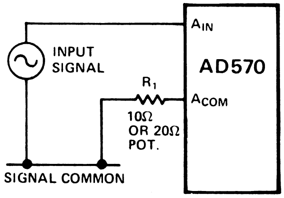
The apparent zero point of the AD570 can be adjusted by inserting an offset voltage between the Analog Common of the device and the actual signal return or signal common. Figure 3 illustrates two methods of providing this offset. Figure 3A shows how the converter zero may be offset by up to ±3 bits to correct the device initial offset and/or input signal offsets. As shown, the circuit gives approximately symmetrical adjustment in unipolar mode. In bipolar mode R2 should be omitted to obtain a symmetrical range.

Figure 3B shows how to offset the zero code by 1/2LSB to provide a code transition between the nominal bit weights.



ZERO OFFSET ADJ
±3 BIT RANGE

Figure 3A.



½ BIT ZERO OFFSET

Figure 3B.

CONTROL AND TIMING OF THE AD570

There are several important timing and control features on the AD570 which must be understood precisely to allow optimal interfacing to microprocessor or other types of control systems. All of these features are shown in the timing diagram in Figure 4.

The normal stand-by situation is shown at the left end of the drawing. The BLANK and $\overline{\text{CONVERT}}$ (B & $\overline{\text{C}}$) line is held high, the output lines will be "open", and the $\overline{\text{DATA READY}}$ ($\overline{\text{DR}}$) line will be high. This mode is the lowest power state of the device (typically 150mW). When the (B & $\overline{\text{C}}$) line is brought low, the conversion cycle is initiated; but the $\overline{\text{DR}}$ and Data lines do not change state. When the conversion cycle is complete (typically 25μs), the $\overline{\text{DR}}$ line goes low, and within 500ns, the Data lines become active with the new data.

About 1.5μs after the B & $\overline{\text{C}}$ line is again brought high, the $\overline{\text{DR}}$ line will go high and the Data lines will go open. When the B & $\overline{\text{C}}$ line is again brought low, a new conversion will begin. The minimum pulse width for the B & $\overline{\text{C}}$ line to blank previous data and start a new conversion is 2μs. If the B & $\overline{\text{C}}$ line is brought high during a conversion, the conversion will stop, and the $\overline{\text{DR}}$ and Data lines will not change. If a 2μs or longer pulse is applied to the B & $\overline{\text{C}}$ line during a conversion, the converter will clear and start a new conversion cycle.

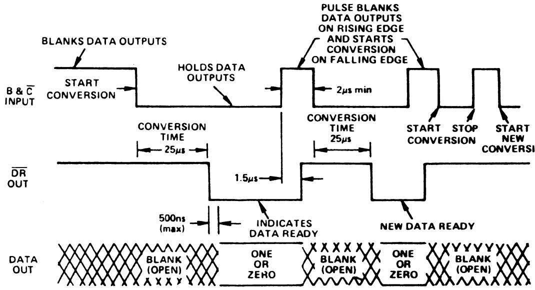


Figure 4. AD570 Timing and Control Sequence

ANALOG DEVICES

Integrated Circuit 10-Bit Analog to Digital Converter

AD571*

FEATURES

Complete A/D Converter with Reference and Clock
Fast Successive Approximation Conversion – 25μs
No Missing Codes Over Temperature
  0 to +70°C – AD571K
  -55°C to +125°C – AD571S
  Digital Multiplexing – 3 State Outputs
18-Pin Ceramic DIP
Low Cost Monolithic Construction

PRODUCT DESCRIPTION

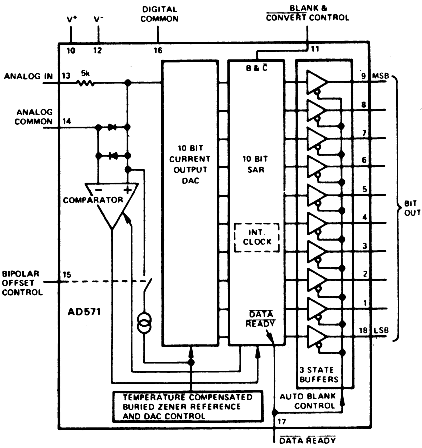
The AD571 is a 10-bit successive approximation A/D converter consisting of a DAC, voltage reference, clock, comparator, successive approximation register and output buffers – all fabricated on a single chip. No external components are required to perform a full accuracy 10-bit conversion in 25μs.

The AD571 incorporates the most advanced integrated circuit design and processing technology available today. It is the first complete converter to employ I^2L (integrated injection logic) processing in the fabrication of the SAR function. Laser trimming of the high stability SiCr thin film resistor ladder network at the wafer stage (LWT) insures high accuracy, which is maintained with a temperature compensated, subsurface Zener reference.

Operating on supplies of +5V to +15V and -15V, the AD571 will accept analog inputs of 0 to +10V, unipolar or ±5V bipolar, externally selectable. As the BLANK and $\overline{\text{CONVERT}}$ input is driven low, the three state outputs will be open and a conversion will commence. Upon completion of the conversion, the $\overline{\text{DATA READY}}$ line will go low and the data will appear at the output. Pulling the BLANK and $\overline{\text{CONVERT}}$ input high blanks the outputs and readies the device for the next conversion. The AD571 executes a true 10-bit conversion with no missing codes in approximately 25μs.

The AD571 is available in two versions for the 0 to +70°C temperature range, the AD571J and K. The AD571S guarantees 10-bit accuracy and no missing codes from -55°C to +125°C.

AD571 FUNCTIONAL BLOCK DIAGRAM



18-PIN DIP

PRODUCT HIGHLIGHTS

1. The AD571 is a complete 10-bit A/D converter. No external components are required to perform a conversion. Full scale calibration accuracy of ±0.3% is achieved without external trims.
2. The AD571 is a single chip device employing the most advanced IC processing techniques. Thus, the user has at his disposal a truly precision component with the reliability and low cost inherent in monolithic construction.
3. The AD571 accepts either unipolar (0 to +10V) or bipolar (-5V to +5V) analog inputs by simply grounding or opening a single pin.
4. The device offers true 10-bit accuracy and exhibits no missing codes over its entire operating temperature range.
5. Operation is guaranteed with -15V and +5V to +15V supplies. The device will also operate with a -12V supply.
6. The AD571S is also available with processing to MIL-STD-883, Class B. The single chip construction and functional completeness make the AD571 especially attractive for high reliability applications.

***Covered by Patent Nos. 3,940,760; 4,213,806; 4,136,349.**

SPECIFICATIONS

(typical @ +25°C with V+ = +5V, V− = −15V, all voltages measured with respect to digital common, unless otherwise indicated)

MODEL	AD571J	AD571K	AD571SD/AD571SD-883[1]
RESOLUTION	10 Bits	*	*
RELATIVE ACCURACY @ 25°C[2]	±1LSB max	±1/2LSB max	±1LSB max
T_{min} to T_{max}	±1LSB max	±1/2LSB max	±1LSB max
FULL SCALE CALIBRATION[3] (With 15Ω Resistor In Series With Analog Input	±2LSB (typ)	*	*
UNIPOLAR OFFSET (max)	±1LSB	±1/2LSB	*
BIPOLAR OFFSET (max)	±1LSB	±1/2LSB	*
DIFFERENTIAL NONLINEARITY (Resolution for Which no Missing Codes are Guaranteed)			
+25°C	10 Bits	*	*
T_{min} to T_{max}	9 Bits	10 Bits	10 Bits
TEMPERATURE RANGE	0 to +70°C	*	−55°C to +125°C
TEMPERATURE COEFFICIENTS			
Guaranteed max Change			
T_{min} to T_{max}			
Unipolar Offset	±2LSB (44ppm/°C)	±1LSB (22ppm/°C)	±2LSB (20ppm/°C)
Bipolar Offset	±2LSB (44ppm/°C)	±1LSB (22ppm/°C)	±2LSB (20ppm/°C)
Full Scale Calibration (With 15Ω Fixed Resistor or 50Ω Trimmer)	±4LSB (88ppm/°C)	±2LSB (44ppm/°C)	±5LSB (50ppm/°C)
POWER SUPPLY REJECTION			
Max Change In Full Scale Calibration			
CMOS Positive Supply (K only) $+13.5 \leq V+ \leq +16.0V$	N.A.	±1LSB max	N.A.
TTL Positive Supply $+4.5V \leq V+ \leq +5.5V$	±2LSB max	±1LSB max	*
Negative Supply $-16.0V \leq V- \leq -13.5V$	±2LSB max	±1LSB max	*
ANALOG INPUT RESISTANCE	3kΩ min	*	*
	5kΩ typ	*	*
	7kΩ max	*	*
ANALOG INPUT RANGES (Analog Input to Analog Common)			
Unipolar	0 to +10V	*	*
Bipolar	−5V to +5V	*	*
OUTPUT CODING			
Unipolar	Positive True Binary	*	*
Bipolar	Positive True Offset Binary	*	*
LOGIC OUTPUT[4]			
Bit Outputs and $\overline{\text{Data}}$ $\overline{\text{Ready}}$			
Output Sink Current	3.2mA min	*	*
(V_{OUT} = 0.4V max, T_{min} to T_{max})	(2TTL Loads)	*	*
Output Source Current (Bit Outputs)[5] (V_{OUT} = 2.4V min, T_{min} to T_{max})	0.5mA min	*	*
Output Leakage When Blanked	±40μA max	*	*
LOGIC INPUT			
Blank and Convert Input			
$0 \leq V_{in} \leq V+$	±40μA max	*	*
Blank – Logic "1"	2.0V min	*	*
Convert – Logic "0"	0.8V max	*	*
CONVERSION TIME	15μs min	*	*
	25μs typ	*	*
	40μs max	*	*

MODEL	AD571J	AD571K	AD571SD/AD571SD-883[1]
POWER SUPPLY			
Absolute Maximum			
V+	+7V	+16.5V	*
V-	-16.5V	*	*
Specified Operating – Rated Performance			
V+	+5V	+5V to +15V	*
V-	-15V	*	*
Operating Range			
V+	+4.5V to +5.5V	+4.5V to +16.5V	*
V-	-12.0V to -16.5V	*	*
Operating Current			
Blank Mode			
V+ = +5V	2mA typ (10mA max)	*	*
V+ = +15V	5mA typ (10mA max)	*	*
V- = -15V	9mA typ (15mA max)	*	*
Convert Mode			
V+ = +5V	5mA	*	*
V+ = +15V	10mA	*	*
V- = -15V	10mA	*	*
PACKAGE OPTIONS[6]			
D18A	AD571JD	AD571KD	AD571SD
N18A[7]	AD571JN	AD571KN	

*Specifications same as AD571J
**Specifications same as AD571K
Specifications subject to change without notice.

NOTES
[1] The AD517S is available processed and screened to the requirements of MIL-STD-883, Class B. When ordering, specify the AD571SD/883B.
[2] Relative accuracy is defined as the deviation of the code transition points from the ideal transfer point on a straight line from the zero to the full scale of the device.
[3] Full scale calibration is guaranteed trimmable to zero with an external 50Ω potentiometer in place of the 15Ω fixed resistor. Full scale is defined as 10 volts minus 1LSB, or 9.990 volts.
[4] Logic Input and Output Thresholds and Levels are a function of V+. They are guaranteed TTL compatible at V+ = +5V, CMOS compatible at V+ = 15V for the AD571K.
[5] The data output lines have active pull-ups to source 0.5mA. The $\overline{\text{DATA READY}}$ line is open collector with a nominal 6kΩ internal pull-up resistor.
[6] See Section 20 for package outline information.
[7] To be available June, 1982.

ABSOLUTE MAXIMUM RATINGS

V+ to Digital Common AD571J, S	0 to +7V
AD571K	0 to +16.5V
V- to Digital Common	0 to -16.5V
Analog Common to Digital Common	±1V
Analog Input to Analog Common	±15V
Control Inputs	0 to V+
Digital Outputs (Blank Mode)	0 to V+
Power Dissipation	800mW

CIRCUIT DESCRIPTION

The AD571 is a complete 10-bit A/D converter which requires no external components to provide the complete successive-approximation analog-to-digital conversion function. A block diagram of the AD571 is shown in Figure 1. Upon receipt of the $\overline{\text{CONVERT}}$ command, the internal 10-bit current output DAC is sequenced by the I^2L successive-approximation register (SAR) from its most-significant bit (MSB) to least-significant bit (LSB) to provide an output current which accurately balances the input signal current through the 5kΩ input resistor. The comparator determines whether the addition of each successively-weighted bit current causes the DAC current sum to be greater or less than the input current; if the sum is less the bit is left on, if more, the bit is turned off. After testing all the bits, the SAR contains a 10-bit binary code which accurately represents the input signal to within ±½LSB (0.05%).

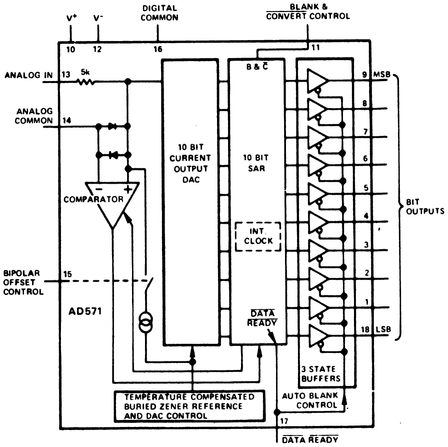


Figure 1. AD571 Functional Block Diagram

Upon completion of the sequence, the SAR sends out a $\overline{\text{DATA READY}}$ signal (active low), which also brings the three-state buffers out of their "open" state, making the bit output lines become active high or low, depending on the code in the SAR. When the BLANK and $\overline{\text{CONVERT}}$ line is brought high, the output buffers again go "open", and the SAR is prepared for another conversion cycle. Details of the timing are given further.

The temperature compensated buried Zener reference provides the primary voltage reference to the DAC and guarantees excellent stability with both time and temperature. The bipolar offset input controls a switch which allows the positive bipolar offset current (exactly equal to the value of the MSB less ½LSB) to be injected into the summing (+) node of the comparator to offset the DAC output. Thus the nominal 0 to +10V unipolar input range becomes a -5V to +5V range. The 5kΩ thin film input resistor is trimmed so that with a full scale input signal, an input current will be generated which exactly matches the DAC output with all bits on. (The input resistor is trimmed slightly low to facilitate user trimming, as discussed on the next page.)

POWER SUPPLY SELECTION

The AD571 is designed for optimum performance using a +5V and -15V supply, for which the AD571J and AD571S are specified. AD571K will also operate with up to a +15V supply, which allows direct interface to CMOS logic. The input logic threshold is a function of V+ as shown in Figure 2. The supply current drawn by the device is a function of both V+ and the operating mode (BLANK or CONVERT). These supply current variations are shown in Figure 3. The supply currents change only moderately over temperature as shown in Figure 7.

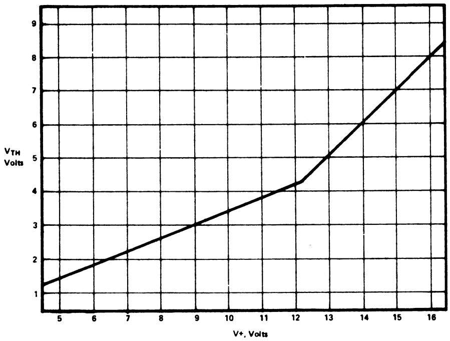


Figure 2. Logic Threshold (AD571K Only)

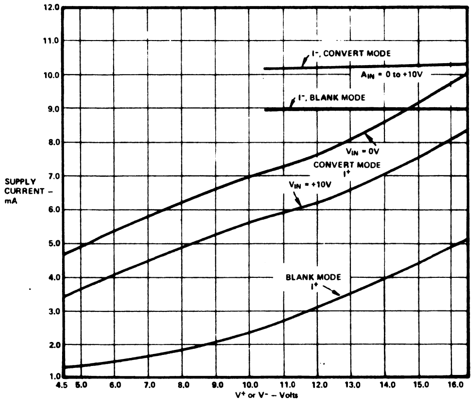


Figure 3. Supply Currents vs. Supply Levels and Operating Modes

CONNECTING THE AD571 FOR STANDARD OPERATION

The AD571 contains all the active components required to perform a complete A/D conversion. Thus, for most situations, all that is necessary is connection of the power supply (+5 and −15), the analog input, and the conversion start pulse. But, there are some features and special connections which should be considered for achieving optimum performance. The functional pin-out is shown in Figure 4.

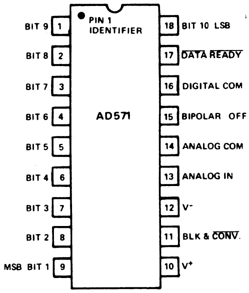


Figure 4. AD571 Pin Connections

FULL SCALE CALIBRATION

The 5kΩ thin film input resistor is laser trimmed to produce a current which matches the full scale current of the internal DAC—plus about 0.3%—when a full scale analog input voltage of 9.990 volts (10 volts − 1LSB) is applied at the input. The input resistor is trimmed in this way so that if a fine trimming potentiometer is inserted in series with the input signal, the input current at the full scale input voltage can be trimmed down to match the DAC full scale current as precisely as desired. However, for many applications the nominal 9.99 volt full scale can be achieved to sufficient accuracy by simply inserting a 15Ω resistor in series with the analog input to pin 13. Typical full scale calibration error will then be about ±2LSB or ±0.2%. If the more precise calibration is desired, a 50Ω trimmer should be used instead. Set the analog input at 9.990 volts, and set the trimmer so that the output code is just at the transition between 1111111110 and 1111111111. Each LSB will then have a weight of 9.766mV. If a nominal full scale of 10.24 volts is desired (which makes the LSB have weight of exactly 10.00mV), a 100Ω resistor in series with a 100Ω trimmer (or a 200Ω trimmer with good resolution) should be used. Of course, larger full scale ranges can be arranged by using a larger input resistor, but linearity and full scale temperature coefficient may be compromised if the external resistor becomes a sizeable percentage of 5kΩ.

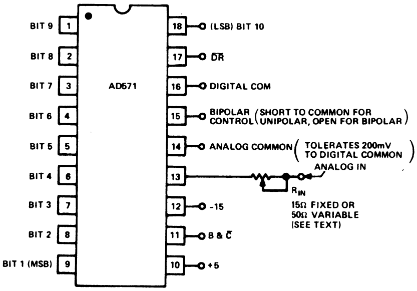

BIT 9 1
18 (LSB) BIT 10
BIT 8 2
17 DR
BIT 7 3
AD571
16 DIGITAL COM
BIT 6 4
15 BIPOLAR CONTROL (SHORT TO COMMON FOR UNIPOLAR, OPEN FOR BIPOLAR)
BIT 5 5
14 ANALOG COMMON (TOLERATES 200mV TO DIGITAL COMMON)
BIT 4 6
13
ANALOG IN
R_IN
15Ω FIXED OR 50Ω VARIABLE (SEE TEXT)
BIT 3 7
12 -15
BIT 2 8
11 B & C
BIT 1 (MSB) 9
10 +5

Figure 5. Standard AD571 Connections

BIPOLAR OPERATION

The standard unipolar 0 to +10V range is obtained by shorting the bipolar offset control pin to digital common. If the pin is left open, the bipolar offset current will be switched into the comparator summing node, giving a −5V to +5V range with an offset binary output code. (−5.00 volts in will give a 10-bit code of 0000000000; an input of 0.00 volts results in an output code of 1000000000 and 4.99 volts at the input yeilds the 1111111111 code). The bipolar offset control input is not directly TTL compatible, but a TTL interface for logic control can be constructed as shown in Figure 6.

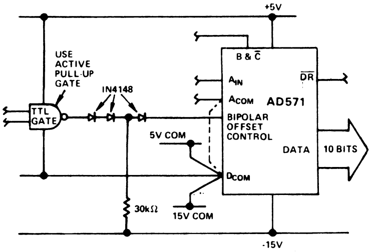


Figure 6. Bipolar Offset Controlled by Logic Gate

Gate Output = 1   Unipolar 0 - 10V Input Range
Gate Output = 0   Bipolar ±5V Input Range

COMMON MODE RANGE

The AD571 provides separate Analog and Digital Common connections. The circuit will operate properly with as much as ±200mV of common mode range between the two commons. This permits more flexible control of system common bussing and digital and analog returns.

In normal operation the Analog Common terminal may generate transient currents of up to 2mA during a conversion. In addition, a static current of about 2mA will flow into Analog Common in the unipolar mode after a conversion is complete. An additional 1mA will flow in during a blank interval with zero analog input. The Analog Common current will be modulated by the variations in input signal.

The absolute maximum voltage rating between the two commons is ±1 volt. We recommend the connection of a parallel pair of back-to-back protection diodes between the commons if they are not connected locally.

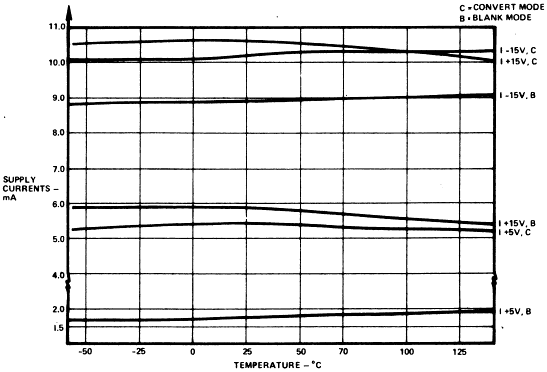
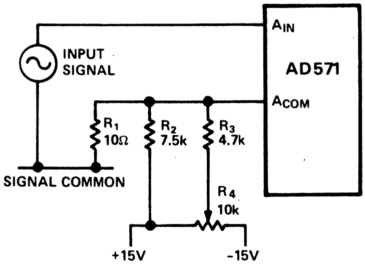


Figure 7. AD571 Power Supply Current vs. Temperature

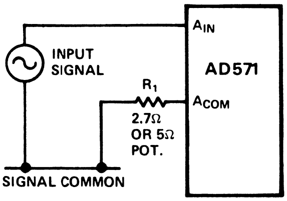
ZERO OFFSET

The apparent zero point of the AD571 can be adjusted by inserting an offset voltage between the Analog Common of the device and the actual signal return or signal common. Figure 8 illustrates two methods of providing this offset. Figure 8A shows how the converter zero may be offset by up to ±3 bits to correct the device initial offset and/or input signal offsets. As shown, the circuit gives approximately symmetrical adjustment in unipolar mode. In bipolar mode R2 should be omitted to obtain a symmetrical range.



ZERO OFFSET ADJ
±3 BIT RANGE

Figure 8. (A)

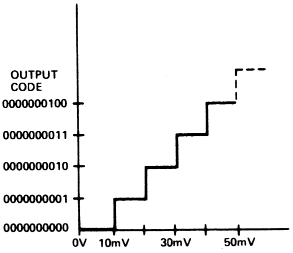


½ BIT ZERO OFFSET

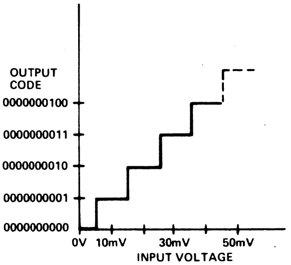
Figure 8. (B)

Figure 9 shows the nominal transfer curve near zero for an AD571 in unipolar mode. The code transitions are at the edges of the nominal bit weights. In some applications it will be preferable to offset the code transitions so that they fall between the nominal bit weights, as shown in the offset characteristics. This offset can easily be accomplished as shown in Figure 8B. At balance (after a conversion) approximately 2mA flows into the Analog Common terminal. A 2.7Ω resistor in series with this terminal will result in approximately the desired ½ bit offset of the transfer characteristics. The nominal 2mA Analog Common current is not closely controlled in manufacture. If high accuracy is required, a 5Ω potentiometer (connected as a rheostat) can be used as R1. Additional negative offset range may be obtained by using larger values of R1. Of course, if the zero transition point is changed, the full scale transition point will also move. Thus, if an offset of ½LSB is introduced, full scale trimming as described on previous page should be done with an analog input of 9.985 volts.

NOTE: During a conversion transient currents from the Analog Common terminal will disturb the offset voltage. Capacitive decoupling should not be used around the offset network. These transients will settle as appropriate during a conversion. Capacitive decoupling will "pump up" and fail to settle resulting in conversion errors. Power supply decoupling which returns to analog signal common, should go to the signal input side of the resistive offset network.



NOMINAL CHARACTERISTICS
REFERRED TO ANALOG COMMON



OFFSET CHARACTERISTICS WITH
2.7Ω IN SERIES WITH ANALOG COMMON

Figure 9. AD571 Transfer Curve - Unipolar Operation (Approximate Bit Weights Shown for Illustration, Nominal Bit Weights ~9.766mV)

CONTROL AND TIMING OF THE AD571

There are several important timing and control features on the AD571 which must be understood precisely to allow optimal interfacing to microprocessor or other types of control systems. All of these features are shown in the timing diagram in Figure 10.

The normal stand-by situation is shown at the left end of the drawing. The BLANK and $\overline{\text{CONVERT}}$ (B & $\overline{\text{C}}$) line is held high, the output lines will be "open", and the $\overline{\text{DATA}}$ $\overline{\text{READY}}$ ($\overline{\text{DR}}$) line will be high. This mode is the lowest power state of the device (typically 150mW). When the (B & $\overline{\text{C}}$) line is brought low, the conversion cycle is initiated; but the $\overline{\text{DR}}$ and Data lines do not change state. When the conversion cycle is complete (typically 25μs), the $\overline{\text{DR}}$ line goes low, and within 500ns, the Data lines become active with the new data.

About 1.5μs after the B & $\overline{\text{C}}$ line is again brought high, the $\overline{\text{DR}}$ line will go high and the Data lines will go open. When the B & $\overline{\text{C}}$ line is again brought low, a new conversion will begin. The minimum pulse width for the B & $\overline{\text{C}}$ line to blank previous data and start a new conversion is 2μs. If the B & $\overline{\text{C}}$ line is brought high during a conversion, the conversion will stop, and the $\overline{\text{DR}}$ and Data lines will not change. If a 2μs or longer pulse is applied to the B & C line during a conversion, the converter will clear and start a new conversion cycle.

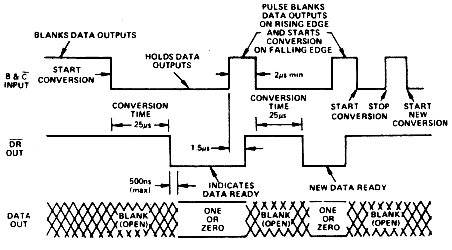


Figure 10. AD571 Timing and Control Sequence

CONTROL MODES WITH BLANK AND $\overline{\text{CONVERT}}$

The timing sequence of the AD571 discussed above allows the device to be easily operated in a variety of systems with differing control modes. The two most common control modes, the Convert Pulse Mode, and the Multiplex Mode, are illustrated here.

Convert Pulse Mode – In this mode, data is present at the output of the converter at all times except when conversion is taking place. Figure 11 illustrates the timing of this mode. The BLANK and $\overline{\text{CONVERT}}$ line is normally low and conversions are triggered by a positive pulse. A typical application for this timing mode is shown in Figure 14 in which μP bus interfacing is easily accomplished with three-state buffers.

Multiplex Mode – In this mode the outputs are blanked except when the device is selected for conversion and readout; this timing is shown in Figure 12. A typical AD571 multiplexing application is shown in Figure 15.

This operating mode allows multiple AD571 devices to drive common data lines. All BLANK and $\overline{\text{CONVERT}}$ lines are held high to keep the outputs blanked. A single AD571 is selected, its BLANK and $\overline{\text{CONVERT}}$ line is driven low and at the end of conversion, which is indicated by $\overline{\text{DATA}}$ $\overline{\text{READY}}$ going low, the conversion result will be present at the outputs. When this data has been read from the 10-bit bus, BLANK and $\overline{\text{CONVERT}}$ is restored to the blank mode to clear the data bus for other converters. When several AD571's are multiplexed in sequence, a new conversion may be started in one AD571 while data is being read from another. As long as the data is read and the first AD571 is cleared within 15μs after the start of conversion of the second AD571, no data overlap will occur.

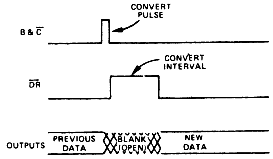


Figure 11. Convert Pulse Mode

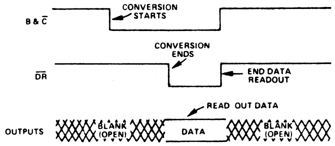


Figure 12. Multiplex Mode

SAMPLE-HOLD AMPLIFIER CONNECTION TO THE AD571

Many situations in high-speed acquisition systems or digitizing of rapidly changing signals require a sample-hold amplifier (SHA) in front of the A-D converter. The SHA can acquire and hold a signal faster than the converter can perform a conversion. A SHA can also be used to accurately define the exact point in time at which the signal is sampled. For the AD571, a SHA can also serve as a high input impedance buffer.

Figure 13 shows the AD571 connected to the AD582 monolithic SHA for high speed signal acquisition. In this configuration, the AD582 will acquire a 10 volt signal in less than 10μs with a droop rate less than 100μV/ms. The control signals are arranged so that when the control line goes low, the AD582 is put into the "hold" mode, and the AD571 will begin its conversion cycle. (The AD582 settles to final value well in advance of the

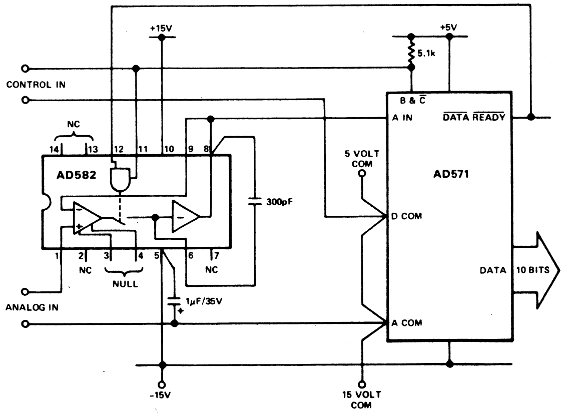


Figure 13. Sample-Hold Interface to the AD571

first comparator decision inside the AD571). The $\overline{\text{DATA READY}}$ line is fed back to the other side of the differential input control gate so that the AD582 cannot come out of the "hold" mode during the conversion cycle. At the end of the conversion cycle, the $\overline{\text{DATA READY}}$ line goes low, automatically placing the AD582 back into the sample mode. This feature allows simple control of both the SHA and the A-D converter with a single line. Observe carefully the ground, supply, and bypass capacitor connections between the two devices. This will minimize ground noise and interference during the conversion cycle to give the most accurate measurements.

INTERFACING THE AD571 TO A MICROPROCESSOR

The AD571 can easily be arranged to be driven from standard microprocessor control lines and to present data to any standard microprocessor bus (4-, 8-, 12-or 16-bit) with a minimum of additional control components. The configuration shown in Figure 14 is designed to operate with 8-bit bus and standard 8080 control signals.

The input control circuitry shown is required to insure that the AD571 receives a sufficiently long B & $\overline{\text{C}}$ input pulse. When the converter is ready to start a new conversion, the B & $\overline{\text{C}}$ line is low, and $\overline{\text{DR}}$ is low. To command a conversion, the start address decode line goes low, followed by $\overline{\text{WR}}$. The B & $\overline{\text{C}}$ line will now go high, followed about 1.5μs later by $\overline{\text{DR}}$. This resets the external flip-flop and brings B & $\overline{\text{C}}$ back to low, which initiates the conversion cycle. At the end of the conversion cycle, the $\overline{\text{DR}}$ line goes low, the data outputs will become active with the new data and the control lines will return to the stand-by state. The new data will remain active until a new conversion is commanded. The self-pulsing nature of this circuit guarantees a sufficient convert pulse width.

This new data can now be presented to the data bus by enabling the three-state buffers when desired. A data word (8-bit or 2-bit) is loaded onto the bus when its decoded address goes low and the $\overline{\text{RD}}$ line goes low. This arrangement presents data to the bus "left-justified," with highest bits in the 8-bit word; a "right-justified" data arrangement can be set up by a simple re-wiring. Polling the converter to determine if conversion is complete can be done by addressing the gate which buffers the $\overline{\text{DR}}$ line, as shown. In this configuration, there is no need for additional buffer register storage since the data can be held indefinitely in the AD571, since the B & $\overline{\text{C}}$ line is continually held low.

BUS INTERFACING WITH A PERIPHERAL INTERFACE CIRCUIT

An improved technique for interfacing to a μP bus involves the use of special peripheral interfacing circuits (or I/O devices), such as the MC6821 Peripheral Interface Adapter (PIA). Shown in Figure 15 is a straighforward application of a PIA to multiplex up to 8 AD571 circuits. The AD571 has 3-state outputs, hence the data bit outputs can be paralleled, provided that only one converter at a time is permitted to be the active state. The $\overline{\text{DATA READY}}$ output of the AD571 is an open collector with resistor pull-up, thus several $\overline{\text{DR}}$ lines can be wire-ored to allow indication of the status of the selected device. One of the 8-bit ports of the PIA is combined with 2-bits from the other port and programmed as a 10-bit input port. The remaining 6-bits of the second port are programmed as outputs and along with the 2 control bits (which act as outputs), are used to control the 8 AD571's. When a control line is in the "1" or high state, the ADC will be automatically blanked. That is, its outputs will be in the inactive open state. If a single control line is switched low, its ADC will convert and the outputs will automatically go active when the conversion is complete. The result can be read from the two peripheral ports; when the next conversion is desired, a different control line can be switched to zero, blanking the previously active port at the same time. Subsequently, this second device can be read by the microprocessor, and so-forth. The status lines are wire-ored in 2 groups and connected to the two remaining control pins. This allows a conversion status check to be made after a convert command, if necessary. The ADC's are divided into two groups to minimize the loading effect of the internal pull-up resistors on the $\overline{\text{DATA READY}}$ buffers. See the Motorola MC6821 data sheet for more application detail.

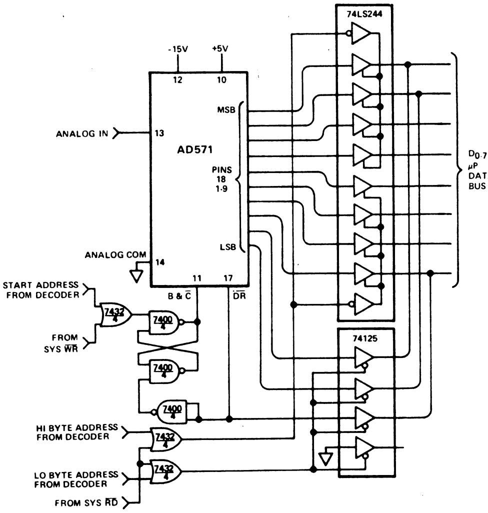

74LS244
-15V
+5V
12
10
MSB
ANALOG IN
13
AD571
PINS 18 1-9
LSB
ANALOG COM
14
11
17
B & $\overline{\text{C}}$
$\overline{\text{DR}}$
START ADDRESS FROM DECODER
FROM SYS $\overline{\text{WR}}$
7432 ¼
7400 ¼
7400 ¼
7400 ¼
HI BYTE ADDRESS FROM DECODER
7432 ¼
LO BYTE ADDRESS FROM DECODER
7432 ¼
FROM SYS $\overline{\text{RD}}$
74125
$D_{0\text{-}7}$ μP DATA BUS

Figure 14. Interfacing AD571 to an 8-Bit Bus (8080 Control Structure)

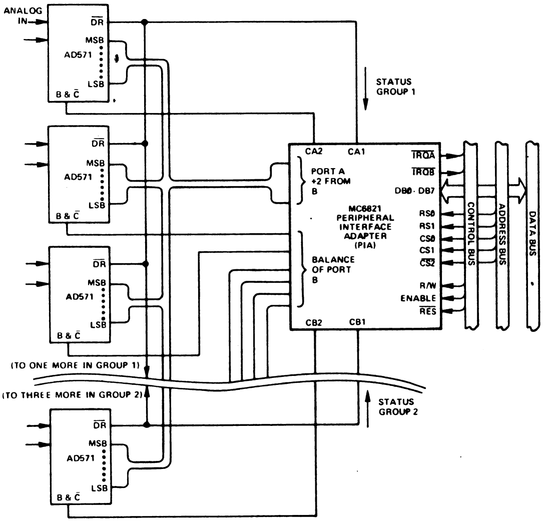


Figure 15. Multiplexing 8 AD571s Using Single PIA for μP Interface. No Other Logic Required (6800 Control Structure).

ANALOG DEVICES

12-Bit Successive Approximation Integrated Circuit A/D Converter

AD572

FEATURES

Performance

True 12-Bit Operation: Max Nonlinearity < ±0.012%
Low Gain T.C.: < ±15ppm/°C (AD572B)
Low Power: 900mW
Fast Conversion Time: < 25μs
Monotonic Feedback DAC Guarantees No Missing Codes

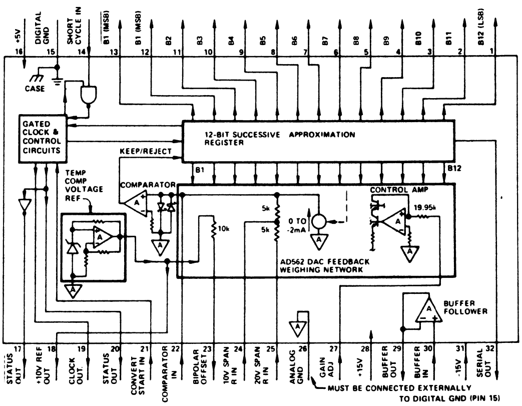
Versatility

Military/Aerospace Temperature Range:
-55°C to +125°C (AD572S)
MIL-STD-883 Processing Available
Positive-True Serial or Parallel Logic Outputs
Short-Cycle Capability

Value

Precision +10V Reference for External Application
Internal Buffer Amplifier
High Reliability Package

AD572 FUNCTIONAL BLOCK DIAGRAM



32-PIN DIP

GENERAL DESCRIPTION

The AD572 is a complete 12-bit successive approximation analog-to-digital converter that includes an internal clock, reference, comparator, and buffer amplifier. Its hybrid IC design utilizes MSI digital and linear monolithic chips and active laser trimming of high-stability thin-film resistors to provide modular performance, flexibility, and ease of use, combined with IC size, price, and reliability.

Important performance characteristics of the AD572 include a maximum linearity error at 25°C of ±0.012%, gain T.C. below 15ppm/°C, typical power dissipation of 900mW, and conversion time of less than 25μs. Of considerable significance in military and aerospace applications is the guaranteed performance from -55°C to +125°C of the AD572S, and the availability of units processed to MIL-STD-883. Monotonic operation of the feedback D/A converter guarantees no missing output codes over temperature ranges of 0 to +70°C, -25°C to +85°C, and -55°C to +125°C.

The design of the AD572 includes scaling resistors that provide analog input signal ranges of ±2.5, ±5.0, ±10, 0 to +5, or 0 to +10 volts. Adding flexibility and value are the +10V precision reference, which also can be used for external applications, and the input buffer amplifier. All digital signals are fully DTL and TTL compatible, and the data output is positive-true and available in either serial or parallel form.

The new AD572 package reduces the predicted failure rate by a factor of two. The new package integrates the device substrate and package in a single ceramic element to eliminate a number of bond wires and interconnections. The new design also eliminates a number of active components to further increase reliability.

The AD572 is available in three versions with differing guaranteed performance characteristics and operating temperature ranges; the "A" and "B" are specified from -25°C to +85°C, and the "S" from -55°C to +125°C.

PRODUCT DESCRIPTION

The AD572 functional diagram and pin-out are shown in Figure 1. The device consists of the following monolithic bipolar transistor and thin-film resistor circuit elements:

1. 12-bit successive-approximation register
2. 12-bit feedback DAC weighing network
3. low-drift comparator
4. temperature-compensated precision +10V reference
5. high-impedance buffer follower
6. gated clock and digital control circuits

SPECIFICATIONS (typical @ +25°C, ±15V and +5V unless otherwise noted)

MODEL	AD572AD	AD572BD	AD572SD
RESOLUTION	12 Bits	*	*
ANALOG INPUTS			
Voltage Ranges			
Bipolar	±2.5, ±5.0, ±10.0V	*	*
Unipolar	0 to +5, 0 to +10V	*	*
Impedance (Direct Input)			
0 to +5V, ±2.5V	2.5kΩ	*	*
0 to +10V, ±5V	5.0kΩ	*	*
±10V	10kΩ	*	*
Buffer Amplifier			
Impedance (min)	100MΩ	*	*
Bias Current	50nA	*	*
Settling Time to 0.01% of FSR for 20V step	2μs	*	*
DIGITAL INPUTS			
Convert Command	Note 1	*	*
Logic Loading	1 TTL Load	*	*
TRANSFER CHARACTERISTICS			
Gain Error (Note 2)	±0.05% FSR (Adj to Zero)	*	*
Unipolar Offset Error	±0.05% FSR (Adj to Zero)	*	*
Bipolar Offset Error	±0.1% FSR (Adj to Zero)	*	*
Linearity Error (max)	0.012% FSR	*	*
Inherent Quantization Error	±½ LSB	*	*
Differential Linearity Error	±½ LSB	*	*
No Missing Codes	Guaranteed: 0 to +70°C	Guaranteed: -25°C to +85°C	Guaranteed: -55°C to +125°C
Power Supply Sensitivity			
±15V	±0.002% FSR/%ΔV_S	*	*
±5V	±0.001% FSR/%ΔV_S	*	*
TEMPERATURE COEFFICIENTS			
Gain (max)	±30ppm/°C (-25°C to +85°C)	±15ppm/°C (-25°C to +85°C)	±15ppm/°C (-25°C to +85°C) ±25ppm/°C (-55°C to +125°C)
Unipolar Offset	±3ppm FSR/°C	±5ppm FSR/°C (max)	**
Bipolar Offset (max)	±15ppm FSR/°C	±7ppm FSR/°C	**
Linearity	±3ppm FSR/°C	±2ppm FSR/°C	**
CONVERSION TIME (max)	25μs	*	*
DIGITAL OUTPUTS (All Codes Positive-True)			
Parallel Data			
Unipolar Code	Binary	*	*
Bipolar Code	Offset Binary/Two's Complement	*	*
Output Drive	2 TTL Loads	*	*
Serial Data (NRZ format)			
Unipolar Code	Binary	*	*
Bipolar Code	Offset Binary	*	*
Output Drive	2 TTL Loads	*	*
Status	Logic "1" during Conversion	*	*
$\overline{\text{Status}}$	Logic "0" during Conversion	*	*
Output Drive	2 TTL Loads	*	*
Internal Clock			
Output Drive	2 TTL Loads	*	*
Frequency	500kHz	*	*
INTERNAL REFERENCE VOLTAGE	+10.00V, ±10mV	*	*
Max External Current	±1mA	*	*
Voltage Temperature Coefficient (max)	±20ppm/°C	±10ppm/°C	*
POWER REQUIREMENTS			
Supply Voltages/Currents	+15V, ±5% @ +25mA	*	*
	-15V, ±5% @ -20mA	*	*
	+5V, ±5% @ +80mA	*	*
Total Power Dissipation	925mW	*	*
TEMPERATURE RANGE			
Specification	-25°C to +85°C	*	-55°C to +125°C
Operating	-55°C to +125°C	*	*
Storage	-55°C to +150°C	*	*

*Same specification as AD572AD

**Same specification as AD572BD

Specifications subject to change without notice.

Note 1 Positive pulse 200ns wide (min). Leading edge ("0" to "1") resets registers. Trailing edge ("1" to "0") initiates conversion.

Note 2 With 50Ω, 1% fixed resistor in place of Gain Adjust pot; see Figures 4 and 5.

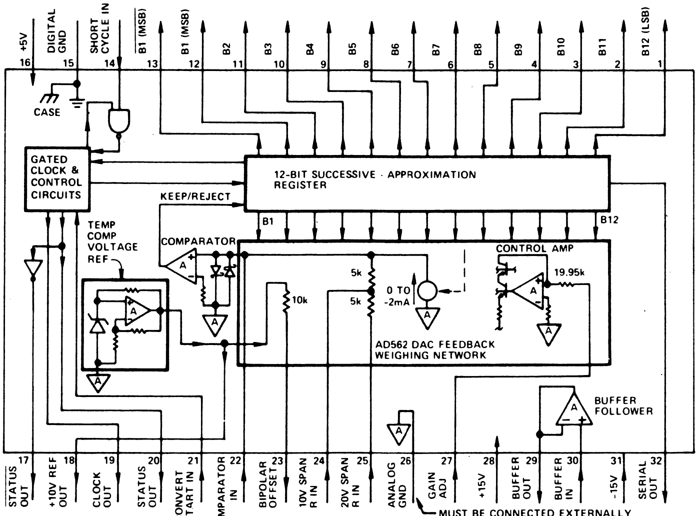


Figure 1. AD572 Functional Diagram & Pinout

The +10V reference is derived from a low T.C. zener reference diode which has its zener voltage amplified and buffered by an op amp. The reference voltage is calibrated to +10V, ±10mV by active laser trimming of the thin-film resistors which determine the closed-loop gain of this op amp.

The DAC chip uses 12 precision, high speed bipolar current steering switches, a control amplifier and a laser-trimmed thin film resistor network to produce a very fast, high accuracy analog output current. The DAC is laser-trimmed to calibrate all bit ratio scale factors to a precision of 0.0005% of FSR (full-scale range) to guarantee no missing codes over the appropriate temperature ranges specified for the AD572A, AD572B, and AD572S versions.

Different unipolar and bipolar analog input ranges can be selected by changing connections at the device terminal pins. The analog voltage input can be applied to either of the span (direct input) resistors. Alternatively, the unity buffer follower can be connected between the analog signal and either direct input terminal when a high impedance input is required.

THEORY OF OPERATION

On receipt of a CONVERT START command, the AD572 converts the voltage at its analog input into an equivalent 12-bit binary number. This conversion is accomplished as follows:

The 12-bit successive-approximation register (SAR) has its 12-bit outputs connected both to the respective device bit output pins and to the corresponding bit inputs of the feedback DAC.

The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

TIMING

The timing diagram is shown in Figure 2. Receipt of a CONVERT START signal sets the STATUS flag, indicating conversion in progress. This, in turn, removes the inhibit applied to the gated clock, permitting it to run through

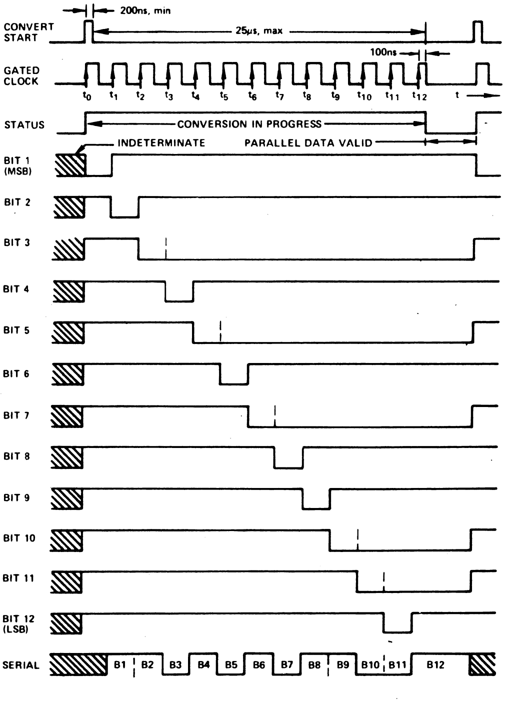


Figure 2. Timing Diagram (Binary Code 110101011001)

13 cycles. All SAR parallel bit and STATUS flip-flops are initialized on the leading edge, and the gated clock inhibit signal removed on the trailing edge of the CONVERT START signal. At time t_0, B_1 is reset and B_2 -B_{12} are set unconditionally. At t_1 the Bit 1 decision is made (keep) and Bit 2 is unconditionally reset. At t_2, the Bit 2 decision is made (keep) and Bit 3 is reset unconditionally. This sequence continues until the Bit 12 (LSB) decision (keep) is made at t_{12}. After a 100ns delay period, the STATUS flag is reset, indicating that the conversion is complete and that the parallel output data is valid. Resetting the STATUS flag restores the gated clock inhibit signal, forcing the clock output to the logic "0" state.

Corresponding serial and parallel data bits become valid on the same positive-going clock edge. Serial data does not change and is guaranteed valid on negative-going clock edges, however; serial data can be transferred quite simply by clocking it into a receiving shift register on these edges (see Figure 8).

Incorporation of this 100ns delay period guarantees that the parallel (and serial) data are valid at the Logic "1" to "0" transition of the STATUS flag, permitting parallel data transfer to be initiated by the trailing edge of the STATUS signal.

BINARY CODING

The AD572 binary output number $N_o = B_1\ B_2\ B_3 \ldots B_{12}$ is related to the analog input voltage E_{in} for all unipolar ranges by the expression:

$$\frac{B_1 2^{11} + B_2 2^{10} + B_3 2^9 + \ldots + B_{12} 2^0}{2^{12}} = \frac{E_{in}}{FSR} \qquad (1)$$

. . .where B_1 = MSB, B_{12} = LSB, and FSR = full-scale range. For all bipolar ranges a fixed bipolar offset equal to $\frac{+FSR}{2}$ is internally summed with E_{in} so that the sum of E_{in} plus this offset will be positive over the rated operating range. For bipolar ranges, expression (1) becomes:

$$\frac{B_1 2^{11} + B_2 2^{10} + B_3 2^9 + \ldots + B_{12} 2^0}{2^{12}} = \frac{E_{in} + \frac{FSR}{2}}{FSR} \qquad (2)$$

Expressions (1) and (2) can be put in an alternate form:

$$\left(\frac{B_1}{2} + \frac{B_2}{4} + \frac{B_3}{8} + \ldots + \frac{B_{12}}{4096}\right) FSR = E_{in} \qquad (3)$$

Unipolar (Binary Coding)

...and...

$$\left(\frac{B_1}{2} + \frac{B_2}{4} + \frac{B_3}{8} + \ldots + \frac{B_{12}}{4096}\right) FSR - \frac{FSR}{2} = E_{in} \qquad (4)$$

Bipolar (Offset Binary Coding)

Several examples will illustrate how this binary coding works.

0 TO +10V INPUT RANGE

Assume FSR = 10V and $B_1\ B_2\ B_3 \ldots B_{12}$ = 110001000001, then from (3), E_{in} = +5V +2.5V +0.1563V + 0.0024V = +7.6587V.

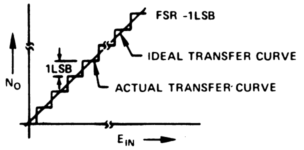
-5V TO +5V INPUT RANGE

Assume FSR = 10V as above, but that the bipolar offset is connected and $B_1\ B_2\ B_3 \ldots B_{12}$ = 0110000000001. Then from (4), E_{in} = (+2.5V + 1.25V + 0.0024V) - 5V = -1.2476V.

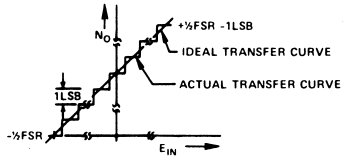
-10V TO +10V INPUT RANGE

Assume the bipolar offset is connected as above, but that the input span is now 20V. Assuming the same digital output code as in the -5V to +5V input range example, from (4), E_{in} = (+5V +2.5V +0.0049V) -10V = -2.4951V, or twice the value of the previous example (neglecting round-off errors).

The encoding process defined by the previous relations (1) and (2) or (3) and (4) determines that the analog input lies within one of the 2^{12} = 4096 quantization levels between 0 and FSR (or -FSR/2 and +FSR/2). Figures 3 (A) and 3 (B) show the actual device transfer curves for unipolar and bipolar ranges (offset binary coding). They also show the ideal straight-line transfer curves which pass through the center of each quantization level. As can be seen from these figures, the actual and ideal transfer curves differ by exactly ±½LSB at the end of each quantization interval, giving rise to the fundamental ±½LSB quantization error inherent in the digitizing process.



(A) Unipolar Range (Binary Coding)

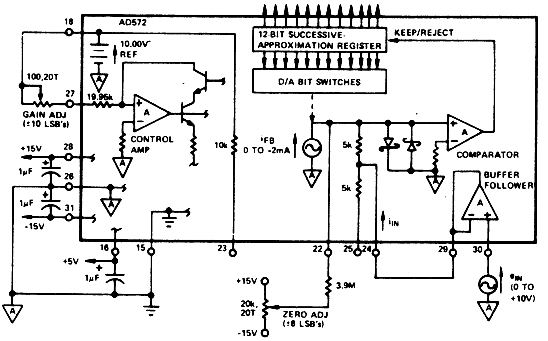


(B) Bipolar Range (Offset Binary Coding)

Figure 3. Unipolar and Bipolar Range Transfer Curves

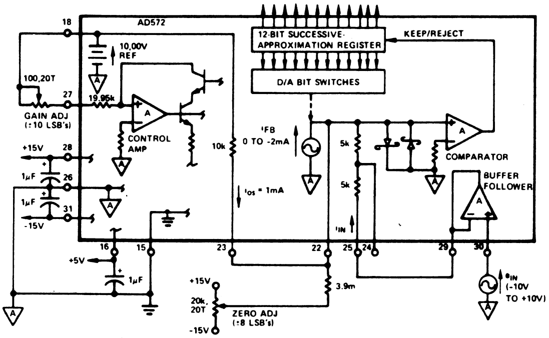
ANALOG INPUT AND POWER CONNECTIONS

Offset Adjust: Analog and power connections for 0 to +10V unipolar and -10V to +10V bipolar input ranges are shown in Figures 4 and 5, respectively. The Bipolar Offset pin 23 is open-circuited for all unipolar input ranges, and connected to Comparator Input pin 22 for all bipolar input ranges. The zero adjust circuit consists of a potentiometer connected across $\pm V_S$ with its slider connected through a 3.9MΩ resistor to Comparator Input pin 22 for all ranges. The tolerance of this fixed resistor is not critical, and a carbon composition type is generally adequate. Using a carbon composition resistor having a -1200ppm/°C tempco contributes a worst-case offset tempco of $8 \times 244 \times 10^{-6} \times 1200$ppm/°C = 2.3ppm/°C of FSR, if the OFFSET ADJ potentiometer is set at either end of its adjustment range. Since the maximum offset adjustment required is typically no more than ±4LSB, use of a carbon composition offset summing resistor typically contributes no more than 1ppm/°C of FSR offset tempco.



NOTE ANALOG (A) AND DIGITAL (⏚) GNDS ARE NOT TIED INTERNALLY AND MUST BE CONNECTED EXTERNALLY

Figure 4. Analog and Power Connections for Unipolar 0 to +10V Input Range with Buffer Follower



NOTE: ANALOG (A) AND DIGITAL (⏚) GNDS ARE NOT TIED INTERNALLY AND MUST BE CONNECTED EXTERNALLY.

Figure 5. Analog and Power Connections for Bipolar -10V to +10V Input Range with Buffer Follower

An alternate offset adjust circuit, which contributes negligible offset tempco if metal film resistors (tempco < 100 ppm/°C) are used, is shown in Figure 6.

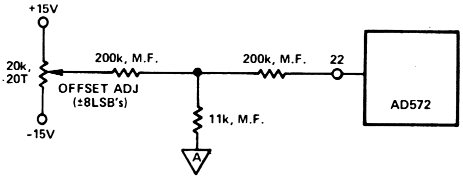


Figure 6. Low Tempco Zero Adj Circuit

In either zero adjust circuit, the fixed resistor connected to pin 22 should be located close to this pin to keep the pin 22 connection runs short, since the Comparator Input pin 22 is quite sensitive to external noise pick-up.

Gain Adjust: The gain adjust circuit consists of a 100Ω potentiometer connected between +10V Reference Output pin 18 and Gain Adjust Input pin 27 for all ranges. Both GAIN and ZERO ADJ potentiometers should be multi-turn, low tempco types; 20T cermet (tempco = 100ppm/°C max) types are recommended. If the 100Ω GAIN ADJ potentiometer is replaced by a fixed 50Ω resistor, absolute gain calibration to ±0.1% of FSR is guaranteed.

Grounding: Analog and digital signal grounds should be kept separate where possible to prevent digital signals from flowing in the analog ground circuit and inducing spurious analog signal noise. Analog Ground pin 26 and Digital Ground pin 15 are not connected internally; these two pins must be connected externally for the device to operate properly. Preferably, this connection is made at only one point, and as close to the device as possible.

Power Supply Bypassing: The ±15V and +5V power leads should be capacitively bypassed for optimum device performance. 1μF tantalum types are recommended; these capacitors should be located close to the device. It is not necessary to shunt these capacitors with disc capacitors to provide additional high frequency power supply decoupling (as is required with some competitive products), since each power lead is bypassed internally with a 0.039μF ceramic capacitor.

CALIBRATION

External ZERO ADJ and GAIN ADJ potentiometers, connected as shown in Figures 3 and 4, are used for device calibration. To prevent interaction of these two adjustments, Zero is always adjusted first and then Gain. Zero is adjusted with the analog input near the most negative end of the analog range (0 for unipolar and -½FSR for bipolar input ranges). Gain is adjusted with the analog input near the most positive end of the analog range.

0 to +10V Range: Set analog input to +1LSB = +0.0024V. Adjust Zero for digital output = 000000000001; Zero is now calibrated. Set analog input to +FSR -2LSB = +9.9952V. Adjust Gain for 111111111110 digital output code; full-scale (Gain) is now calibrated. Half-scale calibration check: set analog input to +5.0000V; digital output code should be 100000000000.

-10V to +10V Range: Set analog input to -9.9951V; adjust Zero for 000000000001 digital output (offset binary) code. Set analog input to +9.9902V; adjust Gain for 111111111110 digital output (offset binary) code. Half-scale calibration check: set analog input to 0.0000V; digital output (offset binary) code should be 100000000000.

Other Ranges: Representative digital coding for 0 to +10V, -5V to +5V, and -10V to +10V ranges is shown in Table 1. Coding relationships and calibration points for 0 to +5V and -2.5V to +2.5V ranges can be found by halving the corresponding code equivalents listed for the 0 to +10V and -5V to +5V ranges, respectively.

Zero and full-scale calibration can be accomplished to a precision of approximately ±¼LSB using the static adjustment procedure described above. By summing a small sine or triangular-wave voltage with the signal applied to the analog input, the output can be cycled through each of the calibration codes of interest to more accurately determine the center (or end points) of each discrete quantization level. A detailed description of this dynamic calibration technique is presented in "A/D Conversion Notes", D. Sheingold, Analog Devices, Inc., 1977, Part II, Chapter 4.

Analog Input - Volts (Center of Quantization Interval)			Input Normalized to FSR		Digital Output Code (Binary for Unipolar Ranges; Offset Binary for Bipolar Ranges)
0 to +10V Range	-5V to +5V Range	-10V to +10V Range	Unipolar Ranges	Bipolar Ranges	B1 (MSB) B12 (LSB)
+9.9976	+4.9976	+9.9951	+FSR-1 LSB	+½FSR-1 LSB	1 1 1 1 1 1 1 1 1 1 1 1
+9.9952	+4.9952	+9.9902	+FSR-2 LSB	+½FSR-2 LSB	1 1 1 1 1 1 1 1 1 1 1 0
⋮	⋮	⋮	⋮	⋮	⋮
+5.0024	+0.0024	+0.0049	+½FSR+1 LSB	+1 LSB	1 0 0 0 0 0 0 0 0 0 0 1
+5.0000	+0.0000	+0.0000	+½FSR	ZERO	1 0 0 0 0 0 0 0 0 0 0 0
⋮	⋮	⋮	⋮	⋮	⋮
+0.0024	-4.9976	-9.9951	+1 LSB	-½FSR+1 LSB	0 0 0 0 0 0 0 0 0 0 0 1
+0.0000	-5.0000	-10.0000	ZERO	-½FSR	0 0 0 0 0 0 0 0 0 0 0 0

Table 1. Digital Output Codes vs Analog Input For Unipolar and Bipolar Ranges

RANGE AND BUFFER FOLLOWER PIN CONNECTIONS

Analog pin connections for each of the ranges, with and without the buffer follower being used, are shown in Table 2.

Range	Buffer Follower	Connect Analog Input To Pin:	Connect Span Pin:	Connect Bipolar Pin 23 To:
0 to +5V	Used	30, and 29 to 24	25 to 22	—
	Not Used	24		
0 to +10V	Used	30, and 29 to 24	—	
	Not Used	24		
-2.5 to +2.5V	Used	30, and 29 to 24	25 to 22	22
	Not Used	24		
-5 to +5V	Used	30, and 29 to 24	—	
	Not Used	24		
-10 to +10V	Used	30, and 29 to 25	—	
	Not Used	25		

Table 2. Range and Buffer Follower Pin Connections

When the analog signal source has a low impedance (as would be the case if it were the output of the sample-hold amplifier of Figure 9), it can be connected to either of the direct input pins 24 or 25. The buffer follower is used in the application as shown in Figure 6, in which the analog input to the converter comes directly from the output of a FET analog multiplexer. The selected channel has a typical r_{on} = 200Ω which has a 3000ppm/°C tempco. If the multiplexer output were connected to the 0 to +10V direct input pin 24 (5kΩ input impedance, nominal), this r_{on} would introduce a 4% gain scale-factor loading error, which is well beyond the normal ±0.25% FSR external gain adjustment range, and a tempco of approximately 3000ppm/°C x 4% = 120ppm/°C. By connecting the buffer between the multiplexer output and direct input, these errors are eliminated. The buffer amplifier input bias current (50nA typical) must flow through the analog signal source, however. This limits the upper practical source impedance to several kilohms so that the offset voltage $I_{BIAS}\ R_{SOURCE}$ can be kept negligible, even though the buffer amplifier dynamic input impedance ⩾ 100MΩ. The buffer amplifier has a 2μs settling time to 0.01% FSR for a 20V input step. This must be added to the conversion time when the input voltage can change significantly between successive conversions (as could be the case in the circuit of Figure 7).

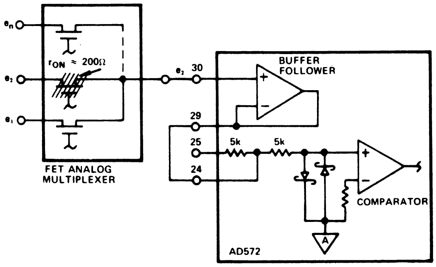


Figure 7. Using Buffer Follower With Multiplexed Analog Input

Short Cycle Input: A Short Cycle Input pin 14 permits the timing cycle shown in Figure 2 to be terminated after any number of desired bits has been converted, permitting somewhat shorter conversion times in applications not requiring full 12-bit resolution. When 12-bit resolution is required, pin 14 is connected to +5V (pin 16). When 10-bit resolution is desired, pin 14 is connected to Bit 11 output pin 2. The conversion cycle then terminates, and the STATUS flag resets after the Bit 10 decision (t_{10} +100ns in timing diagram of Figure 2). Short Cycle pin connections and associated maximum 12, 10, and 8-bit conversion times are summarized in Table 3.

Connect Short Cycle Pin 14 to Pin:	Bits	Resolution (% FSR)	Maximum Conversion Time (μs)	Status Flag Reset at: (Figure 2)
16	12	0.024	25	t_{12} + 100ns
2	10	0.10	21	t_{10} + 100ns
4	8	0.39	17	t_8 + 100ns

Table 3. Short Cycle Connections

(One should note that the calibration voltages listed in Table 1 are for 12-bit resolution only, and are not those corresponding to the center of each discrete quantization interval at reduced bit resolutions.)

DIGITAL OUTPUT DATA

Both parallel and serial data are in positive-true form and outputted from TTL storage registers. Parallel data output coding is binary for unipolar ranges and either offset binary or two's complement binary, depending on whether Bit 1 (pin 12) or its logical inverse $\overline{\text{BIT 1}}$ (pin 13) is used as the MSB. Parallel data becomes valid approximately 200ns before the STATUS flag returns to Logic "0", permitting parallel data transfer to be clocked on the "1" to "0" transition of the STATUS flag.

Serial data coding is binary for unipolar input ranges and offset binary for bipolar input ranges. Serial output is by bit (MSB first, LSB last) in NRZ (non-return-to-zero) format. Serial and parallel data outputs change state on positive-going clock edges. Serial data is guaranteed valid on all negative-going clock edges, permitting serial data to be clocked directly into a receiving register on these edges as shown in Figure 8. There are 13 negative-going clock edges in the complete 12-bit conversion cycle, as shown in Figure 2. The first edge shifts an invalid bit into the register, which is shifted out on the 13th negative-going clock edge. All serial data bits will have been correctly transferred and be in the receiving shift register locations shown at the completion of the conversion period.

APPLICATIONS

Sample-Hold Amplifier: A sample-hold amplifier (SHA) is normally connected between the analog signal source and AD572 analog input when the analog signal can change by more than ½LSB during conversion. Typical SHA-AD572 interconnections are shown in Figure 9. The STATUS output drives the SHA SAMPLE/HOLD input directly. On receipt of a CONVERT START pulse, the STATUS flag changes from "1" to "0" causing SHA mode to change from SAMPLE to HOLD. The SHA output voltage $e_{o\ S\text{-}H}$ is then held constant at the value existing just prior to application of the HOLD command for the complete conversion period. At the end of conversion, the STATUS flag returns to "1", restoring the SHA mode to SAMPLE, and $e_{o\ S\text{-}H}$ again tracks the analog signal voltage $e_{in\ S\text{-}H}$ (after the signal acquisition transient has subsided).

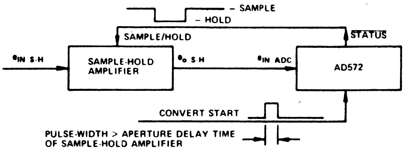
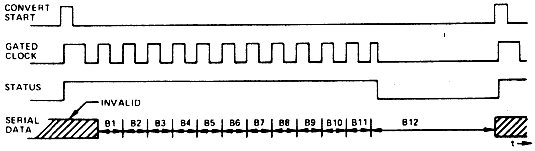
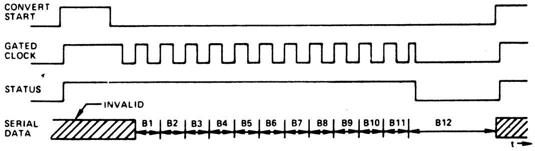


Figure 9. Sample-Hold Amplifier – AD572 Interconnections

Note that the internal (gated) clock is inhibited for the duration of the CONVERT START pulse and does not start running until the termination of this pulse (see timing). This can be used to simplify control signal timing requirements. In the circuit of Figure 9, for example, the CONVERT START signal pulse-width can be extended beyond the aperture delay time of the SHA to assure that $e_{o\ S\text{-}H}$ is in steady-state before conversion is initiated. This assures accurate conversion without requiring additional delay timing circuitry. The effect of varying the CONVERT START pulse-width on the conversion timing cycle is shown in Figure 10.



(a) NARROW CONVERT START PULSE



(b) WIDE CONVERT START PULSE

Figure 10. Effect of Convert Start Pulse-Width on Timing

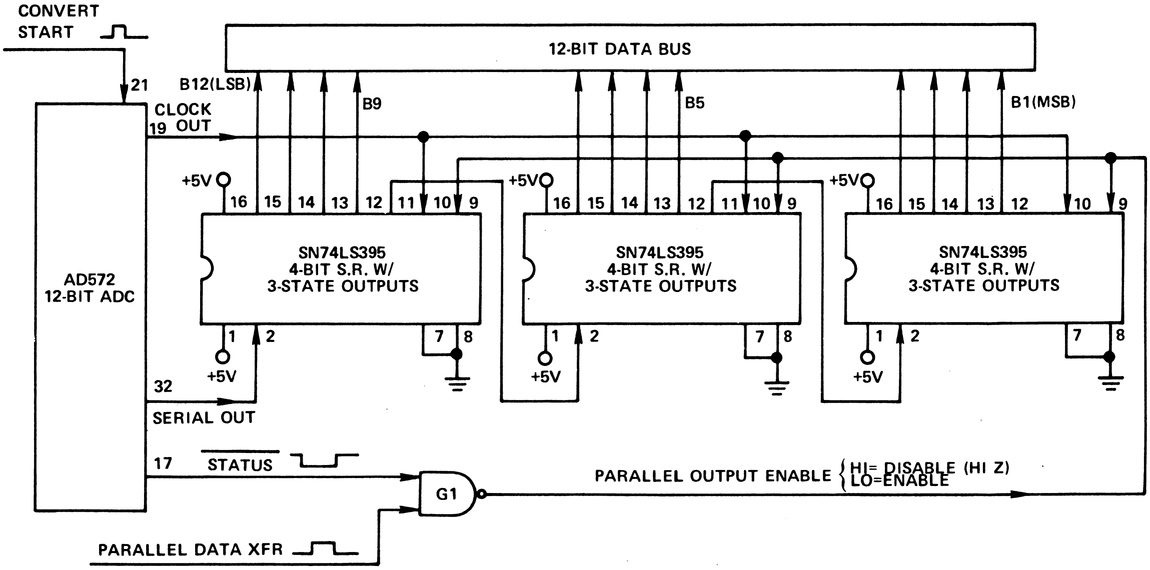


Figure 8. Serial Data Transfer Into Shift Register With Parallel Output to Data Bus

Digital Gain Control: Figure 11 shows a method of varying the AD572 gain digitally, using an 8-bit DAC. The 100Ω GAIN ADJ potentiometer is replaced by a 15Ω fixed resistor. This biases full-scale high by approximately 35Ω/20,000Ω = +0.18% of FSR. The AD559 has a large positive compliance voltage which permits its Current Output pin 4 to be connected directly to the AD572 Reference Input pin 27. The AD559 2.5mA output current is established by the AD580 +2.5V voltage reference connected through a 1kΩ resistor to Reference Current Input pin 14. The 2.5mA DAC full-scale output current removed from the AD572 pin 27 node changes the pin 27 input current -2.5mA x 15Ω/20kΩ = -1.88μA, or -1.88μA/500μA = -0.38% of FSR; this permits a digital gain adjustment range of approximately ±0.2% FSR from nominal.

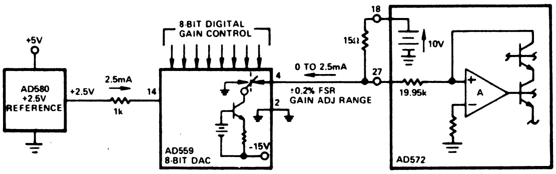


Figure 11. Digital Gain Control Using 8-Bit DAC

AD572 ORDERING GUIDE

Model	Specification Temp Range	Max Gain T.C.	Max Reference T.C.	Guaranteed Temp Range No Missing Codes	Package Option[1]
AD572AD	-25°C to +85°C	±30ppm/°C	±20ppm/°C	0 to +70°C	HY32G
AD572BD	-25°C to +85°C	±15ppm/°C	±10ppm/°C	-25°C to +85°C	HY32G
AD572SD	-55°C to +125°C	±15ppm/°C (-25°C to +85°C) ±25ppm/°C (-55°C to +125°C)	±20ppm/°C	-55°C to +125°C	HY32G
AD572BD/883B AD572SD/883B	Meet all specifications after processing to the requirements of MIL-STD-883, Method 5008, Class B.				

NOTE: D suffix = Dual-In-Line package designator.

[1] See Section 20 for package outline information.

ANALOG DEVICES

Fast, Complete 10-Bit A/D Converter with Microprocessor Interface

AD573*

ADVANCE TECHNICAL DATA

FEATURES

- Complete 10-Bit A/D Converter with Reference, Clock and Comparator
- Full 8- or 16-Bit Microprocessor Bus Interface
- Fast Successive Approximation Conversion – 15μs
- No Missing Codes Over Temperature
- Operates on +5V and −12V to −15V Supplies
- Low Cost Monolithic Construction

PRODUCT DESCRIPTION

The AD573 is a complete 10-bit successive approximation analog to digital converter consisting of a DAC, voltage reference, clock, comparator, successive approximation register (SAR) and 3 state output buffers–all fabricated on a single chip. No external components are required to perform a full accuracy 10-bit conversion in 15μs.

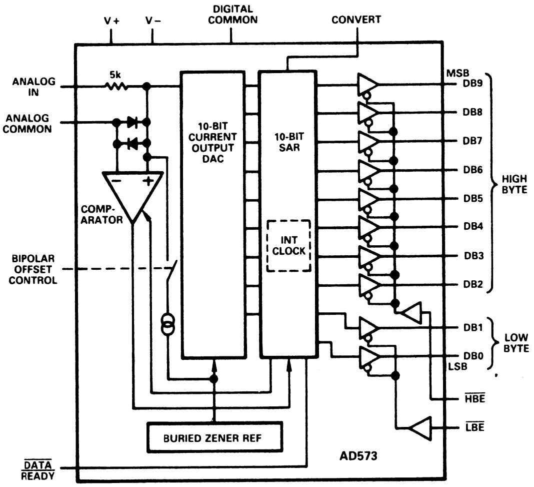
The AD573 incorporates the most advanced integrated circuit design and processing technology available today. The successive approximation function is implemented with I^2L (integrated injection logic). Laser trimming of the high stability SiCr thin film resistor ladder network at the wafer stage (LWT) insures high accuracy, which is maintained with a temperature compensated sub-surface Zener reference.

Operating on supplies of +5V and −12V to −15V, the AD573 will accept analog inputs of 0 to +10V, unipolar, or −5V to +5V, bipolar. A positive pulse on the CONVERT line initiates the 15μs conversion cycle. $\overline{\text{DATA READY}}$ indicates completion of the conversion. $\overline{\text{HIGH BYTE ENABLE}}$ ($\overline{\text{HBE}}$) and $\overline{\text{LOW BYTE ENABLE}}$ ($\overline{\text{LBE}}$) control the 8-bit and 2-bit three state output buffers.

The AD573 is available in two versions for the 0 to +70°C temperature range, the AD573J and AD573K. The AD573S guarantees 10-bit accuracy and no missing codes from −55°C to +125°C.

Two package configurations are offered. The AD573J and AD573K are available in a 20-pin plastic DIP. All versions are offered in a 20-pin hermetically sealed ceramic DIP.

AD573 FUNCTIONAL BLOCK DIAGRAM



PRODUCT HIGHLIGHTS

1. The AD573 is a complete 10-bit A/D converter. No external components are required to perform a conversion.
2. The AD573 interfaces to many popular microprocessors without external buffers or peripheral interface adapters. The 10 bits of output data can be read as a 10-bit word or as 8- and 2-bit words.
3. The device offers true 10-bit accuracy and exhibits no missing codes over its entire operating temperature range.
4. The AD573 accepts either unipolar (0 to +10V) or bipolar (−5V to +5V) analog inputs by simply grounding or opening a single pin.
5. Performance is guaranteed with +5V and −15V supplies. The device will also operate with a −12V supply.
6. The AD573SD/883B is screened in accordance with the Class B requirements of MIL-STD-883, Method 5004. Single chip construction renders the AD573 inherently more reliable than hybrid units. That and its functional completeness make the AD573 especially attractive for high reliability applications.

***Protected by Patents 3,940,760; 4,213,806 and 4,136,349**

SPECIFICATIONS

(typical @ +25°C with V+ = +5V, V− = −15V, all voltages measured with respect to digital common, unless otherwise indicated)

Model	AD573J	AD573K	AD573S[1]
RESOLUTION	10 Bits	*	*
RELATIVE ACCURACY @ 25°C[2]	±1LSB max	±½LSB max	±1LSB max
T_{min} to T_{max}	±1LSB max	±½LSB max	±1LSB max
FULL SCALE CALIBRATION[3] (With 15Ω Resistor In Series With Analog Input)	±2LSB	*	*
UNIPOLAR OFFSET (max)	±1LSB	±½LSB	*
BIPOLAR OFFSET (max)	±1LSB	±½LSB	*
DIFFERENTIAL NONLINEARITY (Resolution for Which No Missing Codes are Guaranteed)			
+25°C	10 Bits	*	*
T_{min} to T_{max}	9 Bits	10 Bits	**
TEMPERATURE RANGE	0 to +70°C	*	−55°C to +125°C
TEMPERATURE COEFFICIENTS			
Guaranteed max Change 25°C to T_{min} or T_{max}			
Unipolar Offset	±2LSB (44ppm/°C)	±1LSB (22ppm/°C)	±2LSB (20ppm/°C)
Bipolar Offset	±2LSB (44ppm/°C)	±1LSB (22ppm/°C)	±2LSB (20ppm/°C)
Full Scale Calibration (With 15Ω Fixed Resistor or 50Ω Trimmer)	±4LSB (88ppm/°C)	±2LSB (44ppm/°C)	±5LSB (50ppm/°C)
POWER SUPPLY REJECTION			
Max Change in Full Scale Calibration			
Positive Supply			
+4.5V≤V+≤+5.5V	±2LSB max	±1LSB max	*
Negative Supply			
−15.75V≤V−≤−14.25V	±2LSB max	±1LSB max	*
−12.6V≤V−≤−11.4V	±2LSB max	±1LSB max	*
ANALOG INPUT IMPEDANCE	3kΩ min	*	*
	5kΩ typ	*	*
	7kΩ max	*	*
ANALOG INPUT RANGES (Analog Input to Analog Common)			
Unipolar	0 to +10V	*	*
Bipolar	−5V to +5V	*	*
OUTPUT CODING			
Unipolar	Positive True Binary	*	*
Bipolar	Positive True Offset Binary	*	*
LOGIC OUTPUT			
Bit Outputs and $\overline{\text{Data Ready}}$			
Output Sink Current	3.2mA min	*	*
(V_{OUT} = 0.4V max, T_{min} to T_{max})	(2TTL Loads)	*	*
Output Source Current (Bit Outputs)[4]			
(V_{OUT} = 2.4V min, T_{min} to T_{max})	0.5mA min	*	*
Output Leakage (3 State)	±40μA max	*	*
LOGIC INPUT (CONVERT, $\overline{\text{HBE}}$, $\overline{\text{LBE}}$)			
Input Current ($0 \leq V_{IN} \leq V+$)	±100μA max	*	*
Logic "1"	2.0V min	*	*
Logic "0"	0.8 max	*	*
CONVERSION TIME	10μs min	*	*
T_{min} to T_{max}	15μs typ	*	*
	20μs max	*	*

Model	AD573J	AD573K	AD573S[1]
POWER SUPPLY			
Absolute Maximum			
V+	+7V	*	*
V−	−16.5V	*	*
Specified Operating – Rated Performance			
V+	+5V	*	*
V−	−15V	*	*
Operating Range			
V+	+4.5V to +5.5V	*	*
V−	−11.4V to −15.75V	*	*
Operating Current			
V+ = +5V	15mA typ (25mA max)	*	*
V− = −15V	9mA typ (15mA max)	*	*

*Specifications same as AD573J.
**Specifications same as AD573K.
Specifications subject to change without notice.

[1] The AD573S is available fully processed and screened to the requirements of MIL-STD-883, Method 5004, Class B. When ordering specify the AD573SD/883B.

[2] Relative accuracy is defined as the deviation of the code transition points from the ideal transfer point on a straight line from the zero to the full scale of the device.

[3] Full scale calibration is guaranteed trimmable to zero with an external 50Ω potentiometer in place of the 15Ω fixed resistor.
Full scale is defined as 10 volts minus 1LSB, or 9.990 volts.

[4] The Data output lines have active pull-ups to source 0.5mA. The $\overline{\text{DATA READY}}$ line is open collector with a nominal 6kΩ internal pull-up resistor.

ABSOLUTE MAXIMUM RATINGS

V+ to Digital Common	0 to +7V
V− to Digital Common	0 to −16.5V
Analog Common to Digital Common	±1V
Analog Input to Analog Common	±15V
Control Inputs	0 to V+
Digital Outputs (High Impedance State)	0 to V+
Power Dissipation	800mW

AD573 ORDERING GUIDE

Model	Package Option[1]	Temperature Range	Relative Accuracy
AD573JN	20-Pin Plastic DIP (N20A)	0 to +70°C	±1LSB max
AD573KN	20-Pin Plastic DIP (N20A)	0 to +70°C	±1/2LSB max
AD573JD	20-Pin Ceramic DIP (D20A)	0 to +70°C	±1LSB max
AD573KD	20-Pin Ceramic DIP (D20A)	0 to +70°C	±1/2LSB max
AD573SD	20-Pin Ceramic DIP (D20A)	−55°C to +125°C	±1LSB max
AD573SD/883B	20-Pin Ceramic DIP (D20A)	−55°C to +125°C	±1LSB max

[1] See Section 20 for package outline information.

FUNCTIONAL DESCRIPTION

A block diagram of the AD573 is shown in Figure 1. The positive CONVERT pulse must be at least 500ns wide. $\overline{DR}$ goes high within 1.5μs after the leading edge of the convert pulse indicating that the internal logic has been reset. The negative edge of the CONVERT pulse initiates the conversion. The internal 10-bit current output DAC is sequenced by the integrated injection logic (I^2L) successive approximation register (SAR) from its most significant bit to least significant bit to provide an output current which accurately balances the input signal current through the 5kΩ resistor. The comparator determines whether the addition of each successively weighted bit current causes the DAC current sum to be greater or less than the input current; if the sum is less, the bit is turned off. After testing all bits, the SAR contains a 10-bit binary code which accurately represents the input signal to within ½LSB (0.05% of full scale).

The SAR drives $\overline{DR}$ low to indicate that the conversion is complete and that the data is available to the output buffers. $\overline{HBE}$ and $\overline{LBE}$ can then be activated to enable the upper 8-bit and lower 2-bit buffers as desired. $\overline{HBE}$ and $\overline{LBE}$ should be brought high prior to the next conversion to place the output buffers in the high impedance state. Accuracy may be affected if $\overline{HBE}$ and $\overline{LBE}$ are in the enabled state during the conversion cycle.

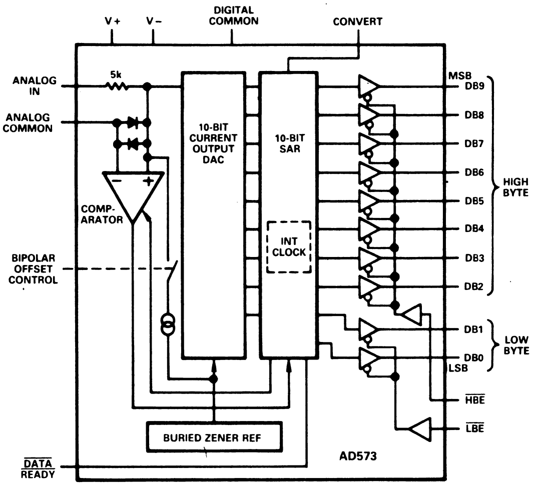


Figure 1. AD573 Functional Block Diagram

The temperature compensated buried Zener reference provides the primary voltage reference to the DAC and ensures excellent stability with both time and temperature. The bipolar offset input controls a switch which allows the positive bipolar offset current (exactly equal to the value of the MSB less ½LSB) to be injected into the summing (+) node of the comparator to offset the DAC output. Thus the nominal 0 to +10V unipolar input range becomes a −5V to +5V range. The 5kΩ thin film input resistor is trimmed so that with a full scale input signal, an input current will be generated which exactly matches the DAC output with all bits on.

UNIPOLAR CONNECTION

The AD573 contains all the active components required to perform a complete A/D conversion. Thus, for many applications, all that is necessary is connection of the power supplies (+5V and −15V), the analog input and the conversion start pulse. However, there are some features and special connections which should be considered for achieving optimum performance. The functional pin-out is shown in Figure 2.

The standard unipolar 0 to +10V range is obtained by shorting the bipolar offset control pin (pin 16) to digital common (pin 17).

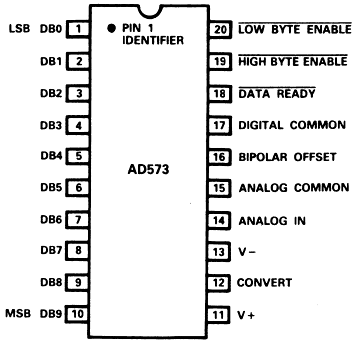


Figure 2. AD573 Pin Connections

Full Scale Calibration

The 5kΩ thin film input resistor is laser trimmed to produce a current which matches the full scale current of the internal DAC–plus about 0.3%–when an analog input voltage of 9.990 volts (10 volts − 1LSB) is applied at the input. The input resistor is trimmed in this way so that if a fine trimming potentiometer is inserted in series with the input signal, the input current at the full scale input voltage can be trimmed down to match the DAC full scale current as precisely as desired. However, for many applications the nominal 9.99 volt full scale can be achieved to sufficient accuracy by simply inserting a 15Ω resistor in series with the analog input to pin 14. Typical full scale calibration error will then be within ±2LSB or ±0.2%. If more precise calibration is desired, a 50Ω trimmer should be used instead. Set the analog input at 9.990 volts, and set the trimmer so that the output code is just at the transition between 1111111110 and 11111111. Each LSB will then have a weight of 9.766mV. If a nominal full scale of 10.24 volts is desired (which makes the LSB have weight of exactly 10.00mV), a 100Ω resistor and a 100Ω trimmer (or a 200Ω trimmer with good resolution) should be used. Of course, larger full scale ranges can be arranged by using a larger input resistor, but linearity and full scale temperature coefficient may be compromised if the external resistor becomes a sizeable percentage of 5kΩ. Figure 3 illustrates the connections required for full scale calibration.

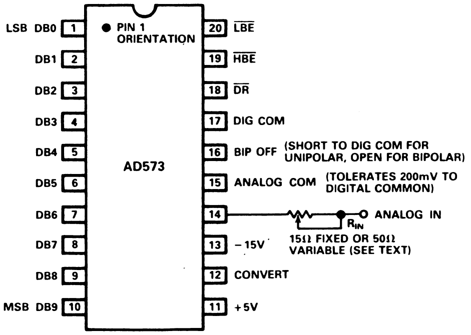


Figure 3. Standard AD573 Connections

Unipolar Offset Calibration

Since the Unipolar Offset is less than ± 1LSB for all versions of the AD573, most applications will not require trimming. Figure 4 illustrates two trimming methods which can be used if greater accuracy is necessary.

Figure 4a shows how the converter zero may be offset by up to ± 3 bits to correct the device initial offset and/or input signal offsets. As shown, the circuit gives approximately symmetrical adjustment in unipolar mode.

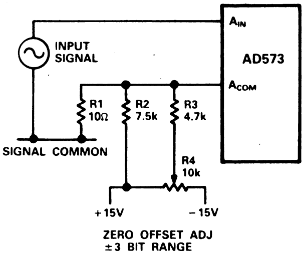


Figure 4a.

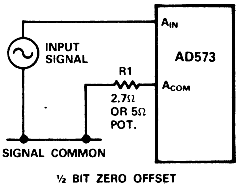


Figure 4b.

Figure 5 shows the nominal transfer curve near zero for an AD573 in unipolar mode. The code transitions are at the edges of the nominal bit weights. In some applications it will be preferable to offset the code transitions so that they fall between the nominal bit weights, as shown in the offset characteristics.

This offset can easily be accomplished as shown in Figure 4b. At balance (after a conversion) approximately 2ma flows into the analog Common terminal. A 2.7Ω resistor in series with this terminal will result in approximately the desired ½ bit offset of the transfer characteristics. The nominal 2mA Analog Common current is not closely controlled in manufacture. If high accuracy is required, a 5Ω potentiometer (connected as a rheostat) can be used as R1. Additional negative offset range may be obtained by using larger values of R1. Of course, if the zero transition point is changed, the full scale transition point will also move. Thus, if an offset of ½LSB is introduced, full scale trimming as described on the previous page should be done with an analog input of 9.985 volts.

NOTE: During a conversion transient currents from the Analog Common terminal will disturb the offset voltage. Capacitive decoupling should not be used around the offset network. These transients will settle as appropriate during a conversion. Capacitive decoupling will "pump up" and fail to settle resulting in conversion errors. Power supply decoupling which returns to analog signal common, should go to the signal input side of the resistive offset network.

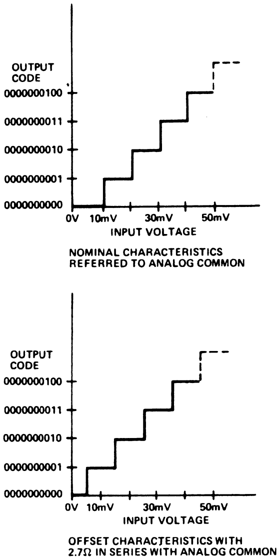


Figure 5. AD573 Transfer Curve – Unipolar Operation (Approximate Bit Weights Shown for Illustration, Nominal Bit Weights ~ 9.766mV)

BIPOLAR CONNECTION

To obtain the bipolar −5V to +5V range with an offset binary output code the bipolar offset control pin is left open.

A −5.00 volt signal will give a 10-bit code of 0000000000; an input of 0.00 volts results in an output code of 1000000000 and 4.99 volts at the input yields the 1111111111 code. The bipolar offset control input is not directly TTL compatible but a TTL interface for logic control can be constructed as shown in Figure 6.

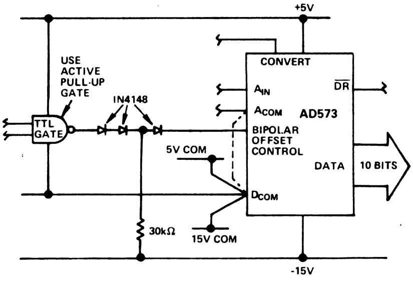


Figure 6. Bipolar Offset Controlled by Logic Gate
Gate Output = 1 Unipolar 0 – 10V Input Range
Gate Output = 0 Bipolar ±5V Input Range

Full Scale Calibration

Full Scale Calibration is accomplished in the same manner as in Unipolar operation except the full scale input voltage is 4.990 volts.

Negative Full Scale Calibration

The circuit in Figure 4a can also be used in Bipolar operation to offset the input voltage (nominally −5V) which results in the 0000000000 code. R2 should be omitted to obtain a symmetrical range.

GROUNDING CONSIDERATIONS

The AD573 provides separate Analog and Digital Common connections. The circuit will operate properly with as much as ±200mV of common mode voltage between the two commons. This permits more flexible control of system common bussing and digital and analog returns.

In normal operation the Analog Common terminal may generate transient currents of up to 2mA during a conversion. In addition a static current of about 2mA will flow into Analog Common in the unipolar mode after a conversion is complete. The Analog Common current will be modulated by the variations in input signal.

The absolute maximum voltage rating between the two commons is ±1 volt. It is recommended that the connection of a parallel pair of back-to-back protection diodes between the commons if they are not connected locally.

CONTROL AND TIMING OF THE AD573

CONVERT, $\overline{HBE}$ and $\overline{LBE}$ are the control pins. Timing for the conversion cycle is shown in Figure 7a. A positive pulse at least 500ns in width must be applied to the CONVERT pin to initiate the conversion. $\overline{DR}$ goes high within 1.5μs after the rising edge of the convert start pulse to indicate that the SAR is reset and goes low when the conversion is complete.

Read timing is shown in Figure 7b. The timing and control of the $\overline{LBE}$ and $\overline{HBE}$ pins are identical. Bringing $\overline{HBE}$ low activates the upper 8-bit 3 state buffer. Driving $\overline{LBE}$ low enables the lower 2-bit buffer.

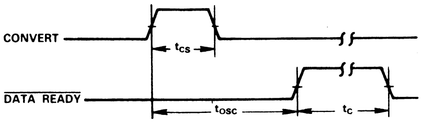


Figure 7a. Convert Timing

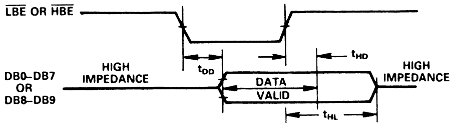


Figure 7b. Read Timing

TIMING SPECIFICATIONS

t_{CS}	500ns min
t_{DSC}	1.5μs max
t_C	10μs min 15μs typ 20μs max
t_{DD}	250ns max
t_{HD}	50ns min
t_{HL}	200ns max

Timing Reference Level is $\frac{V_{IN\,H} + V_{IN\,L}}{2}$ or $\frac{V_{OUT\,H} + V_{OUT\,L}}{2}$

Usually $\overline{HBE}$ and $\overline{LBE}$ are derived from an address decoder gated with the system RD, and often represent adjacent address locations in the microprocessor's memory map. The bit assignments for the two addresses are shown below:

$\overline{HBE}$	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2
$\overline{LBE}$	DB1	DB0	X	X	X	X	X	X

When the AD573 is connected directly to an 8-bit microprocessor bus the 2LSBs (pins 1 and 2) should be hardwired to the desired upper bits (usually the 2MSBs – pins 9 and 10). The six least significant bits of the low byte should be masked out by software to prevent meaningless data from being read. For example, a logical AND operation with 1100000000 will force the unused bits to logic 0.

For use with 16-bit microprocessors, $\overline{HBE}$ and $\overline{LBE}$ are tied together and all 10 data bits are enabled simultaneously The 10-bit word can then be placed either at the high end of the 16-bit word (left-justified format) or at the low end of the 16-bit word (right-justified).

Access time of the three-state buffers is 250ns maximum.

In systems where peripheral interface adapter chips are used, or where dedicated I/O ports exist (as in single-chip microcomputers), the AD573 may be used in a "stand-alone mode". In this mode, $\overline{DR}$ is hard-wired to $\overline{LBE}$ and $\overline{HBE}$ to disable the output buffers during conversion. Upon completion of the conversion cycle, $\overline{DR}$ enables the output drivers, and the 10-bit parallel data can be read.

SAMPLE-HOLD AMPLIFIER CONNECTION TO THE AD573

Many situations in high-speed acquisition systems or digitizing rapidly changing signals require a sample-hold amplifier (SHA) in front of the A-D converter. The SHA can acquire and hold a signal faster than the converter can perform a conversion. A SHA can also be used to accurately define the exact point in time at which the signal is sampled. For the AD573 a SHA can also serve as a high input impedance buffer.

Figure 8 shows the AD573 connected to the AD582 monolithic SHA for high speed signal acquisition. In this configuration, the AD582 will acquire a 10 volt signal in less than 10μs with a droop rate less than 100μV/ms.

$\overline{\text{DR}}$ goes high after the conversion is initiated to indicate that reset of the SAR is complete. In Figure 8 it is also used to put the AD582 into the hold mode while the AD573 begins its conversion cycle. (The AD582 settles to final value well in advance of the first comparator decision inside the AD573).

$\overline{\text{DR}}$ goes low when the conversion is complete placing the AD582 back in the sample mode. Configured as shown in Figure 8, the next conversion can be initiated after a 10μs delay to allow for signal acquisition by the AD582.

Observe carefully the ground, supply, and bypass capacitor connections between the two devices. This will minimize ground noise and interference during the conversion cycle.

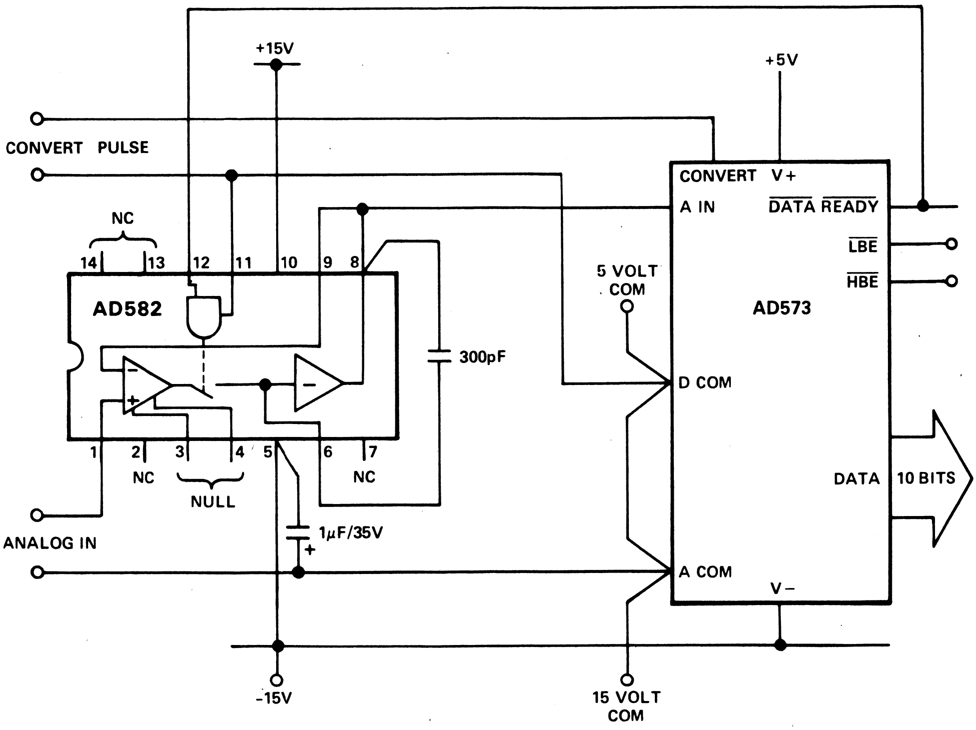


Figure 8. Sample-Hold Interface to the AD573

ANALOG DEVICES

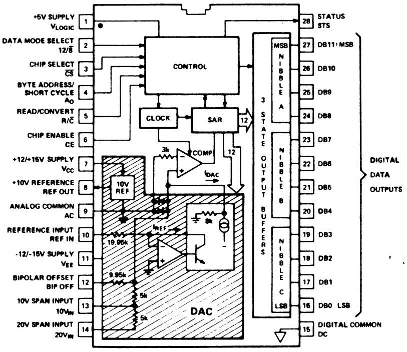
Fast, Complete 12-Bit A/D Converter with Microprocessor Interface

AD574A

FEATURES

- Complete 12-Bit A/D Converter with Reference and Clock
- Full 8- or 16-Bit Microprocessor Bus Interface
- 250ns Bus Access Time
- Guaranteed Linearity Over Temperature
  - 0 to +70°C – AD574AJ, AK, AL
  - −55°C to +125°C – AD574AS, AT, AU
- No Missing Codes Over Temperature
- Fast Successive Approximation Conversion – 25μs
- Buried Zener Reference for Long-Term Stability and Low Gain T.C. 10ppm/°C max AD574AL
  - 12.5ppm/°C max AD574AU
- Low Profile 28-Pin Ceramic DIP
- Low Power: 390mW
- Low Cost

AD574A FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD574A is a complete 12-bit successive-approximation analog-to-digital converter with 3-state output buffer circuitry for direct interface to an 8-, 12-or 16-bit microprocessor bus. The AD574A design is implemented with two LSI chips each containing both analog and digital circuitry, resulting in the maximum performance and flexibility at the lowest cost.

One chip is the high performance AD565A 12-bit DAC and voltage reference. It contains the high speed current output switching circuitry, laser-trimmed thin film resistor network, low T.C. buried zener reference and the precision input scaling and bipolar offset resistors. This chip is laser-trimmed at the wafer stage (LWT) to adjust ladder network linearity, voltage reference tolerance and temperature coefficient, and the calibration accuracy of input scaling and bipolar offset resistors.

The second chip uses the proven LCI (linear-compatible integrated injection logic) process to provide the low-power I^2L successive-approximation register, converter control circuitry, clock, bus interface, and the high performance latching comparator. The precision, low-drift comparator is adjusted for initial input offset error at the wafer stage by the "zener-zap" technique which trims the comparator input stage to 1/10 LSB typical error. This form of trimming, while cumbersome for complex ladder networks, is an attractive alternative to thin film resistor trimming for a simple offset adjustment and eliminates the need for thin film processing for this portion of the circuitry.

The AD574A is available in six different grades. The AD574AJ, AK, and AL grades are specified for operation over the 0 to +70°C temperature range. The AD574AS, AT, and AU are specified for the −55°C to +125°C range. All grades are packaged in a low-profile, 0.600 inch wide, 28-pin hermetically-sealed ceramic DIP.

PRODUCT HIGHLIGHTS

1. The AD574A interfaces to most popular microprocessors with an 8-, 12-, or 16-bit bus without external buffers or peripheral interface controllers. Multiple-mode three-state output buffers connect directly to the data bus while the read and convert commands are taken from the control bus. The 12-bits of output data can be read either as one 12-bit word or as two 8-bit bytes (one with 8 data bits, the other with 4 data bits and 4 trailing zeros).
2. The precision, laser-trimmed scaling and bipolar offset resistors provide four calibrated ranges, 0 to +10 and 0 to +20 volts unipolar, or −5 to +5 and −10 to +10 volts bipolar. Typical bipolar offset and full scale calibration of ±0.1% can be trimmed to zero with one external component each.
3. The internal buried zener reference is trimmed to 10.00 volts with 1% maximum error and 15ppm/°C typical T.C. The reference is available externally and can drive up to 1.5mA beyond that required for the reference and bipolar offset resistors.
4. The two-chip construction renders the AD574A inherently more reliable than hybrid multi-chip designs. All three military grades have guaranteed linearity error over the full −55°C to +125°C and are especially recommended for high performance needs in harsh environments. These units are available processed to MIL-STD-883B, Level B.

SPECIFICATIONS (typical @ +25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = -15V or -12V, unless otherwise specified)

DC AND TRANSFER ACCURACY SPECIFICATIONS

MODEL	AD574AJ	AD574AK	AD574AL	UNITS
RESOLUTION (max)	12	12	12	Bits
LINEARITY ERROR				
25°C (max)	±1	±1/2	±1/2	LSB
T_{min} to T_{max} (max)	±1	±1/2	±1/2	LSB
DIFFERENTIAL LINEARITY ERROR (Minimum resolution for which no missing codes are guaranteed)				
25°C	11	12	12	Bits
T_{min} to T_{max}	11	12	12	Bits
UNIPOLAR OFFSET (max) (Adjustable to zero)	±2	±2	±2	LSB
BIPOLAR OFFSET (max) (Adjustable to zero)	±10	±4	±4	LSB
FULL SCALE CALIBRATION ERROR (with fixed 50Ω resistor from REF OUT to REF IN)				
(Adjustable to zero) 25°C (max)	0.3	0.3	0.3	% of F.S.
T_{min} to T_{max} (Without Initial Adjustment)	0.5	0.4	0.35	% of F.S.
(With Initial Adjustment).	0.22	0.12	0.05	% of F.S.
TEMPERATURE RANGE		0 to +70		°C
TEMPERATURE COEFFICIENTS (Using internal reference)				
Guaranteed max change				
T_{min} to T_{max}				
Unipolar Offset	±2	±1	±1	LSB
	(10)	(5)	(5)	(ppm/°C)
Bipolar Offset	±2	±1	±1	LSB
	(10)	(5)	(5)	(ppm/°C)
Full Scale Calibration	±9	±5	±2	LSB
	(50)	(27)	(10)	(ppm/°C)
POWER SUPPLY REJECTION				
Max change in Full Scale Calibration				
$+13.5V \leqslant V_{CC} \leqslant +16.5V$ or $+11.4V \leqslant V_{CC} \leqslant +12.6V$	±2	±1	±1	LSB
$+4.5V \leqslant V_{LOGIC} \leqslant +5.5V$	±1/2	±1/2	±1/2	LSB
$-16.5V \leqslant V_{EE} \leqslant -13.5V$ or $-12.6V \leqslant V_{EE} \leqslant -11.4V$	±2	±1	±1	LSB
ANALOG INPUTS				
Input Ranges				
Bipolar		-5 to +5		Volts
		-10 to +10		Volts
Unipolar		0 to +10		Volts
		0 to +20		Volts
Input Impedance				
10 Volt Span		5k (3k min, 7k max)		Ω
20 Volt Span		10k (6k min, 14k max)		Ω
POWER SUPPLIES				
Operating Range				
V_{LOGIC}		+4.5 to +5.5		Volts
V_{CC}		+11.4 to +16.5		Volts
V_{EE}		-11.4 to -16.5		Volts
Operating Current				
I_{LOGIC}		30 typ, 40 max		mA
I_{CC}		2 typ, 5 max		mA
V_{EE}		18 typ, 30 max		mA
POWER DISSIPATION		390 typ, 725 max		mW
INTERNAL REFERENCE VOLTAGE		10.00 ±0.1 (max)		Volts
Output Current (available for external loads) (External load should not change during conversion)		1.5 max[1]		mA
PACKAGE TYPE[2]		D28A		

NOTES

[1] The reference should be buffered for operation on ±12V supplies.

[2] See Section 20 for package outline information.

Specifications subject to change without notice.

DC AND TRANSFER ACCURACY SPECIFICATIONS

MODEL	AD574AS	AD574AT	AD574AU	UNITS
RESOLUTION (max)	12	12	12	Bits
LINEARITY ERROR				
25°C (max)	±1	±1/2	±1/2	LSB
-25°C to +85°C (max)	±1	±1/2	±1/2	LSB
-55°C to +125°C (max)	±1	±1	±1	LSB
DIFFERENTIAL LINEARITY ERROR (Minimum resolution for which no missing codes are guaranteed)				
25°C	11	12	12	Bits
T_{min} to T_{max}	11	12	12	Bits
UNIPOLAR OFFSET (max) (Adjustable to zero)	±2	±2	±2	LSB
BIPOLAR OFFSET (max) (Adjustable to zero)	±10	±4	±4	LSB
FULL SCALE CALIBRATION ERROR (with fixed 50Ω resistor from REF IN to REF OUT)				
(Adjustable to zero) 25°C (max)	0.3	0.3	0.3	% of F.S.
T_{min} to T_{max} (Without Initial Adjustment)	0.8	0.6	0.4	% of F.S.
(With Initial Adjustment)	0.5	0.25	0.12	% of F.S.
TEMPERATURE RANGE	-55 to +125			°C
TEMPERATURE COEFFICIENTS (using internal reference)				
Guaranteed max change				
T_{min} to T_{max}				
Unipolar Offset	±2	±1	±1	LSB
	(5)	(2.5)	(2.5)	(ppm/°C)
Bipolar Offset	±4	±2	±1	LSB
	(10)	(5)	(2.5)	(ppm/°C)
Full Scale Calibration	±20	±10	±5	LSB
	(50)	(25)	(12.5)	(ppm/°C)
POWER SUPPLY REJECTION				
Max change in Full Scale Calibration				
$+13.5V \leqslant V_{CC} \leqslant +16.5V$ or $+11.4V \leqslant V_{CC} \leqslant +12.6V$	±2	±1	±1	LSB
$+4.5V \leqslant V_{LOGIC} \leqslant +5.5V$	±1/2	±1/2	±1/2	LSB
$-16.5V \leqslant V_{EE} \leqslant -13.5V$ or $-12.6V \leqslant V_{EE} \leqslant -11.4V$	±2	±1	±1	LSB
ANALOG INPUTS				
Input Ranges				
Bipolar	-5 to +5			Volts
	-10 to +10			Volts
Unipolar	0 to +10			Volts
	0 to +20			Volts
Input Impedance				
10 Volt Span	5k (3k min, 7k max)			Ω
20 Volt Span	10k (6k min, 14k max)			Ω
POWER SUPPLIES				
Operating Range				
V_{LOGIC}	+4.5 to +5.5			Volts
V_{CC}	+11.4 to +16.5			Volts
V_{EE}	-11.4 to -16.5			Volts
Operating Current				
I_{LOGIC}	30 typ, 40 max			mA
I_{CC}	2 typ, 5 max			mA
I_{EE}	18 typ, 30 max			mA
POWER DISSIPATION	390 typ, 725 max			mW
INTERNAL REFERENCE VOLTAGE	10.00 ±0.1 (max)			Volts
Output Current (available for external loads) (External load should not change during conversion)	1.5max[1]			mA
PACKAGE TYPE[2]	D28A			

NOTES

[1] The reference should be buffered for operation on ±12V supplies.

[2] See Section 20 for package outline information.

Specifications subject to change without notice.

DIGITAL CHARACTERISTICS[1] (All grades, $T_{min} - T_{max}$)

	Min	Typ	Max	
Logic Inputs[2] (CE, $\overline{CS}$, R/$\overline{C}$, A_O)				
Voltages				
Logic "1"	+2.0V		+5.5V	
Logic "0"	−0.5V		+0.8V	
Current	−50µA		+50µA	
Capacitance		5pF		
Logic Outputs (DB11–DB0, STS)				
Logic "0"			+0.4V	$I_{SINK} \leq 1.6mA$
Logic "1"	2.4V			$I_{SOURCE} \leq 500\mu A$
Leakage (When in high-Z state)	−40µA		+40µA	DB11 – DB0 Only
Capacitance		5pF		

[1] Detailed Timing Specifications appear in the Digital Interface Section.

[2] 12/$\overline{8}$ Input is not TTL-compatible and must be hard-wired to V_{LOGIC} or DIGITAL COMMON.

ABSOLUTE MAXIMUM RATINGS

(Specifications apply to all grades, except where noted)

V_{CC} to Digital Common	0 to +16.5V
V_{EE} to Digital Common	0 to −16.5V
V_{LOGIC} to Digital Common	0 to +7V
Analog Common to Digital Common	±1V
Control Inputs (CE, $\overline{CS}$, A_O, 12/$\overline{8}$, R/$\overline{C}$) to Digital Common	−0.5V to V_{LOGIC} +0.5V
Analog Inputs (REF IN, BIP OFF, $10V_{IN}$) to Analog Common	±16.5V
$20V_{IN}$ to Analog Common	±24V
REF OUT	Indefinite short to common Momentary short to V_{CC}
Chip Temperature (J, K, L grades)	100°C
(S, T, U grades)	150°C
Power Dissipation	1000mW
Lead Temperature, Soldering	300°C, 10 sec.
Storage Temperature	−65°C to +150°C
Thermal Resistance, θ_{JA}	60°C/W

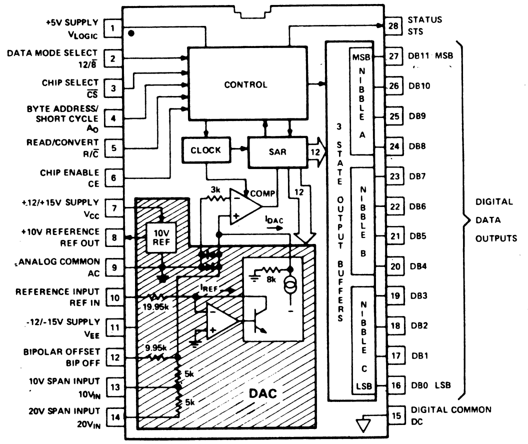


Figure 1. AD574A Block Diagram and Pin Configuration

AD574A ORDERING GUIDE

Model	Temp. Range	Linearity Error Max (T_{min} to T_{max})	Resolution No Missing Codes (T_{min} to T_{max})	Max Full Scale T.C. (ppm/°C)
AD574AJD	0 to +70°C	±1LSB	11 Bits	50.0
AD574AKD	0 to +70°C	±½LSB	12 Bits	27.0
AD574ALD	0 to +70°C	±½LSB	12 Bits	10.0
AD574ASD	−55°C to +125°C	±1LSB	11 Bits	50.0
AD574ASD/883B	−55°C to +125°C	±1LSB	11 Bits	50.0
AD574ATD	−55°C to +125°C	±1LSB	12 Bits	25.0
AD574ATD/883B	−55°C to +125°C	±1LSB	12 Bits	25.0
AD574AUD	−55°C to +125°C	±1LSB	12 Bits	12.5
AD574AUD/883B	−55°C to +125°C	±1LSB	12 Bits	12.5

THE AD574A OFFERS GUARANTEED MAXIMUM LINEARITY ERROR OVER THE FULL OPERATING TEMPERATURE RANGE

DEFINITIONS OF SPECIFICATIONS

LINEARITY ERROR

Linearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale". The point used as "zero" occurs ½LSB (1.22mV for 10 volt span) before the first code transition (all zeros to only the LSB "on"). "Full scale" is defined as a level 1½LSB beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The AD574AK, AL, AT, and AU grades are guaranteed for maximum nonlinearity of ±½LSB. For these grades, this means that an analog value which falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The AD574AJ and AS grades are guaranteed to ±1LSB max error. For these grades, an analog value which falls within a given code width will result in either the correct code for that region or either adjacent one.

Note that the linearity error is not user-adjustable.

DIFFERENTIAL LINEARITY ERROR (NO MISSING CODES)

A specification which guarantees no missing codes requires that every code combination appear in a monotonic increasing sequence as the analog input level is increased. Thus every code must have a finite width. For the AD574AK, AL, AT, and AU grades, which guarantee no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temperature ranges. The AD574AJ and AS grades guarantee no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11 bits must be present; in practice very few of the 12-bit codes are missing.

UNIPOLAR OFFSET

The first transition should occur at a level ½LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following two pages. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with or without external adjustment.

BIPOLAR OFFSET

Similarly, in the bipolar mode, the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value ½LSB below analog common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over temperature.

FULL SCALE CALIBRATION ERROR

The last transition (from 1111 1111 1110 to 1111 1111 1111) should occur for an analog value 1½LSB below the nominal full scale (9.9963 volts for 10.000 volts full scale). The full scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which is typically 0.05 to 0.1% of full scale, can be trimmed out as shown in Figure 5. The full scale calibration error over temperature is given with and without the initial error trimmed out. The temperature coefficients for each grade indicate the maximum change in the full scale gain from the initial value using the internal 10 volt reference.

TEMPERATURE COEFFICIENTS

The temperature coefficients for full-scale calibration, unipolar offset, and bipolar offset specify the maximum change from the initial (25°C) value to the value at T_{min} or T_{max}.

POWER SUPPLY REJECTION

The standard specifications for the AD574A assume use of +5.00 and ±15.00 or ±12.00 volt supplies. The only effect of power supply error on the performance of the device will be a small change in the full scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum change in calibration from the initial value with the supplies at the various limits.

CODE WIDTH

A fundamental quantity for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 least significant bit (LSB) of the full scale range or 2.44mV out of 10 volts for a 12-bit ADC.

QUANTIZATION UNCERTAINTY

Analog-to-digital converters exhibit an inherent quantization uncertainty of ±½LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of given resolution.

LEFT–JUSTIFIED DATA

The data format used in the AD574A is left-justified. This means that the data represents the analog input as a fraction of full-scale, ranging from 0 to $\frac{4095}{4096}$. This implies a binary point to the left of the MSB.

CIRCUIT OPERATION

The AD574A is a complete 12-bit A/D converter which requires no external components to provide the complete successive-approximation analog-to-digital conversion function. A block diagram of the AD574A is shown in Figure 2. The device consists of two chips, one containing the precision 12-bit DAC with voltage reference, the other containing the comparator, successive-approximation register, clock, output buffers and control circuitry.

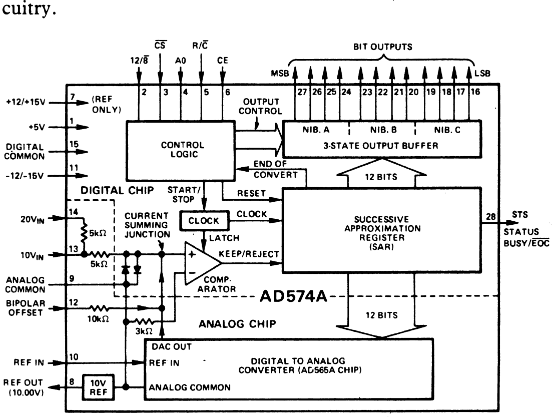


Figure 2. Block Diagram of AD574A 12-Bit A-to-D Converter

When the control section is commanded to initiate a conversion (as described later), it then enables the clock and resets the successive-approximation register (SAR) to all zeros. Once a conversion cycle has begun, it cannot be stopped or re-started and data is not available from the output buffers. The SAR, timed by the clock, will then sequence through the conversion cycle and return an end-of-convert flag to the control section. The control section will then disable the clock, bring the output status flag low, and enable control functions to allow data read functions by external command.

During the conversion cycle, the internal 12-bit current output DAC is sequenced by the SAR from the most-significant-bit (MSB) to least-significant-bit (LSB) to provide an output current which accurately balances the input signal current through the 5kΩ (or 10kΩ) input resistor. The comparator determines whether the addition of each successively-weighted bit current causes the DAC current sum to be greater or less than the input current; if the sum is less, the bit is left on; if more, the bit is turned off. After testing all the bits, the SAR contains a 12-bit binary code which accurately represents the input signal to within ±½LSB.

The temperature-compensated buried Zener reference provides the primary voltage reference to the DAC and guarantees excellent stability with both time and temperature. The reference is trimmed to 10.00 volts ±1%; it can supply up to 1.5mA to an external load in addition to that required to drive the reference input resistor (0.5mA) and bipolar offset resistor (1mA) when the AD574A is powered from ±15V supplies. If the AD574A is used with ±12V supplies, or if external current must be supplied over the full temperature range, an external buffer amplifier is recommended. Any external load on the AD574A reference must remain constant during conversion. The thin film application resistors are trimmed to match the full scale output current of the DAC. There are two 5kΩ input scaling resistors to allow either a 10 volt or 20 volt span. The 10kΩ bipolar offset resistor is grounded for unipolar operation or connected to the 10 volt reference for bipolar operation.

DRIVING THE AD574A ANALOG INPUT

The AD574A is a successive-approximation type analog-to-digital converter. During the conversion cycle, the ADC input current is modulated by the DAC test current at approximately a 500kHz rate. Thus it is important to recognize that the signal source driving the AD574A must be capable of holding a constant output voltage under dynamically–changing load conditions.

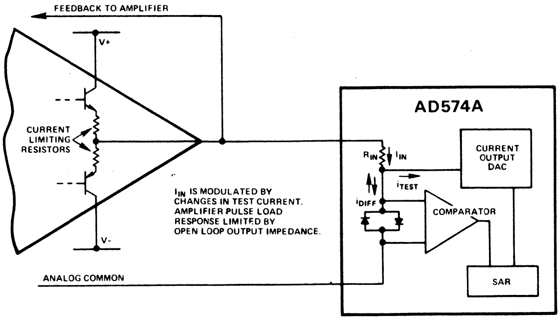

FEEDBACK TO AMPLIFIER
V+
CURRENT LIMITING RESISTORS
V-
ANALOG COMMON
AD574A
R_{IN}
I_{IN}
CURRENT OUTPUT DAC
i_{TEST}
i_{DIFF}
COMPARATOR
SAR
I_{IN} IS MODULATED BY CHANGES IN TEST CURRENT. AMPLIFIER PULSE LOAD RESPONSE LIMITED BY OPEN LOOP OUTPUT IMPEDANCE.

Figure 3. Op Amp – AD574A Interface

The closed loop output impedance of an op amp is equal to the open loop output impedance (usually a few hundred ohms) divided by the loop gain at the frequency of interest. It is often assumed that the loop gain of a follower-connected op amp is sufficiently high to reduce the closed loop output impedance to a negligibly small value, particularly if the signal is low frequency. However, the amplifier driving an AD574A must either have sufficient loop gain at 500kHz to reduce the closed loop output impedance to a low value or have low open loop output impedance.

This can be accomplished either by using a wideband op amp or by placing a discrete-transistor or integrated buffer inside the amplifier's feedback loop.

SUPPLY DECOUPLING AND LAYOUT CONSIDERATIONS

It is critically important that the AD574A power supplies be filtered, well-regulated, and free from high frequency noise. Use of noisy supplies will cause unstable output codes to be generated. Switching power supplies are not recommended for circuits attempting to achieve 12-bit accuracy unless great care is used in filtering any switching spikes present in the output. Remember that a few millivolts of noise represents several counts of error in a 12-bit ADC.

Decoupling capacitors should be used on all power supply pins; the +5V supply decoupling capacitor should be connected directly from pin 1 to pin 15 (digital common) and the $+V_{CC}$ and $-V_{EE}$ pins should be decoupled directly to analog common (pin 9). A suitable decoupling capacitor is a 47μF tantalum type in parallel with a 0.1μF disc ceramic type.

Circuit layout should attempt to locate the AD574A, associated analog input circuitry, and interconnections as far as possible from logic circuitry. For this reason, the use of wire-wrap circuit construction is not recommended. Careful printed-circuit construction is preferred.

UNIPOLAR RANGE CONNECTIONS FOR THE AD574A

The AD574A contains all the active components required to perform a complete 12-bit A/D conversion. Thus, for most situations, all that is necessary is connection of the power supplies (+5, +12/+15 and −12/−15 volts), the analog input, and the conversion initiation command, as discussed on the next page. Analog input connections and calibration are easily accomplished; the unipolar operating mode is shown in Figure 4.

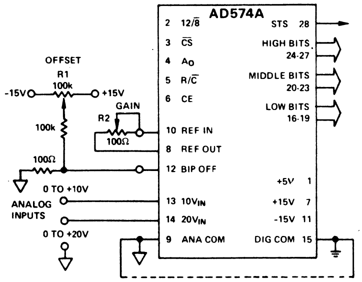


Figure 4. Unipolar Input Connections

All of the thin film application resistors of the AD574A are trimmed for absolute calibration. Therefore, in many applications, no calibration trimming will be required. The absolute accuracy for each grade is given in the specification tables. For example, if no trims are used, the AD574AK guarantees ±2LSB max zero offset error and ±0.3% (12LSB) max full scale error. (Typical full scale error is ±2LSB.) If the offset trim is not required, pin 12 can be connected directly to pin 9; the two resistors and trimmer for pin 12 are then not needed. If the full scale trim is not needed, a 50Ω ±1% metal film resistor should be connected between pin 8 and pin 10.

The analog input is connected between pin 13 and pin 9 for a 0 to +10V input range, between 14 and pin 9 for a 0 to +20V input range. The AD574A easily accommodates an input signal beyond the supplies. For the 10 volt span input, the LSB has a nominal value of 2.44mV, for the 20 volt span, 4.88mV. If a 10.24V range is desired (nominal 2.5mV/bit), the gain trimmer (R2) should be replaced by a 50Ω resistor, and a 200Ω trimmer inserted in series with the analog input to pin 13 (for a full scale range of 20.48V (5mV/bit), use a 500Ω trimmer into pin 14). The gain trim described below is now done with these trimmers. The nominal input impedance into pin 13 is 5kΩ, and 10kΩ into pin 14.

UNIPOLAR CALIBRATION

The AD574A is intended to have a nominal ½LSB offset so that the exact analog input for a given code will be in the middle of that code (halfway between the transitions to the codes above and below it). Thus, when properly calibrated, the first transition (from 0000 0000 0000 to 0000 0000 0001) will occur for an input level of +½LSB (1.22mV for 10V range).

If pin 12 is connected to pin 9, the unit typically will behave in this manner, within specifications. If the offset trim (R1) is used, it should be trimmed as above, although a different offset can be set for a particular system requirement. This circuit will give approximately ± 15mV of offset trim range.

The full scale trim is done by applying a signal 1½LSB below the nominal full scale (9.9963 for a 10V range). Trim R2 to give the last transition (1111 1111 1110 to 1111 1111 1111).

BIPOLAR OPERATION

The connections for bipolar ranges are shown in Figure 5. Again, as for the unipolar ranges, if the offset and gain specifications are sufficient, one or both of the trimmers shown can be replaced by a 50Ω ± 1% fixed resistor. The analog input is applied as for the unipolar ranges. Bipolar calibration is similar to unipolar calibration. First, a signal ½LSB above negative full scale (−4.9988V for the ± 5V range) is applied and R1 is trimmed to give the first transition (0000 0000 0000 to 0000 0000 0001). Then a signal 1½LSB below positive full scale (+4.9963V for the ± 5V range) is applied and R2 trimmed to give the last transition (1111 1111 1110 to 1111 1111 1111).

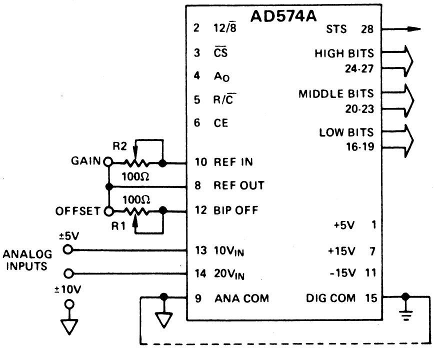


Figure 5. Bipolar Input Connections

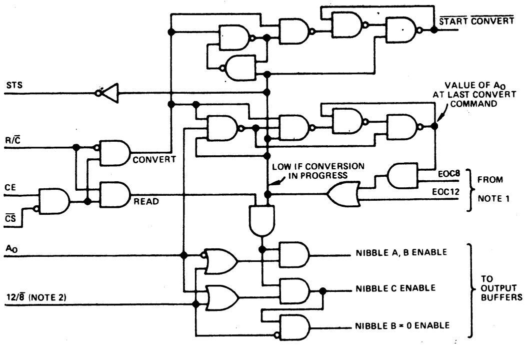
GROUNDING CONSIDERATIONS

The analog common at pin 9 is the ground reference point for the internal reference and is thus the "high quality" ground for the AD574A; it should be connected directly to the analog reference point of the system. In order to achieve all of the high accuracy performance available from the AD574A in an environment of high digital noise content, it is required that the analog and digital commons be connected together at the package. In some situations, the digital common at pin 15 can be connected to the most convenient ground reference point; analog power return is preferred.

CONVERSION START/DATA READ CONTROL LOGIC

The AD574A contains on-chip logic to provide conversion initiation and data read operations from signals commonly available in microprocessor systems. Figure 6 shows the internal logic circuitry of the AD574A.

The control signals CE, $\overline{CS}$, and R/$\overline{C}$ control the operation of the converter. The state of R/$\overline{C}$ when CE and $\overline{CS}$ are both asserted determines whether a data read (R/$\overline{C}$ = 1) or a convert (R/$\overline{C}$ = 0) is in progress. The register control inputs A_O and 12/$\overline{8}$ control conversion length and data format. The A_O line is usually tied to the least significant bit of the address bus. If a conversion is started with A_O low, a full 12-bit conversion cycle is initiated. If A_O is high during a convert start, a shorter 8-bit conversion cycle results. During data read operations, A_O determines whether the three-state buffers containing the 8 MSBs of the conversion result (A_O = 0) or the 4 LSBs (A_O = 1) are enabled. The 12/$\overline{8}$ pin determines whether the output data is to be organized as two 8-bit words (12/$\overline{8}$ tied to DIGITAL COMMON) or a single 12-bit word (12/$\overline{8}$ tied to VLOGIC). The 12/$\overline{8}$ pin is not TTL-compatible and must be hard-wired to either VLOGIC or DIGITAL COMMON. In the 8-bit mode, the byte addressed when A_O is high contains the 4 LSBs from the conversion followed by four trailing zeroes. This organization allows the data lines to be overlapped for direct interface to 8-bit buses without the need for external three-state buffers.



NOTE 1: WHEN $\overline{\text{START CONVERT}}$ GOES LOW, THE EOC (END OF CONVERSION) SIGNALS GO LOW. EOC8 RETURNS HIGH AFTER AN 8-BIT CONVERSION CYCLE IS COMPLETE, AND EOC12 RETURNS HIGH WHEN ALL 12 BITS HAVE BEEN CONVERTED. THE EOC SIGNALS PREVENT DATA FROM BEING READ DURING CONVERSIONS.

NOTE 2: 12/$\overline{8}$ IS NOT A TTL COMPATIBLE INPUT AND SHOULD ALWAYS BE WIRED DIRECTLY TO V_{LOGIC} OR DIGITAL COMMON.

Figure 6. AD574A Control Logic

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_O	Operation
0	X	X	X	X	None
X	1	X	X	X	None
1	0	0	X	0	Initiate 12-Bit Conversion
1	0	0	X	1	Initiate 8-Bit Conversion
1	0	1	Pin 1	X	Enable 12-Bit Parallel Output
1	0	1	Pin 15	0	Enable 8 Most Significant Bits
1	0	1	Pin 15	1	Enable 4LSBs + 4 Trailing Zeroes

Table 1. AD574A Truth Table

It is not recommended that A_O change state during a data read operation. Asymmetrical enable and disable times of the three-state buffers could cause internal bus contention resulting in potential damage to the AD574A.

An output signal, STS, indicates the status of the converter. STS goes high at the beginning of a conversion and returns low when the conversion cycle is complete.

TIMING

The AD574 is easily interfaced to a wide variety of microprocessors and other digital systems. Discussion of the timing requirements of the AD574A control signals will provide the system designer with useful insight into the operation of the device.

Figure 7 shows a complete timing diagram for the AD574A convert start operation. R/$\overline{C}$ should be low before both CE and $\overline{CS}$ are asserted; if R/$\overline{C}$ is high, a read operation will momentarily occur, possibly resulting in system bus contention. Either CE or $\overline{CS}$ may be used to initiate a conversion. As shown in Figure 7, CE is used. If $\overline{\text{CS}}$ is used to trigger conversion or if the specified set-up times are not met, appropriately longer pulses are necessary (to provide at least 200ns when R/$\overline{\text{C}}$, CE, and $\overline{\text{CS}}$ are all valid). Note that CE includes one less propagation delay than $\overline{\text{CS}}$ and is therefore the faster input.

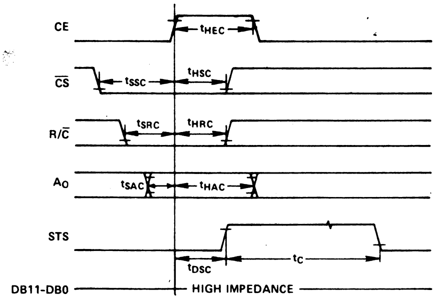


Figure 7. Convert Start Timing

Once a conversion is started and the STS line goes high, convert start commands will be ignored until the conversion cycle is complete. The output data buffers cannot be enabled during conversion.

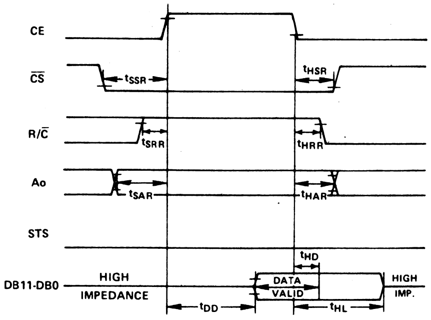


Figure 8. Read Cycle Timing

Figure 8 shows the timing for data read operatons. The AD574A differs from the original AD574 design in that the three-state output buffers feature faster access time and shorter data latency times. This speed improvement simplifies the interface to faster microprocessors. During data read operations, access time is measured from the point where CE and R/$\overline{\text{C}}$ both are high (assuming $\overline{\text{CS}}$ is already low). If $\overline{\text{CS}}$ is used to enable the device, access time is extended by 100ns.

In the 8-bit bus interface mode (12/$\overline{8}$ input wired to DIGITAL COMMON), the address bit, A_O, must be stable at least 150ns prior to $\overline{\text{CE}}$ going high and must remain stable during the entire read cycle. If A_O is allowed to change, damage to the AD574A output buffers may result.

"STAND-ALONE" OPERATION

The AD574A can be used in a "stand-alone" mode, which is useful in systems with dedicated input ports available and thus not requiring full bus interface capability.

AD574A TIMING SPECIFICATIONS

Symbol	Parameter	Min	Typ	Max	Units
CONVERT MODE					
t_{DSC}	STS Delay from CE			300	ns
t_{HEC}	CE Pulse Width	300			ns
t_{SSC}	$\overline{\text{CS}}$ to CE Setup	300			ns
t_{HSC}	$\overline{\text{CS}}$ Low During CE High	200			ns
t_{SRC}	R/$\overline{\text{C}}$ to CE Setup	250			ns
t_{HRC}	R/$\overline{\text{C}}$ Low During CE High	200			ns
t_{SAC}	A_O to CE Setup	0			ns
t_{HAC}	A_O Valid During CE High	300			ns
t_C	Conversion Time				
	8-Bit Cycle	10		24	µs
	12-Bit Cycle	15		35	µs
READ MODE					
t_{DD}	Access Time (from CE)		210	250	ns
t_{HD}	Data Valid after CE Low	25			ns
t_{HL}	Output Float Delay		110	150	ns
t_{SSR}	$\overline{\text{CS}}$ to CE Setup	150			ns
t_{SRR}	R/$\overline{\text{C}}$ to CE Setup	0			ns
t_{SAR}	A_O to CE Setup	150			ns
t_{HSR}	$\overline{\text{CS}}$ Valid After CE Low	50			ns
t_{HRR}	R/$\overline{\text{C}}$ High After CE Low	0			ns
t_{HAR}	A_O Valid After CE low	50			ns

In this mode, CE and 12/$\overline{8}$ are wired high, $\overline{\text{CS}}$ and A_O are wired low, and conversion is controlled by R/$\overline{\text{C}}$. The three-state buffers are enabled when R/$\overline{\text{C}}$ is high and a conversion starts when R/$\overline{\text{C}}$ goes low. This gives rise to two possible control signals–a high pulse or a low pulse. Operation with a low pulse is shown in Figure 9. In this case, the outputs are forced into the high-impedance state in response to the falling edge of R/$\overline{\text{C}}$ and return to valid logic levels after the conversion cycle is completed. The STS line goes high 500ns after R/$\overline{\text{C}}$ goes low and returns low 300ns after data is valid.

If conversion is initiated by a high pulse as shown in Figure 10, the data lines are enabled during the time when R/$\overline{\text{C}}$ is high. The falling edge of R/$\overline{\text{C}}$ starts the next conversion and the data lines return to three-state (and remain three-state) until the next high pulse of R/$\overline{\text{C}}$.

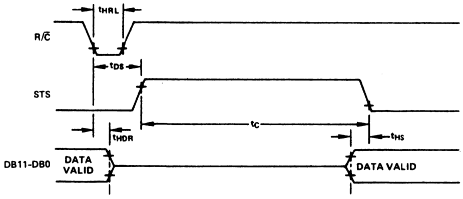


Figure 9. Low Pulse for R/$\overline{\text{C}}$ – Outputs Enabled After Conversion

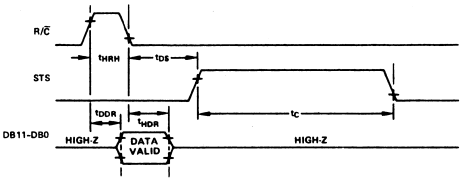


Figure 10. High Pulse for R/$\overline{\text{C}}$ – Outputs Enabled While R/$\overline{\text{C}}$ High, Otherwise High-Z

STAND-ALONE MODE TIMING

Symbol	Parameter	Min	Typ	Max	Units
t_{HRL}	Low R/$\overline{\text{C}}$ Pulse Width	350			ns
t_{DS}	STS Delay from R/$\overline{\text{C}}$			500	ns
t_{HDR}	Data Valid After R/$\overline{\text{C}}$ Low	25			ns
t_{HS}	STS Delay After Data Valid	300		1000	ns
t_{HRH}	High R/$\overline{\text{C}}$ Pulse Width	250			ns
t_{DDR}	Data Access Time			250	ns

ANALOG DEVICES

Very Fast, Complete 12-Bit A/D Converter

AD578

FEATURES

Performance

- **Complete 12-Bit A/D Converter with Reference and Clock**
- **Fast Successive Approximation Conversion: 3μs**
- **Buried Zener Reference for Long Term Stability and Low Gain T.C.: ±30ppm/°C max**
- **Max Nonlinearity: <±0.012%**
- **Low Power: 775mW**
- **Hermetic Package Available**

Versatility

- **Positive-True Parallel or Serial Logic Outputs**
- **Short Cycle Capability**
- **Precision +10V Reference for External Applications**
- **Adjustable Internal Clock**
- **"Z" Models for ±12V Supplies**

PRODUCT DESCRIPTION

The AD578 is a high speed low cost 12-bit successive approximation analog-to-digital converter that includes an internal clock, reference and comparator. Its hybrid IC design utilizes MSI digital and linear monolithic chips in conjunction with a 12-bit monolithic DAC to provide modular performance and versatility with IC size, price and reliability.

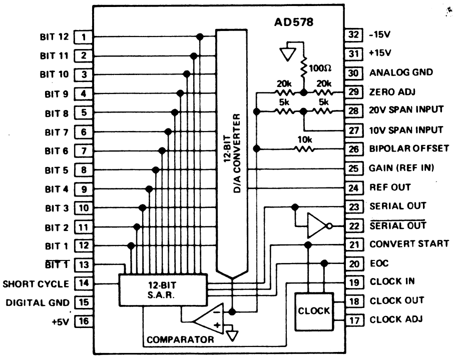
Important performance characteristics of the AD578 include a maximum linearity error at +25°C of ±0.012%, maximum gain temperature coefficient of ±30ppm/°C, typical power dissipation of 775mW and maximum conversion time of 3μs.

The fast conversion speeds of 3μs (L grade) 4.5μs (K grade) and 6μs (J grade) make the AD578 an excellent choice in a variety of applications where system throughput rates from 166kHz to 333kHz are required. In addition, it may be short cycled to obtain faster conversion speeds at lower resolutions.

The design of the AD578 includes scaling resistors that provide analog input signal ranges of ±5V, ±10V, 0 to +10V or 0 to +20V. Adding flexibility and value is the +10V precision reference which can be used for external applications.

The AD578 is available with either the polymer seal (N) for use in benign environmental applications or solder-seal (D) for more harsh or rigorous surroundings. Both are contained in a 32-pin side-brazed, ceramic DIP.

AD578 FUNCTIONAL BLOCK DIAGRAM



32 PIN DIP

PRODUCT HIGHLIGHTS

1. The AD578 is a complete 12-bit A/D converter. No external components are required to perform a conversion.
2. The fast conversion rate of the AD578 makes it an excellent choice for high speed data acquisition and digital audio processing applications.
3. The internal buried zener reference is laser trimmed to 10.00V ±0.1% and ±15ppm/°C typical T.C. The reference is available externally and can provide up to 1mA.
4. The scaling resistors are included on the monolithic DAC for exceptional thermal tracking.
5. Short cycle and external clock capabilities are provided for applications requiring faster conversion speeds and/or lower resolutions.
6. The integrated package construction provides high quality and reliability with small size and weight.

SPECIFICATIONS (typical @ +25°C; ±15V, and +5V unless otherwise noted).

Model	AD578J	AD578K	AD578L
RESOLUTION	12 Bits	*	*
ANALOG INPUTS			
Voltage Ranges			
Bipolar	±5.0V, ±10V	*	*
Unipolar	0 to +10V, 0 to +20V	*	*
Input Impedance			
0 to +10V, ±5V	5kΩ	*	*
±10V, 0 to +20V	10kΩ	*	*
DIGITAL INPUTS			
Convert Command[1]	1LS TTL Load	*	*
Clock Input	1LS TTL Load	*	*
TRANSFER CHARACTERISTICS			
Gain Error[2,3]	±0.1% FSR, ±0.25% FSR max	*	*
Unipolar Offset[3]	±0.1% FSR, ±0.25% FSR max	*	*
Bipolar Offset[3,4]	±0.1% FSR, ±0.25% FSR max	*	*
Linearity Error			
+25°C	±1/2LSB max	*	*
0 to +70°C	±3/4LSB max	*	*
DIFFERENTIAL LINEARITY ERROR (Minimum resolution for which no missing codes are guaranteed)			
+25°C	12 Bits	*	*
0 to +70°C	12 Bits	*	*
POWER SUPPLY SENSITIVITY			
+15V ±10%	3ppm/%ΔV_S typ	*	*
	10ppm/%ΔV_S max	*	*
-15V ±10%	15ppm/%ΔV_S typ	*	*
	25ppm/%ΔV_S max	*	*
+5V ±10%	2ppm/%ΔV_S typ	*	*
	10ppm/%ΔV_S max	*	*
TEMPERATURE COEFFICIENTS			
Gain	±15ppm/°C typ	*	*
	±30ppm/°C max	*	*
Unipolar Offset	±3ppm/°C typ	*	*
	±10ppm/°C max	±5ppm/°C max	**
Bipolar Offset	±8ppm/°C typ	*	*
	±20ppm/°C max	±15ppm/°C max	**
Differential Linearity	±2ppm/°C typ	*	*
CONVERSION TIME[5,6] (max)	6.0μs	4.5μs	3μs
PARALLEL OUTPUTS			
Unipolar Code	Binary	*	*
Bipolar Code	Offset Binary/Two's Complement	*	*
Output Drive	2TTL Loads	*	*
SERIAL OUTPUTS (NRZ FORMAT)			
Unipolar Code	Binary/Complementary Binary	*	*
Bipolar Code	Offset Binary/Comp. Offset Binary	*	*
Output Drive	2TTL Loads	*	*
END OF CONVERSION (EOC)	Logic "1" During Conversion	*	*
Output Drive	8TTL Loads	*	*
INTERNAL CLOCK[7]			
Output Drive	2TTL Loads	*	*
INTERNAL REFERENCE			
Voltage	10.000 ± 10mV	*	*
External Current	±1mA max	*	*
POWER SUPPLY REQUIREMENTS			
Range for Rated Accuracy	4.75 to 5.25 and ±13.5 to ±16.5	*	*
Z Models[8]	4.75 to 5.25 and ±11.8 to ±16.5	*	*
Supply Current +15V	3mA typ, 8mA max	*	*
-15V	22mA typ, 35mA max	*	*
+5V	80mA typ, 110mA max	*	*
Power Dissipation	775mW typ	*	*
TEMPERATURE RANGE			
Operating	0 to +70°C	*	*
Storage	-55°C to +150°C	*	*

NOTES

[1] Positive pulse 200ns wide (min) leading edge (0 to 1) resets outputs. Trailing edge initiates conversion.

[2] With 50Ω, 1% fixed resistor in place of gain adjust potentiometer.

[3] Adjustable to zero.

[4] With 50Ω, 1% resistor between Ref Out and Bipolar Offset (Pins 24 & 26).

[5] Conversion time is defined as the time betweeen the falling edge of convert start and the falling edge of the EOC.

[6] Each grade is specified at the conversion speed shown.

[7] Externally adjustable by a resistor or capacitor.

[8] For "Z" models order AD578ZJ, AD578ZK or AD578ZL.

*Specifications same as AD578J.

**Specifications same as AD578K.

Specifications subject to change without notice.

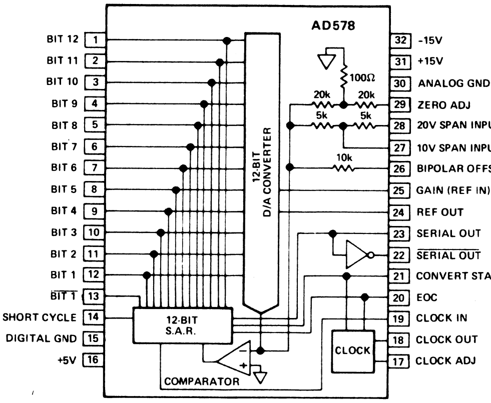


Figure 1. AD578 Functional Diagram and Pinout

The AD578 is a complete 12-bit A/D converter which requires no external components to provide the successive-approximation analog-to-digital conversion function. A block diagram of the AD578 is shown in Figure 1.

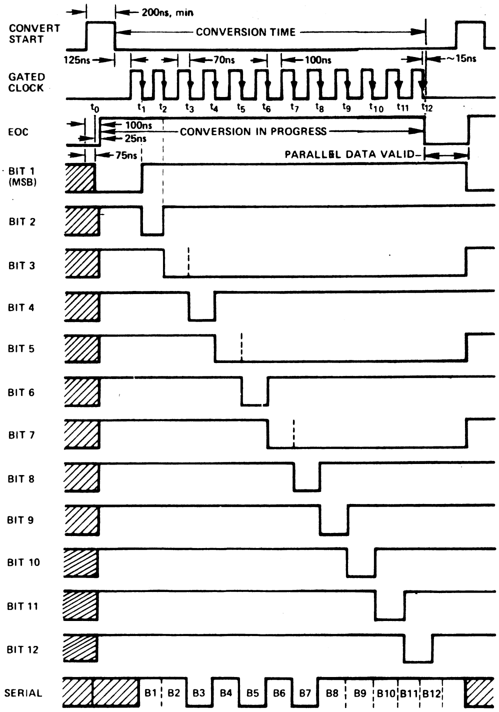
When the control section is commanded to initiate a conversion it enables the clock and resets the successive-approximation register (SAR). The SAR, timed by the clock, sequences through the conversion cycle and returns an end-of-convert flag to the control section. The control section disables the clock and brings the output status flag low. The parallel data bits become valid on the rising edge of the clock pulse starting with t_1 and ending with t_{12}.

During the conversion cycle, the internal 12-bit current output DAC is sequenced by the SAR from the most-significant-bit (MSB) to least-significant-bit (LSB) to provide an output current which accurately balances the input signal current through the 5kΩ (or 10kΩ) input resistor. The comparator determines whether the addition of each successively-weighted bit current causes the DAC current sum to be greater or less than the input current; if the sum is less, the bit is left on; if more, the bit is turned off. After testing all the bits, the SAR contains a 12-bit binary code which accurately represents the input signal to within ±1/2LSB.

The temperature-compensated buried Zener reference provides the primary voltage reference to the DAC and guarantees excellent stability with both time and temperature. The reference is trimmed to 10.00 volts ±0.1%; it is buffered and can supply up to 1.0mA to an external load in addition to the current required to drive the reference input resistor (0.5mA) and bipolar offset resistor (1mA). The thin film application resistors are trimmed to match the full scale output current of the DAC. There are two 5kΩ input scaling resistors to allow either a 10 volt or 20 volt span. The 10kΩ bipolar offset resistor is grounded for unipolar operation or connected to the 10 volt reference for bipolar operation.

UNIPOLAR CALIBRATION

The AD578 is intended to have a nominal 1/2LSB offset so that the exact analog input for a given code will be in the middle of that code (halfway between the transitions to the codes above and below it). Thus, when properly calibrated, the first transition (from 0000 0000 0000 to 0000 0000 0001) will occur for an input level of +1/2LSB (1.22mV for 10V range).



CLOCK
INTERNAL: CONNECT CLOCK OUT (18) TO CLOCK IN (19)
EXTERNAL: CONNECT EXTERNAL CLOCK TO CLOCK IN (19)
CLOCK SHOULD BE AT LEAST 30% DUTY CYCLE WITH MINIMUM PERIOD, T_{MIN} OF 100ns.

Figure 2. AD578 Timing Diagram

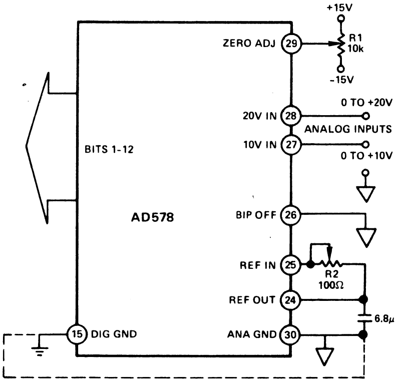


Figure 3. Unipolar Input Connections

If pin 26 is connected to pin 30, the unit will behave in this manner, within specifications. Refer to Table 1 and Figure 5 for further clarification. If the offset trim (R1) is used, it should be trimmed as above, although a different offset can be set for a particular system requirement. This circuit will give approximately ±25mV of offset trim range.

The full scale trim is done by applying a signal 1 1/2LSB below the nominal full scale (9.9963V for a 10V range). Trim R2 to give the last transition (1111 1111 1110 to 1111 1111 1111).

BIPOLAR OPERATION

The connections for bipolar ranges are shown in Figure 4. Again, as for the unipolar ranges, if the offset and gain specifications are sufficient, the 100Ω trimmer shown can be replaced by a 50Ω ±1% fixed resistor. The analog input is applied as for the unipolar ranges. Bipolar calibration is similar to unipolar calibration. First, a signal 1/2LSB above negative full scale (-4.9988V for the ±5V range) is applied, and R1 is trimmed to give the first transition (0000 0000 0000 to 0000 0000 0001). Then, a signal 1 1/2LSB below positive full scale (+4.9963V for the ±5V range) is applied and R2 trimmed to give the last transition (1111 1111 1110 to 1111 1111 1111).

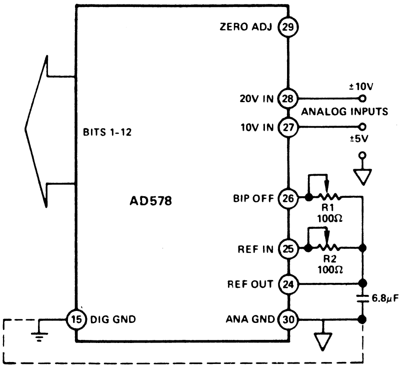


Figure 4. Bipolar Input Connections

ERROR SOURCES

The analog continuum is partitioned into 2^{12} discrete ranges for 12-bit conversion. All analog values within a given quantum are represented by the same digital code, usually assigned to the nominal midrange value. There is an inherent quantization uncertainty of ±1/2LSB, associated with the resolution, in addition to the actual conversion errors.

The actual conversion errors that are associated with A/D converters are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, reference error and power supply rejection. The matching and tracking errors in the AD578 have been minimized by the use of a monolithic DAC that includes the scaling network. The initial gain and offset errors are specified at ±0.1% FSR typical. These errors may be trimmed to zero by the use of the external trim circuits as shown in Figures 3 and 4. Linearity error is defined as the deviation from a true straight line transfer characteristic from a zero analog input which calls for a zero digital output to a point which is defined as full scale. The linearity error is unadjustable and is the most meaningful indication of A/D converter accuracy. Differential nonlinearity is a measure of the deviation in staircase step width between codes from the ideal least significant bit step size (Figure 5).

Monotonic behavior requires that the differential linearity error be less than 1LSB, however a monotonic converter can have missing codes; the AD578 is specified as having no missing codes from 0 to +70°C and thus is monotonic.

There are three types of drift error over temperature: offset, gain and linearity. Offset drift causes a shift of the transfer characteristic left or right over the operating temperature range. Gain drift causes a rotation of the transfer characteristic about the zero or minus full scale point. The worst case accuracy drift is the summation of all three drift errors over temperature. Statistically, however, the drift error behaves as the root-sum-squared (RSS) and can be shown as:

$$RSS = \sqrt{\epsilon_G{}^2 + \epsilon_O{}^2 + \epsilon_L{}^2}$$

ϵ_G = Gain Drift Error (ppm/°C)
ϵ_O = Offset Drift Error (ppm of FSR/°C)
ϵ_L = Linearity Error (ppm of FSR/°C)

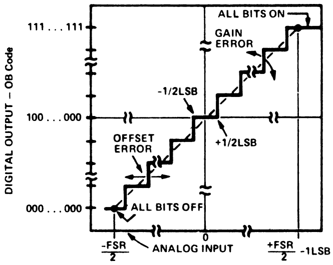


Figure 5. Transfer Characteristic for an Ideal Bipolar A/D

Analog Input — Volts (Center of Quantization Interval)				Digital Output Code (Binary for Unipolar Ranges; Offset Binary for Bipolar Ranges)
0 to +10V Range	0 to +20V Range	-5V to +5V Range	-10V to +10V Range	B1 (MSB) B12 (LSB)
+9.9976	+19.9951	+4.9976	+9.9951	1 1 1 1 1 1 1 1 1 1 1 1
+9.9952	+19.9902	+4.9952	+9.9902	1 1 1 1 1 1 1 1 1 1 1 0
•	•	•	•	•
•	•	•	•	•
+5.0024	+10.0049	+0.0024	+0.0049	1 0 0 0 0 0 0 0 0 0 0 1
+5.0000	+10.0000	+0.0000	+0.0000	1 0 0 0 0 0 0 0 0 0 0 0
•	•	•	•	•
•	•	•	•	•
+0.0024	+0.0051	-4.9976	-9.9951	0 0 0 0 0 0 0 0 0 0 0 1
+0.0000	+0.0000	-5.0000	-10.0000	0 0 0 0 0 0 0 0 0 0 0 0

Table 1. Digital Output Codes vs. Analog Input for Unipolar and Bipolar Ranges

LAYOUT CONSIDERATIONS

Many data-acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return), and Analog Signal Ground. These grounds must be tied together at one point, usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the ground pin of the AD578. Separate ground returns should be provided to minimize the current flow in the path from sensitive points to the system ground point. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

Each of the AD578's supply terminals should be capacitively decoupled as close to the AD578 as possible. A large value capacitor such as 10μF in parallel with a 0.1μF capacitor is usually sufficient. Analog supplies are bypassed to the Analog Power Return pin and the logic supply is bypassed to the Digital GND pin.

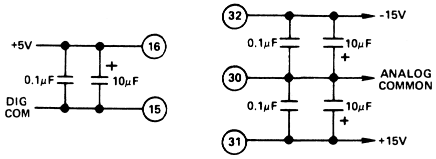


Figure 6. Basic Grounding Practice

To minimize noise the reference output (Pin 24) should be decoupled by a 6.8μF capacitor to pin 30.

CLOCK RATE CONTROL

The internal clock is preset to a nominal conversion time of 5.6μs. It can be adjusted for either faster or slower conversions. For faster conversions connect the appropriate 1% resistor between pin 17 and pin 18 and short pin 18 to pin 19.

For slower conversions connect a capacitor between pin 15 and pin 17.

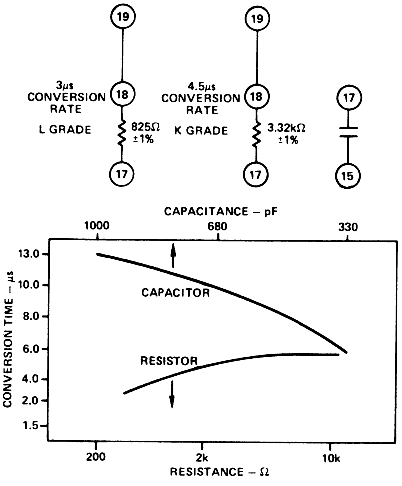


Figure 7. Conversion Time vs. R&C Values

The curves in Figure 7 characterize the conversion time for a given resistor or capacitor connection.

Note: 12-bit operation with no missing codes is not guaranteed when operating in this mode if a particular grades conversion speed specification has been exceeded.

Short Cycle Input – A Short Cycle Input, pin 14, permits the timing cycle shown in Figure 2 to be terminated after any number of desired bits has been converted, allowing somewhat shorter conversion times in applications not requiring full 12-bit resolution. Short cycle pin connections and associated maximum 12-, 10-, and 8-bit conversion times are summarized in Table 2.

Resolution (Bits)	12	10	8
Connect Pin 14 to Pin	16	2	4
Conversion Speed (μs)	3	2.5	2

Table 2. Short Cycle Connections

External Clock – An external clock may be connected directly to the clock input, pin 19. When operating in this mode the convert start should be held high for a minimum of one clock period in order to reset the SAR and synchronize the conversion cycle. A positive going pulse width of 100 to 200 nanoseconds will provide a continuous string of conversions that start on the first rising edge of the external clock after the EOC output has gone low.

External Buffer Amplifier – In applications where the AD578 is to be driven from high impedance sources or directly from an analog multiplexer a fast slewing, wideband op amp like the AD507 should be used.

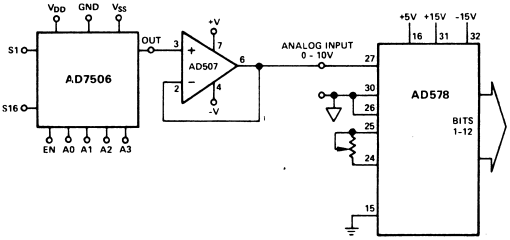


Figure 8. Input Buffer

MICROPROCESSOR INTERFACING

The 3μs conversion time of the AD578 suggests several different methods of interface to microprocessors. In systems where the AD578 is used for high sampling rates on a single signal which is to be digitally processed, CPU-controlled conversion may be inefficient due to the slow cycle times of most microprocessors. It is generally preferable to perform conversions independently, inserting the resultant digital data directly into memory. This can be done using direct memory access (DMA) which is totally transparent to the CPU. Interface to user-designed DMA hardware is facilitated by the guaranteed data validity on the falling edge of the EOC signal.

In many multichannel data acquisition systems, the processor spends a good deal of time waiting for the ADC to complete its cycle. Converters with total conversion times of 25μs to 100μs are not slow enough to justify use of interrupts, nor fast enough to finish converting during one instruction and are usually timed out with loops, or continuously polled for status. The AD578 allows the microprocessor to time out the converter with just a few dummy instructions. For example, an 8085 system running at a 5MHz clock rate will time out an AD578 by pushing a register pair onto the stack and popping the same pair back off the stack. Such a time-out routine only occupies two bytes of program memory but requires 22 clock cycles (4.4μs). The time saved by not having to wait for the converter allows the processor to run much more efficiently, particularly in multichannel systems.

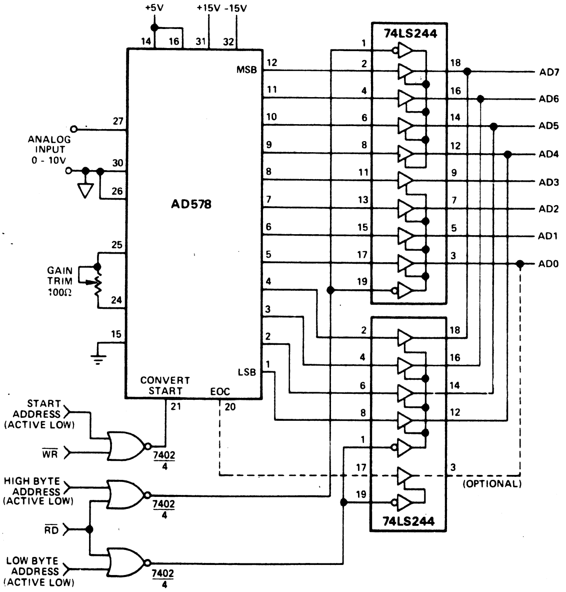


Figure 9. AD578—8085A Interface Connections

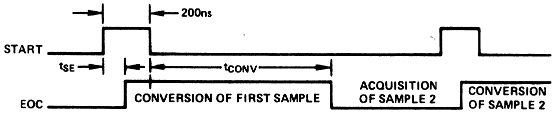
Clearly, 12 bits of data must be broken up for interface to an 8-bit wide data bus. There are two possible formats: right-justified and left-justified. In a right-justified system, the least-significant 8 bits occupy one byte and the four MSB's reside in the low nybble of another byte. This format is useful when the data from the ADC is being treated as a binary number between 0 and 4095. The left-justified format supplies the eight most-significant bits in one byte and the 4LSB's in the high nybble of another byte. The data now represents the fractional binary number relating the analog signal to the full-scale voltage. An advantage to this organization is that the most-significant eight bits can be read by the processor as a coarse indication of the true signal value. The full 12-bit word can then be read only when all 12 bits are needed. This allows faster and more efficient control of a process.

Figure 9 shows a typical connection to an 8085-type bus, using a left justified data format for unipolar inputs. Status polling is optional, and can be read simultaneously with the 4LSBs. If it is desired to right-justify the data, pins 1 through 12 of the AD578 should be reversed, as well as the connections to the data bus and high and low byte address signals.

When dealing with bipolar inputs (±5V, ±10V ranges), using the MSB directly yields an offset binary-coded output. If two's complement coding is desired, it can be produced by substituting $\overline{\text{MSB}}$ (pin 13) for the MSB. This facilitates arithmetic operations which are subsequently performed on the ADC output data.

SAMPLED DATA SYSTEMS

The conversion speed of the AD578 allows accurate digitization of high frequency signals and high throughput rates in multichannel data acquisition systems. The AD578LD, for example, is capable of a full accuracy conversion in 3μs. In order to benefit from this high speed, a fast sample-hold amplifier (SHA) such as the HTC-0300 is required. This SHA has an acquisition time to 0.01% of approximately 300ns, so that a complete sample-convert-acquire cycle can be accomplished in approximately 4μs. This means a sample rate of 250kHz can be realized, allowing a signal with no frequency components above 125kHz to be sampled with no loss of information. Note that the EOC signal from the AD578 places the SHA in the hold mode in advance of the actual start of the conversion cycle, and releases the SHA from the HOLD mode only after completion of the conversion. After allowing at least 300ns for the SHA to acquire the next analog value, the converter can again be started.



EOC IS ASSUMED TO BE TIED TO HOLD INPUT OF SHA

NOTES: t_{SE} = 100ns
t_{CONV} = 3μs (AD578L)
= 4.5μs (AD578K)
= 6μs (AD578J)

Figure 10. Start/EOC Timing for Sampled Data System

AD578 ORDERING GUIDE

Model	Conversion Speed	Package	Package Option[1]
AD578JN	6μs	Polymer-Seal	HY32H
AD578KN	4.5μs	Polymer-Seal	HY32H
AD578LN	3μs	Polymer-Seal	HY32H
AD578JD	6μs	Hermetic-Seal	HY32H
AD578KD	4.5μs	Hermetic-Seal	HY32H
AD578LD	3μs	Hermetic-Seal	HY32H

[1] See Section 20 for package outline information.

ANALOG DEVICES

Very Fast, Complete 10-Bit A/D Converter

AD579

FEATURES

Performance

Complete 10-Bit A/D Converter with Reference and Clock
Fast Successive Approximation Conversion: 1.8μs
Buried Zener Reference for Long Term Stability and Low Gain T.C.: ±30ppm/°C max
Max Nonlinearity: <±0.048%
Low Power: 775mW
Hermetic Package Available

Versatility

Positive-True Parallel or Serial Logic Outputs
Short Cycle Capability
Precision +10V Reference for External Applications
Adjustable Internal Clock
"Z" Models for ±12V Supplies

PRODUCT DESCRIPTION

The AD579 is a high speed low cost 10-bit successive approximation analog-to-digital converter that includes an internal clock, reference and comparator. Its hybrid IC design utilizes MSI digital and linear monolithic chips in conjunction with a 10-bit monolithic DAC to provide modular performance and versatility with IC size, price and reliability.

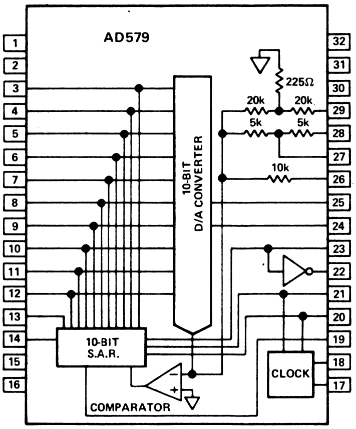
Important performance characteristics of the AD579 include a maximum linearity error at +25°C of ±0.048%, maximum gain temperature coefficient of ±30ppm/°C, typical power dissipation of 775mW and maximum conversion time of 1.8μs.

The fast conversion speeds of 1.8μs (K, B and T grades) and 2.2μs (J grade) make the AD579 an excellent choice in a variety of applications where system throughput rates from 454kHz to 555kHz are required. In addition, it may be short cycled to obtain faster conversion speeds at lower resolutions.

The design of the AD579 includes scaling resistors that provide analog input signal ranges of ±5V, ±10V, 0 to +10V or 0 to +20V. Adding flexibility and value is the +10V precision reference which can be used for external applications.

The AD579 is available with either the polymer seal (N) for use in benign environmental applications or solder-seal (D) for more harsh or rigorous surroundings. Both are contained in a 32-pin side-brazed, ceramic DIP.

AD579 FUNCTIONAL BLOCK DIAGRAM



32-PIN DIP

PRODUCT HIGHLIGHTS

1. The AD579 is a complete 10-bit A/D converter. No external components are required to perform a conversion.
2. The fast conversion rate of the AD579 makes it an excellent choice for high speed data acquisition on systems requiring high throughput rate.
3. The internal buried zener reference is laser trimmed to 10.00V ±0.1% and ±15ppm/°C typ T.C. The reference is available externally and can provide up to 1mA.
4. The scaling resistors are included on the monolithic DAC for exceptional thermal tracking.
5. Short cycle and external clock capabilities are provided for applications requiring faster conversion speeds and/or lower resolutions.
6. The integrated package construction provides high quality and reliability with small size and weight.

SPECIFICATIONS (typical @ +25°C; ±15V, and +5V power supplies unless otherwise noted)

Model	AD579JN	AD579KN	AD579BD	AD579TD
RESOLUTION	10 Bits	*	*	*
ANALOG INPUTS				
Voltage Ranges				
Bipolar	±5.0V, ±10V	*	*	*
Unipolar	0 to +10V, 0 to +20V	*	*	*
Input Impedance				
0 to +10V, ±5V	5kΩ (±20%)	*	*	*
±10V, 0 to +20V	10kΩ (±20%)	*	*	*
DIGITAL INPUTS				
Convert Command[1]	1LS TTL Load	*	*	*
Clock Input	1LS TTL Load	*	*	*
TRANSFER CHARACTERISTICS				
Gain Error[2,3]	±0.1% FSR (±0.25% FSR max)	*	*	*
Unipolar Offset[3]	±0.1% FSR (±0.25% FSR max)	*	*	*
Bipolar Offset[3,4]	±0.1% FSR (±0.25% FSR max)	*	*	*
Linearity Error				
+25°C	±1/2LSB max	*	*	*
T_{min} to T_{max}	±3/4LSB max	*	*	*
DIFFERENTIAL LINEARITY ERROR (Minimum resolution for which no missing codes are guaranteed)				
+25°C	10 Bits	*	*	*
T_{min} to T_{max}	10 Bits	*	*	*
POWER SUPPLY SENSITIVITY				
+15V ±10%	0.005%/%ΔV_S max	*	*	*
-15V ±10%	0.005%/%ΔV_S max	*	*	*
+5V ±10%	0.001%/%ΔV_S max	*	*	*
"Z" Versions				
+12V ±5%	0.007%/%ΔV_S max	*	*	*
-12V ±5%	0.007%/%ΔV_S max	*	*	*
TEMPERATURE COEFFICIENTS				
Gain	±15ppm/°C typ	*	*	*
	±30ppm/°C max	*	*	*
Unipolar Offset	±3ppm/°C typ	*	*	*
	±10ppm/°C max	±5ppm/°C max	**	**
Bipolar Offset	±8ppm/°C typ	*	*	*
	±20ppm/°C max	±15ppm/°C max	**	**
Differential Linearity	±2ppm/°C typ	*	*	*
CONVERSION TIME[5,6] (max)	2.2μs	1.8μs	**	**
Conversion Time T_{min} to T_{max}	2.4μs	2.0μs	**	**
PARALLEL OUTPUTS				
Unipolar Code	Binary	*	*	*
Bipolar Code	Offset Binary/Two's Complement	*	*	*
Output Drive	2LSTTL Loads	*	*	*
SERIAL OUTPUTS (NRZ FORMAT)				
Unipolar Code	Binary/Complementary Binary	*	*	*
Bipolar Code	Offset Binary/Comp. Offset Binary	*	*	*
Output Drive	2LSTTL Loads	*	*	*
END OF CONVERSION (EOC)	Logic "1" During Conversion	*	*	*
Output Drive	8LSTTL Loads	*	*	*
INTERNAL CLOCK[7]				
Output Drive	2LSTTL Loads	*	*	*
INTERNAL REFERENCE				
Voltage	10.000 ± 10mV	*	*	*
Temperature Coefficient	15ppm/°C	*	*	*
External Current	±1mA max	*	*	*
POWER SUPPLY REQUIREMENTS				
Range for Rated Accuracy	4.75 to 5.25 and ±13.5 to ±16.5	*	*	*
Z Models[8]	4.75 to 5.25 and ±11.4 to ±16.5	*	*	*
Supply Current +15V	3mA typ, 8mA max	*	*	*
-15V	22mA typ, 35mA max	*	*	*
+5V	80mA typ, 110mA max	*	*	*
Power Dissipation	775mW typ	*	*	*
TEMPERATURE RANGE				
Operating	0 to +70°C	*	-25°C to +85°C	-55°C to +125°C
Storage	-55°C to +150°C	*	*	*

NOTES

[1] Positive pulse 200ns wide (min) leading edge (0 to 1) resets outputs. Trailing edge initiates conversion.

[2] With 50Ω, 1% fixed resistor in place of gain adjust potentiometer.

[3] Adjustable to zero.

[4] With 50Ω, 1% resistor between Ref Out and Bipolar Offset (Pins 24 & 26).

[5] Conversion time is defined as the time between the falling edge of convert start and the falling edge of the EOC.

[6] Each grade is specified at the conversion speed shown. See Figure 7 for appropriate connections.

[7] Externally adjustable by a resistor or capacitor.

[8] For "Z" models order AD579ZJN, AD579ZKN, AD579ZBD or AD579ZTD.

*Specifications same as AD579JN.

**Specifications same as AD579KN.

Specifications subject to change without notice.

THEORY OF OPERATION

The AD579 is a complete 10-bit A/D converter which requires no external components to provide the successive-approximation analog-to-digital conversion function. A block diagram of the AD579 is shown in Figure 1.

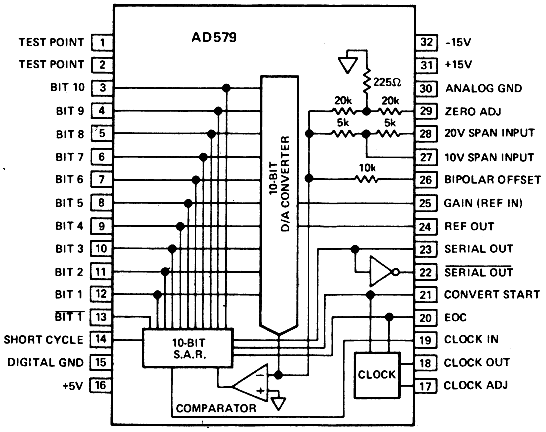


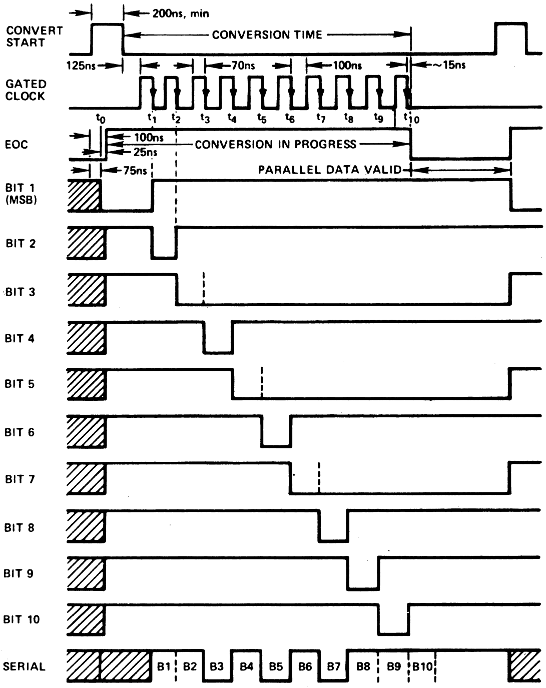
Figure 1. AD579 Functional Diagram and Pinout

On receipt of a CONVERT START command, the AD579 converts the voltage at its analog input into an equivalent bit binary number. This conversion is accomplished as follows: the 10-bit successive-approximation register (SAR) has its 10-bit outputs connected both to the device bit output pins and to the corresponding bit inputs of the feedback DAC. The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

The temperature-compensated buried Zener reference provides the primary voltage reference to the DAC and guarantees excellent stability with both time and temperature. The reference is trimmed to 10.00 volts ±0.1%; it is buffered and can supply up to 1.0mA to an external load in addition to the current required to drive the reference input resistor (0.5mA) and bipolar offset resistor (1mA). The thin film application resistors are trimmed to match the full scale output current of the DAC. There are two 5kΩ input scaling resistors to allow either a 10 volt or 20 volt span. The 10kΩ bipolar offset resistor is grounded for unipolar operation or connected to the 10 volt reference for bipolar operation.

TIMING

The timing diagram is shown in Figure 2. Receipt of a CONVERT START signal sets the STATUS flag, indicating conversion in progress. This, in turn, removes the inhibit applied to the gated clock, permitting it to run through 10 cycles. All SAR parallel bit and STATUS flip-flops are initialized on the leading edge, and the gated clock inhibit signal is removed on the trailing edge of the CONVERT START signal. At time t_0, B_1 is reset and B_2 -B_{10} are set unconditionally. At t_1 the Bit 1 decision is made (keep) and Bit 2 is unconditionally reset. At t_2, the Bit 2 decision is made (keep) and Bit 3 is reset unconditionally. This sequence continues until Bit 10 (LSB) decision (keep) is made at t_{10}. After a 15ns delay period, the STATUS flag is reset, indicating that the conversion is complete and that the parallel output data is valid. Resetting the STATUS flag restores the gated clock inhibit signal, forcing the clock output to Logic "0" state.



CLOCK
INTERNAL: CONNECT CLOCK OUT (18) TO CLOCK IN (19)
EXTERNAL: CONNECT EXTERNAL CLOCK TO CLOCK IN (19)
CLOCK SHOULD BE AT LEAST 30% DUTY CYCLE WITH MINIMUM PERIOD, T_{MIN} OF 100ns.

Figure 2. AD579 Timing Diagram

Serial data does not change and is guaranteed valid on negative-going clock edges, therefore; serial data can be transferred quite simply by clocking it into a receiving shift register on these edges (see Figure 2).

Incorporation of this 15ns delay guarantees that the parallel (and serial) data are valid at the Logic "1" to "0" transition of the STATUS flag, permitting parallel data transfer to be initiated by the trailing edge of the STATUS signal.

UNIPOLAR CALIBRATION

The AD579 is intended to have a nominal 1/2LSB offset so that the exact analog input for a given code will be in the middle of that code (halfway between the transitions to the codes above and below it). Thus, when properly calibrated, the first transition (from 0000 0000 00 to 0000 0000 01) will occur for an input level of +1/2LSB (4.88mV for 10V range).

If pin 26 is connected to pin 30, the unit will behave in this manner, within specifications. Refer to Table 1 and Figure 3 for further clarification. If the offset trim (R1) is used, it should be trimmed as above, although a different offset can be set for a particular system requirement. This circuit will give approximately ±50mV of offset trim range.

The full scale trim is done by applying a signal 1 1/2LSB below the nominal full scale (9.985V for a 10V range). Trim R2 to give the last transition (1111 1111 10 to 1111 1111 11).

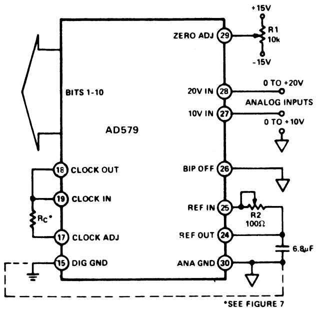


Figure 3. Unipolar Input Connections

BIPOLAR OPERATION

The connections for bipolar ranges are shown in Figure 4. Again, as for the unipolar ranges, if the offset and gain specifications are sufficient, the 100Ω trimmer shown can be replaced by a 50Ω ±1% fixed resistor. The analog input is applied as for the unipolar ranges. Bipolar calibration is similar to unipolar calibration. First, a signal 1/2LSB above negative full scale (-4.9957V for the ±5V range) is applied, and R1 is trimmed to give the first transition (0000 0000 00 to 0000 0000 01). Then, a signel 1 1/2LSB below positive full scale (+4.9853V for the ±5V range) is applied and R2 trimmed to give the last transition (1111 1111 10 to 1111 1111 11).

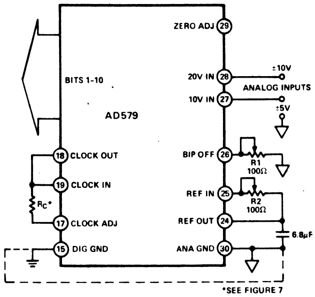


Figure 4. Bipolar Input Connections

ERROR SOURCES

The analog continuum is partitioned into 2^{10} discrete ranges for 10-bit conversion. All analog values within a given quantum are represented by the same digital code, usually assigned to the nominal midrange value. There is an inherent quantization uncertainty of ±1/2LSB, associated with the resolution, in addition to the actual conversion errors.

The actual conversion errors that are associated with A/D converters are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, reference error and power supply rejection.

The matching and tracking errors in the AD579 have been minimized by the use of a monolithic DAC that includes the scaling network. The initial gain and offset errors are specified at ±0.1% FSR typical. These errors may be trimmed to zero by the use of the external trim circuits as shown in Figures 3 and 4. Linearity error is defined as the deviation from a true straight line transfer characteristic from a zero analog input which calls for a zero digital output to a point which is defined as full scale. The linearity error is unadjustable and is the most meaningful indication of A/D converter accuracy. Differential nonlinearity is a measure of the deviation in staircase step width between codes from the ideal least significant bit step size (Figure 5).

Monotonic behavior requires that the differential linearity error be less than 1LSB, however a monotonic converter can have missing codes; the AD579 is specified as having no missing codes from -55°C to +125°C and thus is monotonic.

There are three types of drift error over temperature: offset, gain and linearity. Offset drift causes a shift of the transfer characteristic left or right over the operating temperature range. Gain drift causes a rotation of the transfer characteristic about the zero or minus full scale point. The worst case accuracy drift is the summation of all three drift errors over temperature. Statistically, however, the drift error behaves as the root-sum-squared (RSS) and can be shown as:

$$\text{RSS} = \sqrt{\epsilon_G{}^2 + \epsilon_O{}^2 + \epsilon_L{}^2}$$

ϵ_G = Gain Drift Error (ppm/°C)
ϵ_O = Offset Drift Error (ppm of FSR/°C)
ϵ_L = Linearity Error (ppm of FSR/°C)

Analog Input – Volts (Center of Quantization Interval)				Digital Output Code (Binary for Unipolar Ranges; Offset Binary for Bipolar Ranges)
0 to +10V Range	0 to +20V Range	-5V to +5V Range	-10V to +10V Range	B1 (MSB) B10 (LSB)
+9.9902	+19.9804	+4.9902	+9.9804	1 1 1 1 1 1 1 1 1 1
+9.9804	+19.9609	+4.9804	+9.9609	1 1 1 1 1 1 1 1 1 0
•	•	•	•	•
•	•	•	•	•
+5.0097	+10.0195	+0.0097	+0.0195	1 0 0 0 0 0 0 0 0 1
+5.0000	+10.0000	+0.0000	+0.0000	1 0 0 0 0 0 0 0 0 0
•	•	•	•	•
•	•	•	•	•
+0.0097	+0.0195	-4.9902	-9.9804	0 0 0 0 0 0 0 0 0 1
+0.0000	+0.0000	-5.0000	-10.0000	0 0 0 0 0 0 0 0 0 0

Table 1. Digital Output Codes vs. Analog Input for Unipolar and Bipolar Ranges

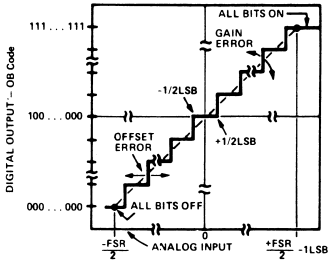


Figure 5. Transfer Characteristic for an Ideal Bipolar A/D

LAYOUT CONSIDERATIONS

Many data acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return), and Analog Signal Ground. These grounds must be tied together at one point, usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the ground pin of the AD579. Separate ground returns should be provided to minimize the current flow in the path from sensitive points to the system ground point. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

Each of the AD579's supply terminals should be capacitively decoupled as close to the AD579 as possible. A large value capacitor such as 10μF in parallel with a 0.1μF capacitor is usually sufficient. Analog supplies are bypassed to the Analog Power Return pin and the logic supply is bypassed to the Digital GND pin.

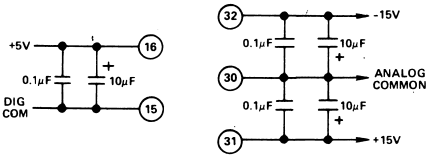


Figure 6. Basic Grounding Practice

To minimize noise the reference output (Pin 24) should be decoupled by a 6.8μF capacitor to pin 30.

CLOCK RATE CONTROL

The internal clock is preset to a nominal conversion time of 4.8μs. It can be adjusted for either faster or slower conversions. For faster conversion connect the appropriate 1% resistor between pin 17 and pin 18 and short pin 18 to pin 19.

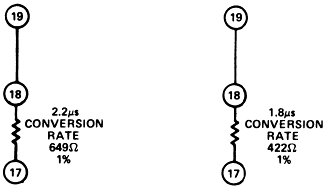


Figure 7. Clock Rate Control Connection

Short Cycle Input – A Short Cycle Input, pin 14, permits the timing cycle shown in Figure 2 to be terminated after any number of desired bits has been converted, allowing somewhat shorter conversion times in applications not requiring full 10-bit resolution. Short cycle pin connections and associated maximum 10- and 8-bit conversion times are summarized in Table 2.

Resolution (Bits)	10	8
Connect Pin 14 to Pin	2	4
Conversion Speed (μs)	1.8	1.5

Table 2: Short Cycle Connections

External Clock – An external clock may be connected directly to the clock input, pin 19. When operating in this mode the convert start should be held high for a minimum of one clock period in order to reset the SAR and synchronize the conversion cycle.

External Buffer Amplifier – In applications where the AD579 is to be driven from high impedance sources or directly from an analog multiplexer a fast slewing, wideband op amp like the LH0033G should be used.

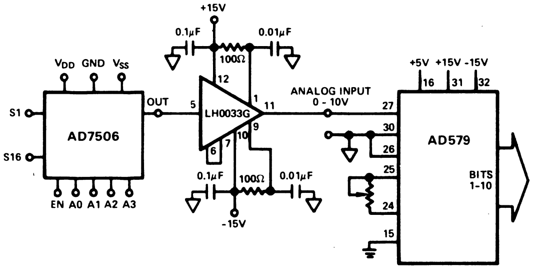
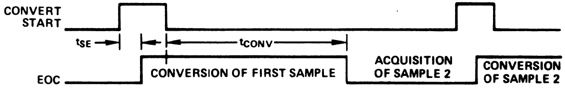


Figure 8. Input Buffer

SAMPLED DATA SYSTEMS

The conversion speed of the AD579 allows accurate digitization of high frequency signals and high throughput rates in multichannel data acquisition systems. The AD579BD, for example, is capable of a full accuracy conversion in 1.8μs. In order to benefit from this high speed, a fast sample-hold amplifier (SHA) such as the HTC-0300 is required. This SHA has an acquisition time to 0.01% of approximately 300ns, so that a complete sample-convert-acquire cycle can be accomplished in approximately 2.5μs. This means a sample rate of 400kHz can be realized, allowing a signal with no frequency components above 200kHz to be sampled with no loss of information. Note that the EOC signal from the AD579 places the SHA in the hold mode in advance of the actual start of the conversion cycle, and releases the SHA from the HOLD mode only after completion of the conversion. After allowing at least 300ns for the SHA to acquire the next analog value, the converter can again be started.



EOC IS ASSUMED TO BE TIED TO HOLD INPUT OF SHA

NOTES: t_{SE} = 100ns

Figure 9. Start/EOC Timing for Sampled Data System

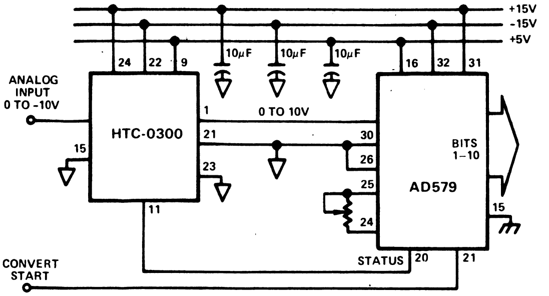


Figure 10. 400kHz – 10-Bit, A/D Conversion System

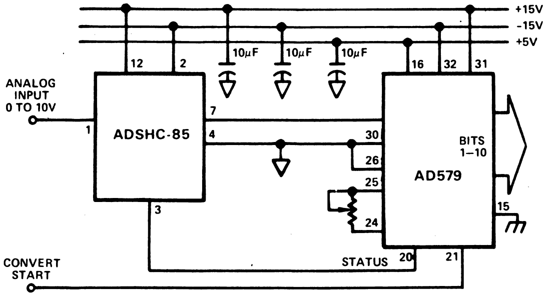


Figure 11. 154kHz – 10-Bit, A/D Conversion System

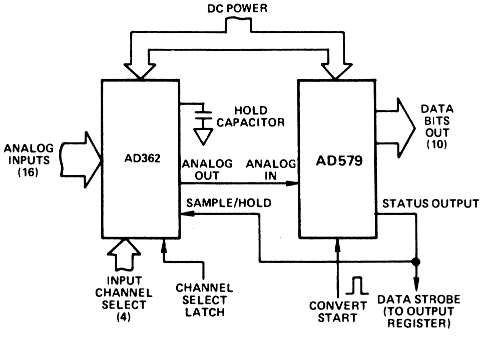


Figure 12. High Speed 10-Bit DAS

A fast (85kHz) 10-bit DAS can be configured using the AD362 and the AD579. The AD362 contains two 8-channel multiplexers, a differential amplifier, a sample-and-hold with high-speed output amplifier, a channel address latch and control logic. The multiplexers may be connected to the differential amplifier in either an 8-channel differential or 16-channel single-ended configuration. A feature of the AD362 is an internal user-controllable analog switch that connects the multiplexers in either a single-ended or differential mode. This allows a single device to perform in either mode without hardwire programming and permits a mixture of single-ended and differential sources to be interfaced by dynamically switching the input mode control.

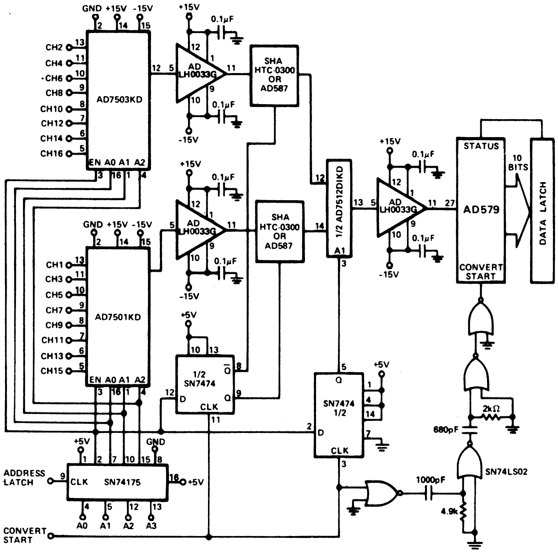


Figure 13. High Speed–165kHz–10-Bit DAS

A high speed 10-bit DAS with a throughput rate of 165kHz can be built around an AD579. The DAS of Figure 13 "Ping Pongs" two sample and hold amplifiers to eliminate the effects of the acquisition time of the sample and hold amplifiers. By applying sequential channel address the AO of the address enables one of the two multiplexers. The incorporation of the flip-flops on the SHA mode controls and the switch address allows a new channel address to be latched in while a conversion is in progress.

AD579 ORDERING GUIDE

Model	Conversion Speed	Package	Temperature Range	Power Supply Range	Package Option[1]
AD579JN	2.2μs	Polymer-Seal	0 to +70°C	±15V ±10%	HY32H
AD579KN	1.8μs	Polymer-Seal	0 to +70°C	±15V ±10%	HY32H
AD579BD	1.8μs	Hermetic Seal	-25°C to +85°C	±15V ±10%	HY32H
AD579TD	1.8μs	Hermetic-Seal	-55°C to 125°C	±15V ±10%	HY32H
AD579ZJN	2.2μs	Polymer-Seal	0 to +70°C	±12V ±5%	HY32H
AD579ZKN	1.8μs	Polymer-Seal	0 to +70°C	±12V ±5%	HY32H
AD579ZBD	1.8μs	Hermetic-Seal	-25°C to +85°C	±12V ±5%	HY32H
AD579ZTD	1.8μs	Hermetic-Seal	-55°C to +125°C	±12V ±5%	HY32H

[1] See Section 20 for package outline information.

ANALOG DEVICES

Fast, Complete, 8-Bit A/D Converter with Microprocessor Interface

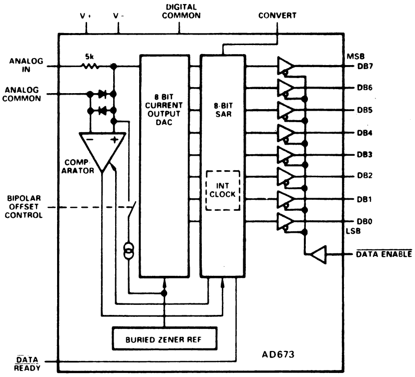
AD673*

ADVANCE TECHNICAL DATA

FEATURES

Complete 8-Bit A/D Converter with Reference, Clock and Comparator
Full Microprocessor Bus Interface
Fast Successive Approximation Conversion – 20µs
No Missing Codes Over Temperature
Operates on +5V and –12V to –15V Supplies
Low Cost Monolithic Construction

AD673 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD673 is a complete 8-bit successive approximation analog to digital converter consisting of a DAC, voltage reference, clock, comparator, successive approximation register (SAR) and 3 state output buffer–all fabricated on a single chip. No external components are required to perform a full accuracy 8-bit conversion in 20µs.

The AD673 incorporates the most advanced integrated circuit design and processing technology available today. The successive approximation function is implemented with I^2L (integrated injection logic). Laser trimming of the high stability SiCr thin film resistor ladder network at the wafer stage (LWT) insures high accuracy, which is maintained with a temperature compensated sub-surface Zener reference.

Operating on supplies of +5V and –12V to –15V, the AD673 will accept analog inputs of 0 to +10V, unipolar, or –5V to +5V, bipolar. A positive pulse on the CONVERT line initiates the 20µs conversion cycle. $\overline{\text{DATA}}$ $\overline{\text{READY}}$ indicates completion of the conversion. $\overline{\text{DATA}}$ $\overline{\text{ENABLE}}$ controls the 8-bit three state output buffer.

The AD673 is available in two versions; the AD673J is specified for the 0 to +70°C temperature range, the AD673S for –55°C to +125°C. Both guarantee full 8-bit accuracy and no missing codes over their respective temperature ranges and are packaged in 20-pin hermetically sealed ceramic DIPs. The AD673J is also offered in an 20-pin plastic DIP.

PRODUCT HIGHLIGHTS

1. The AD673 is a complete 8-bit A/D converter. No external components are required to perform a conversion.
2. The AD673 interfaces to many popular microprocessors without external buffers or peripheral interface adapters.
3. The device offers true 8-bit accuracy and exhibits no missing codes over its entire operating temperature range.
4. The AD673 accepts either unipolar (0 to +10V) or bipolar (–5V to +5V) analog inputs by simply grounding or opening a single pin.
5. Performance is guaranteed with +5V and –15V supplies. The device will also operate with a –12V supply.
6. The AD673SD/883B is screened in accordance with the Class B requirements of MIL-STD-883, Method 5004. Single chip construction renders the AD673 inherently more reliable than hybrid units. That and its functional completeness make the AD673 especially attractive for high reliability applications.

***Protected by Patents 3,940,760; 4,213,806 and 4,136,349**

SPECIFICATIONS

(typical @ +25°C with V+ = +5V, V− = −15V, all voltages measured with respect to digital common, unless otherwise indicated)

Model	AD673J	AD673S[1]
RESOLUTION[2]	8 Bits	*
RELATIVE ACCURACY @ 25°C[2,3,4]	± ½LSB max	*
T_{min} to T_{max}	± ½LSB max	
FULL SCALE CALIBRATION[4,5] (With 15Ω Resistor In Series With Analog Input)	± 2LSB	*
UNIPOLAR OFFSET (max)[4]	± ½LSB	*
BIPOLAR OFFSET (max)[4]	± ½LSB	*
DIFFERENTIAL NONLINEARITY (Resolution for Which No Missing Codes are Guaranteed)		
+25°C	8 Bits	*
T_{min} to T_{max}	8 Bits	*
TEMPERATURE RANGE	0 to +70°C	−55°C to +125°C
TEMPERATURE COEFFICIENTS[4]		
Guaranteed max Change		
25° to T_{min} or T_{max}		
Unipolar Offset	± 1LSB (88ppm/°C)	± 1LSB (40ppm/°C)
Bipolar Offset	± 1LSB (88ppm/°C)	± 1LSB (40ppm/°C)
Full Scale Calibration[6] (With 15Ω Fixed Resistor or 200Ω Trimmer)	± 2LSB (176ppm/°C)	± 2LSB (80ppm/°C)
POWER SUPPLY REJECTION[4]		
Max Change In Full Scale Calibration		
TTL Positive Supply		
$+4.5V \leq V+ \leq +5.5V$	± 2LSB max	*
Negative Supply		
$-15.75V \leq V- \leq -14.25V$	± 2LSB max	*
$-12.6V \leq V- \leq -11.4V$	± 2LSB max	*
ANALOG INPUT RESISTANCE	3kΩ min	*
	5kΩ typ	*
	7kΩ max	*
ANALOG INPUT RANGES		
(Analog Input to Analog Common)		
Unipolar	0 to +10V	*
Bipolar	−5V to +5V	*
OUTPUT CODING		
Unipolar	Positive True Binary	*
Bipolar	Positive True Offset Binary	*
LOGIC OUTPUT		
Bit Outputs and $\overline{\text{Data Ready}}$		
Output Sink Current	3.2mA min	*
(V_{OUT} = 0.4V max, T_{min} to T_{max})	(2TTL Loads)	*
Output Source Current (Bit Outputs)[7]		
(V_{OUT} = 2.4V min, T_{min} to T_{max})	0.5mA min	*
Output Leakage (3 State)	± 40µA max	*
LOGIC INPUT (CONVERT, $\overline{\text{DATA ENABLE}}$)		
Input Current ($0 \leq V_{IN} \leq V+$)	± 100µA max	*
Logic "1"	2.0V min	*
Logic "0"	0.8V max	*
CONVERSION TIME	10µs min	*
T_{min} to T_{max}	20µs typ	*
	30µs max	*

Model	AD673J	AD673S[1]
POWER SUPPLY		
Absolute Maximum		
V+	+7V	*
V−	−16.5V	*
Specified Operating – Rated Performance		
V+	+5V	*
V−	−15V	*
Operating Range		
V+	+4.5V to +5.5V	*
V−	−11.4V to −15.75V	*
Operating Current		
V+ = +5V	15mA typ (25mA max)	*
V− = −15V	9mA typ (15mA max)	*

*Specifications same as AD673J.

[1] The AD673S is available fully processed and screened to the requirements of MIL-STD-883B, Method 5004, Class B. When ordering, specify the AD673SD/883B.

[2] The AD673 is a selected version of the AD573 10-bit A to D converter. As such, some devices may exhibit 9 or 10 bits of relative accuracy or resolution, but that is neither tested nor guaranteed. Only TTL logic inputs should be connected to pins 1 and 2 (or no connection made) or damage may result.

[3] Relative accuracy is defined as the deviation of the code transition points from the ideal transfer point on a straight line from the zero to the full scale of the device.

[4] Specifications given in LSBs refer to the weight of a least significant bit at the 8-bit level, which is 0.39% of full-scale.

[5] Full scale calibration is guaranteed trimmable to zero with an external 200Ω potentiometer in place of the 15Ω fixed resistor. Full scale is defined as 10 volts minus 1LSB, or 9.961 volts.

[6] Full Scale Calibration Temperature Coefficient includes effects of unipolar offset drift as well as gain drift.

[7] The data output lines have active pull-ups to source 0.5mA. The $\overline{\text{DATA READY}}$ line is open collector with a nominal 6kΩ internal pull-up resistor.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

V+ to Digital Common	0 to +7V
V− to Digital Common	0 to −16.5V
Analog Common to Digital Common	±1V
Analog Input to Analog Common	±15V
Control Inputs	0 to V+
Digital Outputs (3 State)	0 to V+
Power Dissipation	800mW

AD673 ORDERING GUIDE

Model	Package[1]	Temperature Range
AD673JN	20-Pin Plastic DIP (N20A)	0 to +70°C
AD673JD	20-Pin Ceramic DIP (D20A)	0 to +70°C
AD673SD	20-Pin Ceramic DIP (D20A)	−55° to +125°C
AD673SD/883B	20-Pin Ceramic DIP (D20A)	−55°C to +125°C

[1] See Section 20 for package outline information.

UNIPOLAR CONNECTION

The AD673 contains all the active components required to perform a complete A/D conversion. Thus, for many applications, all that is necessary is connection of the power supplies (+5V and −15V), the analog input and the conversion start pulse. However, there are some features and special connections which should be considered for achieving optimum performance. The functional pin-out is shown in Figure 1.

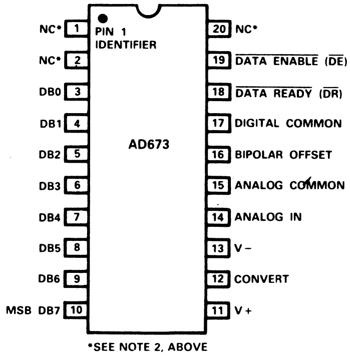


Figure 1. AD673 Pin Connections

The standard unipolar 0 to +10V range is obtained by shorting the bipolar offset control pin (pin 16) to digital common (pin 17).

Full Scale Calibration

The 5kΩ thin film input resistor is laser trimmed to produce a current which matches the full scale current of the internal DAC–plus about 0.3%–when a full scale analog input voltage of 9.961 volts (10 volts − 1LSB) is applied at the input. The input resistor is trimmed in this way so that if a fine trimming potentiometer is inserted in series with the input signal, the input current at the full scale input voltage can be trimmed down to match the DAC full scale current as precisely as desired. However, for many applications the nominal 9.961 volt full scale can be achieved to sufficient accuracy by simply inserting a 15Ω resistor in series with the analog input to pin 14. Typical full scale calibration error will then be about ±2LSB or ±0.8%. If a more precise calibration is desired, a 200Ω trimmer should be used instead. Set the analog input at 9.961 volts, and set the trimmer so that the output code is just at the transition between 11111110 and 11111111. Each LSB will then have a weight of 39.06mV. If a nominal full scale of 10.24 volts is desired (which makes the LSB have weight of exactly 40.00mV), a 50Ω resistor in series with 200Ω trimmer (or a 500Ω trimmer with good resolution) should be used. Of course, larger full scale ranges can be arranged by using a larger input resistor, but linearity and full scale temperature coefficient may be compromised if the external resistor becomes a sizeable percentage of 5kΩ. Figure 2 illustrates the connections required for full scale calibration.

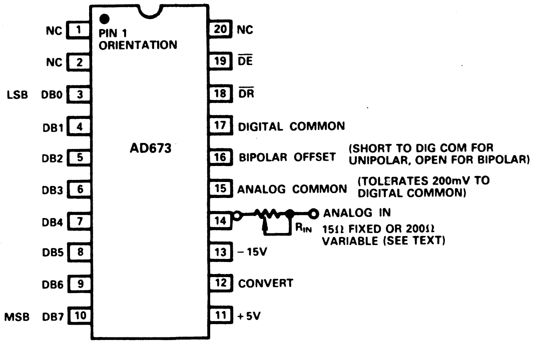

NC 1
NC 2
LSB DB0 3
DB1 4
DB2 5
DB3 6
DB4 7
DB5 8
DB6 9
MSB DB7 10
PIN 1 ORIENTATION
AD673
20 NC
19 DE
18 DR
17 DIGITAL COMMON
16 BIPOLAR OFFSET (SHORT TO DIG COM FOR UNIPOLAR, OPEN FOR BIPOLAR)
15 ANALOG COMMON (TOLERATES 200mV TO DIGITAL COMMON)
14
ANALOG IN
RIN 15Ω FIXED OR 200Ω VARIABLE (SEE TEXT)
13 −15V
12 CONVERT
11 +5V

Figure 2. Standard AD673 Connections

Unipolar Offset Calibration

Since the Unipolar Offset is ± 1LSB for all versions of the AD673, most applications will not require trimming. Figure 3 illustrates two trimming methods which can be used if greater accuracy is necessary.

Figure 3a shows how the converter zero may be offset by up to ± 3 bits to correct the device initial offset and/or input signal offsets. As shown the circuit gives approximately symmetrical adjustment in unipolar mode. Figure 3b shows how to offset the converter zero by 1/2LSB.

BIPOLAR CONNECTION

To obtain the bipolar −5V to +5V range with an offset binary output code the bipolar offset control pin is left open.

A −5.00 volt signal will give an 8-bit code of 00000000; an input of 0.00 volts results in an output code of 10000000 and 4.96 volts at the input yields the 11111111 code.

Full Scale Calibration

Full Scale Calibration is accomplished in the same manner as in unipolar operation except the full scale input voltage is 4.961 volts.

Negative Full Scale Calibration

The circuit in Figure 3a can also be used in bipolar operation to offset the input voltage (nominally −5V) which results in the 00000000 code. R2 should be omitted to obtain a symmetrical range.

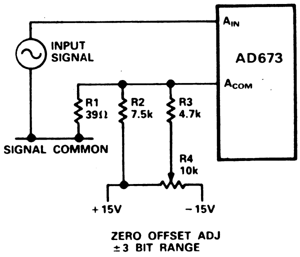


Figure 3a.

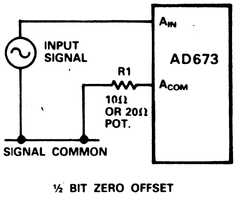


Figure 3b.

CONTROL AND TIMING OF THE AD673

CONVERT and $\overline{\text{DE}}$ are the control pins. Timing for the conversion cycle is shown in Figure 4a. A positive pulse 500ns in width must be applied to the CONVERT pin to initiate the conversion. $\overline{\text{DR}}$ goes high within 1.5µs after the rising edge of the convert start pulse to indicate that the SAR is reset and goes low when the conversion is complete.

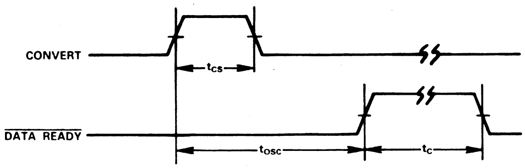


Figure 4a. Convert Timing

Read timing is shown in Figure 4b. Bringing $\overline{\text{DE}}$ low activates the 8-bit 3 state buffer.

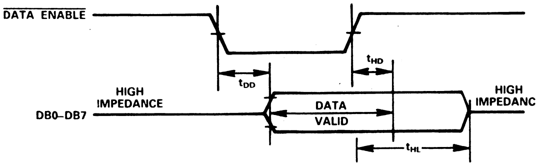


Figure 4b. Read Timing

In systems where peripheral interface adapter chips are used, or where dedicated I/O ports exist (as in single-chip-microcomputers), the AD673 may be used in a "stand-alone mode". In this mode, $\overline{\text{DR}}$ is hard-wired to $\overline{\text{DE}}$ to disable the output buffer during conversion. Upon completion of the conversion cycle, $\overline{\text{DR}}$ enables the output driver, and the 8-bit parallel data can be read.

TIMING SPECIFICATIONS

t_{CS}	500ns min
t_{DSC}	1.5µs max
t_C	10µs min
	20µs typ
	30µs max
t_{DD}	250ns max
t_{HD}	50ns min
t_{HL}	200ns max

Timing Measurement Reference Level is

$$\frac{V_{IN\,H} + V_{IN\,L}}{2} \text{ or } \frac{V_{OUT\,L} + V_{OUT\,H}}{2}$$

ANALOG DEVICES

12-Bit Successive Approximation High Accuracy A/D Converter

AD5200 SERIES

PRELIMINARY TECHNICAL DATA

FEATURES

True 12-Bit Operation: ±1/2LSB max Nonlinearity
Totally Adjustment-Free
Guaranteed No Missing Codes Over the Specified Temperature Range
Hermetically-Sealed Package
Standard Temperature Range: -25°C to +85°C
Military Temperature Range: -55°C to +125°C
MIL-STD-883 Processing Available
Serial and Parallel Outputs
Monolithic DAC with Scaling Resistors for Stability
Low Chip Count for High Reliability
Industry Standard Pin Out
Small 24-Pin DIP

GENERAL DESCRIPTION

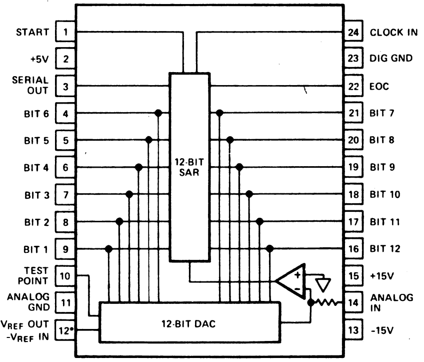
The AD5200 series devices are 12-bit successive approximation analog-to-digital converters. The hybrid design utilizes MSI digital, linear monolithic chips and active laser trimming of high-stability thin-film resistors to provide a totally adjustment free converter—no potentiometers are required for calibration.

The innovative design of the AD5200 series devices incorporates a monolithic 12-bit feedback DAC for reduced chip count and higher reliability. The exceptional temperature coefficients of the monolithic DAC guarantees ±1/2LSB linearity over the entire operating temperature range of -25°C to +85°C for the commercial grade and -55°C to +125°C for the military grade.

The AD5200 series converters are available in 2 input voltage ranges: ±5V (AD5201/AD5204) and ±10V (AD5202/AD5205). The converters are available either complete with an internal buried zener reference or with the option of an external reference for improved absolute accuracy.

The AD5200 series converters are available in two performance grades; the "B" is specified from -25°C to +85°C and the "T" is specified from -55°C to +125°C. The "B" and "T" grades are also available processed to MIL-STD-883 level B requirements. All units are available in a 24-pin hermetically sealed ceramic DIP.

AD5200 SERIES FUNCTIONAL BLOCK DIAGRAM



*PIN 12 FUNCTION: $-V_{REF\ OUT}$ – AD5201, AD5202
$-V_{REF\ IN}$ – AD5204, AD5205

24-PIN DIP

PRODUCT HIGHLIGHTS

1. The AD5200 series devices are laser trimmed at the factory to provide a totally adjustment free converter—no potentiometers are required for 12-bit performance.
2. A monolithic 12-bit feedback DAC is used for reduced chip count and higher reliability.
3. The AD5200 series directly replaces other devices of this type with significant increases in performance.
4. The devices offer true 12-bit accuracy and exhibits no missing codes over the entire operating temperature range.
5. The fast conversion rate of the AD5200 series makes it an excellent choice for applications requiring high system throughput rates.

SPECIFICATIONS (typical @ +25°C, ±15V and +5V unless otherwise noted)

INPUT RANGE	INPUT IMPEDANCE				
-5V to +5V	5.0kΩ	AD5201B	AD5201T	AD5204B	AD5204T
-10V to +10V	10.0kΩ	AD5202B	AD5202T	AD5205B	AD5205T
REFERENCE		Internal	*	External -10.000V	***
RESOLUTION		12 Bits	*	*	*
LINEARITY ERROR, MAX		±1/2LSB	*	*	*
No Missing Codes T_{min} to T_{max}		Guaranteed	*	*	*
ZERO ERROR, MAX		±1LSB	*	*	*
ZERO ERROR, MAX					
T_{min} to T_{max}		±2LSB	*	*	*
ABSOLUTE ACCURACY, MAX		±0.05% of FSR[1]	*	*	*
ABSOLUTE ACCURACY, MAX					
T_{min} to T_{max}		±0.4% of FSR[1]	*	±0.1% of FSR[1]	***
CONVERSION TIME, MAX					
Clock = 260kHz		50µs	*	*	*
LOGIC RATINGS					
Input Logic Commands					
Logic "0"		0.8V max	*	*	*
Logic "1"		+2.0V min	*	*	*
Loading		0.5TTL Load	*	*	*
CLOCK INPUT PULSE WIDTH		100ns min	*	*	*
OUTPUT LOGIC					
Logic "0"		0.4V max	*	*	*
Logic "1"		3.6V (2.4 min)	*	*	*
FANOUT - HIGH		8TTL Loads	*	*	*
FANOUT - LOW		2TTL Loads	*	*	*
POWER SUPPLY REQUIREMENTS					
V_{LOGIC}		+5V ±0.5V	*	*	*
V_{CC}		+15V ±1.5V	*	*	*
V_{DD}		-15V ±1.5V	*	*	*
OPERATING CURRENT					
V_{LOGIC}		25mA (42mA max)	*	*	*
V_{CC}		10mA (25mA max)	*	*	*
V_{EE}		-25mA (-35mA max)	*	*	*
V_{REF}				0.5mA	***
POWER SUPPLY REJECTION					
V_{CC}		±0.005 of FS/of P.S.	*	*	*
V_{EE}		±0.005 of F.S./of P.S.	*	*	*
POWER CONSUMPTION		725mW (0.8W max at 125°C)	*	*	*
OPERATING TEMPERATURE RANGE		-25°C to +85°C	-55°C to +125°C	*	**

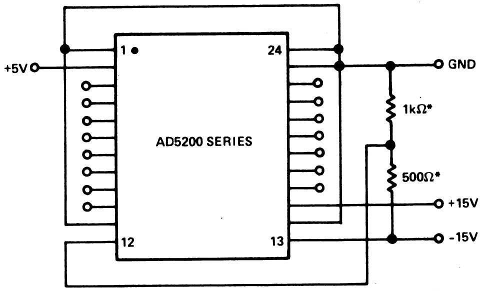
*Sames specifications as AD5201/02B.
**Same specifications as AD5201/02T.
***Same specifications as AD5204/05B.

[1] FSR is Full Scale Range and is equal to the peak to peak input signal.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Positive Supply	+18V
Negative Supply	-18V
Logic Supply	+7V
Analog Input	±25V
Digital Outputs	Logic Supply
Digital Inputs	+5.5V
Reference Supply	-15V



*DIVIDER ADDED FOR EXTERNAL REFERENCE MODELS ONLY.

Burn In Circuit

PROCESSING FOR HIGH RELIABILITY

STANDARD PROCESSING

As part of the standard manufacturing procedure, all models of the AD5200 receive the following processing:

PROCESS	CONDITIONS
1. Pre-Cap Visual Inspection	In-House Criteria
2. Stabilization Bake	24 hours @ +150°C
3. Seal Test, Gross	In-House Criteria
4. Operating Burn-In	48 hours @ +125°C

AD5200 SERIES ORDERING GUIDE

Model	Linearity	Absolute Accuracy	Temperature Range	Package Option[1]
AD520*BD	1/2LSB	2LSB	-25°C to +85°C	HY24C
AD520*BD/883B	1/2LSB	2LSB	-25°C to +85°C	HY24C
AD520*TD	1/2LSB	2LSB	-55°C to +125°C	HY24C
AD520*TD/883B	1/2LSB	2LSB	-55°C to +125°C	HY24C

*Insert number according to desired input voltage range.

[1] See Section 20 for package outline information.

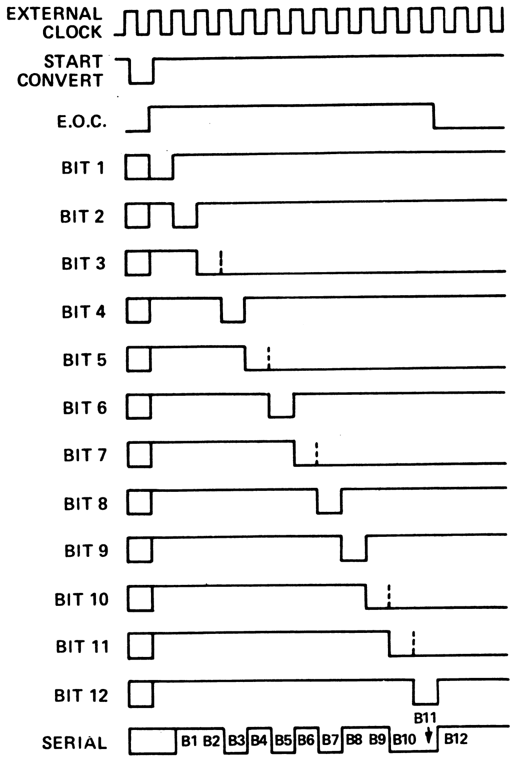


Figure 1. Timing Diagram

TIMING

The timing diagram is shown in Figure 1. A conversion is initiated by holding the start convert low during a rising edge of the clock. The start convert transition must occur at a minimum of 25ns prior to the clock transition. The end of conversion (E.O.C.) signal will be set simultaneously with the initiation of conversion. The actual conversion will not start until the first rising edge of the clock after the start convert is again set high.

Parallel data is valid on the falling edge of the E.O.C. and it will remain valid until the next conversion is initiated. The serial data is in the Non-Return To Zero format and it is valid on the same transition as the parallel data.

An external clock of 260kHz will yield 50μs conversion time. Increasing the clock frequency will decrease the conversion time; the linearity error, however, will increase. Refer to Figure 2 for the acceptable minimum conversion time.

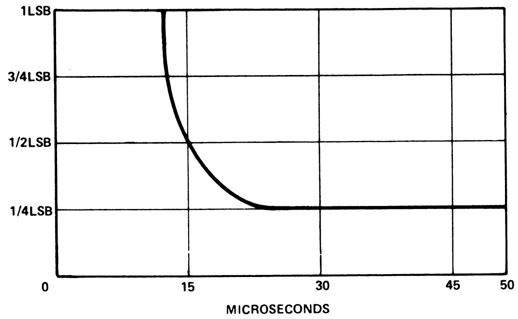


Figure 2. Linearity Error vs. Conversion Time (Normalized)

AD5201/AD5204	AD5202/AD5205	MSB LSB
+5.0000V	+10.000V	0000000000
0.0000V	0.000V	1000000000
-4.9976V	- 9.995V	1111111111

Table 1. Logic Coding (Complementary Offset Binary)

ANALOG DEVICES

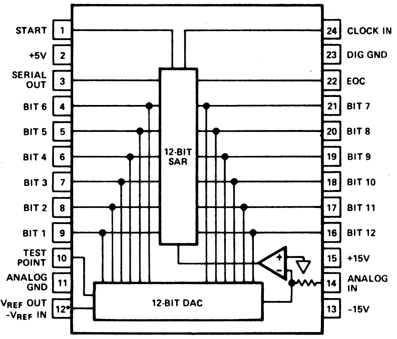
12-Bit Successive Approximation High Accuracy A/D Converter

AD5210 SERIES

FEATURES

- True 12-Bit Operation: ±1/2LSB max Nonlinearity
- Totally Adjustment-Free
- Guaranteed No Missing Codes Over the Specified Temperature Range
- Hermetically-Sealed Package
- Standard Temperature Range: -25°C to +85°C
- Military Temperature Range: -55°C to +125°C
- MIL-STD-883 Processing Available
- Serial and Parallel Outputs
- Monolithic DAC with Scaling Resistors for Stability
- Low Chip Count for High Reliability
- Industry Standard Pin Out
- Small 24-Pin DIP

AD5210 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD5210 series devices are 12-bit successive approximation analog-to-digital converters. The hybrid design utilizes MSI digital, linear monolithic chips and active laser trimming of high-stability thin-film resistors to provide a totally adjustment free converter—no potentiometers are required for calibration.

The innovative design of the AD5210 series devices incorporates a monolithic 12-bit feedback DAC for reduced chip count and higher reliability. The exceptional temperature coefficients of the monolithic DAC guarantees ±1/2LSB linearity over the entire operating temperature range of -25°C to +85°C for the commercial grade and -55°C to +125°C for the military grade.

The AD5210 series converters are available in 2 input voltage ranges: ±5V (AD5211/AD5214) and ±10V (AD5212/AD5215). The converters are available either complete with an internal buried zener reference or with the option of an external reference for improved absolute accuracy.

The AD5210 series converters are available in two performance grades; the "B" is specified from -25°C to +85°C and the "T" is specified from -55°C to +125°C. The "B" and "T" grades are also available processed to MIL-STD-883 level B requirements. All units are available in a 24-pin hermetically sealed ceramic DIP.

PRODUCT HIGHLIGHTS

1. The AD5210 series devices are laser trimmed at the factory to provide a totally adjustment free converter—no potentiometers are required for 12-bit performance.
2. A monolithic 12-bit feedback DAC is used for reduced chip count and higher reliability.
3. The AD5210 series directly replaces other devices of this type with significant increases in performance.
4. The devices offer true 12-bit accuracy and exhibits no missing codes over the entire operating temperature range.
5. The fast conversion rate of the AD5210 series makes it an excellent choice for applications requiring high system throughput rates.

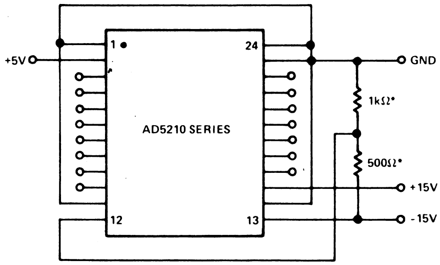
SPECIFICATIONS (typical @ +25°C, ±15V and +5V unless otherwise noted)

INPUT RANGE[1]	INPUT IMPEDANCE				
-5V to +5V	5.0kΩ	AD5211B	AD5211T	AD5214B	AD5214T
-10V to +10V	10.0kΩ	AD5212B	AD5212T	AD5215B	AD5215T
REFERENCE		Internal	*	External -10.000V	***
RESOLUTION		12 Bits	*	*	*
LINEARITY ERROR MAX		±1/2LSB	*	*	*
No Missing Codes T_{min} to T_{max}		Guaranteed	*	*	*
ZERO ERROR, MAX		±1LSB	*	*	*
ZERO ERROR, MAX T_{min} to T_{max}		±2LSB	*	*	*
ABSOLUTE ACCURACY, MAX		±2LSB	*	*	*
ABSOLUTE ACCURACY, MAX T_{min} to T_{max}		±0.4% of FSR[2]	*	±0.1% of FSR[2]	***
CONVERSION TIME, MAX Clock = 1MHz		13μs	*	*	*
LOGIC RATINGS					
Input Logic Commands					
Logic "0"		0.8V max	*	*	*
Logic "1"		+2.0V min	*	*	*
Loading		0.5TTL Load	*	*	*
CLOCK INPUT PULSE WIDTH		100ns min	*	*	*
OUTPUT LOGIC					
Logic "0"		0.4V max	*	*	*
Logic "1"		3.6V (2.4 min)	*	*	*
FANOUT - HIGH		8TTL Loads	*	*	*
FANOUT - LOW		2TTL Loads	*	*	*
POWER SUPPLY REQUIREMENTS					
V_{LOGIC}		+5V ±10%	*	*	*
V_{CC}		+15V ±10%	*	*	*
V_{DD}		-15V ±10%	*	*	*
OPERATING CURRENT					
V_{LOGIC}		25mA (42mA max)	*	*	*
V_{CC}		10mA (16mA max)	*	*	*
V_{DD}		20mA (28mA max)	*	*	*
V_{REF}				0.5mA	***
POWER SUPPLY REJECTION					
V_{CC}		±0.005%/%	*	*	*
V_{DD}		±0.005%/%	*	*	*
POWER CONSUMPTION		575mW	*	*	*
OPERATING TEMPERATURE RANGE		-25°C to +85°C	-55°C to +125°C	*	**

*Same specifications as AD5211/12B.
**Same specifications as AD5211/12T.
***Same specifications as AD5214/15B.
[1] Other input ranges are available, consult factory.
[2] FSR is Full Scale Range and is equal to the peak to peak input signal.
Specifications subject to change without notice.

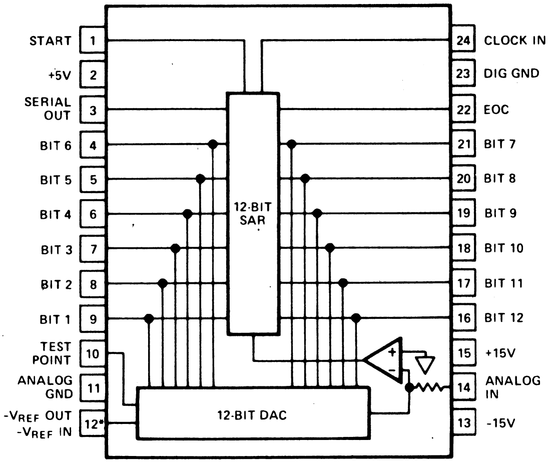
ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Positive Supply	+18V
Negative Supply	-18V
Logic Supply	+7V
Analog Input	±25V
Digital Outputs	Logic Supply
Digital Inputs	+5.5V
Reference Supply	-15V



*DIVIDER ADDED FOR EXTERNAL REFERENCE MODELS ONLY.

Figure 1. Burn In Circuit



*PIN 12 FUNCTION: $-V_{REF\ OUT}$ – AD5211, AD5212
$-V_{REF\ IN}$ – AD5214, AD5215

Figure 2. Pin Designations

AD5211/AD5214	AD5212/AD5215	MSB LSB
+5.0000V	+10.000V	0000000000
0.0000V	0.000V	1000000000
-4.9976V	- 9.995V	1111111111

Table I. Logic Coding (Complementary Offset Binary)

AD5210 SERIES ORDERING GUIDE

Model	Linearity	Absolute Accuracy	Temperature Range	Package Option[1]
AD521*BD	1/2LSB	2LSB	-25°C to +85°C	HY24C
AD521*BD/883B	1/2LSB	2LSB	-25°C to +85°C	HY24C
AD521*TD	1/2LSB	2LSB	-55°C to +125°C	HY24C
AD521*TD/883B	1/2LSB	2LSB	-55°C to +125°C	HY24C

[1] See Section 20 for package outline information.

*Insert number according to desired input voltage range.

THEORY OF OPERATION

On receipt of a CONVERT START command, the AD5210 converts the voltage as its analog input into an equivalent 12-bit binary number. This conversion is accomplished as follows: the 12-bit successive-approximation register (SAR) has its 12-bit outputs connected both to the device bit output pins and to the corresponding bit inputs of the feedback DAC. The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

TIMING

The timing diagram is shown in Figure 3. A conversion is initiated by holding the start convert low during a rising edge of the clock. The start convert transition must occur at a minimum of 25ns prior to the clock transition. The end of conversion (E.O.C.) signal will be set simultaneously with the initiation of conversion. The actual conversion will not start until the first rising edge of the clock after the start convert is again set high. At time t_0, B_1 is reset and B_2–B_{12} are set unconditionally. At t_1 the Bit 1 decision is made and Bit 2 is unconditionally reset. At t_2, the Bit 2 decision is made (keep) and Bit 3 is reset unconditionally. This sequence continues until the Bit 12 (LSB) decision (keep) is made at t_{12}. The STATUS flag is reset at time t_{12} indicating that the conversion is complete and that the parallel output data is valid.

Corresponding serial and parallel data bits become valid on the same positive-going clock edge. Serial data does not change and is guaranteed valid on negative-going clock edges, however; serial data can be transferred quite simply by clocking it into a receiving shift register on these edges (see Figure 3) An external clock of 1MHz will yield 13μs conversion time. Increasing the clock frequency will decrease the conversion time; the linearity error, however, will increase.

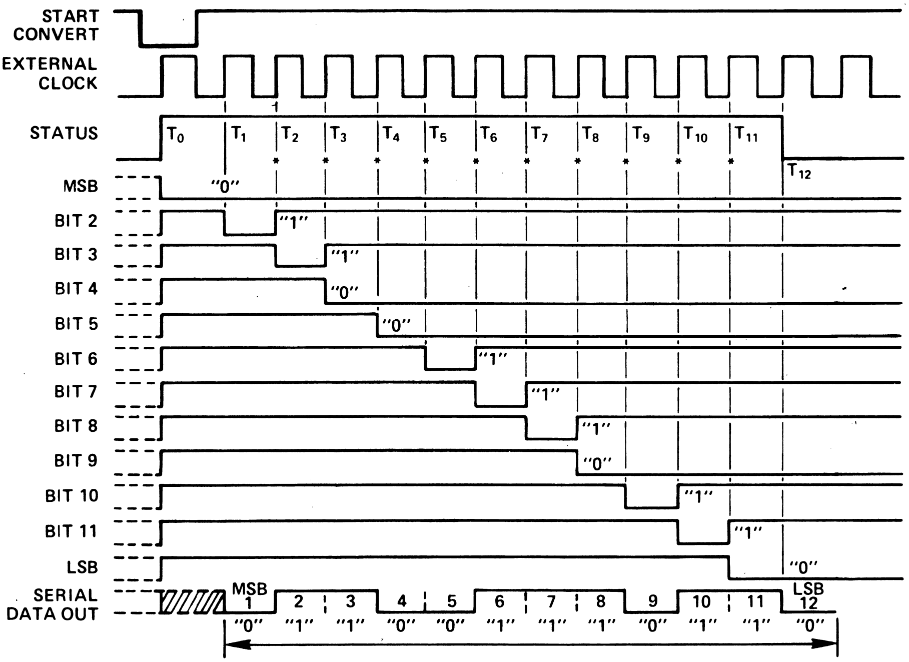


Figure 3. Timing Diagram

The analog continuum is partitioned into 2^{12} discrete ranges for 12-bit conversion. All analog values within a given quantum are represented by the same digital code, usually assigned to the nominal midrange value. There is an inherent quantization uncertainty of ±1/2LSB, associated with the resolution, in addition to the actual conversion errors.

The actual conversion errors that are associated with A/D converters are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, reference error and power supply rejection. The matching and tracking errors in the converter have been minimized by the use of a monolithic DAC that includes the scaling network. The initial gain and offset errors have been internally trimmed to provide an absolute accuracy of ±0.05%. Linearity error is defined as the deviation from a true straight line transfer characteristic from a zero analog input which calls for a zero digital output to a point which is defined as full scale. The linearity error is unadjustable and is the most meaningful indication of A/D converter accuracy. Differential nonlinearity is a measure of the deviation in the staircase step width between codes from the ideal least significant bit step size (Figure 4).

Monotonic behavior requires that the differential linearity error be less than 1LSB, however a monotonic converter can have missing codes; the AD5210 is specified as having no missing codes over the entire temperature range as specified on the data page.

There are three types of drift error over temperature: offset, gain and linearity. Offset drift causes a shift of the transfer characteristic left or right over the operating temperature range. Gain drift causes a rotation of the transfer characteristic about the zero or minus full scale point. The worst case accuracy drift is the summation of all three drift errors over temperature. Statistically, however, the drift error behaves as the root-sum-squared (RSS) and can be shown as:

$$RSS = \sqrt{\epsilon_G{}^2 + \epsilon_O{}^2 + \epsilon_L{}^2}$$

ϵ_G = Gain Drift Error (ppm/°C)

ϵ_O = Offset Drift Error (ppm of FSR/°C)

ϵ_L = Linearity Error (ppm of FSR/°C)

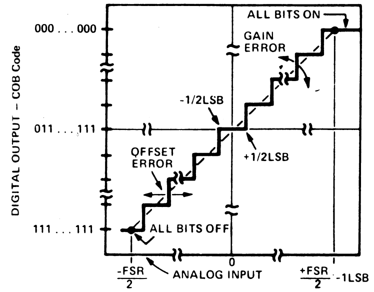
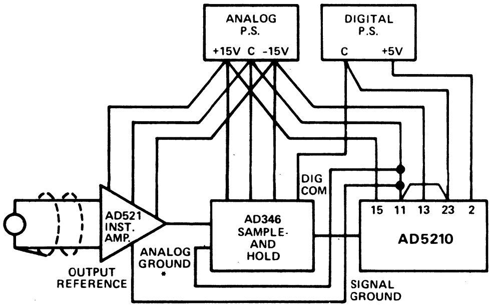


Figure 4. Transfer Characteristics for an Ideal Bipolar A/D

GROUNDING

Many data-acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Digital Ground and Analog Ground (Analog Power Return). These grounds must be tied together at one point, usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the ground pin of the AD5210. Separate ground returns should be provided to minimize the current flow in the path from sensitive points to the system ground point. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.



*IF INDEPENDENT, OTHERWISE RETURN AMPLIFIER REFERENCE TO MECCA AT ANALOG P.S. COMMON

Figure 5. Basic Grounding Practice

Each of the AD5210's supply terminals should be capacitively decoupled as close to the AD5210 as possible. A large value capacitor such as 1µF in parallel with 0.01µF capacitor is usually sufficient. Analog supplies are bypassed to the Analog Ground pin and the logic supply is bypassed to the Digital Ground pin.

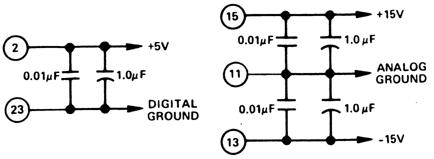


Figure 6. Power Supply Decoupling

SAMPLED DATA SYSTEMS

The conversion speed of the AD5210 allows accurate digitization of high frequency signals and high throughput rates in multichannel data acquisition systems. To make the AD5210 capable of full benefit from this high speed, a fast sample-hold amplifier such as the AD346 or ADSHC-85 is required. Figures 7 and 8 show the use of an AD346 and ADSHC-85 as sample and holds in combination with the AD5210.

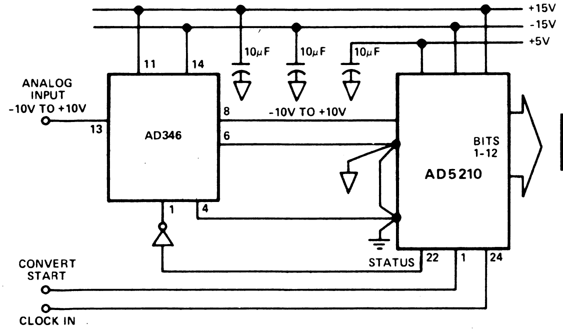


Figure 7. 66.6Hz–12-Bit, A/D Conversion System

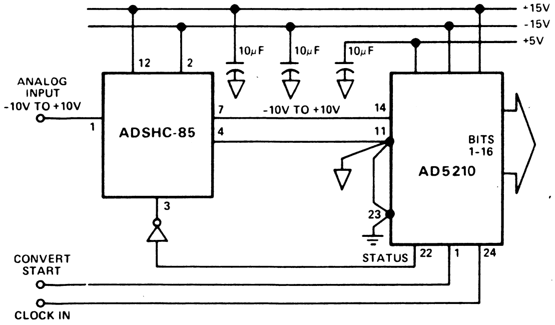


Figure 8. 57.1kHz–12-Bit, A/D Conversion System

In sampled data systems there are two limiting factors in digitizing high frequency signals. The maximum value of input signal frequency that can be acquired and digitized using a sample and hold amplifier and A/D converter combination is influenced by the bandwidth of the SHA, but it is also dictated by:

A. The aperture uncertainty (jitter) of the sample and hold amplifier.

B. The desired accuracy and corresponding resolution of the converter.

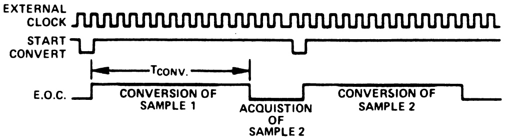
The resolution of an AD5210 is 1 part in 4096 to a tolerance of 0.012% of the full scale range, the maximum value of input signal frequency which can be digitized is determined by:

$$F_{MAX}/ = \frac{2^{-N}}{(2\pi)(\text{Aperture Uncertainty})}$$

$$F_{MAX}/AD346 = \frac{1}{(2\pi)\,(4096)\,(4 \times 10^{-10})} = 97.1\text{kHz}$$

$$F_{MAX}/ADSHC\text{-}85 = \frac{1}{(2\pi)\,(4096)\,(5 \times 10^{-10})} = 77.7\text{kHz}$$

The maximum throughput rate for each of these combinations is again different. The maximum throughput rate is the sum of the sample and hold acquisition time and A/D conversion time as shown in Figure 9.



E. O.C. CONNECTED TO SAMPLE AND HOLD MODE CONTROL

Figure 9. START/E.O.C. Timing for Sampled Data System

When using an AD346 with an AD5210 the throughput rate is, 2.0μs acquisition time plus 13μs conversion time, 66.6kHz. The ADSHC-85 used in combination with an AD5210 is, 4.5μs acquisition time plus 13μs conversion time, 57.1kHz. To meet the requirements of the nyquist sampling criteria, the AD346 and AD5210 combination can be used for input frequencies from dc through 33.3kHz; the ADSHC-85 and AD5210 combination for inputs from dc through 28.5kHz. Input frequencies higher than these (up to the maximum frequency) would result in "under-sampling" of the input signal. Signals up to the maximum frequency could be processed if their bandwidth is less than one-half the sample frequency.

A fast (32kHz) 12-bit DAS can be configured using the AD362 and the AD5210. The AD362 contains two 8-channel multiplexers, a differential amplifier, a sample-and-hold with high-speed output amplifier, a channel address latch and control logic. The multiplexers may be connected to the differential amplifier in either an 8-channel differential or 16-channel single-ended configuration. A feature of the AD362 is an internal user-controllable analog switch that connects the multiplexers in either a single-ended or differential mode. This allows a single device to perform in either mode without hardwire programming and permits a mixture of single-ended and differential sources to be interfaced by dynamically switching the input mode control.

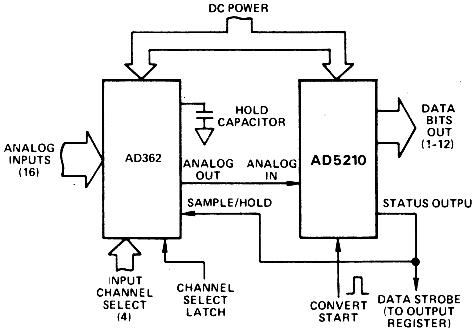


Figure 10. High Speed 12-Bit DAS

CONVERT START USING A POSITIVE EDGE

In some systems it may be inconvenient to generate a negative going start convert pulse of the proper width. The circuit of Figure 11 can be used to start a conversion on the AD5210 series of A/Ds with a positive going edge. To perform a conversion both the convert start signal and the E.O.C. must be low. The output of the inverter and nand gate will then be in the high state. The converter will reset on the next rising clock edge. Resetting brings the E.O.C. to a high state; the inverter goes low; the convert start is still high so the output of the nand gate goes high allowing the conversion to continue immediately. The convert start line has only to be brought back down before the conversion is complete.

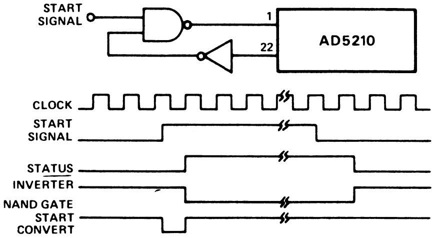


Figure 11. Convert Start Using a Positive Edge

ANALOG DEVICES

Very Fast, Complete 12-Bit A/D Converter

AD5240

FEATURES

Performance

Complete 12-Bit A/D Converter with Reference and Clock
Fast Successive Approximation Conversion: 5μs
Buried Zener Reference for Long Term Stability and Low Gain T.C.: 10ppm/°C
Max Nonlinearity: <±0.012%
Low Power: 775mW Typical
Hermetic Package Available
Low Chip Count – High Reliability
Pin Compatible with AD ADC84/AD ADC85
"Z" Models for ±12V Operation Available
MIL-STD-883B Processing Available
Military Temperature Range -55°C to +125°C

Versatility

Negative-True Parallel or Serial Logic Outputs
Short Cycle Capability
Precision +6.3V Reference for External Applications

PRODUCT DESCRIPTION

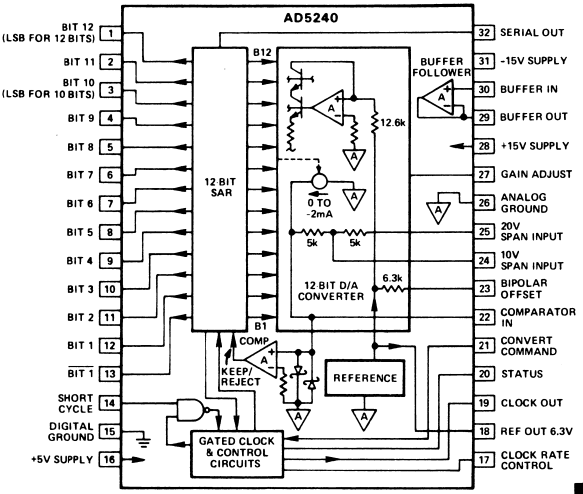
The AD5240 is a high speed low cost 12-bit successive approximation analog-to-digital converter that includes an internal clock, reference and comparator. Its hybrid IC design utilizes MSI digital and linear monolithic chips in conjunction with a 12-bit monolithic DAC to provide modular performance and versatility with IC size, price and reliability.

Important performance characteristics of the AD5240 include a maximum linearity error at +25°C of 0.012%, gain T.C. below 15ppm/°C, typical power dissipation of 775mW, and conversion time of less than 5μs for 12-bit conversions. Of considerable significance in military and aerospace applications is the guaranteed performance from -55°C to +125°C of the AD5240S which is also available processed to MIL-STD-883B. Monotonic operation of the feedback D/A converter guarantees no missing output codes over temperature ranges of 0 to +70°C, and -55°C to +125°C.

The design of the AD5240 includes scaling resistors that provide analog input signal ranges of ±2.5V, ±5V, ±10V, 0 to +5V, or 0 to +10V. Adding flexibility and value are the +6.3V precision reference, which also can be used for external applications, and the input buffer amplifier. All digital signals are fully DTL and TTL compatible, and the data output is negative-true and available in either serial or parallel form.

The AD5240K is specified for operation over the 0 to +70°C temperature range and the AD5240S is specified for the -55°C to +125°C range.

AD5240 FUNCTIONAL BLOCK DIAGRAM



32-PIN DIP

PRODUCT HIGHLIGHTS

1. The AD5240 is a complete 12-bit A/D converter. No external components are required to perform a conversion.
2. The AD5240 directly replaces other devices of this type with significant increases in performance.
3. The fast conversion rate of the AD5240 makes it an excellent choice for applications requiring high system throughput rates.
4. The internal buried zener reference is laser trimmed to 6.3V ±0.1% and 10ppm/°C typical T.C. The reference is available externally and can provide up to 1mA.
5. The integrated package construction provides high quality and reliability with small size and weight.
6. The monolithic 12-bit feedback DAC is used for reduced chip count and high reliability.
7. The AD5240SD/883B comes processed to MIL-STD-883, class B requirements.

SPECIFICATIONS (typical @ +25°C, ±15V and +5V unless otherwise noted)

MODEL	AD5240KD	AD5240SD
RESOLUTION	12 Bits	12 Bits
ANALOG INPUTS		
Voltage Ranges		
Bipolar	±2.5V, ±5V, ±10V	•
Unipolar	0V to +5V, 0V to +10V	•
Impedance (Direct Input)		
0V to +5V, ±2.5V	2.5kΩ(±20%)	•
0V to +10V, ±5V	5kΩ(±20%)	•
±10V	10kΩ(±20%)	•
Buffer Amplifier[1]		
Impedance (min)	100MΩ	•
Bias Current	50nA	•
Offset Voltage	6mV	
Settling Time		
To 0.01% for 20V Step	2μs	•
DIGITAL INPUTS[2]		
Convert Command	Positive Pulse 50ns min Trailing Edge Initiates Conversion	•
Logic Loading	1TTL Load	•
TRANSFER CHARACTERISTICS		
Gain Error[3]	±0.2%	•
Offset Error[3]	Adjustable to Zero	•
Unipolar	±0.1% of FSR[4]	•
Bipolar[5]	±0.2% of FSR[4]	•
Linearity Error (max)[6]		•
Inherent Quantization Error	±0.012% FSR	•
Differential Linearity Error	±1/2LSB	•
No Missing Codes Temperature Range	0 to +70°C	-55°C to +125°C
Power Supply Sensitivity		
±15V	±0.004% of FSR/% V	•
+5V	±0.001% of FSR/% V	•
DRIFT		
Specification Temperature Range	0 to +70°C	-55°C to +125°C
Gain (max)	±30ppm/°C	±25ppm/°C
Offset		
Unipolar	±3ppm/°C	•
Bipolar (max)[5]	±15ppm/°C	±7ppm/°C
Linearity (max)	±2ppm/°C	•
Monotonicity	GUARANTEED	•
CONVERSION SPEED (MAX)	5μs	•
DIGITAL OUTPUT		
(all codes complementary)		
Parallel		
Output Codes[7]		
Unipolar	CSB	•
Bipolar	COB, CTC	•
Output Drive	2TTL Loads	•
Serial Data Codes (NRZ)	CSB, COB	•
Output Drive	2TTL Loads	•
Status	Logic "1" during Conversion	•
Status Output Drive	2TTL Loads	•
Internal Clock		
Clock Output Drive	2TTL Loads	•
Frequency[8]	2.6MHz	•
INTERNAL REFERENCE VOLTAGE	6.3V/±15mV max	•
Max. External Current (with no degradation of specifications)	1.0mA	•
Tempco of Reference	±10ppm/°C	•
POWER REQUIREMENTS		
Rated Voltages	+5V, ±15V	•
Range for Rated Accuracy	4.75V to 5.25V and ±13.5V to ±16.5V	•
Z Models[9]	4.75V to 5.25V and ±11.4V to ±16.5V	•
Supply Drain +15V	15mA max	•
-15V	35mA max	•
+5V	100mA max	•
Total Power Dissipation	1100mW max	•
TEMPERATURE RANGE		
Specification	0 to +70°C	-55°C to +125°C
Operating (Derated Specs)	-25°C to +85°C	
Storage	-65°C to +150°C	•
PACKAGE OPTION[10]	Hermetic Ceramic (HY32F)	Hermetic Ceramic (HY32F)

NOTES

[1] Buffer Settling time adds to conversion speed when buffer is connected to input.

[2] DTL/TTL compatible Logic "0" = 0.8V max, Logic "1" = 2.0V min for digital input, Logic "0" = 0.4V max, Logic "1" = 2.4V min, digital output.

[3] Adjustable to zero.

[4] FSR means Full Scale Range.

[5] Guaranteed at $V_{IN} = 0$ volts.

[6] Error shown is the same as ±1/2LSB max error in % of FSR.

[7] See Table I.

[8] Pin 17 tied to +5V.

[9] For ±12V operaton add "Z" to model number. Input range limited to a maximum of ±5V when input buffer is used.

[10] See Section 20 for package outline information.

•Specifications same as AD5240KD.
Specifications subject to change without notice.

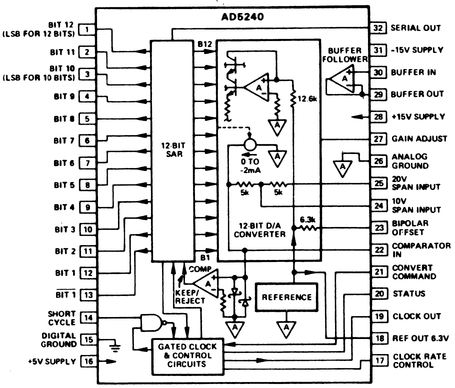


Figure 1. AD5240 Functional Diagram and Pin Out

ORDERING GUIDE

Model	Power Requirements	Temperature Range
AD5240KD	±15V	0 to +70°C
AD5240ZKD	±12V	0 to +70°C
AD5240SD	±15V	-55°C to +125°C
AD5240ZSD	±12V	-55°C to +125°C
AD5240SD/883B	±15V	-55°C to +125°C
AD5240ZSD/883B	±12V	-55°C to +125°C

Typical Performance Curves

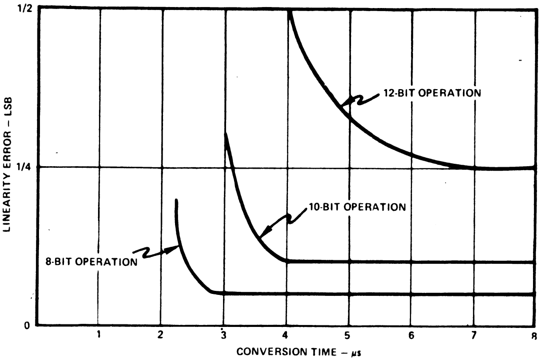


Figure 2. Linearity Error vs. Conversion Speed

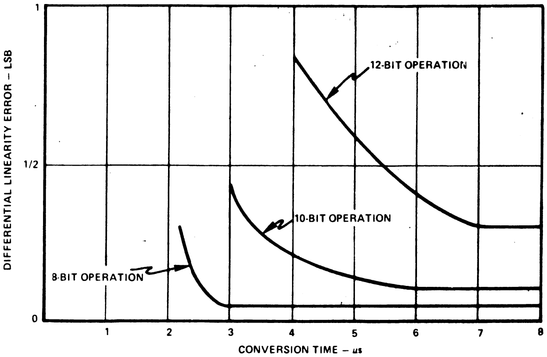


Figure 3. Differential Linearity Error vs. Conversion Speed

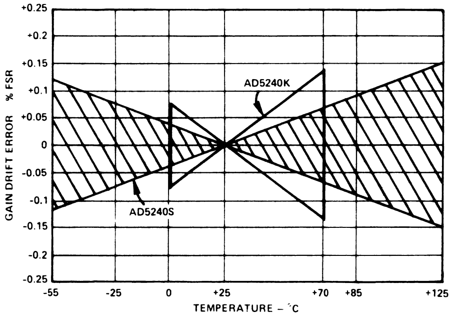


Figure 4. Gain Drift Error (% FSR) vs. Temperature

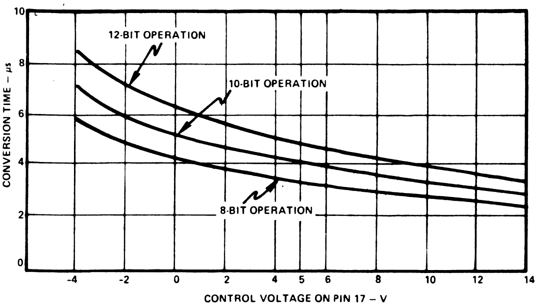


Figure 5. Conversion Speed vs. Control Voltage

The analog continuum is partitioned into 2^{12} discrete ranges for 12-bit conversion. All analog values within a given quantum are represented by the same digital code, usually assigned to the nominal midrange value. There is an inherent quantization uncertainty of ±1/2LSB, associated with the resolution, in addition to the actual conversion errors.

The actual conversion errors that are associated with A/D converters are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, reference error and power supply rejection. The matching and tracking errors in the converter have been minimized by the use of a monolithic DAC that includes the scaling network. The initial gain and offset errors are specified at ±0.2% FSR for gain and ±0.1% FSR for offset. These errors may be trimmed to zero by the use of the external trim circuits as shown in Figures 11 and 13. Linearity error is defined as the deviation from a true straight line transfer characteristic from a zero analog input which calls for a zero digital output to a point which is defined as full scale. The linearity error is unadjustable and is the most meaningful indication of A/D converter accuracy. Differential nonlinearity is a measure of the deviation in the staircase step width between codes from the ideal least significant bit step size (Figure 6).

Monotonic behavior requires that the differential linearity error be less than 1LSB, however a monotonic converter can have missing codes; the AD5240 is specified as having no missing codes over the entire temperature range as specified on the data page.

There are three types of drift error over temperature: offset, gain and linearity. Offset drift causes a shift of the transfer characteristic left or right over the operating temperature range. Gain drift causes a rotation of the transfer characteristic about the zero or minus full scale point. The worst case accuracy drift is the summation of all three drift errors over temperature. Statistically, however, the drift error behaves as the root-sum-squared (RSS) and can be shown as:

$$\text{RSS} = \sqrt{\epsilon_G{}^2 + \epsilon_O{}^2 + \epsilon_L{}^2}$$

ϵ_G = Gain Drift Error (ppm/°C)

ϵ_O = Offset Drift Error (ppm of FSR/°C)

ϵ_L = Linearity Error (ppm of FSR/°C)

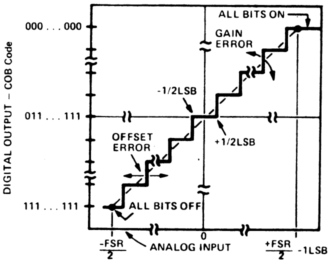


Figure 6. Transfer Characteristics for an Ideal Bipolar A/D

THEORY OF OPERATION

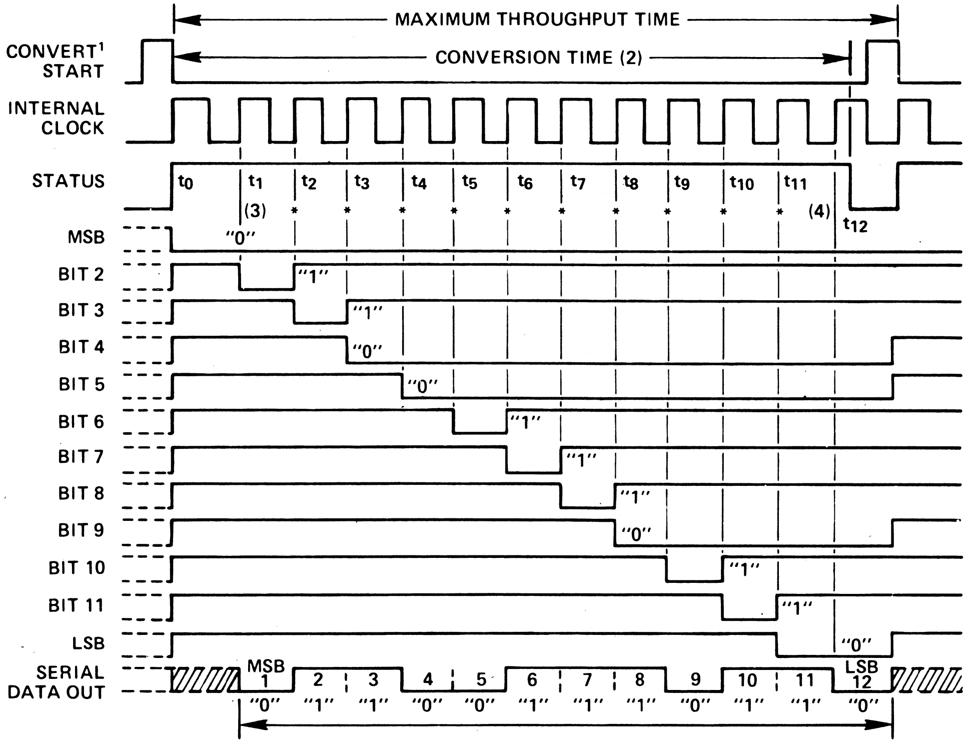
On receipt of a CONVERT START command, the AD5240 converts the voltage as its analog input into an equivalent 12-bit binary number. This conversion is accomplished as follows: the 12-bit successive-approximation register (SAR) has its 12-bit outputs connected both to the device bit output pins and to the corresponding bit inputs of the feedback DAC. The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

TIMING

The timing diagram is shown in Figure 8. Receipt of a CONVERT START signal sets the STATUS flag, indicating conversion in progress. This, in turn, removes the inhibit applied to the gated clock, permitting it to run through 13 cycles. All the SAR parallel bits, STATUS flip-flops, and the gated clock inhibit signal are initialized on the trailing edge of the CONVERT START signal. At time t_0, B_1 is reset and B_2 - B_{12} are set unconditionally. At t_1 the Bit 1 decision is made (keep) and Bit 2 is unconditionally reset. At t_2, the Bit 2 decision is made (keep) and Bit 3 is reset unconditionally. This sequence continues until the Bit 12 (LSB) decision (keep) is made at t_{12}. After a 40ns delay period, the STATUS flag is reset, indicating that the conversion is complete and that the parallel output data is valid. Resetting the STATUS flag restores the gated clock inhibit signal, forcing the clock output to the Logic "0" state.

Corresponding serial and parallel data bits become valid on the same positive-going clock edge. Serial data does not change and is guaranteed valid on negative-going clock edges, however; serial data can be transferred quite simple by clocking it into a receiving shift register on these edges (see Figure 7).

Incorporation of this 40ns delay guarantees that the parallel (and serial) data are valid at the Logic "1" to "0" transition of the STATUS flag, permitting parallel data transfer to be initiated by the trailing edge of the STATUS signal.



NOTES:
1. THE CONVERT START PULSE WIDTH IS 50ns MIN AND MUST REMAIN LOW DURING A CONVERSION. THE CONVERSION IS INITIATED BY THE "TRAILING EDGE" OF THE CONVERT COMMAND.
2. 5μs FOR 12 BITS AND 4.2μs FOR 10 BITS (MAX – PIN 17 TIED TO +5V)
3. MSB DECISION
4. LSB DECISION 40ns PRIOR TO THE STATUS GOING LOW

*BIT DECISIONS

Figure 7. Timing Diagram (Binary Code 011001110110)

DIGITAL OUTPUT DATA

Both parallel and serial data from TTL storage registers are in negative true form. Parallel data output coding is complementary binary for unipolar ranges and either complementary offset binary or complementary two's complement binary, depending on whether BIT 1 (pin 12) or its logical inverse $\overline{\text{BIT 1}}$ (pin 13) is used as the MSB. Parallel data becomes valid approximately 40ns before the STATUS flag returns to Logic "0", permitting parallel data transfer to be clocked on the "1" to "0" transition of the STATUS flag.

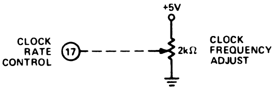
Serial data coding is complementary binary for unipolar input ranges and complementary offset binary for bipolar input ranges. Serial output is by bit (MSB first, LSB last) in NRZ (non-return-to-zero) format. Serial and parallel data outputs change state on positive-going clock edges. Serial data is guaranteed valid 200ns after the rising clock edges, permitting serial data to be clocked directly into a receiving register on the negative-going clock edges as shown in Figure 7. There are 13 negative-going clock edges in the complete 12-bit conversion cycle, as shown in Figure 7. The first edge shifts an invalid bit into the register, which is shifted out on the 13th negative-going clock edge. All serial data bits will have been correctly transferred and be in the receiving shift register locations shown at the completion of the conversion period.

Short Cycle Input: A Short Cycle Input, pin 14, permits the timing cycle shown in Figure 8 to be terminated after any number of desired bits has been converted, permitting somewhat shorter conversion times in applications not requiring full 12-bit resolution. When 12-bit resolution is required, pin 14 is connected to +5V (pin 16). When 10-bit resolution is desired, pin 14 is connected to Bit 11 output pin 2. The conversion cycle then terminates and the STATUS flag resets after the Bit 10 decision (t_{10} +40ns in timing diagram of Figure 7). Short Cycle pin connections and associated maximum 12-, 10- and 8-bit conversion times are summarized in the table below.

Connect Short Cycle Pin 14 To Pin:	Connect Clock Rate Control Pin 17 To	Bits	Resolution (% FSR)	Maximum Conversion Time (μs)	Status Flag Reset
16	16	12	0.024	5.0	t_{12} +40ns
2	16	10	0.100	4.1	t_{10} +40ns
4	16	8	0.390	3.3	t_8 +40ns

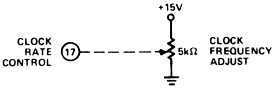
CLOCK RATE CONTROL ALTERNATE CONNECTIONS

If adjustment of the CLOCK RATE is desired for faster conversion speeds, the CLOCK RATE CONTROL may be connected to an external multi-turn trim potentiometer with a TCR of ±100ppm/°C or less as shown in Figures 8 and 9. If the potentiometer is connected to -15V, conversion time can be increased as shown in Figure 8. If these adjustments are used, delete the connections shown in the previous table for pin 17. See Figure 2 for linearity error vs. conversion speed and Figure 5 for the effect of the control voltage on clock speed.



(12-BIT RESOLUTION)
RANGE OF ADJUSTMENT IS 5 TO 6.1μs

Figure 8. 12-Bit Clock Rate Control Optional Fine Adjust



(8- OR 10-BIT RESOLUTION)
RANGE OF ADJUSTMENT IS 2.5 TO 5μs
10-BIT AND 2.2 TO 4.1μs FOR 8-BIT RESOLUTIONS

Figure 9. 8-Bit Clock Rate Control Optional Fine Adjust

INPUT SCALING

The AD5240 inputs should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 10 for circuit details.

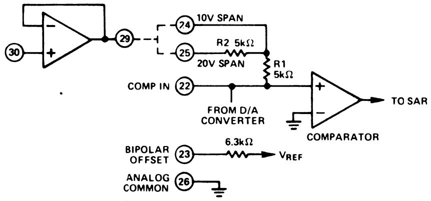


Figure 10. AD5240 Input Scaling Circuit

Input Signal Range	Output Code	Connect Pin 23 To Pin	Connect Pin 25 To	For Direct Input Connect Input Signal To	For Buffered Input Pin 30 Connect Pin 29 To Pin
±10V	COB or CTC	22	Input Signal	25	25
±5V	COB or CTC	22	Open	24	24
±2.5V	COB or CTC	22	Pin 22	24	24
0V to +5V	CSB	26	Pin 22	24	24
0V to +10V	CSB	26	Open	24	24

Table II. Input Scaling Connections

Analog Input Voltage Range		±10V	±5V	±2.5V	0V to +10V	0V to +5V
Code Designation		COB* or CTC**	COB* or CTC**	COB* or CTC**	CSB***	CSB***
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$
	n = 8	78.13mV	39.06mV	19.53mV	39.06mV	19.53mV
	n = 10	19.53mV	9.77mV	4.88mV	9.77mV	4.88mV
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV
Transition Values MSB LSB						
000 . . . 000****	+Full Scale	+10V -3/2LSB	+5V -3/2LSB	+2.5V -3/2LSB	+10V -3/2LSB	+5V -3/2LSB
011 . . . 111	Mid Scale	0	0	0	+5V	+2.5V
111 . . . 110	-Full Scale	-10V +1/2LSB	-5V +1/2LSB	-2.5V +1/2LSB	0 + 1/2LSB	0 +1/2LSB

NOTES:
*COB = Complementary Offset Binary
**CTC = Complementary Two's complement–obtained by using the complement of the most significant bit ($\overline{\text{MSB}}$). $\overline{\text{MSB}}$ is available to pin 13.
***CSB = Complementary Straight Binary.
****Voltages given are the nominal value for transition to the code specified.

Table I. Input Voltage Range and LSB Values

OFFSET ADJUSTMENT

The zero adjust circuit consists of a potentiometer connected across $\pm V_S$ with its slider connected through a 1.8MΩ resistor to Comparator Input pin 22 for all ranges. As shown in Figure 11 the tolerance of this fixed resistor is not critical, and a carbon composition type is generally adequate. Using a carbon composition resistor having a -1200ppm/°C tempco contributes a worst-case offset tempco of $8 \times 244 \times 10^{-6} \times 1200$ppm/°C = 2.3ppm/°C of FSR, if the OFFSET ADJ potentiometer is set at either end of its adjustment range. Since the maximum offset adjustment required is typically no more than ±4LSB, use of a carbon composition offset summing resistor typically contributes no more than 1ppm/°C of FSR offset tempco.

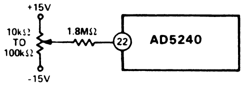


Figure 11. Offset Adjustment Circuit

An alternate offset adjust circuit, which contributes negligible offset tempco if metal film resistors (tempco <100 ppm/°C) are used, is shown in Figure 12.

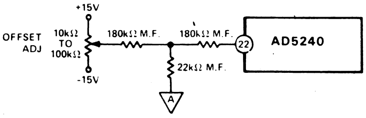


Figure 12. Low Tempco Zero Adjustment Circuit

In either zero adjust circuit, the fixed resistor connected to pin 22 should be located close to this pin to keep the pin connection runs short (Comparator Input pin 22 is quite sensitive to external noise pick-up).

GAIN ADJUSTMENT

The gain adjust circuit consists of a potentiometer connected across $\pm V_S$ with its slider connected through a 10MΩ resistor to the gain adjust pin 27 as shown in Figure 13.

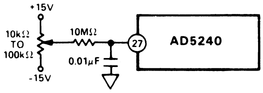


Figure 13. Gain Adjustment Circuit

An alternate gain adjust circuit which contributes negligible gain tempco if metal film resistors (Tempco <100ppm/°C) are used is shown in Figure 14.

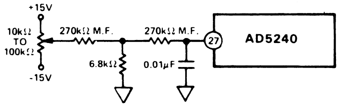
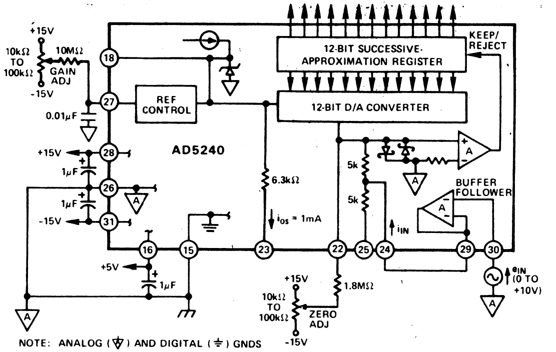


Figure 14. Low Tempco Gain Adjustment Circuit

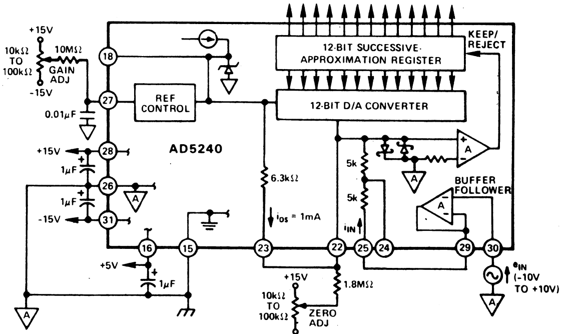
CALIBRATION

External ZERO ADJ and GAIN ADJ potentiometers, connected as shown in Figures 11 and 13 are used for device calibration. To prevent interaction of these two adjustments, Zero is always adjusted first and then Gain. Zero is adjusted with the analog input near the most negative end of the analog range (0 for unipolar and -FS for bipolar input ranges). Gain is adjusted with the analog input near the most positive end of the analog range.



NOTE: ANALOG (▽) AND DIGITAL (⏚) GNDS ARE NOT TIED INTERNALLY AND MUST BE CONNECTED EXTERNALLY.

Figure 15. Analog and Power Connections for Unipolar 0 to +10V Input Range with Buffer Follower



NOTE: ANALOG (▽) AND DIGITAL (⏚) GNDS ARE NOT TIED INTERNALLY AND MUST BE CONNECTED EXTERNALLY.

Figure 16. Analog and Power Connections for Bipolar -10V to +10V Input Range with Buffer Follower

0 to +10V Range: Set analog input to +1LSB = +0.0024V. Adjust Zero for digital output = 111111111110. Zero is now calibrated. Set analog input to +FSR -2LSB = +9.9952V. Adjust Gain for 000000000001 digital output code; full-scale (Gain) is now calibrated. Half-scale calibration check: set analog input to +5.0000V; digital output code should be 011111111111.

-10V to +10V Range: Set analog input to -9.9951V; adjust Zero for 111111111110 digital output (complementary offset binary) code. Set analog input to +9.9902V; adjust Gain for 000000000001 digital output (complementary offset binary) code. Half-scale calibration check: set analog input to 0.0000V; digital output (complementary offset binary) code should be 0111111111111.

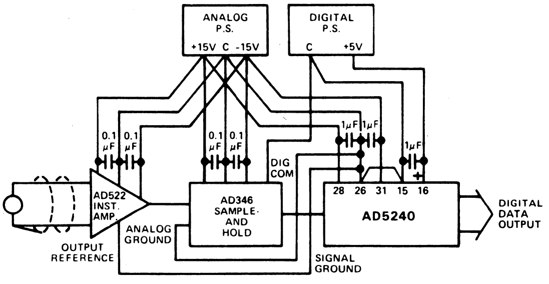
Other Ranges: Representative digital coding for 0 to +10V and -10V to +10V ranges is given above. Coding relationships and calibration points for 0 to +5V, -2.5V to +2.5V and -5V to +5V ranges can be found by halving the corresponding code equivalents listed for the 0 to +10V and -10V to +10V ranges, respectively.

Zero and full-scale calibration can be accomplished to a precision of approximately ±1/4LSB using the static adjustment procedure described above. By summing a small sine or triangular-wave voltage with the signal applied to the analog input, the output can be cycled through each of the calibration codes of interest to more accurately determine the center (or end points) of each discrete quantization level. A detailed description of this dynamic calibration technique is presented in "A/D Conversion Notes", D. Sheingold, Analog Devices, Inc., 1977, Part II, Chapter 4.

GROUNDING

Many data-acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return), and Analog Signal Ground. These grounds must be tied together at one point, usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the ground pin of the AD5240. Separate ground returns should be provided to minimize the current flow in the path from sensitive points to the system ground point. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

Each of the AD5240's supply terminals should be capacitively decoupled as close to the AD5240 as possible. A large value capacitor such as 1μF in parallel with a 0.1μF capacitor is usually sufficient. Analog supplies are bypassed to the Analog supplies are bypassed to the Analog Power Return pin and the logic supply is bypassed to the Logic Power Return pin.



*IF INDEPENDENT, OTHERWISE RETURN AMPLIFIER REFERENCE TO MECCA AT ANALOG P.S. COMMON

Figure 17. Basic Grounding Practice

SAMPLED DATA SYSTEMS

The conversion speed of the AD5240 allows accurate digitization of high frequency signals and high throughput rates in multichannel data acquisition systems. To make the AD5240 capable of full benefit from this high speed, a fast sample-hold amplifier such as the AD346 or ADSHC-85 is required. Figures 18 and 19 show the use of an AD346 and ADSHC-85 as sample and hold's in combination with the AD5240.

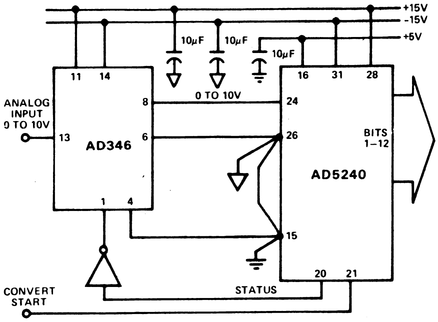


Figure 18. 142.8kHz–12-Bit, A/D Conversion System

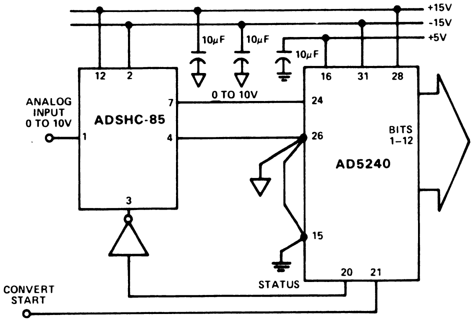


Figure 19. 105kHz–12-Bit, A/D Conversion System

In sampled data systems there are two limiting factors in digitizing high frequency signals. The maximum value of input signal frequency that can be acquired and digitized using a sample and hold amplifier and A/D converter combination is influenced by the bandwidth of the SHA, but it is also dictated by:

A. The aperture uncertainty (jitter) of the sample and hold amplifier.

B. The desired accuracy, and corresponding resolution of the converter.

The resolution of an AD5240 is 1 part in 4096 to a tolerance of 0.012% of the full scale range, the maximum value of input signal frequency which can be digitized is determined by:

$$F_{MAX}/ = \frac{2^{-N}}{(2\pi)\,(\text{Aperture Uncertainty})}$$

$$F_{MAX}/\text{AD346} = \frac{1}{(2\pi)\,(4096)\,(4 \times 10^{-10})} = 97.1\text{kHz}$$

$$F_{MAX}/\text{ADSHC-85} = \frac{1}{(2\pi)\,(4096)(5 \times 10^{-10})} = 77.7\text{kHz}$$

The maximum throughput rate for each of these combinations is again different. The maximum throughput rate is the sum of the sample and hold acquisition time and A/D conversion time as shown in Figure 20.

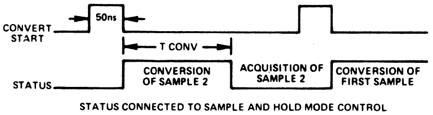

CONVERT START
50ns
T CONV
STATUS
CONVERSION OF SAMPLE 2
ACQUISITION OF SAMPLE 2
CONVERSION OF FIRST SAMPLE
STATUS CONNECTED TO SAMPLE AND HOLD MODE CONTROL

Figure 20. Start/Status Timing for Sampled Data System

When using an AD346 with an AD5240 the throughput rate is, 2.0µs acquisition time plus 5µs conversion time, 142.8kHz. The ADSHC-85 used in combination with an AD5240 is, 4.5µs acquisition time plus 5µs conversion time, 105.3kHz. To meet the requirements of the nyquist sampling criteria, the AD346 and AD5240 combination can be used for input frequencies from dc through 71kHz; the ADSHC-85 and AD5240 combination for inputs from dc through 52kHz. Input frequencies higher than these (up to the maximum frequency) would result in "under-sampling" of the input signal. Signals up to the maximum frequency could be processed if their bandwidth is less than one-half the sample frequency.

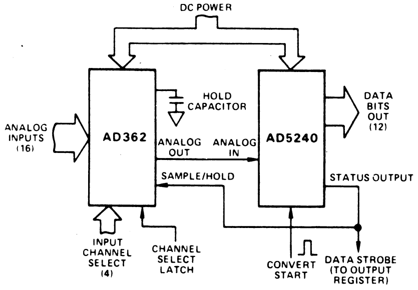


Figure 21. High Speed 12-Bit DAS

A fast (43.5kHz) 12-bit DAS can be configured using the AD362 and the AD5240. The AD362 contains two 8-channel multiplexers, a differential amplifier, a sample-and-hold with high-speed output amplifier, a channel address latch and control logic. The multiplexers may be connected to the differential amplifier in either an 8-channel differential or 16-channel single-ended configuration. A feature of the AD362 is an internal user-controllable analog switch that connects the multiplexers in either a single-ended or differential mode. This allows a single device to perform in either mode without hardwire programming and permits a mixture of single-ended and differential sources to be interfaced by dynamically switching the input mode control.

MICROPROCESSOR INTERFACING

The 5µs conversion time of the AD5240 suggests several differential methods of interface to microprocessors. In systems where the AD5240 is used for high sampling rates on a single signal which is to be digitally processed, CPU-controlled conversion may be inefficient due to the slow cycle times of most microprocessors. It is generally preferable to perform conversions independently, inserting the resultant digital data directly into memory. This can be done using direct memory access (DMA) which is totally transparent to the CPU. Interface to user-designed DMA hardware is facilitated by the guaranteed data validity on the falling edge of the EOC signal.

Clearly, 12 bits of data must be broken up for interface to an 8-bit wide data bus. There are two possible formats: right-justified and left-justified. In a right-justified system, the least significant 8 bits occupy one byte and the four MSBs reside in the low nybble of another byte. This format is useful when the data from the ADC is being treated as a binary number between 0 and 4095. The left-justified format supplies the eight most-significant bits in one byte and the 4LSB's in the high nybble of another byte. The data now represents the fractional binary number relating the analog signal to the full-scale voltage. An advantage to this organization is that the most-significant eight bits can be read by the processor as a coarse indication of the true signal value. The full 12-bit word can then be read only when all 12 bits are needed. This allows faster and more efficient control of a process.

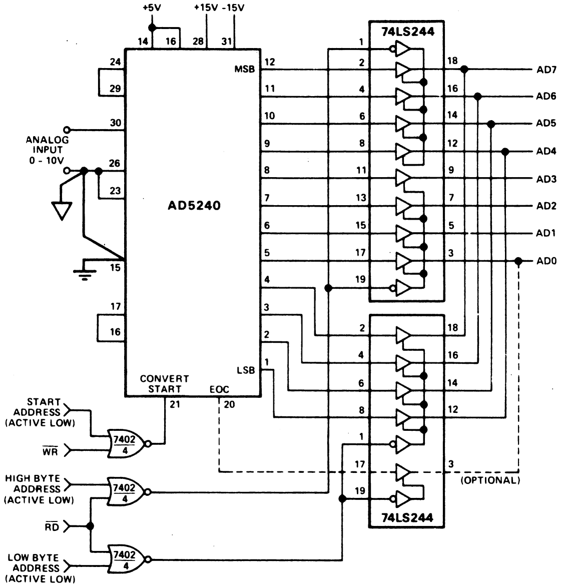


Figure 22. AD5240 Interface Connections

Figure 22 shows a typical connection to an 8085-type bus, using a left justified data format for unipolar inputs. Status polling is optional, and can be read simultaneously with the 4LSBs. If it is desired to right-justify the data, pins 1 through 12 of the AD5240 should be reversed, as well as the connections to the data bus and high and low byte address signals.

When dealing with bipolar inputs (±5V, ±10V ranges), using the MSB directly yields a complementary offset binary-coded output. If complementary two's complement coding is desired, it can be produced by substituting $\overline{\text{MSB}}$ (pin 13) for the MSB. This facilitates arithmetic operations which are subsequently performed on the ADC output data.

ANALOG DEVICES

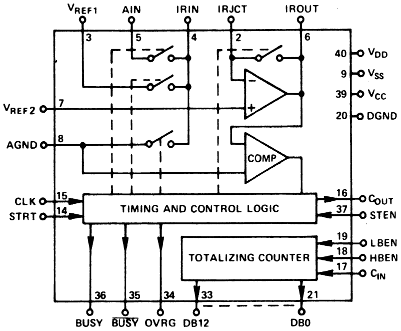
CMOS
13-Bit Monolithic A/D Converter

AD7550

FEATURES

Resolution: 13 Bits, 2's Complement
Relative Accuracy: ±1/2LSB
"Quad Slope" Precision
  Gain Drift: 1ppm/°C
  Offset Drift: 1ppm/°C
Microprocessor Compatible
Ratiometric
Overrange Flag
Very Low Power Dissipation
TTL/CMOS Compatible
CMOS Monolithic Construction

AD7550 FUNCTIONAL BLOCK DIAGRAM



40-PIN DIP

GENERAL DESCRIPTION

The AD7550 is a 13-bit (2's complement) monolithic CMOS analog-to-digital converter on a 118 x 125 mil die packaged in a 40-pin ceramic DIP. Outstanding accuracy and stability (1ppm/°C) is obtained due to its revolutionary integrating technique, called "Quad Slope" (Analog Devices patent No. 3872466). This conversion consists of four slopes of integration as opposed to the traditional dual slope and provides much higher precision.

The AD7550 parallel output data lines have three-state logic and are microprocessor compatible through the use of two enable lines which control the lower eight LSB's (low byte enable) and the five MSB's (high byte enable). An overrange flag is also available which together with the BUSY and $\overline{\text{BUSY}}$ flags can be interrogated through the STATUS ENABLE providing easy microprocessor interface.

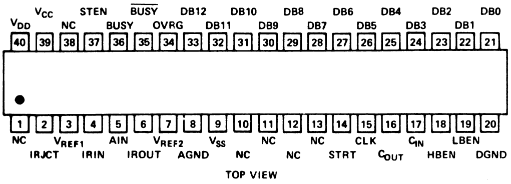
The AD7550 conversion time is about 40ms with a 1MHz clock. Clock can be externally controlled or internally generated by simply connecting a capacitor to the clock pin. A positive start pulse can be self-generated by having a capacitor on the start pin or can be externally applied.

For most applications, the AD7550 needs only three resistors, one capacitor, and a reference voltage since the integrating amplifier, comparator, switches and digital logic are all on the CMOS chip.

A wide range of power supply voltages (±5V to ±12V) with minuscule current requirements make the AD7550 ideal for low power and/or battery operated applications. Selection of the logic (V_{CC}) supply voltage (+5V to V_{DD}) provides direct TTL or CMOS interface on the digital input/output lines.

The AD7550 uses a high density CMOS process featuring double layer metal and silicon nitride passivation to ensure high reliability and long-term stability.

PIN CONFIGURATION



SPECIFICATIONS (V_{DD} = +12V, V_{SS} = -5V, V_{CC} = +5V, V_{REF1} = +4.25V unless otherwise noted)[1]

PARAMETER	TA = +25°C	OVER SPECIFIED TEMPERATURE RANGE	TEST CONDITIONS
ACCURACY			
Resolution		13 Bits 2's Comp min	
Relative Accuracy	±1LSB max	±1 LSB max	f_{CLK} = 500kHz, R_1 = 1MΩ, C_1 = 0.01µF, IRJCT Voltage Adjusted to $\frac{V_{REF1}}{2}$ ±0.6%
Gain Error	±1LSB max		
Gain Error Drift	1ppm/°C typ		
Offset Error	±0.5LSB max		
Offset Error Drift	1ppm/°C typ		
ANALOG INPUTS			
AIN Input Resistance[2]	R1MΩ min		
V_{REF1} Input Resistance[2]	R1MΩ min		
V_{REF2} Leakage Current	10pA typ		
DIGITAL INPUTS			
CIN, LBEN, HBEN, STEN			
V_{INL}	+0.8V max	+0.8V max	V_{CC} = +5V
V_{INH}	+2.4V min	+2.4V min	
V_{INL}	+1.2V max	+1.2V max	V_{CC} = +12V
V_{INH}	+10.8V min	+10.8V min	
I_{INL}, I_{INH}	5nA typ		
START			
V_{INL}	+0.8V max	+0.8V max	V_{CC} = +5V to V_{DD}
V_{INH}	+2.4V min	+2.4V min	
I_{INL}	-1µA typ		V_{CC} = +5V to V_{DD}, BUSY = Low
I_{INH}	+150µA typ		V_{CC} = +5V to V_{DD}, BUSY = High
CLOCK			
V_{INL}	+0.8V max	+0.8V max	V_{CC} = +5V
V_{INH}	+3V min	+3V min	
V_{INL}	+1.2V max	+1.2V max	V_{CC} = +12V
V_{INH}	+10.8V min	+10.8V min	
I_{INL}	-100µA typ		V_{IN} = V_{INL}; V_{CC} = +5V to +12V
I_{INH}	+100µA typ		V_{IN} = V_{INH}; V_{CC} = +5V to +12V
DIGITAL OUTPUTS			
V_{OUTL}	+0.5V max	+0.8V max	V_{CC} = +5V, I_{SINK} = 1.6mA
V_{OUTH}	+2.4V min	+2.4V min	V_{CC} = +5V, I_{SOURCE} = 40µA
V_{OUTL}	+1.2V max	+1.2V max	V_{CC} = +12V, I_{SINK} = 1.6mA
V_{OUTH}	+10.8V min	+10.8V min	V_{CC} = +12V, I_{SOURCE} = 0.6mA
Capacitance (Floating State) (OVRG, BUSY, $\overline{BUSY}$, and DB0–DB12	5pF typ		
I_{LKG} (Floating State) (OVRG, $\overline{BUSY}$, BUSY, and DB0–DB12)	±5nA typ		V_{CC} = +5V to +12V V_{OUT} = 0V and V_{CC}
DYNAMIC PERFORMANCE			
Conversion Time	90ms typ		$V_{IN(CLK)}$ = 0 to +3V, f_{CLK} = 500kHz
	40ms typ		$V_{IN(CLK)}$ = 0 to +3V, f_{CLK} = 1MHz
STEN, HBEN, LBEN Propagation Delay t_{ON}, t_{OFF}	250ns typ, 500ns max		V_{IN}(STEN, HBEN, LBEN) 0 to +3V
External STRT Pulse Duration	800ns min		$V_{IN(STRT)}$ = 0 to +3V
POWER SUPPLIES			
V_{DD} Range	+10V min, +12V max		
V_{SS} Range	-5V min, -12V max		
V_{CC} Range	+5V min, V_{DD} max		
I_{DD}	0.6mA typ, 2mA max		
I_{SS}	0.3mA typ, 2mA max		f_{CLK} = 1MHz
I_{CC}	0.06mA typ, 2mA max		

---

[1] **Full Scale Voltage = ±V_{REF1} ÷ 2.125. For V_{REF1} = +4.25V, FS voltage is ±2.000V.**

[2] **The equivalent input circuit is the integrator resistor R_1 (1MΩ min, 10MΩ max) in series with a voltage source $\frac{V_{REF1}}{2}$, (see Figure 1).**

Specifications subject to change without notice.

ORDERING INFORMATION

Model	Temperature Range	Package
AD7550BD	−25°C to +85°C	Ceramic – (D40A)

See Section 20 for package outline information.

CAUTION:

1. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times. Prior to pulling the devices from the conductive foam, ground the foam to deplete any accumulated charge.
2. V_{CC} should never exceed V_{DD} by more than 0.4V, especially during power ON or OFF sequencing.

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND	0V, +14V
V_{DD} to DGND	0V, +14V
V_{SS} to AGND	0V, −14V
V_{SS} to DGND	0V, −14V
AGND to DGND	0V, +14V
V_{CC} to DGND	0V, V_{DD}
V_{REF1}	V_{SS}, V_{DD}
V_{REF2}	AGND, V_{DD}
AIN	V_{SS}, V_{DD}
IRIN	V_{SS}, V_{DD}
IRJCT	AGND, V_{DD}
IROUT	V_{SS}, V_{DD}
Digital Input Voltage	
HBEN, LBEN, STEN, C_{IN}	DGND, (DGND +27V)
CLK, START	DGND, V_{DD}
Digital Output Voltage	
DB0–DB12, OVRG, BUSY, $\overline{\text{BUSY}}$, C_{OUT}	DGND, V_{CC}
Power Dissipation (Package)	
Up to +50°C	1000mW
Derates above +50°C by	10mW/°C
Storage Temperature	−65°C to +150°C
Operating Temperature	−25°C to +85°C

PIN FUNCTION DESCRIPTION

PIN	MNEMONIC	DESCRIPTION
1	NC	No Connection
2	IRJCT	IntegratoR JunCTion. Summing junction (negative input) of integrating amplifier.
3	V_{REF1}	Voltage REFerence Input
4	IRIN	IntegratoR INput. External integrator input R is connected between IRJCT and IRIN.
5	AIN	Analog INput. Unknown analog input voltage to be measured. Fullscale AIN equals $V_{REF}/2.125$.
6	IROUT	IntegratoR OUTput. External integrating capacitor C_1 is connected between IROUT and IRJCT.
7	V_{REF2}	Voltage REFerence ÷ 2 Input
8	AGND	Analog GrouND
9	V_{SS}	Negative Supply (-5V to -12V)
10	NC	No Connection
11	NC	No Connection
12	NC	No Connection
13	NC	No Connection
14	STRT	STaRT Conversion. When STRT goes to a Logic "1," the AD7550's digital logic is set up and BUSY is latched "high." When STRT returns "low," conversion begins in synchronization with CLK. Reinitiating STRT during conversion causes a conversion restart. STRT can be driven from an external logic source or can be programmed for continuous conversion by connecting an external capacitor between STRT and DGND. An externally applied STRT command must be a positive pulse of at least 800 nanoseconds to ensure proper set-up of the AD7550 logic.
15	CLK	CLocK Input. The CLK can be driven from external logic, or can be programmed for internal oscillation by connecting an external capacitor between CLK and DGND.
16	C_{OUT}	Count OUT provides a number (N) of gated clock pulses given by: $N = \left[\frac{AIN}{V_{REF1}}\ 2.125 + 1\right]\ 4096$
17	C_{IN}	Count IN is the input to the output counter. 2's complement binary data appears on the DB0 through DB12 output lines (if the HBEN and LBEN enable lines are "high") if C_{OUT} is connected to C_{IN}.
18	HBEN	High Byte ENable is the three-state logic enable input for the DB8-DB12 data outputs. When HBEN is low, the DB8—DB12 outputs are floating. When HBEN is "high," digital data appears on the data lines.
19	LBEN	Low Byte ENable is the three-state logic enable for DB0—DB7. When LBEN is "low," DB0—DB7 are floating. When "high," digital data appears on the data lines.
20	DGND	Digital GrouND is the ground return for all digital logic and the comparator.
21	DB0	Data Bit 0 (least significant bit)
22	DB1	↑
23	DB2	
24	DB3	
25	DB4	
26	DB5	
27	DB6	CODE: 2's Complement
28	DB7	
29	DB8	
30	DB9	
31	DB10	
32	DB11	↓
33	DB12	Data Bit 12 (most significant bit)
34	OVRG	OVerRange indicates a Logic "1" if AIN exceeds plus or minus full scale by at least 1/2 LSB. OVRG is a three-state output and floats until STEN is addressed with a Logic "1".
35	$\overline{BUSY}$	Not BUSY. $\overline{BUSY}$ indicates whether conversion is complete or in progress. $\overline{BUSY}$ is a three-state output which floats until STEN is addressed with a Logic "1." When addressed, $\overline{BUSY}$ will indicate either a "1" (conversion complete) or a "0" (conversion in progress).
36	BUSY	BUSY indicates conversion status. BUSY is a three-state output which floats until STEN is addressed with a Logic "1." When addressed, BUSY indicates a "0" (conversion complete) or a "1" (conversion in progress).
37	STEN	STatus ENable is the three-state control input for BUSY, $\overline{BUSY}$, and OVRG.
38	NC	No Connection
39	V_{CC}	Logic Supply. Digital inputs and outputs are TTL compatible if V_{CC} = +5V, CMOS compatible for V_{CC} = +10V to V_{DD}.
40	V_{DD}	Positive Supply +10V to +12V.

PRINCIPLES OF OPERATION

BASIC OPERATION

The essence of the quad slope technique is best explained through Figures 1 and 2.

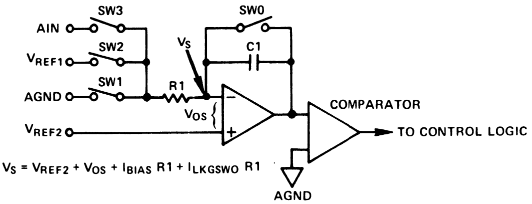


Figure 1. Quad Slope Integrator Circuit

The inputs AGND (analog ground), V_{REF1} and AIN (analog input) are applied in sequence to an integrator (Figure 1), creating four slopes (phases 1 through 4, Figure 2) at the integrator output. Voltage V_S is ideally equal to $\frac{V_{REF1}}{2}$, but if not, will create an error count "n" that will be minimized by the "quad-slope" conversion process. V_{REF1} and V_{REF2} must be positive voltages.

The equivalent integrator input voltages and their integration times are shown in Table 1.

TABLE 1
INTEGRATOR EQUIVALENT INPUT VOLTAGES AND INTEGRATION TIMES

Phase	Input Voltage	Integration Time
1	AGND$-V_S$	$t_1 = K_1t$
2	$V_{REF1}-V_S$	$t_2 = (K_1 + n)t$
3	AIN$-V_S$	$t_3 = (2K_1 - n)t$
4	$V_{REF1}-V_S$	$t_4 = (K_3 - 2K_1 + n - 2N)t$

NOTE: **Ideally $V_S = V_{REF2} = 1/2\ V_{REF1}$**

where:

t = The CLK period
n = System error count
K_1 = A fixed count equal to 4352 counts
K_2 = A fixed count equal to 17408 counts ($K_2 = 4K_1$)
K_3 = A fixed count equal to 25600 counts
N = Digital output count corresponding to the analog input voltage, AIN

PHASE 0

After the start pulse is applied, switch SW2 is closed (all other switches open) and the integrator output is ramped to comparator zero crossing. Phase 0 can be considered the reset phase of the converter, and always has a duration $t_0 = R_1C_1$ (integrator time constant). Upon zero crossing, counters K_1 and K_2 are started, switch SW2 is opened and SW1 is closed.

PHASE 1

Phase 1 integrates (AGND $-$ V_S) for a fixed period of time (by counter K_1) equal to $t_1 = K_1t$. At the end of phase 1, switch SW1 is opened and SW2 is closed.

PHASE 2

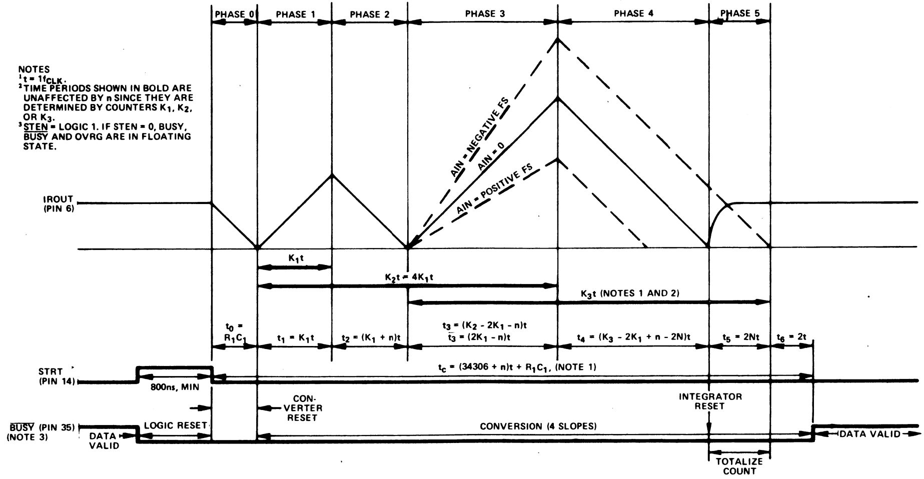
The integrator input is switched to ($V_{REF1} - V_S$) and the output ramps down until zero crossing is achieved. The integration time $t_2 = (K_1 + n)t$ includes the error count "n" due to offsets, etc. At the end of phase 2, switch SW2 is opened, SW3 is closed, and a third counter (K_3) is started.

PHASE 3

Phase 3 integrates the analog input (AIN $-$ V_S) until counter K_2 counts $4K_1t$. At this time SW3 is opened and SW2 is closed again.

PHASE 4

Phase 4 integrates ($V_{REF1} - V_S$) and the comparator output ramps down until zero crossing once again is achieved. Since the comparator always approaches zero crossing from the same slope, propagation delay is constant and hysteresis effect is eliminated.



NOTES
[1] $t = 1f_{CLK}$.
[2] TIME PERIODS SHOWN IN BOLD ARE UNAFFECTED BY n SINCE THEY ARE DETERMINED BY COUNTERS K_1, K_2, OR K_3.
[3] $\overline{STEN}$ = LOGIC 1. IF STEN = 0, BUSY, $\overline{BUSY}$ AND OVRG ARE IN FLOATING STATE.

Figure 2. Quad Slope Timing Diagram

The time t_5 between the phase 4 zero crossing and the termination of counter K_3 is considered equal to 2N counts. N, the number of counts at the C_{OUT} terminal, is obtained by a divide-by-two counter stage. This reduces "jitter" effect. Barring third (and higher) order effects, it can be proven that:

$$N = \underbrace{\left(\frac{AIN}{V_{REF1}} - 1\right) \cdot 2K_1 + \frac{K_3}{2}}_{\text{ideal transfer function}} + \underbrace{\left(\frac{AIN}{V_{REF1}} - 1\right) \cdot \left[\frac{AGND}{V_{REF1}}(1 + 2\alpha) - \alpha^2\right] \cdot 2K_1}_{\text{error term}} \qquad \text{(EQN 1)}$$

where:

$$\alpha = \frac{2V_S - V_{REF1}}{V_{REF1}}$$

The ideal case assumes:

$AGND = 0V$

$V_S = \frac{V_{REF1}}{2}$, therefore $\alpha = 0$

Then (EQN 1) simplifies to:

$$\boxed{N = \frac{AIN}{V_{REF1}} \cdot 8704 + 4096} \qquad \text{(EQN 2)}$$

or

$$\boxed{N = \frac{AIN}{V_{FS}} \cdot 4096 + 4096} \qquad \text{(EQN 3)}$$

where:

$$V_{FS} = \text{full scale input voltage} = \frac{V_{REF1}}{2.125}$$

The parallel output (DB0–DB12) of the AD7550 represents the number N in binary 2's complement coding when the C_{OUT} pin is connected to the C_{IN} pin (see Table II).

TABLE II
OUTPUT CODING (Bipolar 2's Complement)

Analog Input (Note 1)	N (Note 2)	Parallel Digital Output (Note 3)		
		OVRG	DB12	DB0
+Overrange	–	1	0	1 1 1 1 1 1 1 1 1 1 1 1
$+V_{FS}$ $(1-2^{-12})$	8191	0	0	1 1 1 1 1 1 1 1 1 1 1 1
$+V_{FS}$ (2^{-12})	4097	0	0	0 0 0 0 0 0 0 0 0 0 0 1
0	4096	0	0	0 0 0 0 0 0 0 0 0 0 0 0
$-V_{FS}$ (2^{-12})	4095	0	1	1 1 1 1 1 1 1 1 1 1 1 1
$-V_{FS}$	0	0	1	0 0 0 0 0 0 0 0 0 0 0 0
–Overrange	–	1	1	0 0 0 0 0 0 0 0 0 0 0 0

Notes

1 $V_{FS} = \frac{V_{REF1}}{2.125}$

2 N = number of counts at C_{OUT} pin

3 C_{OUT} strapped to C_{IN}; LBEN, HBEN and STEN = Logic 1

ERROR ANALYSIS

Equation 1 shows that only α and AGND generate error terms. Their impact can be analyzed as follows:

Case 1: $AGND = 0, \alpha \neq 0$

Error sources such as capacitor-leakage (I_L) and op amp offset (e) cause α to be different from zero. Under this condition,

$$\alpha = \frac{2(e + I_L R_1)}{V_{REF1}}$$

where $I_L R_1$ is the equivalent error voltage generated by leakage I_L.

The evaluation of this error term is best demonstrated through the following example:

Assume:

$e = 5mV$, $I_L = 5nA$, $R_1 = 1M\Omega$ and $V_{REF1} = 4.25V$.

Then:

$\alpha = 4.7 \times 10^{-3}$

and:

$$N = \left[\frac{AIN}{V_{REF1}} - 1\right] \times 8704 + 12800 - \underbrace{\left[\frac{AIN}{V_{REF1}} - 1\right] \times 22.1 \times 10^{-6} \times 8704}_{\text{error term } N_\epsilon}$$

Therefore, the error count N_ϵ is as follows:

For $AIN = -V_{FS}$: $N_\epsilon = 0.28$ counts = 0.28LSB
$AIN = 0$: $N_\epsilon = 0.19$ counts = 0.19LSB
$AIN = +V_{FS}$: $N_\epsilon = 0.09$ counts = 0.09LSB

The above example shows the strong reduction of the circuit errors because of the α^2 term in (EQN 1). Another consequence of this effect is that N_ϵ is always positive, regardless of the polarity of the circuit errors.

Case 2: $AGND \neq 0, \alpha = 0$

When AGND is different from the signal ground, then this error will come through on a first-order basis. Indeed:

$$N = \left[\frac{AIN}{V_{REF1}} - 1\right] \cdot 8704 + 12800 + \underbrace{\left[\frac{AIN}{V_{REF1}} - 1\right] \cdot \frac{AGND}{V_{REF1}}}_{\text{error term } N_\epsilon}$$

The following example demonstrates the impact of AGND.

Let $AGND = 1mV$ and $V_{REF1} = 4.25V$.

For $AIN = -V_{FS}$, then $N_\epsilon = 3.01$ counts
$AIN = 0$, then $N_\epsilon = 2.05$ counts
$AIN = +V_{FS}$, then $N_\epsilon = 1.08$ counts

Therefore, ground loops should be minimized because a 330μV difference between AGND and signal ground will cause 1 count (1 LSB) of error when the analog input is at minus full scale. An optimized ground system is shown in Figure 7.

OPERATING GUIDELINES

The following steps, in conjunction with Figure 3, explain the calculations of the component values required for proper operation.

1. DETERMINATION OF V_{REF1}

When the full scale voltage requirement (VFS) has been ascertained, the reference voltage can be calculated by:

$V_{REF1} = 2.125\ (V_{FS})$

V_{REF1} must be positive for proper operation.

2. SELECTION OF C_3 (INTERNAL CLOCK OPERATION)

For internal clock operation, connect capacitor C_3 to the clock pin as shown in Figure 3. The clock frequency versus capacitor C_3 is shown in Figure 4.

The clock frequency must be limited to 1.3MHz for proper operation.

3. SELECTION OF INTEGRATOR COMPONENTS (R_1 AND C_1)

To ensure that the integrator's output doesn't saturate to its bound (V_{DD}) during the phase (3) integration cycle, the integrator time constant (R_1C_1) should be approximately equal to:

$$\pi = R_1C_1 = \frac{V_{REF1}\ (9 \times 10^3)}{f_{CLK}\ (V_{DD} - 4V}$$

The integrator components R_1 and C_1 can be selected by referring to Figure 5 and/or Figure 6. Figure 5 plots the time constant (R_1C_1) versus clock frequency for different reference voltages. Figure 6 is a direct plot of the required C_1 versus f_{CLK} for R_1 values of 1MΩ and 10MΩ.

R_1 can be a standard 10% resistor, but must be selected between 1MΩ to 10MΩ.

The integrating capacitor "C_1" must be a low leakage, low dielectric absorption type such as teflon, polystyrene or polypropylene. To minimize noise, the outside foil of C_1 must be connected to IR_{OUT}.

4. CONVERSION TIME

As shown in Figure 2, the conversion time is independent of the analog input voltage AIN, and is given by:

$$t_{convert} = t_{STRT} + \frac{34306}{f_{CLK}} + R_1C_1$$

where:

t_{STRT} = STRT pulse duration
R_1C_1 = Integrator Time Constant
f_{CLK} = CLK Frequency

For example, if $V_{EEF1} = 4.25V$, $R_1 = 1M\Omega$, $C_1 = 4{,}000pF$ and CLK = 1MHz, the conversion time (not including t_{STRT}, which is normally only microseconds in duration) is approximately 40 milliseconds.

5. EXTERNAL OR AUTO STRT OPERATION

The STRT pin can be driven externally, or with the addition of C_2, made to self-start.

The size of C_2 determines the length of time from end of conversion until a new conversion is initiated. This is the "data valid" time and is given by:

$t_{DAV} \approx (1.7 \times 10^6\Omega)\ C_2 + 20\mu s$

When first applying power to the AD7550, a 0V to V_{DD} positive pulse (power up restart) is required at the STRT terminal to initiate auto STRT operation.

6. INITIAL CALIBRATION

Trim R_4 (Figure 3) so that pin 2 (IRJCT) equals 1/2 V_{REF1} ±0.6%. When measuring the voltage on IRJCT, apply a Logic "1" to the STRT terminal.

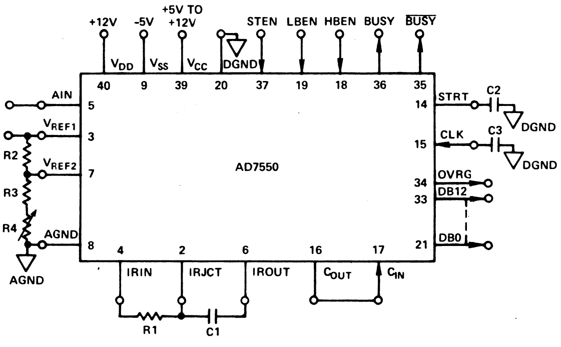


Figure 3. Operation Diagram

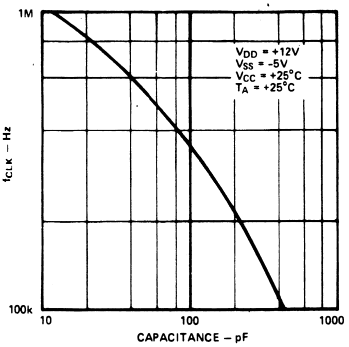


Figure 4. f_{CLK} vs. C_3

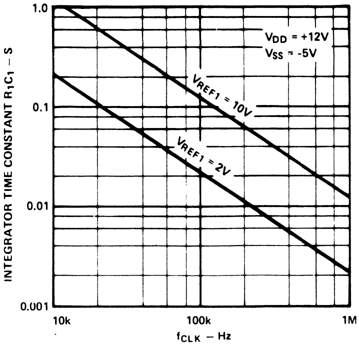


Figure 5. Integrator Time Constant (R_1C_1) vs. f_{CLK} for Different Reference Voltages

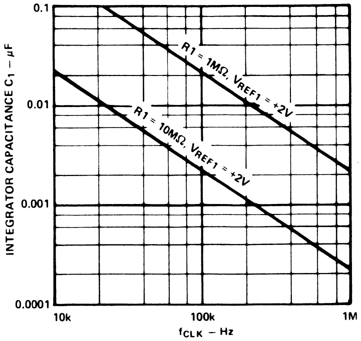


Figure 6. Integrator Capacitance (C_1) vs. f_{CLK} for Different Integrator Resistances (R_1)

APPLICATION HINTS

When operating at f_{CLK} greater than 500kHz, the following steps are recommended to minimize errors due to noise coupling (see Figure 7).

1. Decouple AIN (pin 5), V_{REF1} (pin 3) and V_{REF2} (pin 7) through 0.01µF to signal ground.
2. Signal ground must be located as close to pin 8 (AGND) as possible.
3. Keep the lead lengths of R_1 and C_1 toward pin 2 (IRJCT) as short as possible. In addition, both components should lie over the analog ground plane. If C_1 has an outside foil, connect it to pin 6 (IROUT), not pin 2.
4. Hold the data bit enables (HBEN, LBEN) in the 0 state during conversion. This is easily accomplished by tying STEN to the 1 state and driving HBEN and LBEN with BUSY. This prevents the DB0 through DB12 outputs from coupling noise into the integrator during the phase 1–4 active integration periods.

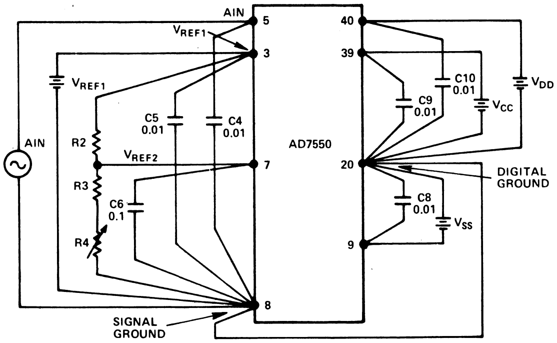


Figure 7. Ground System

ANALOG DEVICES

CMOS 12-Bit Plus Sign Monolithic A/D Converter

AD7552

FEATURES

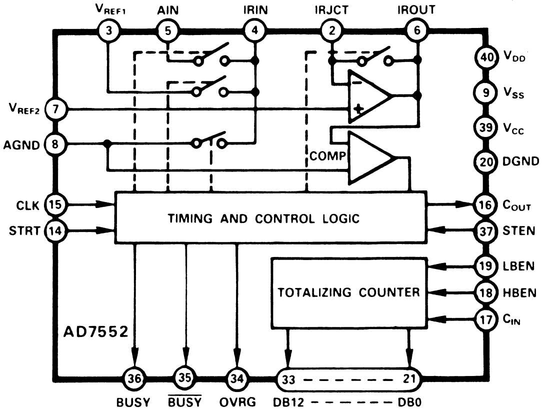
12-Bit Binary with Polarity and Overrange
Accuracy ±1LSB
Microprocessor Compatible
Ratiometric Operation
Low Power Dissipation
Low Cost

GENERAL DESCRIPTION

The AD7552 is a 12-bit plus sign and overrange monolithic CMOS analog to digital converter. The "Quad Slope" conversion algorithm (Analog Devices patent No. 3872466) converts any offset voltages due to the integrator, comparator etc. to a digital number and subsequently reduces the total system drift error to a second order effect.

The AD7552 parallel output data lines have three-state logic and are microprocessor compatible. Separate enable lines control the lower eight LSBs (low byte enable) and the five MSBs (high byte enable). An overrange flag is also available which together with the BUSY and $\overline{\text{BUSY}}$ flags can be interrogated through the STATUS ENABLE providing easy microprocessor interface.

AD7552 FUNCTIONAL BLOCK DIAGRAM



PRODUCT HIGHLIGHTS

1. The output data (12-bits plus sign) may be directly accessed under control of two byte enable signals for a simple parallel bus interface. The overrange and converter busy signals are accessed by a status enable signal.
2. The AD7552 conversion time is approximately 160ms with a 250kHz clock.
3. Serial count out available for isolated A/D conversion via opto-isolators.
4. A conversion start can be controlled by an externally applied signal or, with the addition of a capacitor, the converter can be made to self start.
5. For most applications, the AD7552 needs only three resistors, one capacitor, and a reference voltage since the integrating amplifier, comparator, switches and digital logic are all on the CMOS chip.

SPECIFICATIONS (V_{DD} = +12V, V_{CC} = +5V, V_{SS} = −5V, V_{REF1} = +4.25V unless otherwise noted)[1]

Parameter	T_A = +25°C	T_A = 0 to +70°C	Units	Conditions/Comments
ACCURACY				
Resolution	12-bits plus sign	12-bits plus sign		±4096 counts, binary 2's complement coding
Accuracy of Reading (Including Noise)	±1	±1	Counts max	f_{CLK} = 250kHz, R1 = 1.8MΩ. C1 = 0.01μF 95% of conversions meet this specification
Noise (Flicker)	±1	±1	Counts max	From nominal reading, not exceeded 95% of time
	±2	±2	Counts max	From nominal reading, not exceeded 99% of time
ANALOG INPUTS				
AIN (pin 5) Input Resistance[2]	R1	R1	MΩ min	R1 is the external integrating resistor
V_{REF1} (pin 3) Input Resistance[2]	R1	R1	MΩmin	connected between IROUT AND IRJCT
V_{REF2} (pin 7) Leakage Current	1	10	nA typ	
DIGITAL INPUTS				
CIN (pin 17), HBEN (pin 18), LBEN (pin 19), STEN (pin 37)				
V_{IL}	+0.8	+0.8	V max	V_{CC} = +5V
V_{IH}	+2.4	+2.4	V min	
V_{IL}	+1.2	+1.2	V max	V_{CC} = +12V (V_{IL} = 10% of V_{CC})
V_{IH}	+10.8	+10.8	V min	(V_{IH} = 90% of V_{CC})
I_{IL}, I_{IH}	1	1	μA max	V_{CC} = +5V to +12V
START (pin 14)				
V_{IL}	+0.8	+0.8	V max	V_{CC} = +5V to V_{DD}
V_{IH}	+3.0	+3.0	V min	
I_{IL}	−5/−50	−5/−50	μA typ/max	V_{CC} = +5V to V_{DD}, BUSY (pin 36) = V_{OL}
I_{IH}	+0.5/+2.0	+0.5/+2.0	mA typ/max	V_{CC} = +5V to V_{DD}, BUSY (pin 36) = V_{OH}
CLOCK (pin 15)				
V_{IL}	+0.8	+0.8	V max	V_{CC} = +5V
V_{IH}	+3.0	+3.0	V min	
V_{IL}	+1.2	+1.2	V max	V_{CC} = +12V (V_{IL} = 10% of V_{CC})
V_{IH}	+10.8	+10.8	V min	(V_{IH} = 90% of V_{CC})
I_{IL}	−0.1/−1.0	−0.1/−1.0	mA typ/max	V_{IN} = V_{IL}; V_{CC} = +5V to +12V
I_{IH}	+0.1/+1.0	+0.1/+1.0	mA typ/max	V_{IN} = V_{IH}; V_{CC} = +5V to +12V
DIGITAL OUTPUTS				
C_{OUT} (pin 16), OVRG (pin 34) $\overline{\text{BUSY}}$ (pin 35), BUSY (pin 36) and DB0–DB12 (pins 21–33)				
V_{OL}	+0.8	+0.8	V max	V_{CC} = +5V, I_{SINK} = 1.6mA
V_{OH}	+4.0	+4.0	V min	V_{CC} = +5V, I_{SOURCE} = 40μA
V_{OL}	+1.2	+1.2	V max	V_{CC} = +12V, I_{SINK} = 1.6mA
V_{OH}	+10.8	+10.8	V min	V_{CC} = +12V, I_{SOURCE} = 0.6mA
Capacitance per Pin[3]	5	5	pF typ	Outputs in high impedance state
Leakage per Pin	1	1	μA max	Outputs in high impedance state
DYNAMIC PERFORMANCE				
Conversion Time	160	160	ms typ	R1 = 1.8MΩ, C1 = 0.01μF, f_{CLK} = 250kHz
Propagation Delays[3]				
STEN to BUSY, $\overline{\text{BUSY}}$, or OVRG	400	700	ns max	Typically 250ns at +25°C (see next page) STEN going HIGH (+3V) or LOW (0V)
LBEN to DB0–DB7	300	500	ns max	Typically 160ns at +25°C (see next page) LBEN going HIGH (+3V) or LOW (0V)
HBEN to DB8–DB12	300	500	ns max	Typically 160ns at +25°C (see next page) LBEN going HIGH (+3V) or LOW (0V)
STRT Pulse Width	300	500	ns min	Typically 220ns at +25°C V_{IN} (STRT) = 0 to +3V
POWER SUPPLIES				
V_{DD}	+10/+12	+10/+12	V min/max	
V_{SS}	−5/−12	−5/−12	V min/max	
V_{CC}	+5/V_{DD}	+5/V_{DD}	V min/max	
I_{DD}	0.8/2	0.8/2	mA typ/max	STRT (pin 14) held HIGH,
I_{SS}	0.3/2	0.3/2	mA typ/max	digital outputs floating.
I_{CC}	0.1/1	0.1/1	mA typ/max	V_{CC} = +5V
	0.5/2	0.5/2	mA typ/max	V_{CC} = +12V

NOTES

[1] Full scale voltage = ±V_{REF1} ÷ 2.125. For V_{REF1} = +4.25V FS voltage is ±2.00V.

[2] The equivalent input circuit is the integrator resistor R1 in series with a voltage source V_{REF2} (= V_{REF}/1 ÷ 2, see Figure 1).

[3] Guaranteed but not tested.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND	0V, +14V
V_{DD} to DGND	0V, +14V
V_{SS} to AGND	0V, −14V
V_{SS} to DGND	0V, −14V
AGND to DGND	0V, +14V
V_{CC} to DGND	0V, V_{DD}
V_{REF1}	V_{SS}, V_{DD}
V_{REF2}	AGND, V_{DD}
AIN	V_{SS}, V_{DD}
IRIN	V_{SS}, V_{DD}
IRJCT	AGND, V_{DD}
IROUT	V_{SS}, V_{DD}
Digital Input Voltage	
HBEN, LBEN, STEN, C_{IN}	DGND, (DGND +27V)
CLK, START	DGND, V_{DD}
Digital Output Voltage	
DB0–DB12, OVRG, BUSY, $\overline{BUSY}$, C_{OUT}	DGND, V_{CC}
Operating Temperature Range	0 to +70°C
Storage Temperature	+65°C to +150°C
Power Dissipation (Package)	
Up to +50°C	1000mW
Derates above +50°C by	10mW/°C
Lead Temperature (Soldering, 10secs)	+300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION:

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The foam should be discharged to the destination socket before devices are removed.

WARNING!

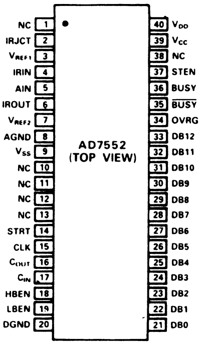
ESD SENSITIVE DEVICE

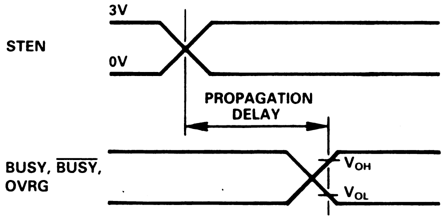
ORDERING INFORMATION

Model	Temperature Range	Package[1]
AD7552KN	0 to +70°C	Plastic DIP (N40A)

[1] See Section 20 for package outline information.

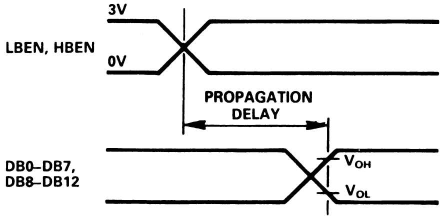
PIN CONFIGURATION





TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$

STEN to BUSY, $\overline{BUSY}$, or OVRG Propagation Delays



LBEN to DB0–DB7, HBEN to DB8–DB12 Propagation Delays

PIN FUNCTION DESCRIPTION

PIN	MNEMONIC	DESCRIPTION
1	NC	No Connection
2	IRJCT	IntegratoR JunCTion. Summing junction (negative input) of integrating amplifier.
3	V_{REF1}	Voltage REFerence Input (normally +4.25 volts).
4	IRIN	IntegratoR INput. External integrating resistor R1 is connected between IRJCT and IRIN.
5	AIN	Analog INput. Unknown analog input voltage to be measured. Full scale AIN equals $V_{REF}/2.125$.
6	IROUT	IntegratoR OUTput. External integrating capacitor C1 is connected between IROUT and IRJCT.
7	V_{REF2}	Voltage REFerence ÷ 2 Input. V_{REF2} is normally obtained by a potential divider circuit as shown in Figure 3.
8	AGND	Analog GrouND
9	V_{SS}	Negative Supply (−5V to −12V)
10	NC	No Connection
11	NC	No Connection
12	NC	No Connection
13	NC	No Connection
14	STRT	STaRT Conversion. When STRT goes to a Logic "1", the AD7552's digital logic is set up and BUSY is latched "high". When STRT returns "low", conversion begins in synchronization with CLK. Reinitiating STRT during conversion causes a conversion restart. STRT can be driven from an external logic source or can be programmed for continuous conversion by connecting an external capacitor between STRT and DGND. An externally applied STRT command must be a positive pulse of at least 300 nanoseconds to ensure proper set-up of the AD7552 internal logic.
15	CLK	CLocK Input. The CLK can be driven from external logic, or can be programmed for internal oscillation by connecting an external capacitor between CLK and DGND.
16	C_{OUT}	Count OUT provides a number (N) of gated clock pulses given by: $$N = \left[\frac{AIN}{V_{REF1}} 2.125 + 1\right] 4096$$
17	C_{IN}	Count IN is the input to the output counter. 2's complement binary data appears on the DB0 through DB12 output lines (if the HBEN and LBEN enable lines are "high") if C_{OUT} is connected to C_{IN}.
18	HBEN	High Byte ENable is the three-state logic enable input for the DB8–DB12 data outputs. When HBEN is "low", the DB8–DB12 outputs are floating. When HBEN is "high," digital data appears on the data lines.
19	LBEN	Low Byte ENable is the three-state logic enable for DB0–DB7. When LBEN is "low," DB0–DB7 are floating. When "high," digital data appears on the data lines.
20	DGND	Digital GrouND is the ground return for all digital logic and the comparator.
21	DB0	Data Bit 0 (least significant bit)
22	DB1	↑
23	DB2	
24	DB3	
25	DB4	
26	DB5	
27	DB6	CODE: 2's Complement
28	DB7	
29	DB8	
30	DB9	
31	DB10	
32	DB11	↓
33	DB12	Data Bit 12 (most significant bit)
34	OVRG	OVerRanGe indicates a Logic "1" if AIN exceeds plus or minus full scale by at least 1/2LSB. OVRG is a three-state output and floats until STEN is addressed with a Logic "1".
35	$\overline{\text{BUSY}}$	Not BUSY. $\overline{\text{BUSY}}$ indicates whether conversion is complete or in progress. $\overline{\text{BUSY}}$ is a three-state output which floats until STEN is addressed with a Logic "1." When addressed, $\overline{\text{BUSY}}$ will indicate either a "1" (conversion complete) or a "0" (conversion in progress).
36	BUSY	BUSY indicates conversion status. BUSY is three-state output which floats until STEN is addressed with a Logic "1." When addressed, BUSY indicates a "0" (conversion complete) or a "1" (conversion in progress).
37	STEN	STatus ENable is the three-state control input for BUSY, $\overline{\text{BUSY}}$, and OVRG. When STEN is "high", the three outputs are enabled.
38	NC	No Connection
39	V_{CC}	Logic Supply. Digital inputs and outputs are TTL compatible if $V_{CC} = +5V$, CMOS compatible for $V_{CC} = +10V$ to V_{DD}.
40	V_{DD}	Positive Supply +10V to +12V.

Quad Slope Theory of Operation

Component limitations such as switch leakage, as well as operational amplifier offset voltage and bias current (and the temperature dependency of these errors), are major obstacles when designing high resolution integrating A/D converters. The AD7552 utilizes a patented *quad slope* conversion technique (Analog Devices Patent No. 3872466) to reduce the effects of such errors to second order effects.

Figure 1 shows a simplified quad slope integrator circuit. The various inputs AGND (Analog Ground), V_{REF1}, and AIN (Analog Input) are applied in sequence to the integrator via switches 1-3 (see Table 1), creating four slopes at the integrator output (phase 1-4 of Figure 2). If the equivalent summing junction voltage V_S is precisely $0.5V_{REF1}$, the phase 1 and phase 2 integration times are equal, indicating there are no input errors. If $V_S \neq 0.5V_{REF1}$ (due to amplifier offset voltage, bias current, etc.), an error count "n" is obtained. The analog input integration cycle (phase 3) is subsequently lengthened or shortened by "n" counts, depending on whether the error was positive or negative.

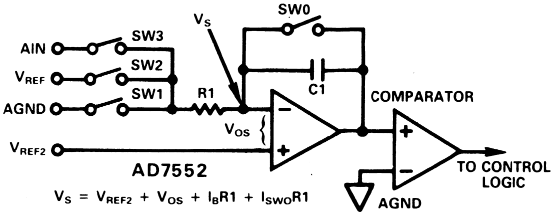


Figure 1. Simplified Quad Slope Integrator Circuit

Phase	Input Voltage	Integration Time
1	AGND–V_S	$t_1 = K_1t$
2	V_{REF1}–V_S	$t_2 = (K_1 + n)t$
3	AIN–V_S	$t_3 = (2K_1 - n)t$
4	V_{REF1}–V_S	$t_4 = (K_3 - 2K_1 + n - 2N)t$

Table 1. Integrator Equivalent Input Voltages and Integration Times

where:

t = The CLK period
n = System error count
K_1 = A fixed count equal to 4352 counts
K_2 = A fixed count equal to 17408 counts ($K_2 = 4K_1$)
K_3 = A fixed count equal to 25600 counts
N = Digital output count corresponding to the analog input voltage, AIN

The time t_5 between the phase 4 zero crossing and the termination of counter K_3 is considered equal to 2N counts. N, the number of counts at the C_{OUT} terminal, is obtained by a divide-by-two counter stage. This reduces "jitter" effect. Barring third (and higher) order effects, it can be proven that:

$$\underbrace{N = \left(\frac{AIN}{V_{REF1}} - 1\right)\cdot 2K_1 + \frac{K_3}{2}}_{\text{ideal term}} + \underbrace{\left(\frac{AIN}{V_{REF1}} - 1\right)\cdot\left[\frac{AGND}{V_{REF1}}(1 + 2\alpha) - \alpha^2\right]\cdot 2K_1}_{\text{error term}} \qquad \text{(EQN 1)}$$

where:

AGND = Voltage at AD7552 pin 8 (AGND) measured with respect to V_{REF1} and AIN signal common ground. (Ideally, AGND = 0V)

α is an error term equal to $\dfrac{2V_S - V_{REF1}}{V_{REF1}}$

Ideally α = when $V_S = 0.5V_{REF1}$.

NOTE:
$V_S = V_{REF2} + V_{OS} + I_B R_1 + I_{SWO} R_1$

WHERE:
$V_{REF2} = 0.5V_{REF1}$ if no error is present
V_{OS} = Offset voltage of integrator amplifier
$I_B R1$ = Equivalent integrator amplifier offset voltage due to bias current of integrator amplifier
$I_{SWO} R1$ = Equivalent integrator amplifier offset voltage due to SW0 leakage current.

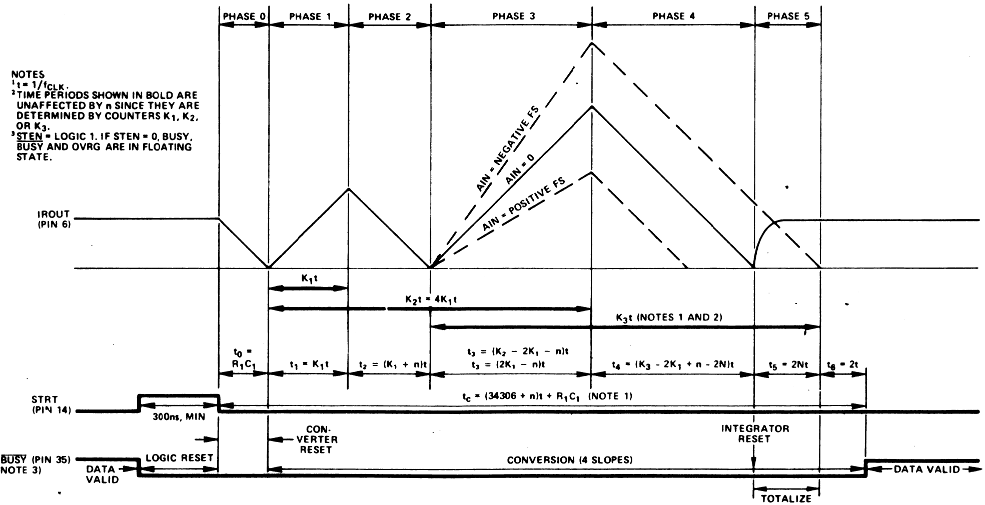


Figure 2. Quad Slope Timing Diagram

The ideal case assumes:

$$AGND = 0V$$

$$V_S = \frac{V_{REF1}}{2}\text{, therefore } \alpha = 0$$

Then (EQN 1) simplifies to:

$$N = \frac{AIN}{V_{REF1}} \cdot 8704 + 4096 \qquad \text{(EQN 2)}$$

or

$$N = \frac{AIN}{FS} \cdot 4096 + 4096 \qquad \text{(EQN 3)}$$

where:

$$FS = \text{full scale input voltage} = \frac{V_{REF1}}{2.125}$$

Equation 1 shows that only α and AGND generate error terms. Errors due to $\alpha \neq 0$ are strongly reduced because of the α^2 term in equation 1. Errors due to AGND $\neq 0$ will, however, have a first order effect on the system performance. Great care should be taken in any circuit layout to minimize or eliminate ground loops between AGND and signal ground. A recommended grounding system is shown in Figure 5.

OUTPUT CODING

The parallel output (DB0–DB12) of the AD7552 represents the number N in binary 2's complement coding when the C_{OUT} pin is connected to the C_{IN} pin (see Table 2).

Analog Input (Note 1)	N (Note 2)	Parallel Digital Output (Note 3)		
		OVRG	DB12	DB11 DB0
+ Overrange	8191	1	0	1111 1111 1111
+ (FS – 1LSB)	8191	0	0	1111 1111 1111
+ 1LSB	4097	0	0	0000 0000 0001
0	4096	0	0	0000 0000 0000
– 1LSB	4095	0	1	1111 1111 1111
– (FS – 1LSB)	1	0	1	0000 0000 0001
– FS	0	0	1	0000 0000 0000
– Overrange	0	1	1	0000 0000 0000

NOTES:

[1] $FS = \frac{V_{REF1}}{2.125}$; 1 Least Significant Bit (LSB) = $FS(2^{-12})$

[2] N = number of counts at C_{OUT} pin

[3] C_{OUT} strapped to C_{IN}; LBEN and HBEN = Logic 1

Table 2. Output Coding (Bipolar 2's Complement

ANALOG CIRCUIT SET-UP AND OPERATION

The following steps, in conjunction with the analog circuitry of Figure 3 explain the selection of the various component values required for proper operation.

1. **Determination of V_{REF1}**

   The reference voltage V_{REF1} and the full scale input voltage FS are related by

   $$V_{REF1} = 2.125\ (FS)$$

   V_{REF1} must be positive for proper operation. A typical value of V_{REF1} is +4.251. An AD584 may be used to provide the reference.

2. **Selection of Integrator Components R1 and C1**

   The integrator time constant should be approximately equal to

   $$R1\,C1 \approx \frac{V_{REF1}(9 \times 10^3)}{f_{CLK}(V_{DD} - 4V)}$$

   The integrating capacitor C1 should be a low leakage, low dielectric absorption type such as Teflon, polystyrene or polypropylene. To minimize noise, the outside foil of C1 should be connected to the output of the integrating amplifier and not to its summing junction.

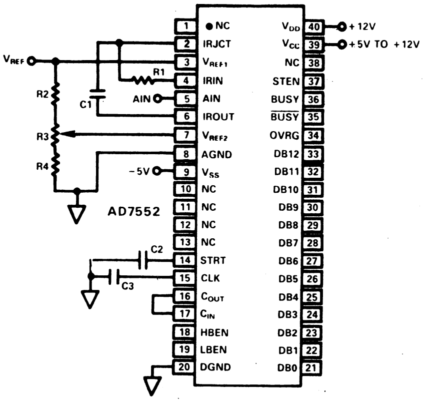


Figure 3. AD7552 Operational Diagram

   Improper selection of the integrator time constant (time constant = R1 C1) may cause excessive noise due to the integrator output swing being too low, or may cause nonlinear operation if the integrator output attempts to exceed the rated output voltage of the amplifier.

3. **Determining Conversion Time**

   As shown in Figure 2, the conversion time is independent of the analog input voltage AIN, and is given by:

   $$t_{CONVERT} = t_{STRT} + \frac{34306}{f_{CLK}} + R1\,C1$$

   where:

   t_{STRT} = STRT pulse duration.
   R_1C_1 = Integrator Time Constant.
   f_{CLK} = CLK Frequency at pin 15.

4. **External or Auto STRT Operation**

   The STRT pin can be driven externally, or with the addition of C2, made to self-start.

   The value of C2 determines the length of time from end of conversion until a new conversion is initiated. This is the "data valid" time and is given by:

   $$t_{DAV} \approx (1.17 \times 10^6\Omega)\ C2 + 20\mu s$$

   When first applying power to the AD7552, a 0V to V_{DD} positive pulse (power up restart) is required at the STRT terminal to initiate auto STRT operation. See APPLICATIONS HINTS No. 5.

5. **Internal Clock Operation**

   The CLK input, pin 15, should normally be driven from an external crystal frequency source, particularly if operation above 250kHz is required. However, for noncritical applications an internal clock oscillator can be activated when a capacitor is connected from pin 15 to DGND. Figure 4 shows a typical curve of clock frequency versus capacitance, C3. Due to process variations the actual operating frequency for a given value of C3 can vary from device to device by up to 100%. Consequently it may be necessary to "tune" C3 to provide the correct clock frequency for a given V_{REF1} and R1C1. For proper operation the clock frequency should be limited to 250kHz. Conversion speeds of up to 80ms can be obtained by increasing the clock frequency to 500kHz. However the flicker due to noise will also increase. See APPLICATIONS HINTS No. 8.

6. **Initial Calibration**

   Trim R3 (Figure 3) so that the voltage on pin 2 (IRJCT) equals $1/2V_{REF1}$ ±0.6%. During this trim and measurement cycle apply a logic HIGH to pin 14 (STRT). This will prevent the AD7552 from executing a conversion.

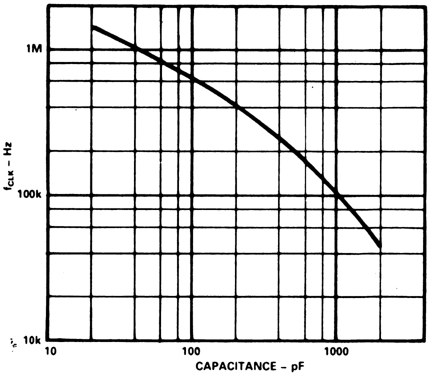


Figure 4. Internal Clock Frequency vs. C3

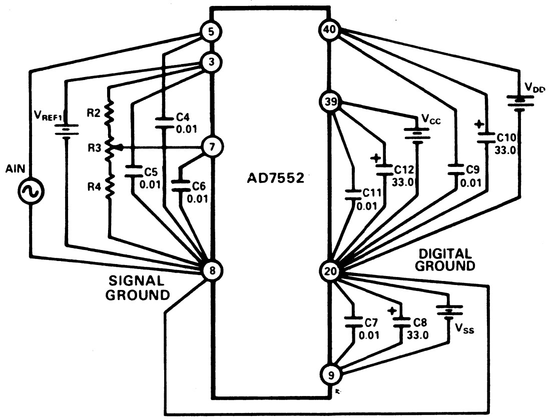
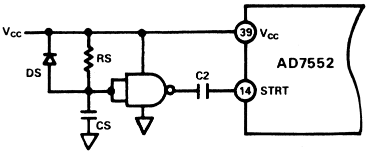


Figure 5. Recommended Grounding System

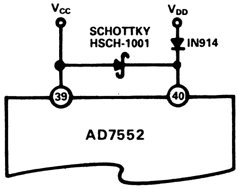
APPLICATIONS HINTS

1. Decouple AIN (pin 5), V_{REF1} (pin 3) and V_{REF2} (pin 7) through 0.01μF to signal ground.
2. Signal ground must be located as close to pin 8 (AGND) as possible.
3. Keep the lead lengths of R1 and C1 toward pin 2 (IRJCT) as short as possible. In addition, both components should lie over the analog ground plane. If C1 has an outside foil, connect it to pin 6 (IROUT), not pin 2.
4. Hold the data bit enables (HBEN, LBEN) in the 0 state during conversion. This is easily accomplished by tying $\overline{\text{STEN}}$ to the 1 state and driving HBEN and LBEN with $\overline{\text{BUSY}}$. This prevents the DB0 through DB12 outputs from coupling noise into the integrator during the phase 1–4 active integration periods.
5. To avoid the requirement of providing a positive STRT pulse on power-up to initiate the auto start operation, the following circuit may be used.

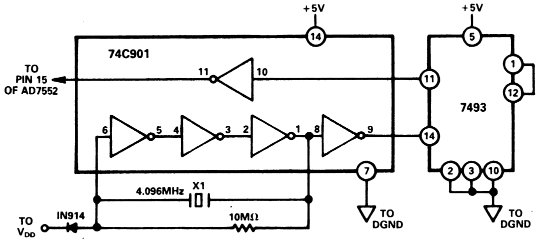


The output of the open collector NAND gate is initially high on power-up. When the charging voltage on CS reaches the input threshold level of the NAND gate, the output goes low and remains low to allow the AD7552 to self start.

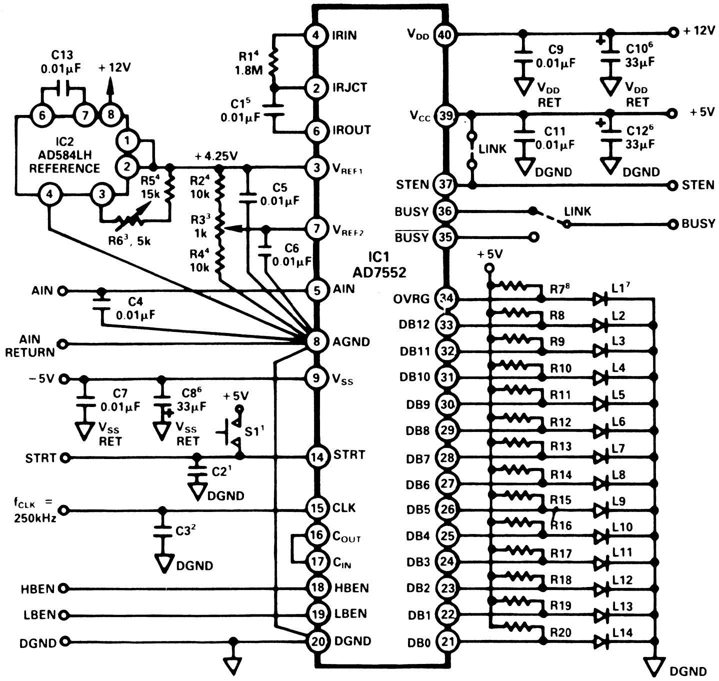
6. Under no circumstances should V_{CC} exceed V_{DD} especially during power-up and power-down. In cases where this situation could occur the following diode protection scheme is recommended.



7. Some solder fluxes and cleaning materials can form slightly conductive films which cause leakage effects across the integrating capacitor. The user is cautioned to ensure that the manufacturing process for circuits using the AD7522 does not allow such films to remain after assembly. Otherwise the accuracy and noise performance of the device will be affected.
8. A suggested crystal oscillator circuit is shown below for use with a V_{CC} of +5V. It uses a standard 4.096MHz crystal which is divided down by 16 to produce a clock frequency of 256kHz.



9. A printed circuit layout for an evaluation board is shown in Figure 8a and 8b. Figure 6 shows the circuit diagram for this evaluation board with component values for f_{CLK} = 250kHz, V_{REF1} = +4.25V operation. Figure 7 shows the component overlay for Figure 8a. Note that either $\overline{\text{BUSY}}$ (pin 35) or BUSY (pin 36) is available at the edge connector via a wire link. Note also that STEN (pin 37) may be tied high via a wire link.



NOTES:

[1] S1 IS A PUSHBUTTON SWITCH TO INITIATE AUTO-START OPERATION. S1 AND C2 ARE NOT REQUIRED FOR EXTERNAL START OPERATION.

[2] C3 IS NOT REQUIRED FOR EXTERNAL CLOCK OPERATION.

[3] FOR CALIBRATION HOLD PIN 14 (STRT) HIGH. ADJUST R6 UNTIL THE VOLTAGE ON PIN 3 (V_{REF1}) IS 4.250V. ADJUST R3 UNTIL THE VOLTAGE ON PIN 2 (IRJCT) IS 2.125 ±0.025V.

[4] R1, R2, R4, R5 1% TOLERANCE, METAL FILM.

[5] C1 MUST BE A LOW LEAKAGE, LOW DIELECTRIC ABSORPTION TYPE SUCH AS TEFLON, POLYSTYRENE OR POLYPROPYLENE.

[6] C8, C10 AND C12 ARE SOLID ELECTROLYTE TANTULUM CAPACITORS.

[7] L1 - L14 ARE LEDS, MONSANTO MV55 OR EQUIVALENT.

[8] R7 - R13 AND R14 - R20 ARE PROVIDED BY TWO THICK-FILM RESISTOR NETWORKS, EACH IN AN 8-PIN SINGLE-IN-LINE PACKAGE. SUITABLE NETWORKS AVAILABLE FROM BECKMAN INSTRUMENTS INC., 2500 HARBOR BOULEVARD, FULLTERTON, CA 92634, MODEL NO. 764-1-4K7.

Figure 6. Evaluation Board Circuit with Component Values for f_{CLK} = 250kHz, V_{REF1} = +4.25V

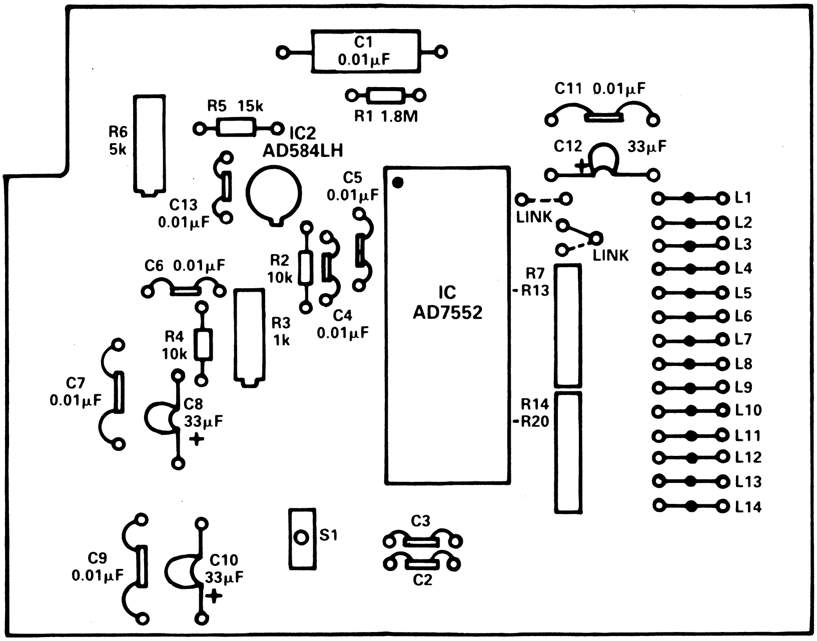


Figure 7. Component Overlay for Figure 8a

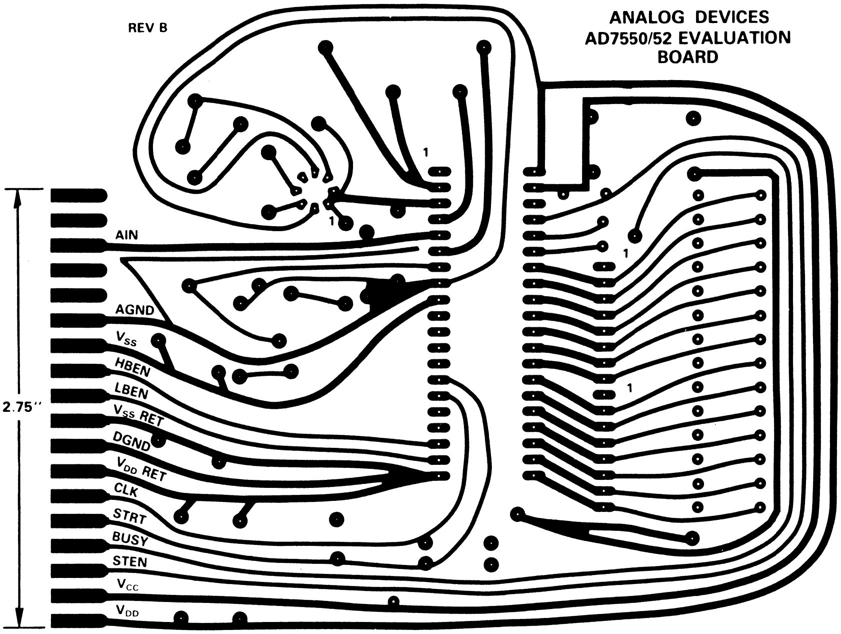


Figure 8a. Component Side

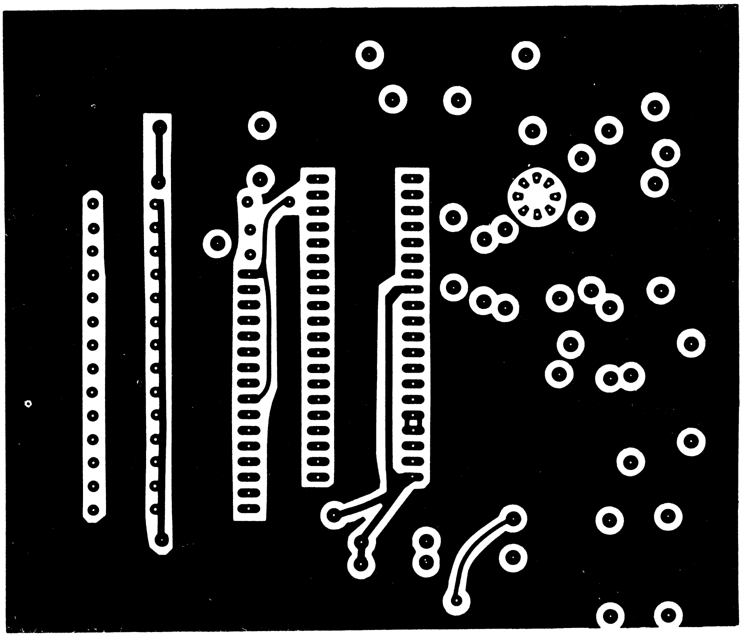


Figure 8b. Foil Side

OBTAINING SIGN-MAGNITUDE 4 DIGIT BCD CODING FROM THE AD7552

Referring to Figure 9 when a convert start pulse is received the four decade presettable up/down counter is loaded with the value 4096. The low level on the up/down count input (Q of X1 = 0) places the CD4029 counters into the count down mode. The contents of the four decade BCD counter are decremented each time a pulse is detected on C_{OUT}. The number of pulses appearing on C_{OUT} is related to both the magnitude and the polarity of the input voltage. If the counter reaches the all 0's state, the flip-flop (X1) is set, placing a high level signal on the up/down count input. The counter will now count up on succeeding C_{OUT} pulses.

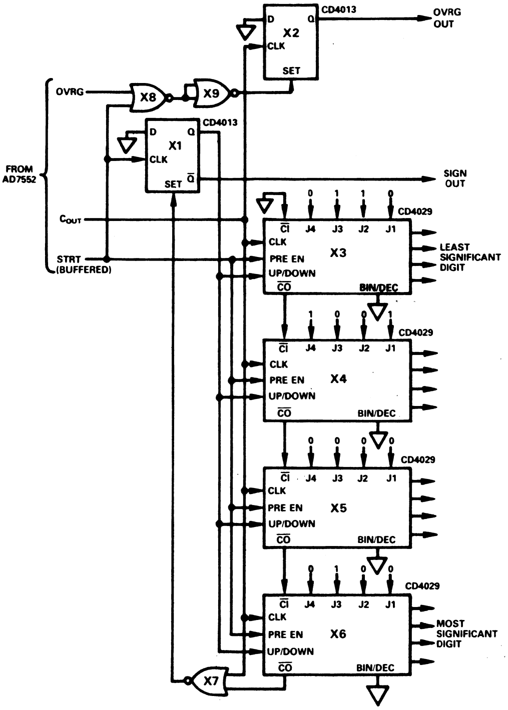


Figure 9. Sign-Magnitude BCD Conversion Circuitry

		SIGN-MAGNITUDE BCD CODING[1]					
Analog Input[2]	**N[3]**	**OVRG**	**Sign**	**Digit 4**	**Digit 3**	**Digit 2**	**Digit 1**
+ Overrange	8191	1	0	4	0	9	5
+ FS – 1LSB	8191	0	0	4	0	9	5
+ 1LSB	4097	0	0	0	0	0	1
0+	4096	0	0	0	0	0	0
0–	4096	0	1	0	0	0	0
– 1LSB	4095	0	1	0	0	0	1
– (FS – 1LSB)	1	0	1	4	0	9	5
– FS	0	1	1	4	0	9	6
– Overrange	0	1	1	4	0	9	6

NOTES

[1] Using circuit of Figure 9.

[2] FS = V_{REF1} ÷ 2.125; 1 Least Significant Bit (LSB) = FS(2^{-12}).

[3] N = number of counts at C_{OUT} pin.

Table 3. Sign-Magnitude BCD Coding

Referring to Table 3 no counts occur on C_{OUT} when the input voltage is either overrange or equal to – FS. Since the most negative value which can be represented in sign-magnitude coding is – (FS – 1LSB) whereas in two's complement coding it is – FS, the X2 flip-flop of Figure 9 ensures that the OVRG output is high if either AIN is overrange or AIN = – FS. Note that there are two codes for zero analog input. This is the result of gating the carry out signal from X6 with the input clock signal C_{OUT}. As mentioned previously, the number of counts at the C_{OUT} terminal is obtained by an internal divide-by-two counter stage. Depending on whether the number of counts to this divide-by-two was odd or event C_{OUT} can remain in either a high or a low state at the end of phase 4. If AIN is negative and less than 1/2LSB (AIN = 0 –), C_{OUT} is high after outputting 4096 counts thus preventing the sign flag from changing. If AIN is positive and less than 1/2LSB, C_{OUT} is low after outputting 4096 counts allowing the sign flag to change. If the carry out signal from X6 is directly connected back to X1, then the code for AIN = 0 – vanishes leaving one code (the 0 + one) for 0V.

This circuit may be used to provide direct readout of analog input voltage with proper scaling of the reference voltage and serial output C_{OUT}. For instance, dividing C_{OUT} by two and adjusting V_{REF1} = + 4.352V gives a FS voltage of 2.048V which will be displayed directly.

		SIGN-MAGNITUDE CODING[1]												
Analog Input[2]	**N[3]**	**OVRG**	**DB12**	**DB11**	**DB10**	**DB9**	**DB8**	**DB7**	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**
+ Overrange	8191	1	0	1	1	1	1	1	1	1	1	1	1	1	1
+ FS – 1LSB	8191	0	0	1	1	1	1	1	1	1	1	1	1	1	1
+ 1LSB	4097	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	4096	0	0	0	0	0	0	0	0	0	0	0	0	0	0
– 1LSB	4095	0	1	0	0	0	0	0	0	0	0	0	0	0	1
– (FS – 1LSB)	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
– FS	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
– Overrange		1	1	0	0	0	0	0	0	0	0	0	0	0	0

NOTES

[1] Using circuit of Figure 10.

[2] FS = V_{REF1} ÷ 2.125; 1 Least Significant Bit (LSB) = FS(2^{-12}).

[3] N = number of counts at C_{OUT} pin.

Table 4. Sign-Magnitude Binary Coding

OBTAINING SIGN-MAGNITUDE BINARY CODING FROM THE AD7552

The circuit of Figure 10 converts the two's complement coding from the AD7552 into sign-magnitude coding. It does this by complementing the AD7552 data and adding 1LSB whenever DB12 is high. In sign-magnitude coding the most negative value that can be represented is −(FS− 1LSB); in two's complement coding it is −FS. The OR gate in Figure 10 ensures only valid output codes are produced (see Table 4). Note that there is only one code for zero scale.

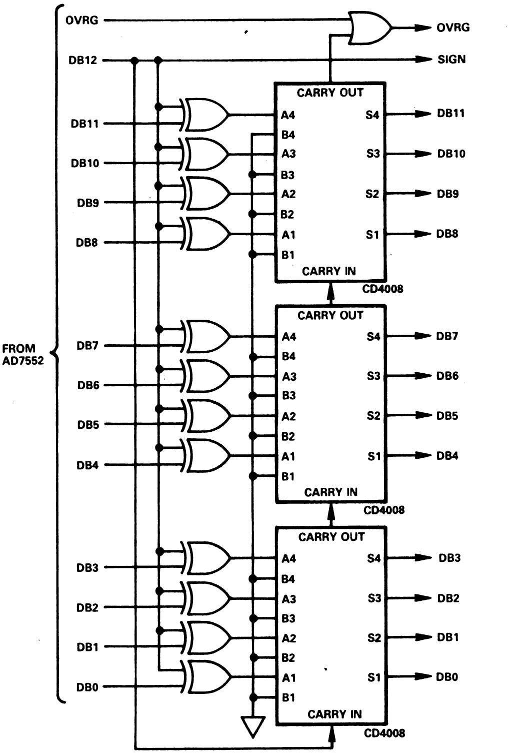


Figure 10. Sign-Magnitude Binary Conversion Circuitry

MICROPROCESSOR INTERFACING

The three-state output capability of the AD7552 allows the multiplexing of the data and status lines onto a single 8-bit wide bus. Figure 11 shows the AD7552 directly interfaced to the 6800 with convert start, data read, etc., all under program control. Note that the two status lines OVRG and BUSY are connected to the data bus in the MSB and LSB positions so that they can easily be interrogated by reading the status word to the microprocessor accumulator, rotating right or left through carry and then checking the carry flag.

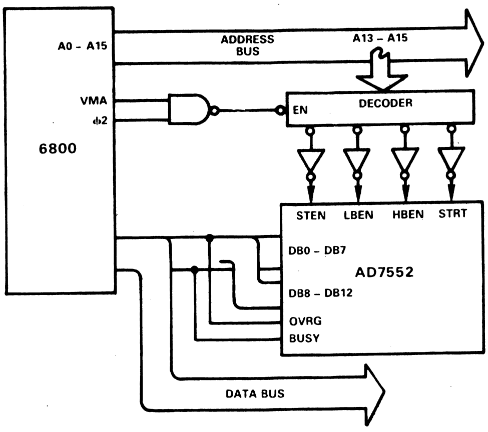


Figure 11. AD7552-6800 Direct Interface

Care should be taken when using fast-access memory or operating at high temperatures to ensure that the AD7552 output drivers relinquish the data bus in time to avoid any possible bus conflict with the following instruction. In any situation where bus conflict is likely, the interfacing technique of Figure 12 is recommended.

AD7552–8085A INTERFACE

Figure 12 shows the AD7552 interfaced to the 8085A. In this application the two status lines share the data bus with the data high byte (DB8–DB12) since the STEN and HBEN inputs are driven simultaneously from a single decoded address. The 8282 data latch which buffers the AD7552 three state drivers from the microprocessor bus ensures that the bus is relinquished promptly at the end of a data read instruction.

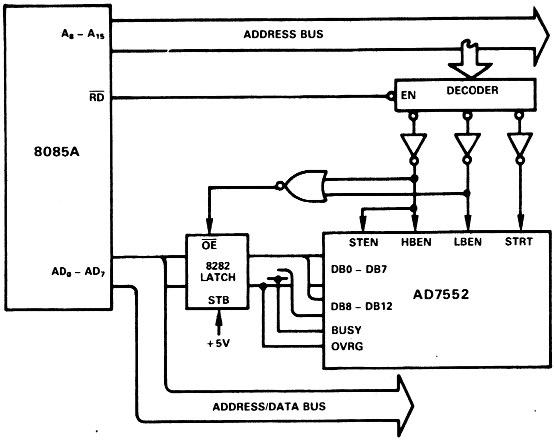


Figure 12. AD7552-8085A Direct Interface

CONTINUOUS CONVERSION MODE

Figure 13 shows the AD7552 connected for continuous conversion. The conversion STRT signal is synchronized with the ALE signal of the 8085A. The $\overline{\text{BUSY}}$ signal is used to update the 8-bit data latches at a time when the microprocessor is not attempting a read operation. Thus the AD7552 appears to the microprocessor as memory which can be read at any time although scrambled data can result if a data update occurs between reading the high byte and low byte data. One method of avoiding this is to read data only after an update has occurred. The microprocessor can be interrupted to perform a data read by tying the AD7552 STRT input to one of the RST inputs on the 8085A.

OPTO–ISOLATED SERIAL INTERFACE

Figure 14 shows a serial interface to the MCS-85 system. This system can accommodate a remote interface where a common-mode voltage is expected to exist between system grounds.

Port C of the 8155 is configured as a control port. Port B is an input port. This port configuration is necessary if sign and/or overrange information is required. Magnitude information is obtained by interrogating the 8155 counter value. The rising edge of $\overline{\text{BUSY}}$ is used to cause an interrupt on the RST 7.5 line. The value ($2^{14} - C_{OUT}$) in the 8155 timer should now be read. When $\overline{\text{BUSY}}$ returns low, the 8155 counter is reset to FF_H. The falling edge of $\overline{\text{BUSY}}$ also latches the sign and overrange data into port B. This is indicated by a rising edge on BF (buffer full) which can be used to call the 8085 CPU to read port B data.

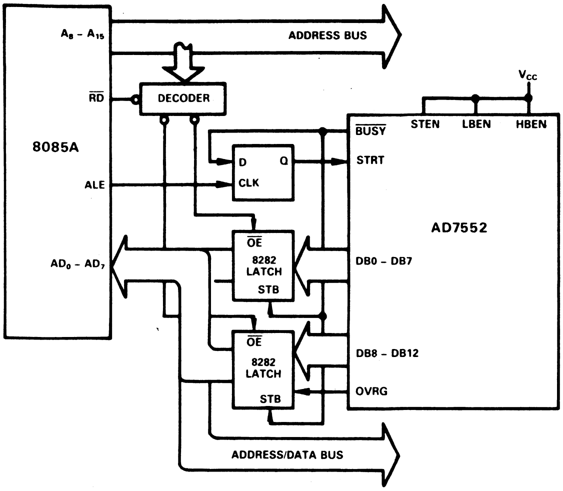
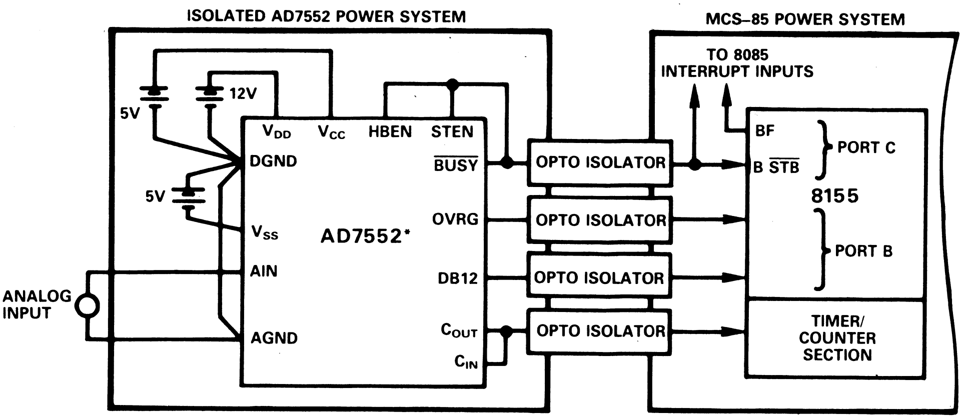


Figure 13. AD7552 in Continous Conversion Mode



*AD7552 USING AUTO-START FACILITY

Figure 14. Optically Isolated Serial AD7552/MCS-85 Interface

ANALOG DEVICES

CMOS 4½/5½ Digit ADC Subsystem

AD7555

PRELIMINARY TECHNICAL DATA

FEATURES

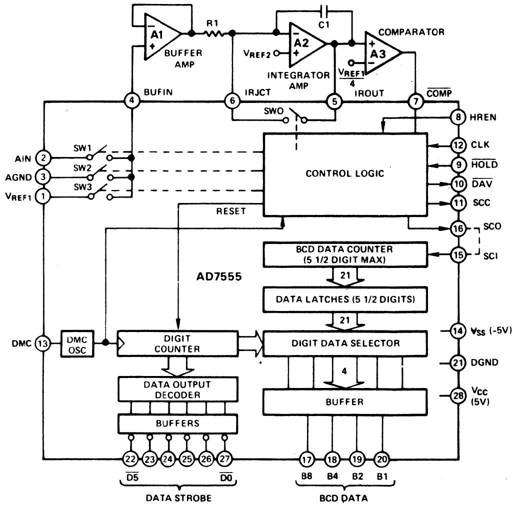
- **Resolution: ±4 1/2 Digits BCD or ±20k Count Binary Capability for 5 1/2 Digit Resolution or Custom Data Formats**
- **Data Format: Multiplexed BCD (for Display) and Serial Count (for External Linearization, Data Reformatting, or Microprocessor Interface)**
- **Accuracy: ±1 Count in ±20k Counts**
- **Scale Factor Drift: 0.2ppm/°C Using Only Medium-Precision Op Amps**
- **Requires only a Single Positive Reference**
- **Overrange Display**
- **Auto Calibration Capability**
- **Interfaces to TTL or 5V CMOS**
- **$\overline{\text{HOLD}}$ Input and SCC (System Conversion Complete) Output for Interface Flexibility**

GENERAL DESCRIPTION

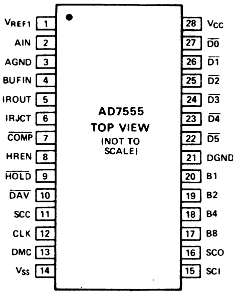
The AD7555 is a 4 1/2 digit, monolithic CMOS, quad slope integrating ADC subsystem designed for display or microprocessor interface applications. Use of the high resolution enable input expands the display format to 5 1/2 digits BCD. With SCO (Serial Count Out) connected to SCI (Serial Count In), the output data format is multiplexed BCD suitable for visual display purposes. As an added feature, SCO can also be used with rate multipliers for linearization, or with BCD or binary counters for data reformatting (up to 200k binary counts).

The quad slope conversion algorithm (Analog Devices patent No. 3872466) converts the external amplifier's input drift errors to a digital number and subsequently reduces the total system drift error to a second order effect. Using only inexpensive, medium-precision amplifiers a scale factor drift of 0.2ppm/°C is achieved.

AD7555 FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



ORDERING INFORMATION

Model	Package	Operating Temperature Range
AD7555BD	28 Pin Side Brazed Ceramic – (D28B)	-25°C to +85°C
AD7555KN	28 Pin Molded Plastic – (N28A)	0 to +70°C

See Section 20 for package outline information.

SPECIFICATIONS (V_{CC} = +5V, V_{SS} = -5V, V_{REF1} = +4.0960V, F_{CLK} = 614.4kHz, AGND = 0V)

PARAMETER	LIMIT AT T_A = +25°C	LIMIT AT T_A = T_{min}, T_{max}	UNITS	CONDITIONS/COMMENTS
ANALOG SWITCHES				
R_{ON} (Switch 1-3)	800	1200	Ω max	$-2V \leqslant AIN \leqslant +2V$ Refer to Functional Diagram
ΔR_{ON} (Switch 1) versus AIN	300	500	Ω typ	$-2V \leqslant AIN \leqslant +2V$
Mismatch Between Any Two Switches (excluding SW0)	300	500	Ω typ	$-2V \leqslant AIN \leqslant +2V$
I_{LKG} (Switch OFF)				
SW0 (pin 6)	1	70	nA max	IRJCT (pin 5) = +2.048V $0V \leqslant$ IROUT (pin 5) $\leqslant +10V$
SW1 (pin 2)	1	70	nA typ	AIN = +2V to -2V, BUFIN = 0V and +4.096V
SW2 (pin 3)	1	70	nA typ	AGND = 0V, BUFIN = -2V to +2V, +4.096V
SW3 (pin 1)	1	70	nA typ	V_{REF1} = +4.096V, BUFIN = -2V to +2V
I_{LKG} (BUFIN, pin 4)	3	200	nA typ	Any 1 of SW1, 2, 3 on
CONTROL INPUTS (pins 7, 8, 9, 15)				
V_{INH}	3.0	3.0	V min	
V_{INL}	0.8	0.8	V max	
I_{INH} or I_{INL}	1	10	µA max	V_{IN} = 0V or V_{CC}
CLOCK INPUTS (pin 12 and 13)				
V_{INH} (CLK)	3.5	3.5	V min	
V_{INL} (CLK)	0.8	0.8	V max	
V_{INH} (DMC)	3.0	3.0	V min	
V_{INL} (DMC)	0.8	0.8	V max	
I_{INH} (CLK)	1.0	1.5	mA max	
I_{INL} (CLK)	-1.0	-1.5	mA max	
I_{INH} (DMC)	200	300	µA max	
I_{INL} (DMC)	-100	-150	µA max	
DIGITAL OUTPUTS				
$\overline{D0}$ - $\overline{D5}$ (pins 22-27)				
V_{OH}	4.5	4.5	V min	I_{SOURCE} = 40µA
V_{OL}	4.0	4.0	V max	I_{SINK} = 5mA (Display Driver Load)
V_{OL}	0.5	0.8	V max	I_{SINK} = 1.6mA (TTL Load)
B1, B2, B4, B8, $\overline{DAV}$, SCC, SCO (pins 20, 19, 18, 17, 10, 11, 16)				
V_{OH}	4.0	4.0	V min	I_{SOURCE} = 40µA
V_{OL}	0.5	0.8	V max	I_{SINK} = 1.6mA
DYNAMIC PERFORMANCE				
DMC Pulse Width	5	5	µs min	See Figure 3
DMC Frequency	100	100	kHz max	Typical f_{DMC} is 1.5kHz with C_{DMC} = 0.01µF
CLK Frequency	1.5	1.5	MHz max	
Propagation Delays				
DMC HIGH to $\overline{DAV}$ HIGH	5	7	µs max	See Figure 3
DMC HIGH to $\overline{DAV}$ LOW	5	7	µs max	
DMC HIGH to BCD Data on B8, B4, B2, B1	5	5	µs max	
DMC LOW to Digit Strobe (D0 - D5) LOW	5	5	µs max	
POWER SUPPLY				
I_{CC}	5	5	mA max	During Conversion
I_{SS}	5	5	mA max	During Conversion
V_{CC} Range	+5 to +17	+5 to +17	V	See Absolute Maximum Ratings
V_{SS} Range	-5 to -17	-5 to -17	V	

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

V_{CC} to DGND	+17V
V_{SS} to DGND	-17V
V_{CC} to V_{SS}	+22V
Digital Outputs	V_{CC}, DGND
Digital Inputs	
DMC (Pin 13), CLK (Pin 12)	V_{SS}, V_{CC}
All other Logic Inputs	DGND, +17V
Analog Inputs/Outputs	
AGND to DGND (Positive Limitation)	V_{CC} or V_{IROUT}*
AGND to DGND (Negative Limitation)	V_{SS} or V_{IROUT} -20V†
AIN (Pin 2), V_{REF1} (Pin 1), BUFIN (Pin 4)	V_{CC}, V_{SS}
IRJCT (Pin 6), IROUT (Pin 5)	+27V, AGND
Operating Temperature Range	
AD7555KN (Plastic)	0 to +70°C
AD7555BD (Ceramic)	-25°C to +85°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10s)	+300°C
Power Dissipation (package)	
Plastic (AD7555KN)	
To +50°C	1200mW
Derate above +50°C by	12mW/°C
Ceramic (AD7555BD)	
To +50°C	1000mW
Derate above +50°C by	10mW/°C

*Whichever is the least positive.
†Whichever is the least negative.

NOTE:
Do not apply voltages to any AD7555 digital output, AIN or V_{REF1} before V_{SS} and V_{CC} are applied. Additionally, the voltages at AIN, V_{REF1} or any digital output must never exceed V_{CC} and V_{SS} (if an op amp output is used to drive AIN it must be powered by the AD7555 V_{CC} and V_{SS} supply voltages). Do not allow any digital input to swing below DGND. V_{DD}, the external op-amps positive supply voltage, should be applied before V_{CC}.

CAUTION:
ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The foam should be discharged to the destination socket before devices are removed.

SYSTEM ELECTRICAL CHARACTERISTICS (T_A = 0 to +45°C)
Characteristics refer to the system of Figures 6a and 6b. V_{CC} = +5V, V_{SS} = -5V, V_{REF1} = +4.096V, error count n calibrated to zero at T_A = +25°C as described in the calibration section unless otherwise noted. Switch leakages and limitations in temperature performance of auxiliary components (such as the integrating capacitor) cause performance degradations above +45°C.

CHARACTERISTIC	LIMIT	CONDITIONS/COMMENTS
Resolution	4 1/2 Digit BCD 5 1/2 Digit BCD	±20,000 Counts ±200,000 Counts (See Note 1)
Relative Accuracy	±1 Count max ±10 Count max	4 1/2 Digit BCD 5 1/2 Digit BCD (See Notes 1 and 2)
Count Uncertainty Due to Noise (Flicker)	±1/2 Count max ±2 Counts max	4 1/2 Digit BCD 5 1/2 Digit BCD (See Note 1)
Conversion Time	610ms max 1,760ms max	4 1/2 Digit BCD 5 1/2 Digit BCD (See Note 1)

NOTES:
[1] 4 1/2 digit mode; f_{CLK} = 614.4kHz, HREN = LOW, R_1 = 360kΩ
C_1 = 0.22µF
5 1/2 digit mode; f_{CLK} = 1.024MHz, HREN = HIGH, R_1 = 750kΩ
C_1 = 0.22µF
[2] Assumes voltage reference (V_{REF1}) TC of 0ppm/°C.

Applying the AD7555

AD7555 PIN DESCRIPTION		
ANALOG FUNCTIONS		
V_{REF1}	(Pin 1):	+4.096V Reference Input
AIN	(Pin 2):	Analog Input Voltage (±2V Full Scale)
AGND	(Pin 3):	Analog Signal Common Ground
BUFIN	(Pin 4):	To External Buffer Amplifier Input
IROUT	(Pin 5):	From Integrator Amplifier Output
IRJCT	(Pin 6):	To Integrator Amplifier Summing Junction
LOGIC INPUTS		
$\overline{\text{COMP}}$	(Pin 7):	Input from the external comparator.
HREN	(Pin 8):	High Resolution Enable, determines converter resolution HREN = LOGIC LOW, Full Scale = ±1.9999V (100μV resolution) HREN = LOGIC HIGH, Full Scale = ±1.99999V (10μV resolution)
$\overline{\text{HOLD}}$	(Pin 9):	Hold Input $\overline{\text{HOLD}}$ = LOGIC HIGH, the ADC converts and updates the displays continuously as per the timing diagram of Figure 3. $\overline{\text{HOLD}}$ = LOGIC LOW, the ADC is reset and conversion is disabled. Data from the last complete conversion continues to be displayed. To ensure most recent data is displayed, $\overline{\text{HOLD}}$ should not be taken LOW when $\overline{\text{DAV}}$ is HIGH. When $\overline{\text{HOLD}}$ returns HIGH, the next leading edge of DMC initiates a new conversion.
DMC	(Pin 13):	Display Multiplexer Clock, can be driven from an external logic source, or with the addition of an external capacitor, will self oscillate. With an external capacitor of 10,000pF, DMC oscillates at approximately 1.5kHz at a 5% to 10% duty cycle, suitable for display purposes.
CLK	(Pin 12):	Clock Input for maximum line rejection in the 4 1/2 digit mode; 50Hz: f_{CLK} = 512kHz (= 4.096MHz ÷ 8) 60Hz: f_{CLK} = 614.4kHz (= 4.915MHz ÷ 8) 50/60Hz: f_{CLK} = 409.6kHz (= 3.2768MHz ÷ 8) For maximum line rejection in the 5 1/2 digit mode; 50/60Hz, f_{CLK} = 1.024MHz (= 4.096MHz ÷ 4)
SCI	(Pin 15):	Serial Count In. Input to totalizing counter in the AD7555. SCI is normally connected to SCO for direct count totalization.
SUPPLY INPUTS		
V_{CC}	(Pin 28):	Positive Supply Input (+5V)
V_{SS}	(Pin 14):	Negative Supply Input (−5V)
DGND	(Pin 21):	Digital Ground

LOGIC OUTPUTS		
B8 - B1	(Pins 17 - 20)	BCD8 - BCD1 output, Active HIGH (See table 1)
$\overline{\text{D5}}$	(Pin 22):	10^{-5} digit output, Active LOW in 5 1/2 digit mode, stays HIGH in 4 1/2 digit mode
$\overline{\text{D4}}$ - $\overline{\text{D1}}$	(Pins 23-27)	10^{-4} - 10^{-1} digit outputs, Active LOW
$\overline{\text{D0}}$	(Pin 27):	10^0 /overflow/polarity output, Active LOW
SCC	(Pin 11):	System conversion complete, goes HIGH when conversion is complete, returns LOW on comparator crossing at end of phase 0 integration period.
SCO	(Pin 16):	Serial Count Out, a serial output pulse train proportional in length to the magnitude of AIN. SCO can be externally pulled HIGH while $\overline{\text{DAV}}$ = HIGH to display the error count "n" for calibration purposes (see calibration section).
$\overline{\text{DAV}}$	(Pin 10):	Data Valid – When low, $\overline{\text{DAV}}$ indicates that the data being presented on the BCD output bus is valid. $\overline{\text{DAV}}$ goes high on the first positive edge of DMC after a conversion is complete and returns low two DMC pulses later. When it returns low, the digit counter is reset to $\overline{\text{D0}}$. This is termed the MASTER RESET.

DATA		B8	B4	B2	B1	LED DISPLAY WHEN USING 7447 SEGMENT DECODER
0		0	0	0	0	0
1		0	0	0	1	1
2		0	0	1	0	2
3		0	0	1	1	3
4		0	1	0	0	4
5		0	1	0	1	5
6		0	1	1	0	6
7		0	1	1	1	7
8		1	0	0	0	8
9		1	0	0	1	9
OVERFLOW		1	1	0	0	⊔
DIGIT 0 ONLY	+1	0	0	0	0	+1
	-1	0	0	1	0	−1
	+	1	1	0	0	+
	-	0	1	1	1	−

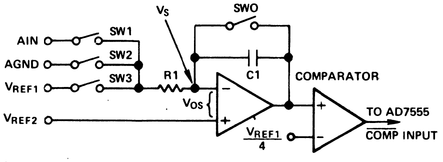
Table 1. Output Coding

Quad Slope Theory of Operation

Component limitations such as switch leakage, as well as operational amplifier offset voltage and bias current (and the temperature dependency of these errors), are major obstacles when designing high resolution integrating A/D converters.

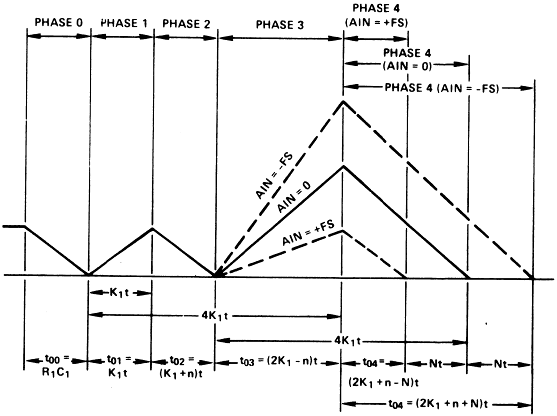
The AD7555 however, utilizes a patented *quad slope* conversion technique (Analog Devices Patent No. 3872466) to reduce the effects of such errors to second order effects.

Figure 1 shows a simplified quad slope integrator circuit. The various inputs AGND (Analog Ground), V_{REF1}, and AIN (Analog Input) are applied in sequence to the integrator via switches 1-3 (see Table 2), creating four slopes at the integrator output (phase 1-4 of Figure 2). If the equivalent summing junction voltage V_S is precisely $0.5V_{REF1}$, the phase 1 and phase 2 integration times are equal, indicating there are no input errors. If $V_S \neq 0.5V_{REF1}$ (due to amplifier offset voltage, bias current, etc.), an error count "n" is obtained. The analog input integration cycle (phase 3) is subsequently lengthened or shortened by "n" counts, depending on whether the error was positive or negative.



$V_S = V_{REF2} + V_{OS} + I_{BIAS}R_1 + I_{LKGSWO}R_1$

Figure 1. Simplified Quad Slope Integrator Circuit



NOTES:
1. FOR 4 1/2 DIGIT MODE, K_1 = 10,240
$t = 4 \times 1/f_{CLK}$, WHERE f_{CLK} IS CLOCK FREQUENCY AT PIN 12
2. FOR 5 1/2 DIGIT MODE, K_1 = 102,400
$t = 2/f_{CLK}$, WHERE f_{CLK} IS CLOCK FREQUENCY AT PIN 12
3. n = ERROR COUNT DUE TO AMPLIFIER OFFSETS ETC. AND CAN BE POSITIVE OR NEGATIVE.

Figure 2. Quad Slope Integrator Output

The final effect is to reduce the analog input error terms to second order effects. This can be proven by solving the differential equations obtained during the phase 1 through phase 4 integration periods. Barring third (and higher) order effects, the solutions are given in equations 1 and 2.

$$N_{(AIN \geq 0)} = \underbrace{K_T\left[\frac{AIN}{V_{REF1}}\right]}_{\text{IDEAL TERM}} \underbrace{+K_T\left[\frac{AIN}{V_{REF1}} - 1\right]\left[-a^2 + \frac{AGND}{V_{REF1}}(1+2a)\right]}_{\text{ERROR TERM}} \qquad \text{EQN1}$$

$$N_{(AIN < 0)} = \underbrace{-K_T\left[\frac{AIN}{V_{REF1}}\right]}_{\text{IDEAL TERM}} \underbrace{-K_T\left[\frac{AIN}{V_{REF1}} - 1\right]\left[-a^2 + \frac{AGND}{V_{REF1}}(1+2a)\right]}_{\text{ERROR TERM}} \qquad \text{EQN2}$$

WHERE:

N = Number of counts appearing at AD7555 Serial Count Out pin corresponding to the analog input voltage, AIN.

AIN = Analog Input Voltage to be digitized

K_T = 40960 counts (4 1/2 Digit Mode)
409600 counts (5 1/2 Digit Mode)

AGND = Voltage at AD7555 pin 3 (AGND) measured with respect to V_{REF1} and AIN signal common ground. (Ideally, AGND = 0V)

a is an error term equal to $\frac{2V_S - V_{REF1}}{V_{REF1}}$

Ideally $a = 0$ when $V_S = 0.5V_{REF1}$.

NOTE:

$V_S = V_{REF2} + V_{OS1} + V_{OS2} + I_{B2}R_1 + I_{SWO}R_1$

WHERE:

V_{REF2} = $0.5V_{REF1}$ if no error is present

V_{OS1} = Offset voltage of buffer amplifier A1 (required to buffer the effect of ΔR_{ON} of SW1 - SW2)

V_{OS2} = Offset voltage of integrator amplifier A2

$I_{B2}R_1$ = Equivalent integrator amplifier offset voltage due to bias current of A2

$I_{SWO}R_1$ = Equivalent integrator amplifier offset voltage due to SWO leakage current.

If AGND = 0, then the error terms of EQN 1 and 2 contain only second order effects due to $a \neq 0$. Thus, the AD7555 is a powerful tool which allows high precision system performance to be obtained when using only moderate precision op amps.

Other advantages of the quad slope technique include bipolar operation using a single positive voltage reference, and the fact that since the comparator propagation delay is constant hysteresis effects are eliminated. (This is because the comparator always approaches the zero crossing from the same direction).

Phase	Switch Closed (Figure 1)	Equivalent Input Voltage	Integration Time
0	SW3	$V_{REF1} - V_S$	$t_{00} = R_1C_1$
1	SW2	AGND - V_S	$t_{01} = K_1t$
2	SW3	$V_{REF1} - V_S$	$t_{02} = (K_1 + n)t$
3	SW1	AIN - V_S	$t_{03} = (2K_1 - n)t$
4	SW3	$V_{REF1} - V_S$	$t_{04} = (2K_1 + n \pm N)t$
5	SWO	RESET INTEGRATOR	

Table 2. Integrator Equivalent Input Voltages and Integration Times

TIMING AND CONTROL

Figure 3 shows the AD7555 timing. SCC goes HIGH at the end of SCO indicating conversion is complete. $\overline{DAV}$ goes HIGH on the 1st leading edge of DMC after conversion is complete. New data is strobed into the data latches (see functional diagram) on the leading edge of the 2nd DMC. $\overline{DAV}$ returns low on the leading edge of the 3rd DMC.

BCD data is placed on B1, B2, B4, B8 on the positive edge of DMC while the digit counter is incremented on the negative edges of DMC.

A reset phase (phase 0) is initiated on the 4th DMC after conversion is complete. SCC returns low at the phase 0 comparator crossing indicating a conversion start.

If the DMC oscillator is set up to free run (C8 in Figure 6b causes DMC to run at about 1.5kHz), the AD7555 will continuously convert and update the displays.

Externally controlling the generation of DMC pulses provides a means of controlling data outputting for computer interface applications. Microprocessor Interfacing page illustrates how to use this feature to interface the AD7555 to a microprocessor.

DISPLAY

The output data format of the AD7555 is multiplexed BCD as per the Timing Diagram of Figure 3. The output code format is shown in Table 1.

Overflow causes digit 1 through digit 4 (digit 1 through digit 5 in 5 1/2 digit mode) to output a BCD 12 (1100). Overflow does not affect digit 0. Therefore, a positive overflow is displayed as +/. ⊔⊔⊔⊔ and a negative overflow as –/. ⊔⊔⊔⊔ when using the 7447 seven-segment decoder.

PRINTED CIRCUIT LAYOUT

To ensure performance with the system specifications Figures 5a and 5b show the recommended P.C. board layout for the AD7555. Figure 4 shows the component overlay for Figure 5a.

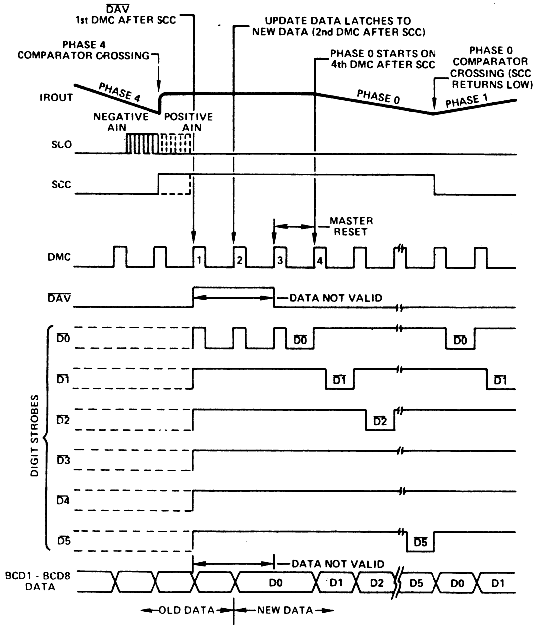


Figure 3. Timing Diagram (Self Start DPM Mode)

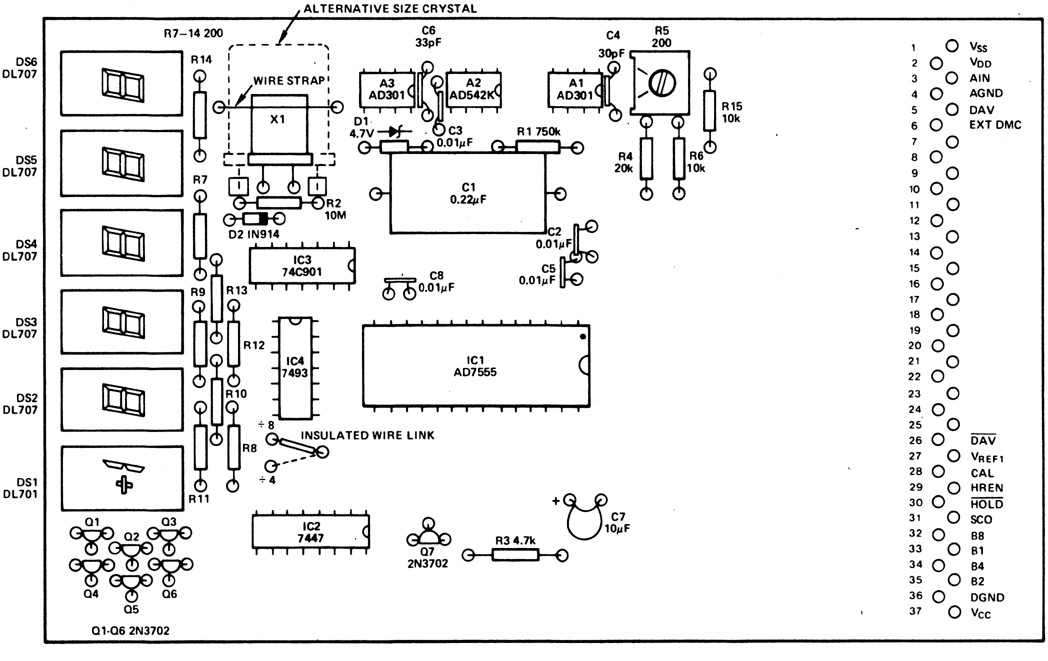


Figure 4. Component Overlay for Figure 5a

Note that a pad already exists on the PCB layout for an AD584LH voltage reference, suitable for 4 1/2 digit operation.

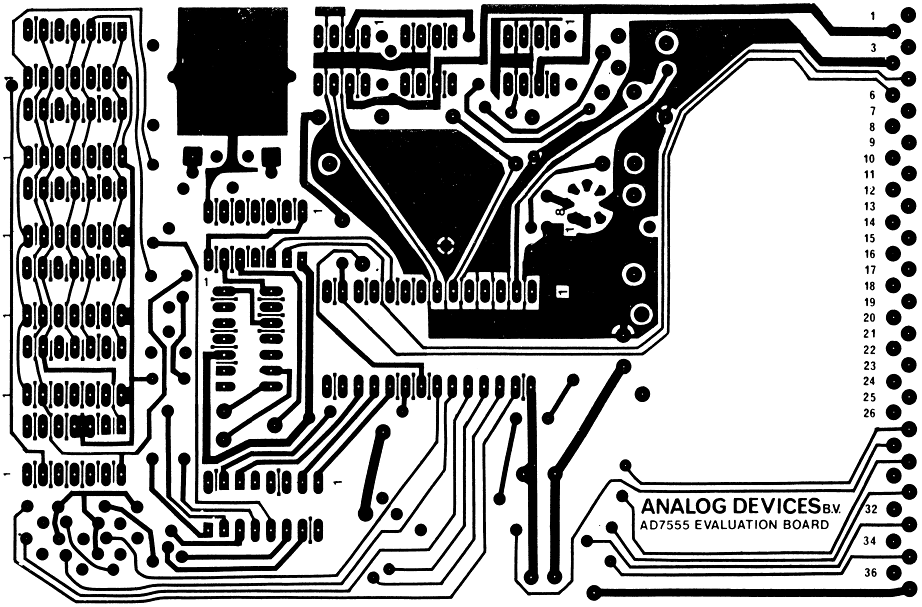


Figure 5a. Component Side (Reduced Scale)

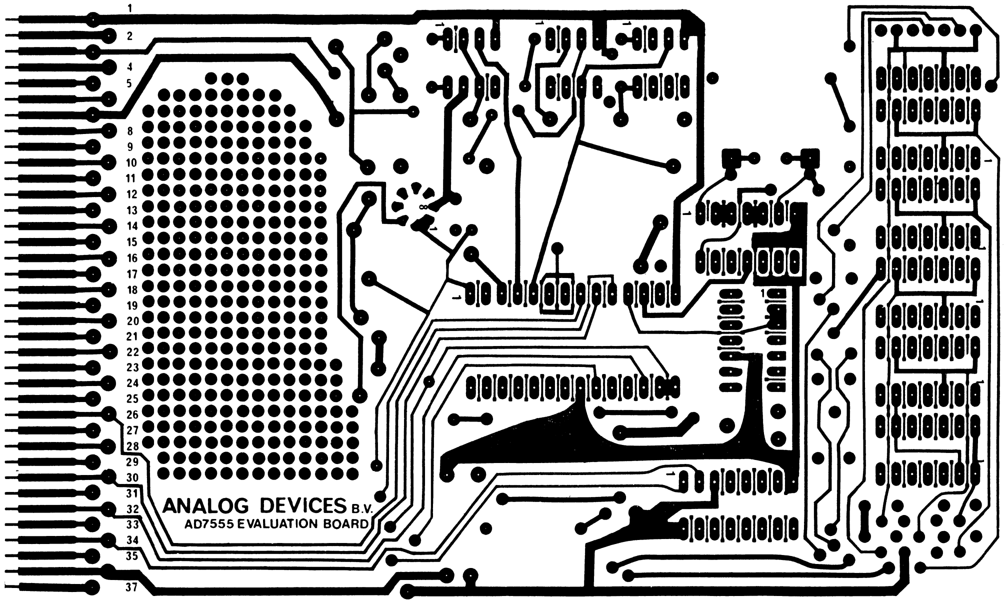


Figure 5b. Foil Side (Reduced Scale)

ANALOG CIRCUIT SET-UP AND OPERATION

The following steps, in conjunction with the analog circuitry of Figure 6a explain the selection of the various component values required for proper operation.

1. **Selection of Integrator Components R_1 and C_1**
   Improper selection of the integrator time constant (time constant = R_1C_1) may cause excessive noise due to the integrator output level being too low, or may cause non-linear operation if the integrator output attempts to exceed the rated output voltage of the amplifier. The integrator time constant R_1C_1 must be:

$$\frac{(V_{REF1})(K_a)}{(f_{CLK})(7V)} \geqslant R_1C_1 \geqslant \frac{(V_{REF1})(K_a)}{(f_{CLK})(V_{DD}-5V)}$$

   Where:

   V_{DD} is the integrator amplifier positive supply voltage
   f_{CLK} is the clock frequency at pin 12
   $K_a = 8.2 \times 10^4$ (4 1/2 digit mode)
   or 4.0×10^5 (5 1/2 digit mode)

   The integrating capacitor must be a low leakage, low dielectric absorption type such as teflon (5 1/2 digit mode), polystyrene or polypropylene (4 1/2 digit mode). To minimize noise injection, the outside foil of C1 must be connected to the output of the integrating amplifier, not to its summing junction.

   The recommended maximum value for R1 in both the 4 1/2 digit and 5 1/2 digit mode is 750kΩ. Higher values may cause noise injection.

2. **Determing Conversion Time**
   Maximum conversion time occurs when A_{IN} = -FS and is given by

   4 1/2 DIGIT MODE

   $t_{CONVERT} = (325{,}760)(t_{CLK}) + R_1C_1$

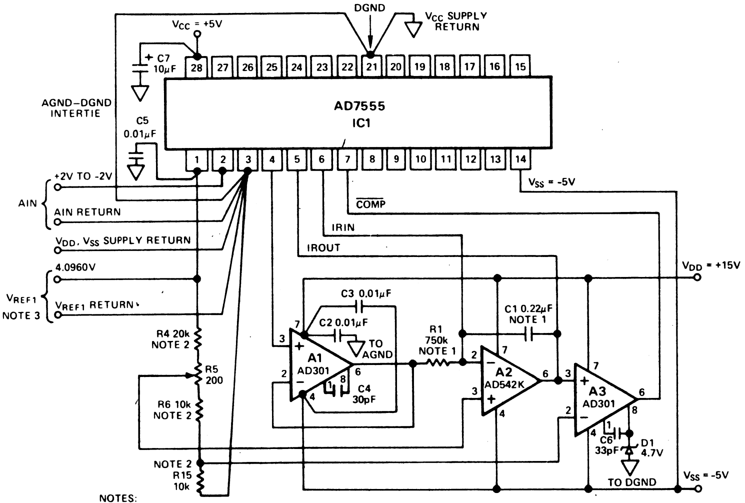
   5 1/2 DIGIT MODE

   $t_{CONVERT} = (1{,}628{,}800)(t_{CLK}) + R_1C_1$

   Where:

   t_{CLK} = Period of CLK as measured at pin 12
   R_1C_1 = Integrator Time Constant

3. **Initial Calibration**
   a. Adjust V_{REF1} so that the voltage at pin 1 (V_{REF1}) of the AD7555 is +4.0960V.
   b. Apply 0V to AIN and adjust R5 (V_{REF2} Adjust) for display 0.0000. (See optional calibration procedure on the next page for more precise calibration.)



NOTES:
1. R_1C_1 VALUES SHOWN ARE FOR 5 1/2 DIGIT MODE. FOR 4 1/2 DIGIT MODE R_1 = 360k, C_1 = 0.22µF. SUITABLE CAPACITORS AVAILABLE FROM COMPONENT RESEARCH CO. INC., 1655 26th STREET, SANTA MONICA, CA. 90404. (STOCK NUMBER FOR 0.22µF CAPACITOR IS D11B224KXW).
2. R4, R6, R15 1% TOLERANCE
3. FOR 4 1/2 DIGIT MODE USE AD584LH, FOR 5 1/2 DIGIT MODE A TEMPERATURE CONTROLLED BURIED ZENER REFERENCE SUCH AS THE LM399H SHOULD BE USED.

Figure 6a. Analog Circuit Diagram

APPLICATION HINTS

1. See Note under Absolute Maximum Ratings for proper power sequencing and input/output voltage ratings.
2. For linear operation the absolute magnitude of AIN cannot exceed 1/2 V_{REF1}. In no case must AIN be more negative than V_{SS}.
3. Do not leave unused CMOS inputs floating.
4. Check that integrator components R1 and C1 are chosen as per paragraph 1 of the setup and operation section on this page and that initial calibration as per paragraph 3 has been accomplished. A resistor value no larger than 750kΩ is recommended to minimize noise pickup.
5. For optimum normal mode noise rejection, use the crystal frequencies shown in the applications section.
6. In order for the calibrate mode (on the next page) to display the error count properly it can be shown that
   $V_{REF2} \geqslant V_{REF1} \times 0.4883$
   Specifically, for V_{REF1} = 4.0960V
   $V_{REF2} \geqslant 2V$

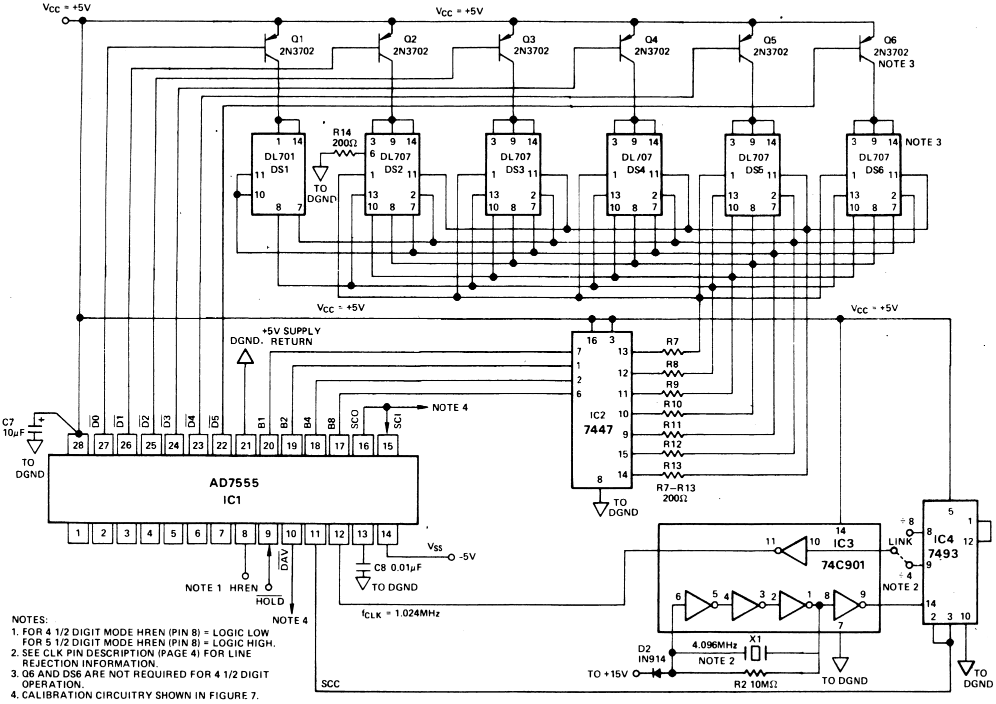
LOGIC AND DISPLAY CIRCUITRY

The AD7555 possesses 4 1/2 digit accuracy with potential for 5 1/2 digit resolution. Figure 6b shows the logic and display circuitry when operating the AD7555 with this high resolution.

MODIFYING THE FULL SCALE DISPLAY

Availability of the SCO and SCI terminals on the AD7555 provides flexibility for range-switching and modified data-format applications.

For example, in the 5 1/2 digit mode, inserting a ÷5 counter between SCO and SCI provides a full scale count at SCI of 39,999 counts (199,999÷5).



NOTES:
1. FOR 4 1/2 DIGIT MODE HREN (PIN 8) = LOGIC LOW
FOR 5 1/2 DIGIT MODE HREN (PIN 8) = LOGIC HIGH.
2. SEE CLK PIN DESCRIPTION (PAGE 4) FOR LINE REJECTION INFORMATION.
3. Q6 AND DS6 ARE NOT REQUIRED FOR 4 1/2 DIGIT OPERATION.
4. CALIBRATION CIRCUITRY SHOWN IN FIGURE 7.

Figure 6b. Logic and Display Circuitry (for 5 1/2 Digit Resolution)

CALIBRATING THE AD7555

When the AD7555 is placed in the *calibrate* mode, any resulting error voltage in V_S (summing junction voltage), due to drift, etc., will be contained in the resulting display. To display the error SC1 and SCO must be taken HIGH (only allowable when $\overline{\text{DAV}}$ is HIGH). In the *calibrate* mode the display indicates +ƀ.0480 ±n (+ƀ.04800 ±n in 5 1/2 digit mode) where ƀ indicates a blanked digit and n is a number representing the reference input errors. This gives the change required in V_{REF2} ($\pm\Delta V_{REF2}$) for proper calibration (ie., $n \approx 0$). The exact relationship between n and ΔV_{REF2} can be shown to be equal to:

$$\Delta V_{REF2} = \frac{(V_{REF1})n}{40{,}960 + n} \quad \text{(4 1/2 digit operation)}$$

$$\Delta V_{REF2} = \frac{(V_{REF1})10n}{40{,}960 + 10n} \quad \text{(5 1/2 digit operation)}$$

For this capability to operate, $|V_{REF2}|$ must be 1/2 V_{REF1} ±2%.

Figure 7 shows the hardware connections for manual calibration. With the switch in the *calibrate* mode, adjust V_{REF2} (potentiometer R5 as shown in Figure 6a) until the display reads +ƀ.0480 (+ƀ0.04800 in 5 1/2 digit mode). The AD7555 is now calibrated to the center of its error correcting range.

Return the switch to *normal* to resume normal conversion.

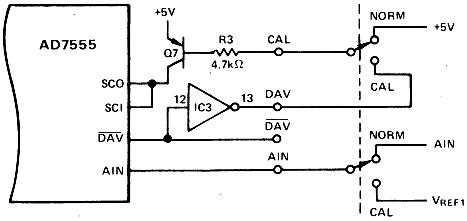


Figure 7. Hardware Requirements for Manual Calibration of n = 0

Microprocessor Interfacing

AD7555 AS A POLLED INPUT DEVICE (MCS-85 SYSTEM)

Figure 8 shows an AD7555/8085 interface. The DMC clock input of the AD7555 is controlled by the microcomputer via an output port of the 8155.

Typical timing for this interface mode is shown in Figure 9. $\overline{\text{DAV}}$ goes HIGH on the 1st DMC leading edge after SCC goes HIGH. It returns LOW on the rising edge of the 3rd DMC pulse. Digit zero is availabe on B1, B2, B4 and B8 at this time. The leading edge of the 4th DMC pulse initiates a new conversion and places digit 1 on B1, B2, B4 and B8.

Table 3 shows a procedure for polling the AD7555.

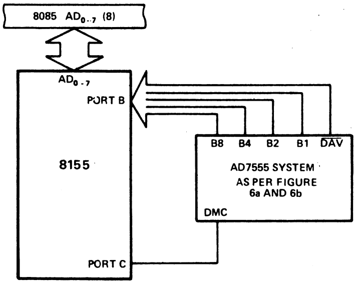


Figure 8. AD7555 as a Polled Input Device

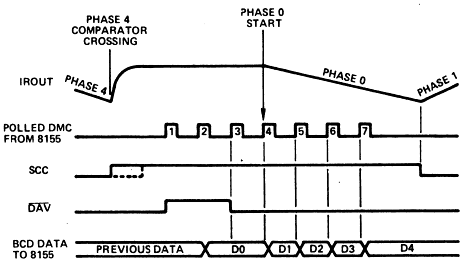


Figure 9. Timing Diagram for Operation as a Polled Input Device (8085/AD7555)

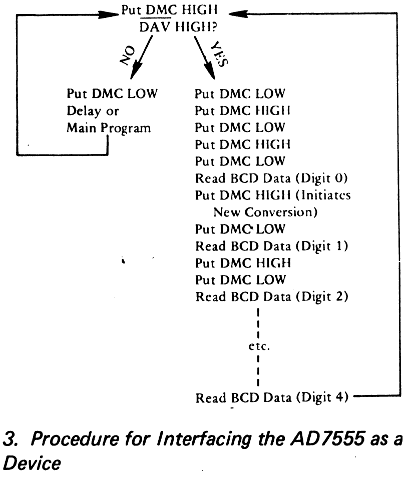


Table 3. Procedure for Interfacing the AD7555 as a Polled Input Device

AD7555 AS AN INTERRUPTING INPUT DEVICE (MCS-85 SYSTEM)

The AD7555 DMC oscillator provides DMC pulses until SCC (System Conversion Complete) goes high. This causes an interrupt on the RST 7.5 line whereby the three-state buffer is activated and the microprocessor takes control of DMC. Table 4 shows a procedure for using the AD7555 in this mode. Figure 10 shows the basic hookup.

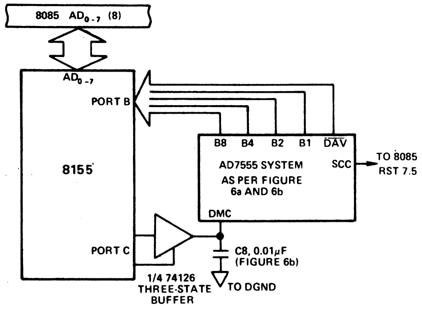


Figure 10. AD7555 as an Interrupting Input Device (MCS-85 System)

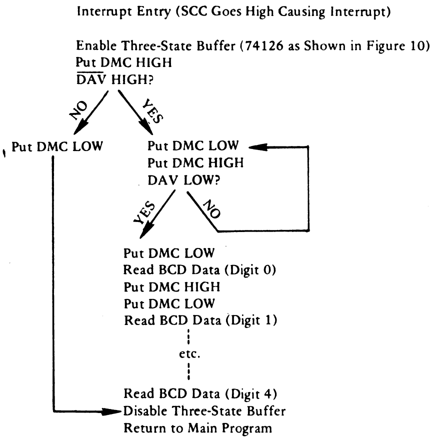
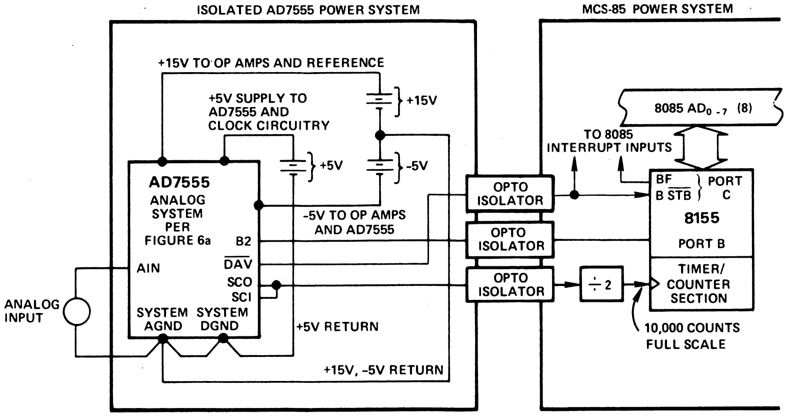


Table 4. Procedure for Interfacing the AD7555 as an Interrupting Input Device

OPTO-ISOLATED SERIAL INTERFACE

Figure 11 shows a serial interface to the MCS-85 system. This system can accommodate a remote interface where a common-mode voltage is expected to exist between system grounds. The 8155 counter/timer is only 14 bits long, i.e., it can only count down from 2^{14}; therefore SCO output from the AD7555 (20k counts full scale) has to be divided by 2 with consequent reduction in system resolution.

Port C of the 8155 is configured as a control port. Port B is an input port. This port configuration is necessary if sign information is required. Magnitude information is obtained by interrogating the 8155 counter value. The rising edge of $\overline{\text{DAV}}$ is used to cause an interrupt on the RST 7.5 line. The value $\left(2^{14} - \left|\frac{\text{SCO}}{2}\right|\right)$ in the 8155 counter should now be read. When $\overline{\text{DAV}}$ returns low the 8155 counter is reset to FF_H. Sign information is checked at this time since $\overline{D_0}$ BCD data is present and stable on the BCD bus (see Figure 9). The B2 line of the BCD bus is latched into port B by the signal on $\overline{\text{B STB}}$ i.e. the falling edge of $\overline{\text{DAV}}$. This causes a rising edge signal on BF (buffer full) to call the 8085 CPU to read the B2 bit. B2 bit is HIGH for negative data, LOW for positive data.



NOTE:
SYSTEM RESOLUTION CAN BE INCREASED BY PROVIDING SUFFICIENT COUNTER CAPACITY TO TOTALIZE 20k (OR 200k) COUNTS.

Figure 11. Optically Isolated Serial AD7555/MCS-85 Interface (Full Scale = 10,000 Counts)

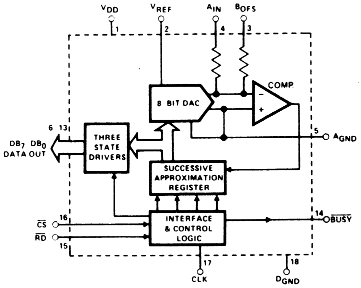
ANALOG DEVICES

CMOS
μP Compatible 8-Bit ADC

AD7574

FEATURES
8-Bit Resolution
No Missed Codes over Full Temperature Range
Fast Conversion Time: 15μs
Interfaces to μP like RAM, ROM or Slow-Memory
Low Power Dissipation: 30mW
Ratiometric Capability
Single +5V Supply
Low Cost
Internal Comparator and Clock Oscillator

AD7574 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

AD7574 is a low-cost, 8-bit μP compatible ADC which uses the successive-approximations technique to provide a conversion time of 15μs.

Designed to be operated as a memory mapped input device, the AD7574 can be interfaced like static RAM, ROM, or slow memory. It's $\overline{CS}$ (decoded device address) and $\overline{RD}$ ($\overline{READ/WRITE}$ control) inputs are available in all μP memory systems. These two inputs control all ADC operations such as starting conversion or reading data. The ADC output data bits use three-state logic, allowing direct connection to the μP data bus or system input port.

Internal clock, +5V operation, on-board comparator and interface logic, as well as low power dissipation (30mW) and fast conversion time make the AD7574 ideal for most ADC/μP interface applications. Small size (18-pin DIP) and monolithic reliability will find wide use in avionics, instrumentation, and process automation applications.

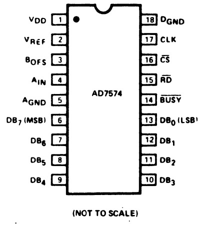
ORDERING INFORMATION

Differential Nonlinearity	Temperature Range and Package[1]		
	Plastic (N18B) 0 to +70°C	Ceramic (D18B) -25°C to +85°C	Ceramic (D18B) -55°C to +125°C
±7/8LSB	AD7574JN	AD7574AD[2]	AD7574SD[2]
±3/4LSB	AD7574KN	AD7574BD[2]	AD7574TD[2]

[1] See Section 20 for package outline information.

[2] Available 100% screened to MIL-STD-883, Class B. To order, add "/883B" to part number shown. See note 1, next page for details.

PIN CONFIGURATION



18-PIN DIP
TOP VIEW

CAUTION:

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The foam should be discharged to the destination socket before devices are removed.

WARNING!

ESD SENSITIVE DEVICE

DC SPECIFICATIONS ($V_{DD} = +5V$, $V_{REF} = -10V$, Unipolar Configuration, $R_{CLK} = 180k\Omega$, $C_{CLK} = 100pF$, unless otherwise noted)

PARAMETER	LIMITS		UNITS	CONDITIONS/COMMENTS
	$T_A = +25°C$	T_{min}, T_{max}[1]		
ACCURACY				
Resolution	8	8	Bits	
Relative Accuracy Error				
AD7574JN, AD, SD	±3/4	±3/4	LSB max	
AD7574KN, BD, TD	±1/2	±1/2	LSB max	Relative Accuracy and Differential Nonlinearity are measured dynamically using the external clock circuit of Fig. 7b. Clock frequency is 500kHz (conversion time 15μs)
Differential Nonlinearity				
AD7574JN, AD, SD	±7/8	±7/8	LSB max	
AD7574KN, BD, TD	±3/4	±3/4	LSB max	
Full Scale Error (Gain Error)				Full Scale Error is measured after calibrating out offset error. See Fig. 8a and associated calibration procedure for offset. Max Full Scale change from +25°C to T_{min} or T_{max} is ±2 LSB.
AD7574JN, AD, SD	±5	±6.5	LSB max	
AD7574KN, BD, TD	±3	±4.5	LSB max	
Offset Error[2]				
AD7574JN, AD, SD	±60	±80	mV max	Maximum Offset change from +25°C to T_{min} or T_{max} is ±20mV.
AD7574KN, BD, TD	±30	±50	mV max	
Mismatch Between B_{OFS} (pin 3) and A_{IN} (pin 4) Resistances[3]	±1.5	±1.5	%	
ANALOG INPUTS				
Input Resistance				
At V_{REF} (pin 2)	5/10/15	5/10/15	kΩ min/typ/max	
At B_{OFS} (pin 3)	10/20/30	10/20/30	kΩ min/typ/max	
At A_{IN} (pin 4)	10/20/30	10/20/30	kΩ min/typ/max	
V_{REF} (for specified performance)	-10	-10	V	±5% for specified transfer accuracy.
V_{REF} Range[4]	-5 to -15	-5 to -15	V	Degraded transfer accuracy.
Nominal Analog Input Range				
Unipolar Mode	0 to $+\lvert V_{REF}\rvert$		V	
Bipolar Mode	$-\lvert V_{REF}\rvert$ to $+\lvert V_{REF}\rvert$		V	
LOGIC INPUTS				
$\overline{RD}$ (pin 15), $\overline{CS}$ (pin 16)				
V_{INH} Logic HIGH Input Voltage	+3.0	+3.0	V min	
V_{INL} Logic LOW Input Voltage	+0.8	+0.8	V max	
I_{IN} Input Current	1	10	μA max	$V_{IN} = 0V, V_{DD}$
C_{IN} Input Capacitance[5]	5	5	pF max	
CLK (pin 17)				
V_{INH} Logic HIGH Input Voltage	+3.0	+3.0	V min	
V_{INL} Logic LOW Input Voltage	+0.4	+0.4	V max	
I_{INH} Logic HIGH Input Current	+2	+3	mA max	During Conversion: $V_{IN(CLK)} \geqslant V_{INH(CLK)}$
I_{INL} Logic LOW Input Current	1	10	μA max	During Conversion: $V_{IN(CLK)} \leqslant V_{INL(CLK)}$ (see circuit of Fig. 7b if external clock operation is required).
LOGIC OUTPUTS				
BUSY (pin 14), DB_7 to DB_0 (pins 6-13)				
V_{OH} Output HIGH Voltage	+4.0	+4.0	V min	$I_{SOURCE} = 40\mu A$
V_{OL} Output LOW Voltage	+0.4	+0.8	V max	$I_{SINK} = 1.6mA$
I_{LKG} DB_7 to DB_0 Floating Stage Leakage	1	10	μA max	$V_{OUT} = 0V$ or V_{DD}
Floating State Output Capacitance (DB_7 to DB_0)[5]	7	7	pF max	
Output Code	Unipolar Binary, Offset Binary			See Figs. 8a, 9a, 10a and 8b, 9b, 10b.
POWER REQUIREMENTS				
V_{DD}	+5	+5	V	±5% for specified performance.
I_{DD} (STANDBY)	5	5	mA max	$A_{IN} = 0V$, ADC in RESET condition.
I_{REF}	V_{REF} divided by 5kΩ		max	Conversion complete, prior to RESET.

NOTES:

[1] Temperature ranges as follows: JN, KN (0 to +70°C)
AD, BD (-25°C to +85°C)
SD, TD (-55°C to +125°C)

Screening to MIL-STD-883 is available./883B versions are 100% screened to method 5004 for a class B device. Final electrical tests are performed to +25°C and +85°C (AD, BD versions) or +25°C and +125°C (SD, TD versions).

[2] Typical offset temperature coefficient is ±150μV/°C.

[3] R_{BOFS}/R_{AIN} mismatch causes transfer function rotation about positive Full Scale. The effect is an offset and a gain term when using the circuit of Figure 9a.

[4] Typical value, not guaranteed or subject to test.

[5] Guaranteed but not tested.

Specifications subject to change without notice.

AC Specifications

(V_{DD} = +5V, C_{CLK} = 100pF, R_{CLK} = 180kΩ unless otherwise noted)

SYMBOL	SPECIFICATION	LIMIT at T_A = +25°C	LIMIT at $T_A = T_{min}$	LIMIT at $T_A = T_{max}$	CONDITIONS
STATIC RAM INTERFACE MODE (See Figure 1 and Table 1)					
t_{CS}	$\overline{\text{CS}}$ Pulse Width Requirement	100ns min	150ns min	150ns min	
t_{WSCS}	$\overline{\text{RD}}$ to $\overline{\text{CS}}$ Setup Time	0 min	0 min	0 min	
t_{CBPD}	$\overline{\text{CS}}$ to $\overline{\text{BUSY}}$ Propagation Delay	90ns typ 120ns max	70ns typ 120ns max	150ns typ 180ns max	$\overline{\text{BUSY}}$ Load = 20pF
		120ns typ 150ns max	100ns typ 150ns max	180ns typ 200ns max	$\overline{\text{BUSY}}$ Load = 100pF
t_{BSR}	$\overline{\text{BUSY}}$ to $\overline{\text{RD}}$ Setup Time	0 min	0 min	0 min	
t_{BSCS}	$\overline{\text{BUSY}}$ to $\overline{\text{CS}}$ Setup Time	0 min	0 min	0 min	
t_{RAD}	Data Access Time	120ns typ 150ns max	100ns typ 150ns max	180ns typ 220ns max	DB_0 - DB_7 Load = 20pF
		240ns typ 300ns max	220ns typ 300ns max	300ns typ 400ns max	DB_0 - DB_7 Load = 100pF
t_{RHD}	Data Hold Time	80ns typ 50ns min 120ns max	40ns typ 30ns min 80ns max	120ns typ 80ns min 180ns max	
t_{RHCS}	$\overline{\text{CS}}$ to $\overline{\text{RD}}$ Hold Time	250ns max	200ns max	500ns max	
t_{RESET}	Reset Time Requirement	3µs min	3µs min	3µs min	
$t_{CONVERT}$	Conversion Time using internal clock oscillator	See typical data of Figure 7a			
$t_{CONVERT}$	Conversion Time using external clock	15µs	15µs	15µs	f_{CLK} = 500kHz circuit of Figure 7b
ROM INTERFACE MODE (See Figure 2 and Table 2)					
t_{RAD}	Data Access Time	Same as RAM Mode			
t_{RHD}	Data Hold Time	Same as RAM Mode			
t_{WBPD}	$\overline{\text{RD}}$ HIGH to $\overline{\text{BUSY}}$ Propagation Delay	400ns typ 1.5µs max	350ns typ 1.0µs max	1µs typ 2.0µs max	$\overline{\text{BUSY}}$ Load = 20pF
t_{BSR}	$\overline{\text{BUSY}}$ to $\overline{\text{RD}}$ LOW Setup Time	$\overline{\text{RD}}$ can go LOW prior to $\overline{\text{BUSY}}$ = HIGH, but must not return HIGH until $\overline{\text{BUSY}}$ = HIGH. See Table 2			
$t_{CONVERT}$	Conversion Time using internal clock oscillator	See typical data of Figure 7a. Add 2µs to data shown in Figure 7a for ROM Mode			
SLOW – MEMORY INTERFACE MODE (See Figure 3 and Table 3)					
t_{CBPD}	$\overline{\text{CS}}$ to $\overline{\text{BUSY}}$ Propagation Delay	Same as RAM Mode			
t_{RESET}	Reset Time Requirement	Same as RAM Mode			
t_{RAD}	Data Access Time	Same as RAM Mode			
t_{RHD}	Data Hold Time	Same as RAM Mode			
$t_{CONVERT}$	Conversion Time	Same as RAM Mode			

ABSOLUTE MAXIMUM RATINGS

V_{DD} to A_{GND}	0V, +7.0V
V_{DD} to D_{GND}	0V, +7.0V
A_{GND} to D_{GND}	-0.3V, V_{DD}
Digital Input Voltage to D_{GND} (pins 15 and 16)	-0.3V, +15.0V
Digital Output Voltage to D_{GND} (pins 6 - 14)	-0.3V, V_{DD}
CLK Input Voltage (pin 17) to D_{GND}	-0.3V, V_{DD}
V_{REF} (pin 2)	±20V
V_{BOFS} (pin 3)	±20V
V_{AIN} (pin 4)	±20V

Operating Temperature Range	
JN, KN	0°C to +70°C
AD, BD	-25°C to +85°C
SD, TD	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10 secs.)	+300°C
Power Dissipation (Package)	
Plastic (suffix N)	
to +70°C	670mW
Derate above +70°C by	8.3mw/°C
Ceramic (suffix D)	
to +75°C	450mW
Derate above +75°C by	6mW/°C

TERMINOLOGY

RESOLUTION: Resolution is a measure of the *nominal* analog change required for a 1 - bit change in the A/D converter's digital output. While normally expressed in a number of bits, the analog resolution of an n - bit unipolar A/D converter is $(2^{-n})(V_{REF})$. Thus the AD7574, an 8 - bit A/D converter, can resolve analog voltages as small as $(1/256)(V_{REF})$ when operated in a unipolar mode. When operated in a bipolar mode, the resolution is $(1/128)(V_{REF})$. Resolution does not imply accuracy. *Usable* resolution is limited by the differential nonlinearity of the A/D converter.

RELATIVE ACCURACY: Relative accuracy is the deviation of the ADC's actual code transition points from a straight line drawn between the device's measured zero and measured full scale transition points. Relative accuracy, therefore, is a measure of code *position*.

DIFFERENTIAL NONLINEARITY: Differential nonlinearity in an ADC is a measure of the size of an analog voltage range associated with any digital output code. As such differential nonlinearity specifies code width (usable resolution). An ADC with a specified differential nonlinearity of ±n bits will exhibit codes ranging in width from 1LSB - nLSB to 1LSB + nLSB. A specified differential nonlinearity of less than ±1LSB guarantees no - missing - codes operation.

TIMING & CONTROL OF THE AD7574

STATIC RAM INTERFACE MODE

Table 1 and Figure 1 show the truth table and timing requirements for AD7574 operation as a static RAM.

A convert start is initiated by executing a memory WRITE instruction to the address location occupied by the AD7574 (once conversion has started, subsequent memory WRITES have no effect). A data READ is performed by executing a memory READ instruction to the AD7574 address location.

$\overline{\text{BUSY}}$ must be HIGH before a data READ is attempted, i.e. the total delay between a convert start and a data READ must be at least as great as the AD7574 conversion time. The delay can be generated by inserting NOP instructions (or other program instructions) between the WRITE (start convert) and READ (read data) operations. Once $\overline{\text{BUSY}}$ is HIGH (conversion complete), a data READ is performed by executing a memory READ instruction to the address location occupied by the AD7574. The data readout is destructive, i.e. when RD returns HIGH, the converter is internally reset.

The RAM interface mode uses distinctly different commands to start conversion (memory WRITE) or read the data (memory READ). This is in contrast to the ROM mode where a memory READ causes a data READ *and* a conversion restart.

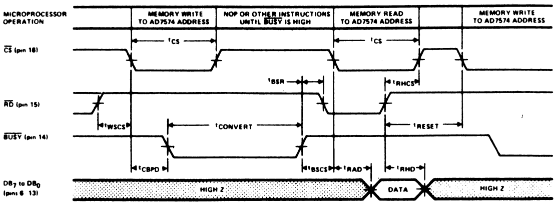


Figure 1. Static RAM Mode Timing Diagram

AD7574 INPUTS		AD7574 OUTPUTS		AD7574 OPERATION
$\overline{\text{CS}}$	$\overline{\text{RD}}$	$\overline{\text{BUSY}}$	$DB_7 - DB_0$	
L	H	H	HIGH Z	WRITE CYCLE (START CONVERT)
L	↓	H	HIGH Z → DATA	READ CYCLE (DATA READ)
L	↑	H	DATA → HIGH Z	RESET CONVERTER
H	X^1	X	HIGH Z	NOT SELECTED
L	H	L	HIGH Z	NO EFFECT, CONVERTER BUSY
L	↓	L	HIGH Z	NO EFFECT, CONVERTER BUSY
L	↑	L	HIGH Z	NOT ALLOWED, CAUSES INCORRECT CONVERSION

Note 1: If $\overline{\text{RD}}$ goes LOW to HIGH when $\overline{\text{CS}}$ is LOW, the ADC is internally reset. $\overline{\text{RD}}$ has no effect while $\overline{\text{CS}}$ is HIGH. See application hint No. 1.

Table 1. Truth Table, Static RAM Mode

ROM INTERFACE MODE

Table 2 and Figure 2 show the truth table and timing requirements for interfacing the AD7574 like Read Only Memory.

$\overline{\text{CS}}$ is held LOW and converter operation is controlled by the $\overline{\text{RD}}$ input. The AD7574 $\overline{\text{RD}}$ input is derived from the decoded device address. MEMRD should be used to enable the address decoder in 8080 systems. VMA should be used to enable the address decoder in 6800 systems. A data READ is initiated by executing a memory READ instruction to the AD7574 address location. The converter is automatically restarted when $\overline{\text{RD}}$ returns HIGH. As in the RAM mode, attempting a data READ before $\overline{\text{BUSY}}$ is HIGH will result in incorrect data being read.

The advantage of the ROM mode is its simplicity. The major disadvantage is that the data obtained is relatively poorly defined in time inasmuch as executing a data READ automatically starts a new conversion. This problem can be overcome by executing two READs separated by NO-OPS (or other program instructions) and using only the data obtained from the second READ.

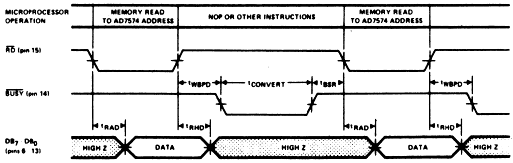


Figure 2. ROM Mode Timing Diagram ($\overline{\text{CS}}$ Held LOW)

AD7574 INPUTS		AD7574 OUTPUTS		AD7574 OPERATION
$\overline{\text{CS}}$	$\overline{\text{RD}}$	$\overline{\text{BUSY}}$	$DB_7 - DB_0$	
L	↓	H	HIGH Z → DATA	DATA READ
L	↑	↓	DATA → HIGH Z	RESET AND START NEW CONVERSION
L	↓	L	HIGH Z	NO EFFECT, CONVERTER BUSY
L	↑	L	HIGH Z	NOT ALLOWED, CAUSES INCORRECT CONVERSION

Table 2. Truth Table, ROM Mode

SLOW-MEMORY INTERFACE MODE

Table 3 and Figure 3 show the truth table and timing requirements for interfacing the AD7574 as a slow-memory. This mode is intended for use with processors which can be forced into a WAIT state for at least 12μs (such as the 8080, 8085 and SC/MP). The major advantage of this mode is that it allows the μP to start conversion, WAIT, and then READ data with a single READ instruction.

In the slow-memory mode, $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are tied together. It is suggested that the system ALE signal (8085 system) or SYNC signal (8080 system) be used to latch the address. The decoded device address is subsequently used to drive the AD7574 $\overline{\text{CS}}$ and $\overline{\text{RD}}$ inputs. $\overline{\text{BUSY}}$ is connected to the microprocessor READY input.

When the AD7574 is NOT addressed, the $\overline{\text{CS}}$ and $\overline{\text{RD}}$ inputs are HIGH. Conversion is initiated by executing a memory READ to the AD7574 address. $\overline{\text{BUSY}}$ subsequently goes LOW (forcing the μP READY input LOW) placing the μP in a WAIT state. When conversion is complete ($\overline{\text{BUSY}}$ is HIGH) the μP completes the memory READ.

Do not attempt to perform a memory WRITE in this mode, since three-state bus conflicts will arise.

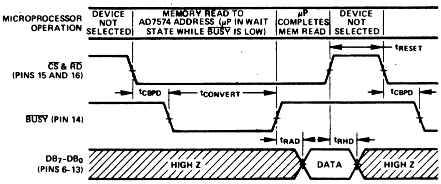


Figure 3. Slow Memory Mode Timing Diagram ($\overline{CS}$ and $\overline{RD}$ Tied Together)

AD7574 INPUTS	AD7574 OUTPUTS		AD7574 OPERATION
$\overline{CS}$ & $\overline{RD}$	$\overline{BUSY}$	DB_7 - DB_0	
H	H	HIGH Z	NOT SELECTED
↓	H → L	HIGH Z	START CONVERSION
L	L	HIGH Z	CONVERSION IN PROGRESS, μP IN WAIT STATE
L	↑	HIGH Z → DATA	CONVERSION COMPLETE, μP READS DATA
↑	H	DATA → HIGH Z	CONVERTER RESET AND DESELECTED
H	H	HIGH Z	NOT SELECTED

Table 3. Truth Table, Slow Memory Mode

GENERAL CIRCUIT INFORMATION

BASIC CIRCUIT DESCRIPTION

The AD7574 uses the successive approximations technique to provide an 8-bit parallel digital output. The control logic was designed to provide easy interface to most microprocessors. Most applications require only passive clock components (R & C), a -10V reference, and +5V power.

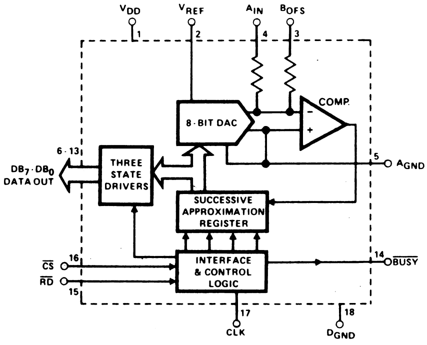


Figure 4. AD7574 Functional Diagram

Figure 4 shows the AD7574 functional diagram. Upon receipt of a start command either via the $\overline{CS}$ or $\overline{RD}$ pins for Control Logic and Timing Details), $\overline{BUSY}$ goes low indicating conversion is in progress. Successive bits, starting with the most significant bit (MSB), are applied to the input of a DAC. The comparator determines whether the addition of each successive bit causes the DAC output to be greater than or less than the analog input, A_{IN}. If the sum of the DAC bits is less than A_{IN}, the trial bit is left ON, and the next smaller bit is tried. If the sum is greater than A_{IN}, the trial bit is turned OFF and the next smaller bit is tried. Each successively smaller bit is tried and compared to A_{IN} in this manner until the least significant bit (LSB) decision has been made. At this time $\overline{BUSY}$ goes HIGH (conversion is complete) indicating the successive approximation register contains a valid representation of the analog input. The $\overline{RD}$ control (see the previous page for details) can then be exercised to activate the three-state buffers, placing data on the DB_0 - DB_7 data output pins. $\overline{RD}$ returning HIGH causes the clock oscillator to run for 1 cycle, providing an internal ADC reset (i.e. the SAR is loaded with code 10000000).

DAC CIRCUIT DETAILS

The current weighting D/A converter is a precision multiplying DAC. Figure 5 shows the functional diagram of the DAC as used in the AD7574. It consists of a precision Silicon Chromium thin film R/2R ladder network and 8 N-channel MOSFET switches operated in single-pole-double-throw.

The currents in each 2R shunt arm are binarily weighted, i.e. the current in the MSB arm is V_{REF} divided by 2R, in the second arm is V_{REF} divided by 4R, etc. Depending on the DAC logic input (A/D output) from the successive approximation register, the current in the individual shunt arms is steered either to A_{GND} or to the comparator summing point.

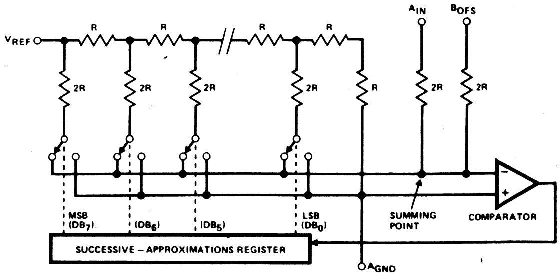


Figure 5. D/A Converter As Used In AD7574

OPERATING THE AD7574

APPLICATION HINTS

1. TIMING & CONTROL
   In the AD7574 when a conversion is finished the fresh data must be read before a new conversion can be started.
   Failure to observe the timing restrictions of Figures 1, 2 or 3 may cause the AD7574 to change interface modes. For example, in the RAM mode, holding $\overline{CS}$ LOW too long after $\overline{RD}$ goes HIGH will cause a new convert start (i.e. the converter moved into the ROM mode).
2. LOGIC DEGLITCHING IN uP APPLICATIONS
   Unspecified states on the address bus (due to different rise and fall times on the address bus) can cause glitches at the AD7574 $\overline{CS}$ or $\overline{RD}$ terminals. These glitches can cause unwanted convert starts, reads, or resets. The best way to avoid glitches is to gate the address decoding logic with RD or WR (8080) or VMA (6800) when in the ROM or RAM mode. When in the slow-memory mode, the ALE (8085) or SYNC (8080) signal should be used to latch the address.
3. INPUT LOADING AT V_{REF}, A_{IN} AND B_{OFS}
   To prevent loading errors due to the finite input resistance at the V_{REF}, A_{IN} or B_{OFS} pins, low impedance driving sources must be used (i.e. op amp buffers or low output-Z reference).
4. RATIOMETRIC OPERATION
   Ratiometric performance is inherent to A/D converters such as the AD7574 which use a multiplying DAC weighting network. However, the user should recognize that comparator limitations such as offset voltage, input noise and gain will cause degradation of the transfer characteristics when operating with reference voltages less than -10V in magnitude.
5. OFFSET CORRECTION
   Offset error in the transfer characteristic can be trimmed by offsetting the buffer amplifier which drives the AD7574 A_{IN} pin (pin 4). This can be done either by summing a cancellation current into the amplifier's summing junction, or by tapping a voltage divider which sits between V_{DD} and V_{REF} and applying the tap voltage to the amplifier's positive input (an example of a resistive tap offset adjust is shown in Figure 10a where R_8, R_9 and R_{10} can be used to offset the ADC).
6. ANALOG AND DIGITAL GROUND
   It is recommended that A_{GND} and D_{GND} be connected locally to prevent the possibility of injecting noise into the AD7574. In systems where the A_{GND}-D_{GND} intertie is not local, connect back-to-back diodes (IN914 or equivalent) between the AD7574 A_{GND} and D_{GND} pins.
7. INITIALIZATION AFTER POWER – UP
   Execute a memory READ to the AD7574 address location, and subsequently ignore the data. The AD7574 is internally reset when reading out data, i.e. the data readout is destructive.

CLOCK OSCILLATOR

The AD7574 has an internal asynchronous clock oscillator which starts upon receipt of a convert start command, and ceases oscillating when conversion is complete.

The clock oscillator requires an external R and C as shown in Figure 6. Nominal conversion time versus R_{CLK} and C_{CLK} is shown in Figure 7a. The curves shown in Figure 7a are applicable when operating in the RAM or slow-memory interface modes. When operating in the ROM interface mode, add 2μs to the typical conversion time values shown.

The AD7574 is guaranteed to provide transfer accuracy to published specifications for conversion times down to 15μs, as indicated by the unshaded region of Figure 7a. Conversion times faster than 15μs can cause transfer accuracy degradation.

OPERATION WITH EXTERNAL CLOCK

For applications requiring a conversion time close to or equal to 15μs, an external clock is recommended. Using an external clock precludes the possibility of converting faster than 15μs (which can cause transfer accuracy degradation) due to temperature drift – as may be the case when using the internal clock oscillator.

Figure 7b shows how the external clock must be connected. The $\overline{BUSY}$ output of the AD7574 is connected to the three-state enable input of a 74125 three-state buffer. R_1 is used as a pullup, and can be between 6kΩ and 100kΩ. A 500kHz clock will provide a conversion time of 15μs.

The external clock should be used only in the static-RAM or slow-memory interface mode, and *not* in the ROM mode.

Timing constraints for external clock operation are as follows:

STATIC RAM MODE

1. When initiating a conversion, $\overline{CS}$ should go LOW on a positive clock edge to provide optimum settling time for the MSB.
2. A data READ can be initiated any time after BUSY = 1.

SLOW-MEMORY MODE

1. When initiating a conversion, $\overline{CS}$ and $\overline{RD}$ should go LOW on a positive clock edge to provide optimum settling time for the MSB.

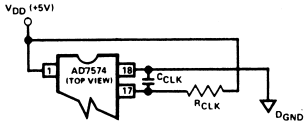


Figure 6. Connecting R_{CLK} and C_{CLK} To CLK Oscillator

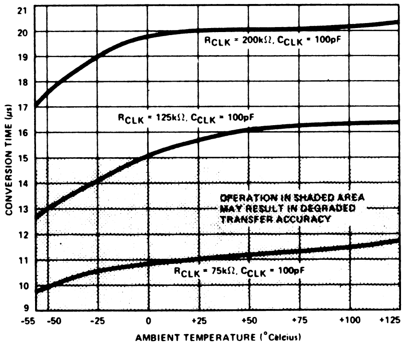


Figure 7a. Typical Conversion Time vs. Temperature For Different R_{CLK} and C_{CLK} (Applicable to RAM and Slow-Memory Modes. For ROM Mode add 2μs to values shown)

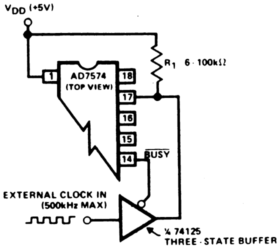


Figure 7b. External Clock Operation (Static RAM and Slow-Memory Mode)

UNIPOLAR BINARY OPERATION

Figures 8a and 8b show the analog circuit connections and typical transfer characteristic for unipolar operation. An AD584 is used as the -10V reference.

Calibration is as follows:

OFFSET

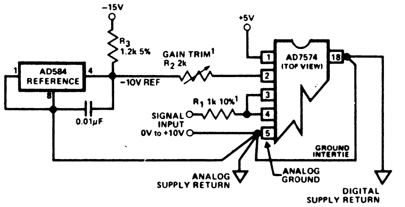
Offset must be trimmed out in the signal conditioning circuitry used to drive the signal input terminals shown in Figure 8a. An example of an offset trim is shown in Figure 10a, where R_8, R_9 and R_{10} comprise a simple voltage tap which is applied to the amplifier's positive input.

1. Apply -39.1mV (1 LSB) to the input of the buffer amplifier used to drive R_1 (i.e. +39.1mV at R_1).
2. While performing continuous conversions, adjust the offset potentiometer (described above) until DB_7 - DB_1 are LOW and the LSB (DB_0) flickers.

GAIN (FULL SCALE)

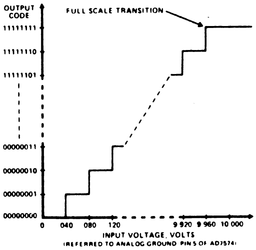
Offset adjustment must be performed before gain adjustment.

1. Apply -9.961V to the input of the buffer amplifier used to drive R_1 (i.e. +9.961V at R_1).
2. While performing continuous conversions, adjust trim pot R_2 until DB_7 - DB_1 are HIGH and the LSB (DB_0) flickers.



Note 1: R_1 and R_2 can be omitted if gain trim is not required

Figure 8a. AD7574 Unipolar (0V to +10V) Operation (Output Code is Straight Binary)



Note: Approximate bit weights are shown for illustration. Nominal bit weight for a -10V reference is ≈ 39.1mV

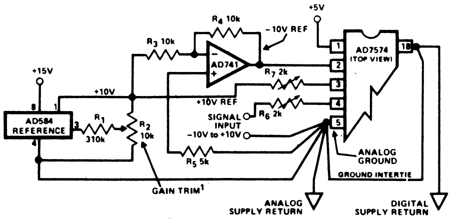
Figure 8b. Nominal Transfer Characteristic For Unipolar Circuit of Figure 8a

BIPOLAR (OFFSET BINARY) OPERATION

Figures 9a and 9b illustrate the analog circuitry and transfer characteristic for bipolar operation. Output coding is offset binary. As in unipolar operation, offset correction can be performed at the buffer amplifier used to drive the signal input terminals of Figure 9a (Resistors R_8, R_9 and R_{10} in Figure 10a show how offset trim can be done at the buffer amplifier).

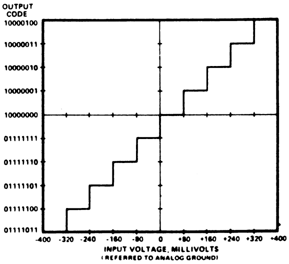
Calibration is as follows:

1. Adjust R_6 and R_7 for minimum resistance across the potentiometers.
2. Apply +10.000V to the buffer amplifier used to drive the signal input (i.e. -10.000V at R_6).
3. While performing continuous conversions, trim R_6 or R_7 (whichever required) until DB_7 - DB_1 are LOW and the LSB (DB_0) flickers.
4. Apply 0V to the buffer amplifier used to drive the signal input terminals.
5. Doing continuous conversions, trim the offset circuit of the buffer amplifier until the ADC output code flickers between 01111111 and 10000000.
6. Apply +10.000V to the input of the buffer amplifier (i.e. -10.000V as applied to R_6).
7. Doing continuous conversions, trim R_2 until DB_7 - DB_1 are LOW and the LSB (DB_0) flickers.
8. Apply -9.922V to the input of the buffer amplifier (i.e. +9.922V at the input side of R_6).
9. If the ADC output code is not 11111110 ±1 bit, repeat the calibration procedure.



Note 1: R_1 and R_2 can be omitted if gain trim is not required

Figure 9a. AD7574 Bipolar (-10V to +10V) Operation (Output Code is Offset Binary)



Note: Approximate bit weights are shown for illustration. Nominal bit weight for ± 10V full scale is ≈ 78.1mV

Figure 9b. Nominal Transfer Characteristic Around Major Carry for Bipolar Circuit of Figure 9a

OPERATING THE AD7574

BIPOLAR (COMPLEMENTARY OFFSET BINARY) OPERATION

Figure 10a shows the analog connections for complementary offset binary operation. The typical transfer characteristic is shown in Figure 10b. In this bipolar mode, the ADC is fooled into believing it is operated in a unipolar mode - i.e. the +10V to -10V analog input is conditioned into a 0 to +10V signal range. R_2 is the gain adjust, while R_9 is the offset adjust.

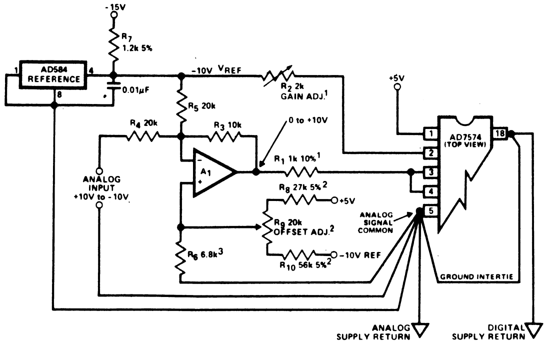
Calibration is as follows (adjust offset before gain):

OFFSET

1. Apply OV to the analog input shown in Figure 10a.
2. While performing continuous conversions, adjust R_9 until the converter output flickers between codes 01111111 and 10000000.

GAIN (FULL SCALE)

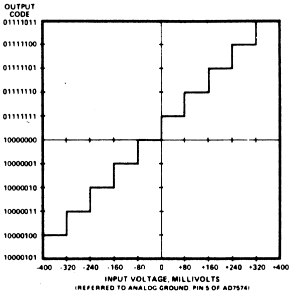
1. Apply -9.922V across the analog input terminals shown in Figure 10a.
2. While performing continuous conversions, adjust R_2 until DB_7 - DB_1 are HIGH and the LSB (DB_0) flickers between HIGH and LOW.



Notes:

1. R_1 and R_2 can be omitted if gain trim is not required
2. R_8, R_9 and R_{10} can be omitted if offset trim is not required
3. $R_6||R_8||R_{10} = 5k\Omega$. If R_8, R_9 and R_{10} not used, make $R_6 = 5k\Omega$

Figure 10a. AD7574 Bipolar Operation (-10V to +10V) (Output Code is Complementary Offset Binary)



Note: Approximate bit weights are shown for illustration. Nominal bit weight for ±10V full scale is ≈78.1mV

Figure 10b. Nominal Transfer Characteristic Around Major Carry for Bipolar Circuit of Figure 10a

ANALOG DEVICES

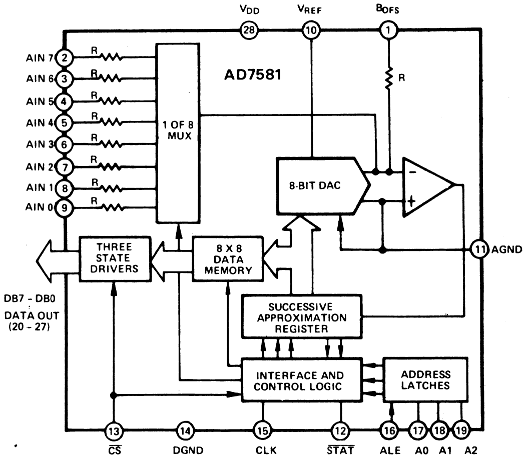
CMOS µP Compatible 8-Bit 8-Channel DAS

AD7581

FEATURES

- 8-Bit Resolution
- On-Chip 8 X 8 Dual-Port Memory
- No Missed Codes Over Full Temperature Range
- Interfaces Directly to Z80/8085/6800
- CMOS, TTL Compatible Digital Inputs
- Three-State Data Drivers
- Ratiometric Capability
- Interleaved DMA Operation
- Fast Conversion
- A/D Process Totally Transparent to µP
- Low Cost

AD7581 FUNCTIONAL BLOCK DIAGRAM

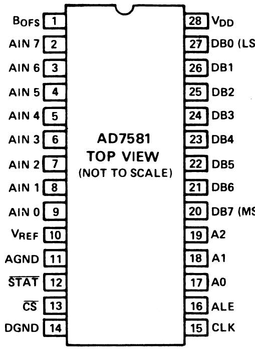


GENERAL DESCRIPTION

The AD7581 is a microprocessor compatible 8 bit, 8 channel, memory buffered, data-acquisition system on a monolithic CMOS chip. It consists of an 8 bit successive approximation A/D converter, an 8 channel multiplexer, 8 X 8 dual-port RAM, three-state DATA drivers (for interface), address latches and microprocessor compatible control logic. The device interfaces directly to 8080, 8085, Z80, 6800 and other microprocessor systems.

The successive approximation conversion takes place on a continuous, channel sequencing, basis using microprocessor control signals for the clock. Data is automatically transferred to its proper location in the 8 X 8 dual-port RAM at the end of each conversion. When under microprocessor control, a READ DATA operation is allowed at any time for any channel since on-chip logic provides interleaved DMA. The facility to latch the address inputs (A_0 - A_2) with ALE enables the AD7581 to interface with µP systems which feature either shared or separate address and data buses.

PIN CONFIGURATION



ORDERING INFORMATION

Differential Nonlinearity	Temperature Range 0 to +70°C	 -25°C to +85°C
±1 7/8LSB	AD7581JN	AD7581AD
±7/8LSB	AD7581KN	AD7581BD
±3/4LSB	AD7581LN	AD7581CD

PACKAGE IDENTIFICATION[1]

Suffix D: Ceramic DIP – (D28B)
Suffix N: Plastic DIP – (N28A)

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[1] See Section 20 for package outline information.

DC SPECIFICATIONS (V_{DD} = +5V, V_{REF} = -10V, Unipolar Operation, unless otherwise stated)

Parameter	Version[1]	Typical at +25°C	Limit Over Temperature	Units	Conditions/Comments
ACCURACY					
Resolution	All	8	8	Bits	
Relative Accuracy	JN, AD	±1 7/8	±1 7/8 max	LSB	
	KN, BD	±3/4	±3/4 max	LSB	
	LN, CD	±1/2	±1/2 max	LSB	
Differential Nonlinearity	JN, AD	±1 7/8	±1 7/8 max	LSB	
	KN, BD	±7/8	±7/8 max	LSB	
	LN, CD	±3/4	±3/4 max	LSB	
Offset Error[2]	JN, AD	200	200 max	mV	Adjustable to zero, see Figure 7a.
	KN, BD	80	80 max	mV	
	LN, CD	50	50 max	mV	
Gain Error					
Worst Channel	JN, AD	±3	±6 max	LSB	Adjustable to zero, see Figure 7a.
	KN, BD	±2	±4 max	LSB	Gain Error is Measured After Offset Calibration. Max Full Scale Change for Any Channel from +25°C to T_{min} or T_{max} is ±2LSB.
	LN, CD	±1	±2 max	LSB	
Gain Match Between Channels	JN, AD	2	3 max	LSB	Adjustable to zero, see Figure 7a.
	KN, BD	1 1/2	2 max	LSB	
	LN, CD	1	1 max	LSB	
B_{OFS} Gain Error	All	-2 1/2	–	LSB	
ANALOG INPUTS					
Input Resistance					
At V_{REF} (pin 10)	All	10/20/30	10/20/30	kΩ min/typ/max	
At B_{OFS} (pin 1)[3]	All	10/20/30	10/20/30	kΩ min/typ/max	
At Any Analog Input (pins 2-9)	All	10/20/30	10/20/30	kΩ min/typ/max	
V_{REF} (For Specified Performance)	All	-10	-10	V	±5%
V_{REF} Range[4]	All	-5 to -15	-5 to -15	V	
Nominal Analog Input Range					
Unipolar Mode	All	0 to $+V_{REF}$,	0 to $+V_{REF}$	V	See Figure 7 and 8.
		0 to $-V_{REF}$	0 to $-V_{REF}$	V	
Bipolar Mode	All	$-V_{BOFS} \leqslant V_{AIN} \leqslant \lvert V_{REF} \rvert - V_{BOFS}$			See Figure 9
DIGITAL INPUTS					
$\overline{CS}$ (pin 13), ALE (pin 16), A_0 - A_2 (pins 17-19), CLK (pin 15)					
V_{INH} Logic HIGH Input Voltage	All	+2.2	+2.4 min	V	
V_{INL} Logic LOW Input Voltage	All	+0.4	+0.8 max	V	
I_{IN} Input Current	All	0.01	1 max	μA	V_{IN} = 0V, V_{DD}
C_{IN} Input Capacitance[5]	All	4	5 max	pF	
DIGITAL OUTPUTS					
STAT (pin 12), DB_7 to DB_0 (pins 20-27)					
V_{OH} Output HIGH Voltage	All	+4.8	+4.5 min	V	I_{SOURCE} = 40μA
V_{OL} Output LOW Voltage	All	+0.4	+0.6 max	V	I_{SINK} = 1.6mA
I_{LKG} DB_7 to DB_0 Floating State Leakage	All	0.3	10 max	μA	
Floating State Output Capacitance (DB_7 - DB_0)	All	5	10 max	pF	V_{OUT} = 0V to V_{DD}
Output Code	All	Unipolar Binary Figure 7			
		Complementary Binary Figure 8			
		Offset Binary Figure 9			
POWER REQUIREMENTS					
V_{DD}	All	+5	+5	V	
I_{DD} - Static	All	3 typ	5 max	mA	
I_{DD} - Dynamic	All	3 typ	8 max	mA	f_{CLK} = 1MHz

Notes:

[1] Temperature range as follows: JN, KN, LN (0 to +70°C), AD, BD, CD (-25°C to +85°C).

[2] Typical offset temperature coefficient is ±150μV/°C.

[3] R_{BOFS}/R_{AIN} (0-7) mismatch causes transfer function rotation about positive full scale. The effect is an offset and a gain term when using the circuits of Figure 8a, and Figure 9a.

[4] Typical value, not guaranteed or subject to test.

[5] Guaranteed but not tested.

[6] Typical change in B_{OFS} gain from +25°C to T_{min} to T_{max} is ±2 LSB's.

Specifications subject to change without notice.

AC SPECIFICATIONS (V_{DD} = +5V, V_{REF} = -10V, Unipolar Operation, unless otherwise noted)

Symbol	Specification	Typical at +25°C	Limit Over Temperature	Units	Conditions
t_H	ALE pulse width	50	80 min	ns	See "Switching Terminology"
t_{ALS}	Address valid to latch set-up time	45	70 min	ns	
t_{ALH}	Address valid to latch hold time	10	20 min	ns	
t_{LCS}	Address latch to $\overline{CS}$ set-up time	10	20 min	ns	
t_{ACC}	$\overline{CS}$ to output propagation delay	200	250 max	ns	C_L = 100pF
t_{CW}	$\overline{CS}$ pulse width	250	280 min	ns	
t_{CF}	$\overline{CS}$ to output float propagation delay	50	80 max	ns	
t_{CLZ}	$\overline{CS}$ to low impedance bus	100	150 max	ns	
f_{CLK}	Clock frequency for stated accuracy	1600	1200 max[1]	kHz	

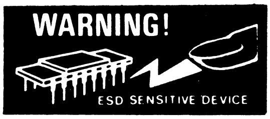
[1] Guaranteed conversion time of 66.6μs/channel with 1200kHz clock.

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND	+7V
V_{DD} to DGND	+7V
AGND to DGND	-0.3V, V_{DD}
Digital Input Voltage to DGND (pins 13, 16–19)	+15V
Digital Output Voltage to DGND (pins 12, 20–27)	-0.3V, V_{DD}
CLK (pin 15) input voltage to DGND	+15V
V_{REF} (pin 10) to AGND	±25V
V_{BOFS} (pin 1) to AGND	±17V
AIN (0–7) (pin 9–2)	±17V
Operating Temperature Range JN, KN, LN	0 to +70°C
AD, BD, CD	-25°C to +85°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10 secs)	+300°C
Power Dissipation (Package) Plastic (Suffix N) to +50°C	1200mW
Derate above +70°C by	12mW/°C
Ceramic (Suffix D) to +50°C	1000mW
Derate above +50°C by	10mW/°C

CAUTION:

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The foam should be discharged to the destination socket before devices are removed.



GENERAL CIRCUIT INFORMATION

BASIC CIRCUIT DESCRIPTION

The AD7581 accepts eight analog inputs and sequentially converts each input into an eight-bit binary word using the successive approximation technique. The conversion results are stored in an 8 X 8 bit dual-port RAM. The device runs either directly from the microprocessor clock (in 6800 type systems) or from some suitable signal (e.g. ALE in 8085 type systems). Most applications require only a −10V reference and a +5V supply. Start-up logic is included on the device to establish the correct sequences on power-up. A maximum of 800 clock pulses are required for this period. Figure 1 shows the AD7581 functional diagram.

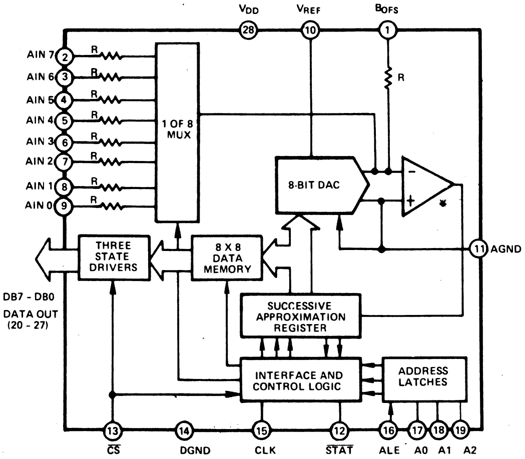


Figure 1. AD7581 Functional Diagram

Conversion of a single channel requires 80 input clock periods and a complete scan through all channels requires 640 input clock periods. When a channel conversion is complete, the successive approximation register contents are loaded into the proper channel location of the 8 X 8 RAM. At this time a status signal output, $\overline{STAT}$ (pin 12), gives a short negative going pulse (8 clock periods). This negative going $\overline{STAT}$ pulse is extended to 72 clock periods when channel 1 conversion is complete. An external pulse-width detector connected to the status pin can be used to derive conversion-related timing signals for microprocessor interrupts (see Channel Identification opposite page). Simultaneous with $\overline{STAT}$ going low, the MUX address is decremented. Eight clock periods later the next conversion is started.

Automatic interleaved DMA is provided by on-chip logic to ensure that memory updates take place at instants when the microprocessor is not addressing memory. Memory locations are addressed by A_0, A_1 and A_2. This address may be latched by ALE for systems which feature a multiplexed address/data bus or alternatively, for systems which have separate address and data buses, the address latches can be made transparent by tying ALE (pin 16) HIGH. $\overline{CS}$ (pin 13) activates three-state buffers to place addressed data on the $DB_0 - DB_7$ data output pins.

A/D CIRCUIT DETAILS

In the successive approximation technique, successive bits, starting with the most significant bit (DB_7), are applied to the input of the D/A converter. The DAC output is then compared to the unknown analog input voltage, A_{IN} (n), using a comparator. If the DAC output is greater than $A_{IN}(n)$, the data latch for the trial bit is reset to zero, and the next smaller data bit is tried. If the DAC output is less than $A_{IN}(n)$, the trial data bit stays in the "1" state, and the next smaller data bit is tried. Each successive bit is tried, compared to $A_{IN}(n)$, and set or reset in this manner until the least significant bit (DB_0) decision is made. The successive approximation register now contains a valid digital representation of $A_{IN}(n)$. $A_{IN}(n)$ is assumed to be stable during conversion.

The current weighting D/A converter is a precision multiplying DAC. Figure 2 shows the functional diagram of the DAC as used in the AD7581. It consists of a precision Silicon Chromium thin film R/2R ladder network and 8 N-channel MOSFET switches operated in single-pole-double-throw.

The currents in each 2R shunt arm are binarily weighted i.e., the current in the MSB arm is V_{REF} divided by 2R, in the second arm is V_{REF} divided by 4R, etc. Depending on the D/A logic input (A/D output) from the successive approximation register, the current in the individual shunt arms is steered either to A_{GND} or to the comparator summing point.

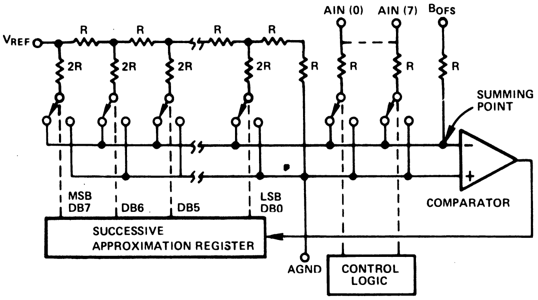


Figure 2. D/A Converter as Used in AD7581

TIMING AND CONTROL OF THE AD7581

CHANNEL SELECTION

Table 1 shows the truth table for the address inputs. The input address is latched when ALE goes LOW. When ALE is HIGH the address input latch is transparent.

A2	A1	A0	ALE	Channel Data To Be Read
0	0	0	1	Channel 0
0	0	1	1	Channel 1
0	1	0	1	Channel 2
0	1	1	1	Channel 3
1	0	0	1	Channel 4
1	0	1	1	Channel 5
1	1	0	1	Channel 6
1	1	1	1	Channel 7

Table 1. Channel Selection Truth Table

TIMING AND CONTROL

A typical timing diagram is shown in Figure 3. When $\overline{\text{CS}}$ is HIGH, the three-state data drivers are in the high-impedance state. When $\overline{\text{CS}}$ goes LOW the data drivers switch to the low-impedance state (i.e., low impedance to DGND or to V_{DD}). Output data is valid after time t_{ACC}.

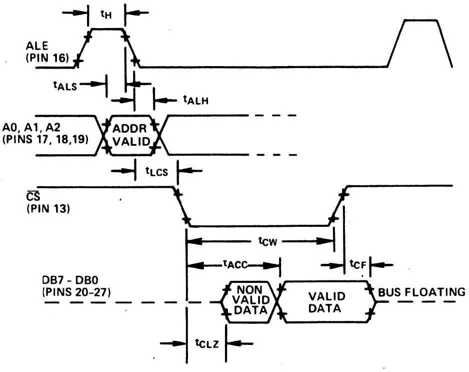


Figure 3. Timing Diagram for the AD7581

SWITCHING TERMINOLOGY

t_H: ALE pulse width requirement.
t_{ALH}: Address Valid to latch hold time.
t_{ALS}: Address Valid to latch set-up time.
t_{LCS}: Address latch to Chip Select set-up time.
t_{CW}: Chip Select pulse width requirement.
t_{ACC}: Chip Select to valid data propagation delay.
t_{CF}: Chip Select to output data float propagation delay.
t_{CLZ}: Chip Select to low impedance data bus.

CHANNEL IDENTIFICATION

In some real-time applications, it may be necessary to provide an interrupt signal when a particular channel receives updated data. To achieve this, it is necessary to identify which channel is currently under conversion. The $\overline{\text{STAT}}$ output provides an identifying signal by staying low for an additional 64 clock periods over normal (8 clock periods) when channel 0 is active. This is illustrated in Figure 4. Memory update takes place on a rising edge of a clock pulse and is completed in 200ns. This occurs 6 clock periods before $\overline{\text{STAT}}$ goes low.

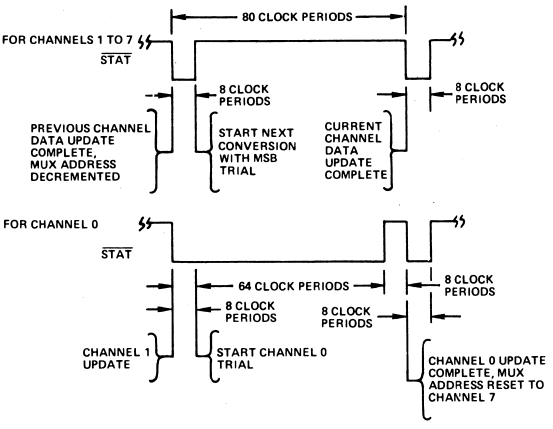


Figure 4. $\overline{\text{STAT}}$ Output for Channel Identification

One simple circuit using the $\overline{\text{STAT}}$ output is shown in Figure 5. The time constant RC is chosen such that X_2 ignores the normal $\overline{\text{STAT}}$ low pulse width (8 clock periods wide) but respond to the much wider $\overline{\text{STAT}}$ low pulse width (72 clock periods wide) occurring during channel 0 conversion. Typically for a $1\mu s$ clock period $C = 0.022\mu F$, $R = 1.8k\Omega$.

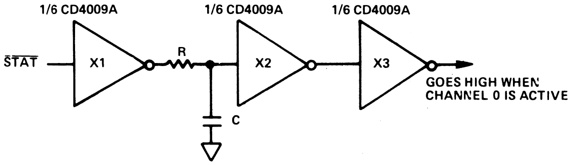
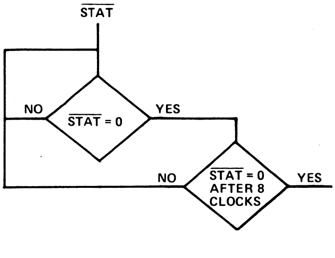


Figure 5. Hardware Channel Identification

Another possibility is to use the microprocessor to interrogate the $\overline{\text{STAT}}$ output and hence determine channel identity. A simple routine is shown in Figure 6.



$\overline{\text{STAT}}$
NO
$\overline{\text{STAT}}$ = 0
YES
NO
$\overline{\text{STAT}}$ = 0 AFTER 8 CLOCKS
YES

Figure 6. Software Channel Identification

OPERATING THE AD7581

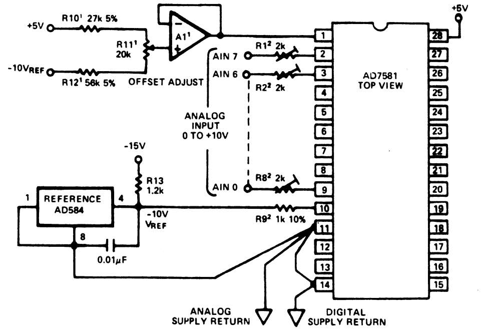
UNIPOLAR BINARY OPERATION

Figures 7a and 7b show the analog circuit connections and typical transfer characteristic for unipolar operation (0V to +10V). An AD584 is used for the -10V reference. Calibration is as follows (device clocked i.e., continuous conversions);

OFFSET:

Comparator offset is trimmed out via the bipolar offset pin B_{OFS}. R10, R11 and R12 comprise a simple voltage tap buffered by A1 and feeding into B_{OFS}.

1. Since comparator offset will be the same regardless of which channel is active, take A_0, A_1 and A_2 LOW and and exercise ALE to latch the address.
2. With AIN 0 = 19.5mV (1/2LSB) adjust R11, i.e., the offset voltage on B_{OFS}, until $DB_7 - DB_1$ are LOW and DB_0 (LSB) flickers.



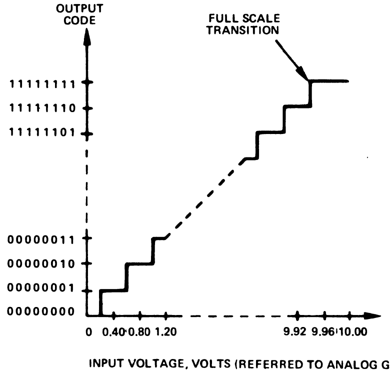
NOTES:
¹A1, R10, R11 AND R12 CAN BE OMITTED IF OFFSET TRIM IS NOT REQUIRED AND B_{OFS} CAN BE TIED TO AGND.
²R1-R8 AND R9 CAN BE OMITTED IF GAIN TRIM IS NOT REQUIRED.

Figure 7a. AD7581 Unipolar (0V to +10V) Operation (Output Code is Straight Binary)

GAIN (FULL SCALE)

In many applications gain adjustment is not required thus removing the need for trimmers in the analog channels. For channels requiring gain trim, the following procedure is recommended. Offset adjustment must be performed before gain adjustment.

1. Apply +9.941V (FS - 1 1/2LSB) to all input channels AIN (0-7).



NOTE: APPROXIMATE BIT WEIGHTS ARE SHOWN FOR ILLUSTRATION. BIT WEIGHT FOR A -10V REFERENCE IS ≈ 39.1mV.

Figure 7b. Transfer Characteristic for Unipolar Circuit of Figure 7a

2. Select required channel n via A_0, A_1, A_2 and latch the Address using ALE.
3. Adjust trimmer RN of selected channel until $DB_7 - DB_1$ are HIGH and the LSB (DB_0) flickers.
4. Select next channel requiring gain trim and repeat steps 2 and 3.

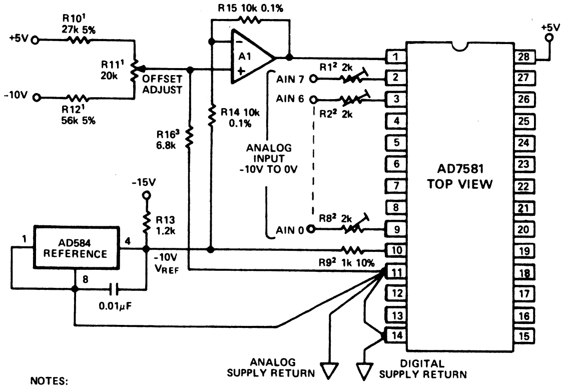
UNIPOLAR (COMPLEMENTARY BINARY) OPERATION

Figures 8a and 8b show the analog circuit connections and typical transfer characteristic for unipolar (complementary binary) operation.
Calibration is as follows (continuous conversions);

OFFSET:

Comparator offset is trimmed out via the bipolar offset pin B_{OFS}. R10, R11 and R12 comprise a simple voltage tap buffered by A1 and feeding into B_{OFS}.

1. Since comparator offset will be the same regardless of which channel is active, take A_0, A_1 and A_2 LOW and exercise ALE to latch the address.
2. With AIN 0 = -9.98V (-FS + 1/2LSB) adjust R11, i.e., the offset voltage on B_{OFS}, until $DB_7 - DB_1$ are LOW and the LSB (DB_0) flickers.



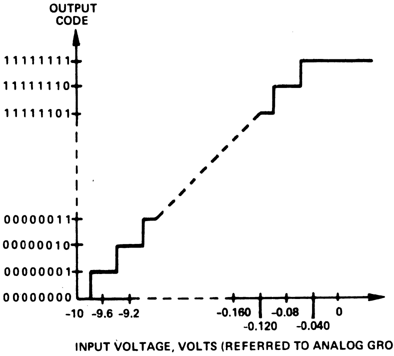
NOTES:
¹R10, R11 AND R12 CAN BE OMITTED IF OFFSET TRIM IS NOT REQUIRED.
²R1 - R8 AND R9 CAN BE OMITTED IF GAIN TRIM IS NOT REQUIRED.
³R16/R10/R12 = 5kΩ. IF R10, R11 AND R12 ARE NOT USED, MAKE R16 = 5kΩ.

Figure 8a. AD7581 (0V to -10V) Operation (Output Code is Complementary Binary)

GAIN (FULL SCALE)

In many applications gain adjustment is not required thus removing the need for trimmers in the analog channels. For channels requiring gain trim, the following procedure is recommended. Offset adjustment must be performed before gain adjustment.

1) Apply -58.6mV (1 1/2LSB) to all input channels AIN (0-7).
2) Select required channel n via A_0, A_1, A_2 and exercise ALE to latch the address.
3) Adjust trimmer RN of selected channel until $DB_7 - DB1$ are HIGH and the LSB (DB_0) flickers.
4) Select next channel requiring gain trim and repeat step 2 and 3.



NOTE: APPROXIMATE BIT WEIGHTS ARE SHOWN FOR ILLUSTRATION. BIT WEIGHT FOR A -10V REFERENCE IS ≈ 39.1mV.

Figure 8b. Transfer characteristic for Unipolar Circuit of Figure 8a

BIPOLAR (OFFSET BINARY) OPERATION

Figures 9a and 9b illustrate the analog circuitry and transfer characteristic for ±5V bipolar operation. Output coding is offset binary. Comparator offset correction is again applied to the B_{OFS} pin.

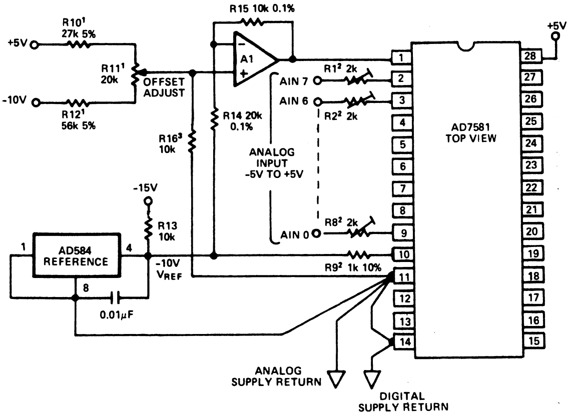
Calibration is as follows (continuous conversions);

OFFSET:

1. Apply -4.980V (-F.S. + 1/2LSB) to all input channels, AIN (0-7).
2. Trim R11 of the comparator offset circuit until $DB_7 - DB_1$ are LOW and the LSB (DB_0) flickers.

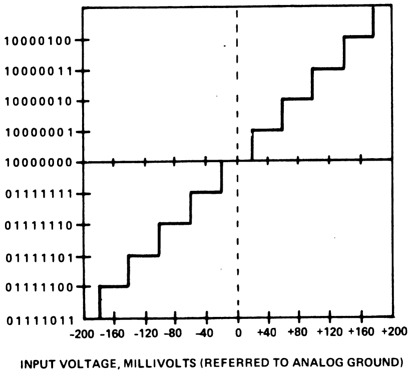
GAIN (FULL SCALE)

1. Apply +4.984V (+F.S. - 1/2LSB) to all input channels, AIN (0-7).
2. Select required channel n via A_0, A_1, A_2, and latch the address using ALE.
3. Adjust trimmer RN of selected channel until $DB_7 - DB_1$ are HIGH and the LSB (DB_0) flickers.
4. Select next channel requiring gain trim and repeat steps 2 and 3.
5. Apply 0V to each gain-trimmed channel. If the ADC output code does not flicker between 01111111 and 10000000 repeat the calibration procedure.



NOTES:
[1] R10, R11 AND R12 CAN BE OMITTED IF OFFSET TRIM IS NOT REQUIRED.
[2] R1 - R8 AND R9 CAN BE OMITTED IF GAIN TRIM IS NOT REQUIRED.
[3] R16/R10/R12 = 6.8kΩ. IF R10, R11 AND R12 ARE NOT USED, MAKE R16 = 6.8kΩ.

Figure 9a. AD7581 Bipolar (-5V to +5V) Operation (Output Code is Offset Binary)



NOTE:
APPROXIMATE BIT WEIGHTS ARE SHOWN FOR ILLUSTRATION.
BIT WEIGHT FOR ±5V FULL SCALE IS ≈ 39.1mV.

Figure 9b. Transfer Characteristic Around Major Carry for Bipolar Circuit of Figure 9a

INTERFACING THE AD7581

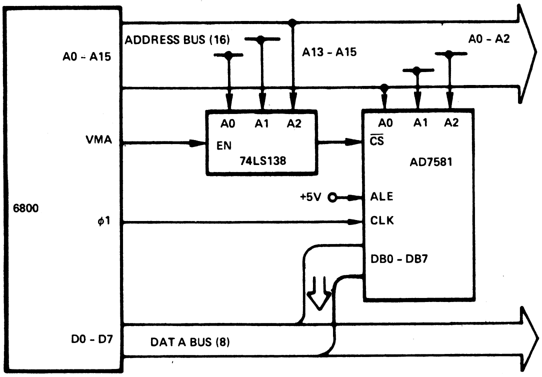


Figure 10. AD7581/6800 Interface

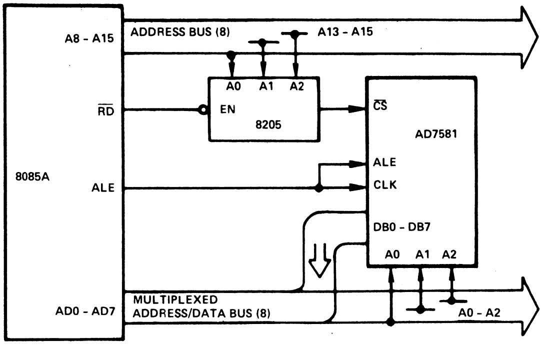


Figure 11. AD7581/8085 Interface

NOTES:

1. ANALOG AND DIGITAL GROUND
   It is recommended that A_{GND} and D_{GND} be connected locally to prevent the possibility of injecting noise into the AD7581. In systems where the A_{GND} - D_{GND} intertie is not local, connect back-to-back diodes (1N914 or equivalent) between the AD7581 A_{GND} and D_{GND} pins.
2. LOGIC DEGLITCHING IN μP APPLICATIONS
   Unspecified states on the address bus (due to different rise and fall times on the address bus) can cause glitches at the AD7581 $\overline{CS}$ terminal. These glitches can cause unwanted reads. The best way to avoid glitches is to gate the address decoding logic, e.g., with RD (8080), $\overline{RD}$ (8085) or VMA (6800).

ANALOG DEVICES

12-Bit Successive Approximation Integrated Circuit A/D Converter

AD ADC80

FEATURES

True 12-Bit Operation: Max Nonlinearity ±0.012%
Low Gain T.C.: ±30ppm/°C max
Low Power: 800mW
Fast Conversion Time: 25µs
Precision 6.3V Reference for External Application
Short-Cycle Capability
Serial or Parallel Data Outputs
Monolithic DAC with Scaling Resistors for Stability
Low Chip Count—High Reliability
Industry Standard Pinout
"Z" Models for ±12V Supplies

PRODUCT DESCRIPTION

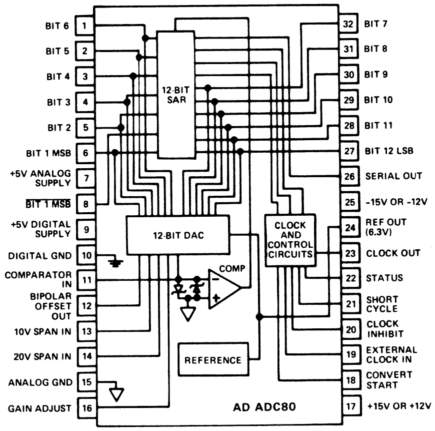
The AD ADC80 is a complete 12-bit successive approximation analog-to-digital converter that includes an internal clock, reference and comparator. Its hybrid IC design utilizes MSI digital and linear monolithic chips in conjunction with a 12-bit monolithic DAC to provide modular performance and versatility with IC size, price and reliability.

Important performance characteristics of the AD ADC80 include a maximum linearity error at +25°C of ±0.012%, max gain T.C. of 30ppm/°C, typical power dissipation of 800mW and max conversion time of 25µs. Monotonic operation of the feedback D/A converter guarantees no missing codes over the temperature range of -25°C to +85°C.

The design of the AD ADC80 includes scaling resistors that provide analog signal ranges of ±2.5, ±5.0, ±10, 0 to +5 or 0 to +10 volts. The 6.3V precision reference may be used for external applications. All digital signals are fully DTL and TTL compatible; output data may be read in both serial and parallel form.

The AD ADC80 is available in two performance grades, the AD ADC80-12 (0.012% of FSR max) and the AD ADC80-10 (0.048% of FSR max). Both grades are specified for use over the -25°C to +85°C temperature range and both are available in a 32-pin hermetically sealed ceramic DIP.

AD ADC80 FUNCTIONAL BLOCK DIAGRAM



32-PIN DIP

PRODUCT HIGHLIGHTS

1. The AD ADC80 is a complete 12-bit A/D converter. No external components are required to perform a conversion.
2. A monolithic 12-bit feedback DAC is used for reduced chip count and higher reliability.
3. The internal buried zener reference is laser trimmed to 6.3 volts. The reference voltage is available externally and can supply up to 1.5mA beyond that required for the reference and bipolar offset current.
4. The scaling resistors are included on the monolithic DAC for exceptional thermal tracking.
5. The AD ADC80 directly replaces other devices of this type with significant increases in performance.
6. The fast conversion rate of the AD ADC80 makes it an excellent choice for applications requiring high system throughput rates.
7. The short cycle and external clock options are provided for applications requiring faster conversion speeds or lower resolutions.

SPECIFICATIONS (typical @ +25°C, ±15V and +5V unless otherwise noted)

MODEL	AD ADC80-12	AD ADC80-10
RESOLUTION	12 Bits	10 Bits
ANALOG INPUTS		
Voltage Ranges		
Bipolar	±2.5V, ±5V, ±10V	
Unipolar	0V to +5V, 0V to +10V	
Impedance (Direct Input)		
0V to +5V, ±2.5V	2.5kΩ	*
0V to +10V, ±5V	5kΩ	*
±10V	10kΩ	*
DIGITAL INPUTS[1]		
Convert Command	Positive Pulse 100ns Wide (min) ("0" to "1" Initiates Conversion)	
Logic Loading	1TTL Load	
External Clock	1TTL Load	
TRANSFER CHARACTERISTICS ERROR		
Gain Error[2]	±0.1% of FSR[3]	*
Offset Error[2]		
Unipolar	±0.05% of FSR	*
Bipolar	±0.1% of FSR	*
Linearity Error (max)[4]	±0.012% of FSR	±0.048% of FSR
Inherent Quantization Error	±1/2LSB	*
Differential Linearity Error	±1/2LSB	*
No Missing Codes Temperature Range	-25°C to +85°C	*
Power Supply Sensitivity		
±15V	±0.0030% of FSR/% V_S	*
+5V	±0.0015% of FSR/% V_S	*
DRIFT		
Specification Temperature Range	-25°C to +85°C	*
Gain (max)	±30ppm/°C	*
Offset		
Unipolar	±3ppm of FSR/°C	*
Bipolar (max)	±15ppm of FSR/°C	*
Linearity (max)	±3ppm of FSR/°C	*
Monotonicity	GUARANTEED	*
CONVERSION SPEED[5]	22μs typ, 25μs max	21μs max
DIGITAL OUTPUT		
(all codes complementary)		
Parallel		
Output Codes[6]		
Unipolar	CSB	
Bipolar	COB, CTC	
Output Drive	2TTL Loads	
Serial Data Codes (NRZ)	CSB, COB	
Output Drive	2TTL Loads	
Status	Logic "1" During Conversion	
Status Output Drive	2TTL Loads	
Internal Clock		
Clock Output Drive	2TTL Loads	
Frequency[7]	575kHz	
INTERNAL REFERENCE VOLTAGE	6.3V ±10mV	
Max. External Current (with no degradation of specifications)	1.5mA	
Tempco of Drift	±10ppm/°C typ, ±20ppm/°C max	
POWER REQUIREMENTS		
Rated Voltages	±15V, +5V	
Range for Rated Accuracy	4.75V to 5.25V and ±14.0V to ±16.0V	
Z Models[8]	4.75V to 5.25V and ±11.4V to ±16.0V	
Supply Drain +15V	+10mA	
-15V	-20mA	
+5V	+70mA	
TEMPERATURE RANGE		
Specification	-25°C to +85°C	
Operating (Derated Specs)	-55°C to +100°C	
Storage	-55°C to +125°C	
PACKAGE OPTION[9]	HY32E	

NOTES:

[1] DTL/TTL compatible i.e., Logic "0" = 0.8V max, Logic "1" = 2.0V min for digital inputs, Logic "0" = +0.4V max and "1" = 2.4V min digital outputs.

[2] Adjustable to zero with external trimpots.

[3] FSR means Full Scale Range- for example, unit connected for ±10V range has 20V FSR.

[4] Error shown is the same as ±1/2LSB max for resolution of A/D converter.

[5] Conversion time with internal clock.

[6] See Table 1.
CSB – Complementary Straight Binary
COB – Complementary Offset Binary
CTC – Complementary Two's Complement

[7] For conversion speeds specified.

[8] For Z models order AD ADC80Z-12 or AD ADC80Z-10.

[9] See Section 20 for package outline information.

*Specifications same as AD ADC80-12.

Specifications subject to change without notice.

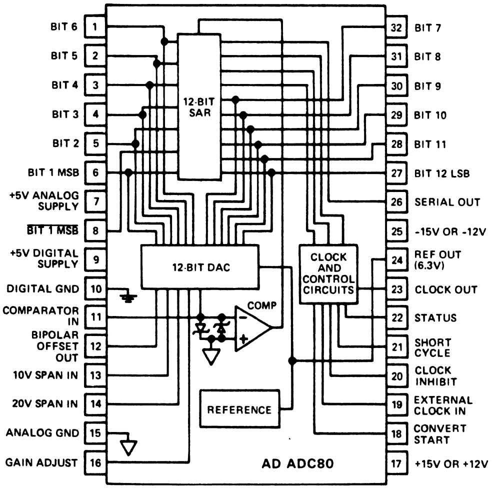


Figure 1. AD ADC80 Functional Diagram and Pinout

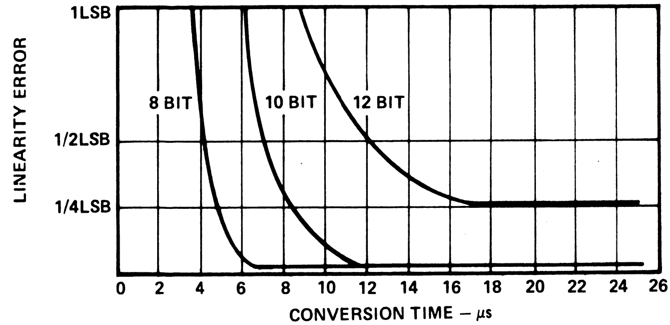


Figure 2. Linearity Error vs. Conversion Time (Normalized)

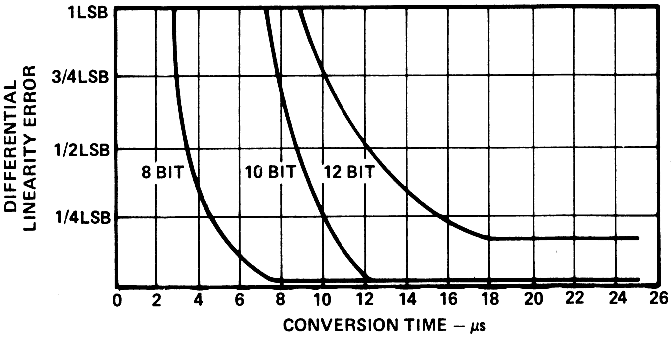


Figure 3. Differential Linearity Error vs. Conversion Time (Normalized)

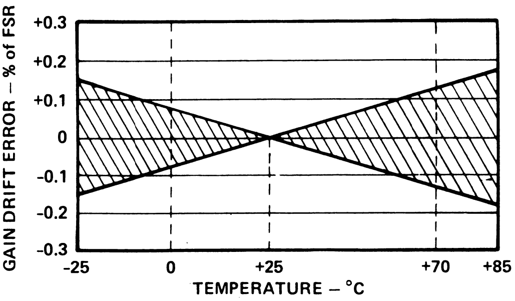


Figure 4. Maximum Gain Drift Error – % of FSR vs. Temperature

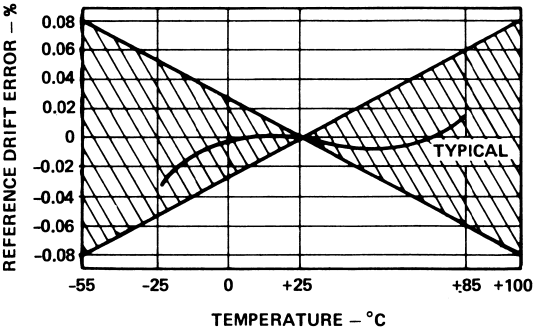


Figure 5. Reference Drift – % Error vs. Temperature

The analog continuum is partitioned into 2^{12} discrete ranges for 12-bit conversion. All analog values within a given quantum are represented by the same digital code, usually assigned to the nominal midrange value. There is an inherent quantization uncertainty of ±1/2LSB, associated with the resolution, in addition to the actual conversion errors.

The actual conversion errors that are associated with A/D converters are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, reference error and power supply rejection. The matching and tracking errors in the AD ADC80 have been minimized by the use of a monolithic DAC that includes the scaling network. The initial gain and offset errors are specified at ±0.1% FSR for gain and ±0.05% FSR for offset. These errors may be trimmed to zero by the use of the external trim circuits as shown in Figures 7 and 9. Linearity error is defined as the deviation from a true straight line transfer characteristic from a zero analog input which calls for a zero digital output to a point which is defined as full scale. The linearity error is unadjustable and is the most meaningful indication of A/D converter accuracy. Differential nonlinearity is a measure of the deviation in staircase step width between codes from the ideal least significant bit step size (Figure 6).

Monotonic behavior requires that the differential linearity error be less than 1LSB, however a monotonic converter can have missing codes; the AD ADC80 is specified as having no missing codes over the entire temperature range from -25°C to +85°C.

There are three types of drift error over temperature: offset, gain and linearity. Offset drift causes a shift of the transfer characteristic left or right over the operating temperature range. Gain drift causes a rotation of the transfer characteristic about the zero or minus full scale point. The worst case accuracy drift is the summation of all three drift errors over temperature. Statistically, however, the drift error behaves as the root-sum-squared (RSS) and can be shown as:

$$\text{RSS} = \sqrt{\epsilon_G^2 + \epsilon_O^2 + \epsilon_L^2}$$

ϵ_G = Gain Drift Error (ppm/°C)

ϵ_O = Offset Drift Error (ppm of FSR/°C)

ϵ_L = Linearity Error (ppm of FSR/°C)

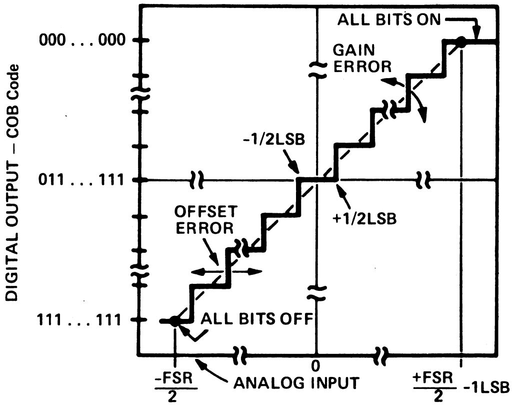


Figure 6. Transfer Characteristic for an Ideal Bipolar A/D

OFFSET ADJUSTMENT
The zero adjust circuit consists of a potentiometer connected across $\pm V_S$ with its slider connected through a 1.8MΩ resistor to Comparator Input pin 11 for all ranges. As shown in Figure 7 the tolerance of this fixed resistor is not critical, and a carbon composition type is generally adequate. Using a carbon composition resistor having a -1200ppm/°C tempco contributes a worst-case offset tempco of $8 \times 244 \times 10^{-6} \times 1200\text{ppm}/^\circ\text{C} = 2.3\text{ppm}/^\circ\text{C}$ of FSR, if the OFFSET ADJ potentiometer is set at either end of its adjustment range. Since the maximum offset adjustment required is typically no more than ±4LSB, use of a carbon composition offset summing resistor typically contributes no more than 1ppm/°C of FSR offset tempco.

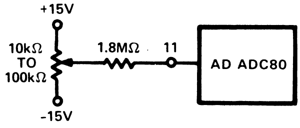


Figure 7. Offset Adjustment Circuit

An alternate offset adjust circuit, which contributes negligible offset tempco if metal film resistors (tempco <100 ppm/°C) are used, is shown in Figure 8.

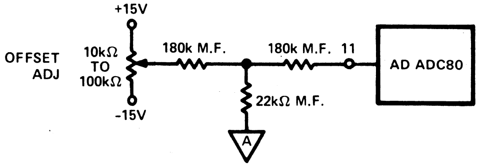


Figure 8. Low Tempco Zero Adjustment Circuit

In either zero adjust circuit, the fixed resistor connected to pin 11 should be located close to this pin to keep the pin 11 connection runs short (Comparator Input pin 11 is quite sensitive to external noise pick-up).

GAIN ADJUSTMENT
The gain adjust circuit consists of a potentiometer connected across $\pm V_S$ with its slider connected through a 10MΩ resistor to the gain adjust pin 16 as shown in Figure 9.

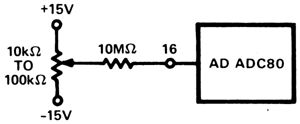


Figure 9. Gain Adjustment Circuit

An alternate gain adjust circuit which contributes negligible gain tempco if metal film resistors (Tempco <100ppm/°C) are used is shown in Figure 10.

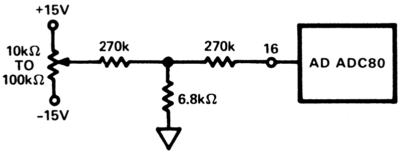


Figure 10. Low Tempco Gain Adjustment Circuit

THEORY OF OPERATION

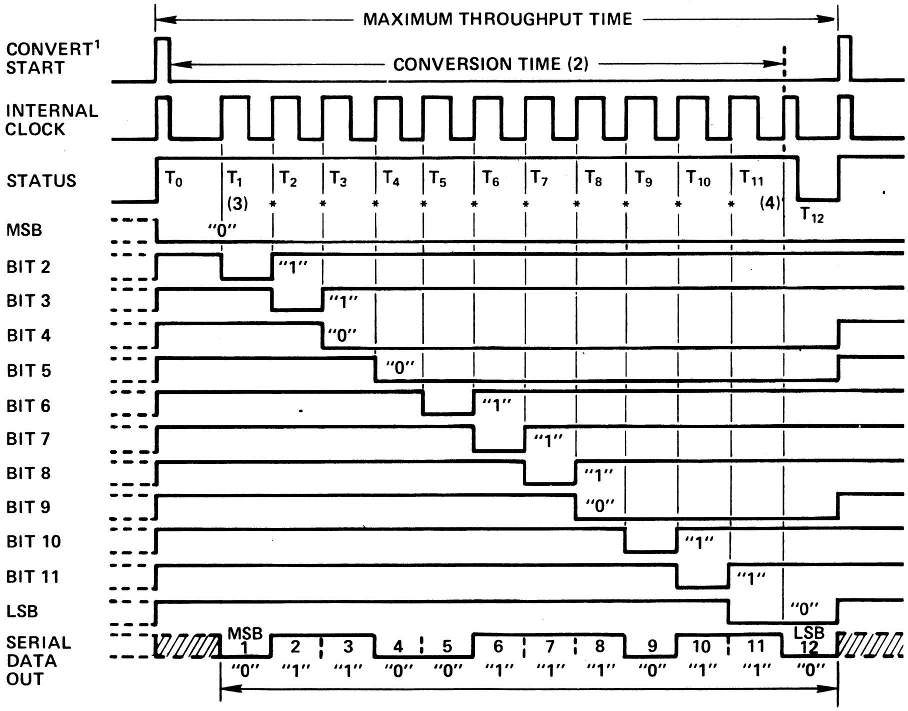
On receipt of a CONVERT START command, the AD ADC80 converts the voltage at its analog input into an equivalent 12-bit binary number. This conversion is accomplished as follows: the 12-bit successive-approximation register (SAR) has its 12-bit outputs connected both to the device bit output pins and to the corresponding bit inputs of the feedback DAC. The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

TIMING

The timing diagram is shown in Figure 11. Receipt of a CONVERT START signal sets the STATUS flag, indicating conversion in progress. This, in turn, removes the inhibit applied to the gated clock, permitting it to run through 13 cycles. All SAR parallel bit and STATUS flip-flops are initialized on the leading edge, and the gated clock inhibit signal is removed on the trailing edge of the CONVERT START signal. At time t_0, B_1 is reset and B_2 -B_{12} are set unconditionally. At t_1 the Bit 1 decision is made (keep) and Bit 2 is unconditionally reset. At t_2, the Bit 2 decision is made (keep) and Bit 3 is reset unconditionally. This sequence continues until the Bit 12 (LSB) decision (keep) is made at t_{12}. After a 40ns delay period, the STATUS flag is reset, indicating that the conversion is complete and that the parallel output data is valid. Resetting the STATUS flag restores the gated clock inhibit signal, forcing the clock output to the Logic "0" state.

Corresponding serial and parallel data bits become valid on the same positive-going clock edge. Serial data does not change and is guaranteed valid on negative-going clock edges, however; serial data can be transferred quite simply by clocking it into a receiving shift register on these edges (see Figure 11).

Incorporation of this 40ns delay guarantees that the parallel (and serial) data are valid at the Logic "1" to "0" transition of the STATUS flag, permitting parallel data transfer to be initiated by the trailing edge of the STATUS signal.



NOTES:

1. THE CONVERT START PULSE WIDTH IS 100ns MIN AND MUST REMAIN LOW DURING A CONVERSION. THE CONVERSION IS INITIATED BY THE "RISING EDGE" OF THE CONVERT COMMAND.
2. 25μs FOR 12 BITS AND 21μs FOR 10 BITS (MAX).
3. MSB DECISION
4. LSB DECISION 40ns PRIOR TO THE STATUS GOING LOW

*BIT DECISIONS

Figure 11. Timing Diagram (Binary Code 011001110110)

DIGITAL OUTPUT DATA

Both parallel and serial data from TTL storage registers are in negative true form. Parallel data output coding is complementary binary for unipolar ranges and either complementary offset binary or complementary two's complement binary, depending on whether BIT 1 (pin 6) or its logical inverse BIT 1 (pin 8) is used as the MSB. Parallel data becomes valid approximately 40ns before the STATUS flag returns to Logic "0", permitting parallel data transfer to be clocked on the "1" to "0" transition of the STATUS flag.

Serial data coding is complementary binary for unipolar input ranges and complementary offset binary for bipolar input ranges. Serial output is by bit (MSB first, LSB last) in NRZ (non-return-to-zero) format. Serial and parallel data outputs change state on positive-going clock edges. Serial data is guaranteed valid 200ns after the rising clock edges, permitting serial data to be clocked directly into a receiving register on these edges as shown in Figure 11. There are 13 negative-going clock edges in the complete 12-bit conversion cycle, as shown in Figure 11. The first edge shifts an invalid bit into the register, which is shifted out on the 13th negative-going clock edge. All serial data bits will have been correctly transferred and be in the receiving shift register locations shown at the completion of the conversion period.

Short Cycle Input: A Short Cycle Input, pin 21, permits the timing cycle shown in Figure 11 to be terminated after any number of desired bits has been converted, permitting somewhat shorter conversion times in applications not requiring full 12-bit resolution. When 12-bit resolution is required, pin 21 is connected to +5V (pin 9). When 10-bit resolution is desired, pin 21 is connected to Bit 11 output pin 28. The conversion cycle then terminates, and the STATUS flag resets after the Bit 10 decision (t_{10} +40ns in timing diagram of Figure 11). Short Cycle pin connections and associated maximum 12-, 10- and 8-bit conversion times are summarized in Table I.

Connect Short Cycle Pin 21 to Pin:	Bits	Resolution (% FSR)	Maximum Conversion Time (μs)	Status Flag Reset
9	12	0.024	25	t_{12} +40ns
28	10	0.100	21	t_{10} +40ns
30	8	0.390	17	t_8 +40ns

Table I. Short Cycle Connections

INPUT SCALING

The AD ADC80 input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 12 for circuit details.

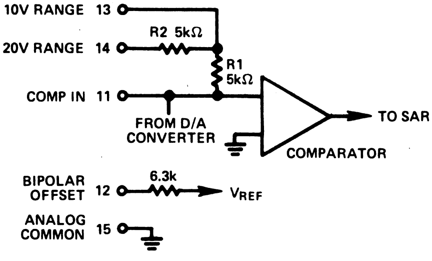


Figure 12. AD ADC80 Input Scaling Circuit

Input Signal Range	Output Code	Connect Pin 12 To Pin	Connect Pin 14 To	Connect Input Signal To
±10V	COB or CTC	11	Input Signal	14
±5V	COB or CTC	11	Open	13
±2.5V	COB or CTC	11	Pin 11	13
0V to +5V	CSB	15	Pin 11	13
0V to +10V	CSB	15	Open	13

Table II. AD ADC80 Input Scaling Connections

Binary (BIN) Output		INPUT VOLTAGE RANGE AND LSB VALUES				
Analog Input Voltage Range	Defined As:	±10V	±5V	±2.5V	0V to +10V	0V to +5V
Code Designation		COB* or CTC**	COB* or CTC**	COB* or CTC**	CSB***	CSB***
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$
	n = 8	78.13mV	39.06mV	19.53mV	39.06mV	19.53mV
	n = 10	19.53mV	9.77mV	4.88mV	9.77mV	4.88mV
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV
Transition Values MSB LSB						
000 . . . 000****	+Full Scale	+10V -3/2LSB	+5V -3/2LSB	+2.5V -3/2LSB	+10V -3/2LSB	+5V -3/2LSB
011 . . . 111	Mid Scale	0	0	0	+5V	+2.5V
111 . . . 110	-Full Scale	-10V +1/2LSB	-5V +1/2LSB	-2.5V +1/2LSB	0 + 1/2LSB	0 +1/2LSB

NOTES:

*COB = Complementary Offset Binary

**CTC = Complementary Two's complement—obtained by using the complement of the most significant bit ($\overline{\text{MSB}}$). $\overline{\text{MSB}}$ is available on pin 8.

***CSB = Complementary Straight Binary.

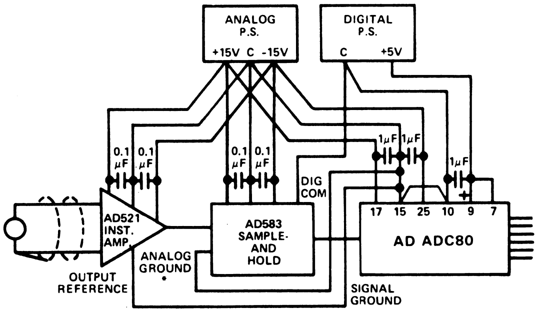
****Voltages given are the nominal value for transition to the code specified.

Table III. Input Voltages and Code Definitions

GROUNDING

Many data-acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return), and Analog Signal Ground. These grounds must be tied together at one point, usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the ground pin of the AD ADC80. Therefore, separate ground returns should be provided to minimize the current flow in the path from sensitive points to the system ground point and the two device grounds should be tied together. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

Each of the AD ADC80's supply terminals should be capacitively decoupled as close to the AD ADC80 as possible. A large value capacitor such as 1μF in parallel with a 0.1μF capacitor is usually sufficient. Analog supplies are bypassed to the Analog Power Return pin and the logic supply is bypassed to the Logic Power Return pin.



*IF INDEPENDENT, OTHERWISE RETURN AMPLIFIER REFERENCE TO MECCA AT ANALOG P.S. COMMON

Figure 13. Basic Grounding Practice

CONTROL MODES

The timing sequence of the AD ADC80 allows the device to be easily operated in a variety of systems with different control modes. The most common control modes are illustrated in Figures 14–17.

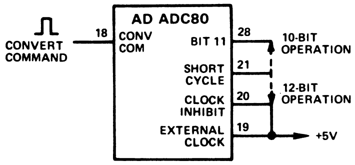


Figure 14. Internal Clock—Normal Operating Mode. Conversion Initiated by the Rising Edge of the Convert Command. The Internal Clock Runs Only During Conversion.

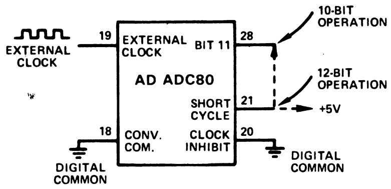


Figure 15. Continuous Conversion with External Clock. Conversion is Initiated by 14th Clock Pulse. Clock Runs Continuously.

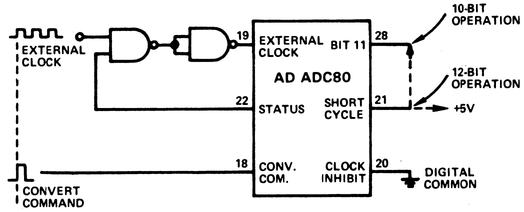


Figure 16. Continuous External Clock. Conversion Initiated by Rising Edge of Convert Command. The Convert Command must be Synchronized with Clock.

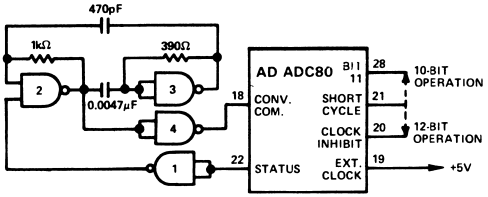


Figure 17. Continuous Conversion with Internal Clock. Conversion is Initiated by the 14th Clock Pulse. Clock Runs Continuously. The Oscillator Formed by Gates 2 and 3 Insures that the Conversion Process will Start When Logic Power is First Turned On.

CALIBRATION

External ZERO ADJ and GAIN ADJ potentiometers, connected as shown in Figures 18 and 19, are used for device calibration. To prevent interaction of these two adjustments, Zero is always adjusted first and then Gain. Zero is adjusted with the analog input near the most negative end of the analog range (0 for unipolar and -FS for bipolar input ranges). Gain is adjusted with the analog input near the most positive end of the analog range.

0 to +10V Range: Set analog input to +1LSB = +0.0024V. Adjust Zero for digital output = 111111111110. Zero is now calibrated. Set analog input to +FSR -2LSB = +9.9952V. Adjust Gain for 000000000001 digital output code; full-scale (Gain) is now calibrated. Half-scale calibration check: set analog input to +5.0000V; digital output code should be 011111111111.

-10V to +10V Range: Set analog input to -9.9951V; adjust Zero for 111111111110 digital output (complementary offset binary) code. Set analog input to +9.9902V; adjust Gain for 000000000001 digital output (complementary offset binary) code. Half-scale calibration check: set analog input to 0.0000V; digital output (complementary offset binary) code should be 0111111111111.

Other Ranges: Representative digital coding for 0 to +10V and -10V to +10V ranges is given above. Coding relationships and calibration points for 0 to +5V, -2.5V to +2.5V and -5V to +5V ranges can be found by halving the corresponding code equivalents listed for the 0 to +10V and -10V to +10V ranges, respectively.

Zero and full-scale calibration can be accomplished to a precision of approximately ±1/4LSB using the static adjustment procedure described above. By summing a small sine or triangular-wave voltage with the signal applied to the analog input, the output can be cycled through each of the calibration codes of interest to more accurately determine the center (or end points) of each discrete quantization level. A detailed description of this dynamic calibration technique is presented in "A/D Conversion Notes", D. Sheingold, Analog Devices, Inc., 1977, Part II, Chapter 3.

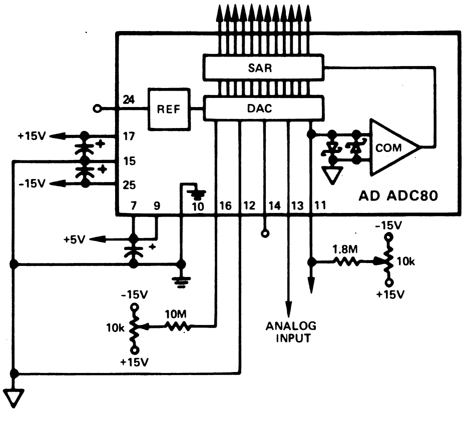


Figure 18. Analog and Power Connections for Unipolar 0-10V Input Range

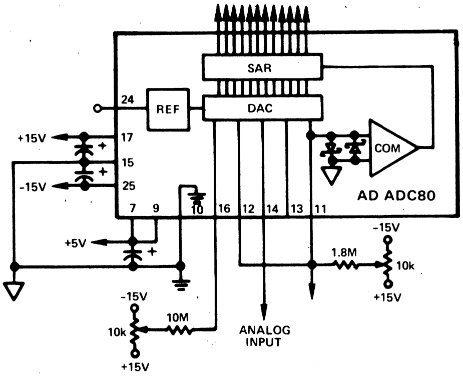


Figure 19. Analog and Power Connections for Bipolar ±10V Input Range

MULTICHANNEL CONVERSION

In multichannel conversion systems, elements of the acquisition chain may be shared by two or more input sources. This sharing may occur in a number of ways, depending on the desired properties of the multiplexed system.

The data acquisition system shown in Figure 20 is a low cost solution to digitizing data from many analog channels. For most efficient use of time, the multiplexer is acquiring the next channel to be converted while the sample-hold is holding the previous output level for conversion. When conversion is complete, the status line from the converter causes the S/H to return to the sample mode and acquire the new data. After the acquisition time is completed, the sample hold can be switched to hold. A conversion can then begin and the multiplexer can be switched to the next channel.

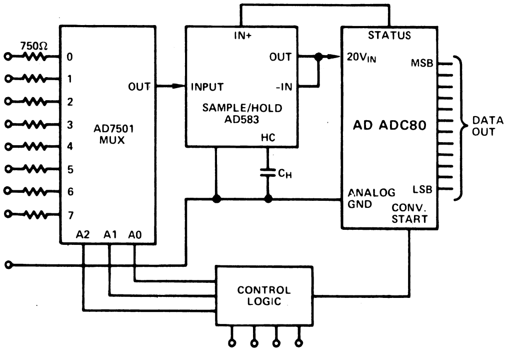


Figure 20. Data Acquisition System

ANALOG DEVICES

Fast, Complete 12-Bit A/D Converter

AD ADC84/AD ADC85

FEATURES

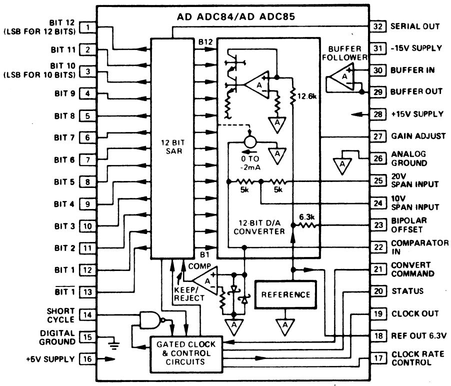
Performance

Complete 12-Bit A/D Converter with Reference and Clock
Fast Successive Approximation Conversion: 10μs
Buried Zener Reference for Long Term Stability and Low Gain T.C.: 10ppm/°C
Max Nonlinearity: <±0.012%
Low Power: 880mW Typical
Hermetic Package Available
Low Chip Count – High Reliability
Industry Standard Pin Out
"Z" Models for ±12V Operation Available
MIL-STD-883B Processing Available
Military Temperature Range -55°C to +125°C

Versatility

Negative-True Parallel or Serial Logic Outputs
Short Cycle Capability
Precision +6.3V Reference for External Applications

AD ADC84/AD ADC85 FUNCTIONAL BLOCK DIAGRAM



32-PIN DIP

PRODUCT DESCRIPTION

The AD ADC84/AD ADC85 series devices are high speed low cost 10- and 12-bit successive approximation analog-to-digital converters that include an internal clock, reference and comparator. Its hybrid IC design utilizes MSI digital and linear monolithic chips in conjunction with a 12-bit monolithic DAC to provide modular performance and versatility with IC size, price and reliability.

Important performance characteristics of the AD ADC84/AD ADC85 series include a maximum linearity error at +25°C of ±0.012%, gain T.C. below 15ppm/°C, typical power dissipation of 880mW, and conversion time of less than 10μs for the 12-bit versions. Of considerable significance in military and aerospace applications is the guaranteed performance from -55°C to +125°C of the AD ADC85S which is also available processed to MIL-STD-883B. Monotonic operation of the feedback D/A converter guarantees no missing output codes over temperature ranges of 0 to +70°C, -25°C to +85°C, and -55°C to +125°C.

The design of the AD ADC84/AD ADC85 includes scaling resistors that provide analog input signal ranges of ±2.5, ±5, ±10, 0 to +5, or 0 to +10 volts. Adding flexibility and value are the +6.3V precision reference, which also can be used for external applications, and the input buffer amplifier. All digital signals are fully DTL and TTL compatible, and the data output is negative-true and available in either serial or parallel form.

The AD ADC84/AD ADC85 series devices are available in two different performance grades. The devices are specified for either 10-bit accuracy (±0.048% FSR max) or 12-bit accuracy (±0.012% FSR max) with 6μs, 10μs max conversion times respectively.

The AD ADC84 and AD ADC85C specified for operation over the 0 to +70°C temperature range. The AD ADC85 and AD ADC85S are specified for the -25°C to +85°C, -55°C to +125°C ranges respectively.

PRODUCT HIGHLIGHTS

1. The AD ADC84/AD ADC85 series devices are complete 12-bit A/D converters. No external components are required to perform a conversion.
2. The AD ADC84/AD ADC85 directly replaces other devices of this type with significant increases in performance.
3. The fast conversion rate of the AD ADC84/AD ADC85 makes it an excellent choice for applications requiring high system throughput rates.
4. The internal buried zener reference is laser trimmed to 6.3V ±0.1% and ±10ppm/°C typical T.C. The reference is available externally and can provide up to 1mA.
5. The integrated package construction provides high quality and reliability with small size and weight.
6. The monolithic 12-bit feedback DAC is used for reduced chip count and higher reliability.
7. The AD ADC85S/883B comes processed to MIL-STD-883, class B requirements.

SPECIFICATIONS (typical @ +25°C, ±15V and +5V unless otherwise noted)

MODEL	AD ADC84	AD ADC85C	AD ADC85	AD ADC85S	UNITS
RESOLUTION	10/12	10/12	10/12	10/12	Bits
ANALOG INPUTS					
Voltage Ranges					
Bipolar	±2.5, ±5, ±10	*	*	*	Volts
Unipolar	0 to +5, 0 to +10	*	*	*	Volts
Impedance (Direct Input)					
0V to +5V, ±2.5V	2.5(±20%)	*	*	*	kΩ
0V to +10V, ±5V	5(±20%)	*	*	*	kΩ
±10V	10(±20%)	*	*	*	kΩ
Buffer Amplifier[1]					
Impedance (min)	100	*	*	*	MΩ
Bias Current	50	*	*	*	nA
Settling Time					
To 0.01% for 20V Step	2	*	*	*	µs
DIGITAL INPUTS[2]					
Convert Command	Positive Pulse 50ns min Trailing Edge Initiates Conversion	*	*	*	
Logic Loading	1	*	*	*	TTL Load
TRANSFER CHARACTERISTICS					
Gain Error[3]	±0.1(±0.25% max)	*	*	*	%
Offset Error[3]	Adjustable to Zero	*	*	*	
Unipolar	±0.05(±0.2% max)	*	*	*	% of FSR[4]
Bipolar[5]	±0.1(±0.25% max)	*	*	*	% of FSR
Linearity Error (max)[6]	±0.048/±0.012	*	*	*	% of FSR
Inherent Quantization Error	±0.5	*	*	*	LSB
Differential Linearity Error	±0.5	*	*	*	LSB
No Missing Codes Temperature Range	0 to +70	0 to +70	-25 to +85	-55 to +125	°C
Power Supply Sensitivity					
±15V	±0.004	*	*	*	% of FSR/%V
+5V	±0.001	*	*	*	% of FSR/%V
DRIFT					
Specification Temperature Range	0 to +70	*	-25 to +85	-55 to +125	°C
Gain (max)	±30	±40/±25	±20/±15	±25	ppm/°C
Offset					
Unipolar	±3	*	*	±5 max	ppm/°C
Bipolar (max)[5]	±15	±20/±12	±10/±7	±10	ppm/°C
Linearity (max)	±3	*	±3/±2	*	ppm/°C
Monotonicity	GUARANTEED	*	*	*	
CONVERSION SPEED (MAX)	6/10	*	*	*	µs
DIGITAL OUTPUT					
(all codes complementary)					
Parallel					
Output Codes[7]					
Unipolar	CSB	*	*	*	
Bipolar	COB, CTC	*	*	*	
Output Drive	2	*	*	*	TTL Loads
Serial Data Codes (NRZ)	CSB, COB	*	*	*	
Output Drive	2	*	*	*	TTL Loads
Status	Logic "1" during Conversion	*	*	*	
Status Output Drive	2	*	*	*	TTL Loads
Internal Clock					
Clock Output Drive	2	*	*	*	TTL Loads
Frequency	1.9/1.22	*	*	*	MHz
INTERNAL REFERENCE VOLTAGE	6.3/±15mV max	*	*	*	Volts
Max. External Current (with no degradation of specifications)	1.0	*	*	*	mA
Tempco of Drift, (max)	±20/max	±10 typ	±5 typ	±5 typ	ppm/°C
POWER REQUIREMENTS					
Rated Voltages	+5, ±15	*	*	*	Volts
Range for Rated Accuracy	4.75 to 5.25 and ±13.5 to ±16.5	*	*	*	Volts
Z Models[8]	4.75 to 5.25 and ±11.4 to ±16.5	*	*	*	Volts
Supply Drain +15V	25 max	*	*	*	mA
-15V	30 max	*	*	*	mA
+5V	100 max	*	*	*	mA
Total Power Dissipation	1100 max	*	*	*	mW
TEMPERATURE RANGE					
Specification	0 to +70	*	-25 to +85	-55 to +125	°C
Operating (Derated Specs)	-25 to +85	*			°C
Storage	-55 to +125	*	*	*	°C
PACKAGE	Ceramic	Hermetic Ceramic	Hermetic Ceramic	Hermetic Ceramic	

NOTES

[1] Buffer Settling time adds to conversion speed when buffer is connected to input.

[2] DTL/TTL compatible Logic "0" = 0.8V max, Logic "1" = 2.0V min for digital output, Logic "0" = 0.4V max, Logic "1" = 2.4V min.

[3] Adjustable to zero.

[4] FSR means Full Scale Range.

[5] Guaranteed at V_{IN} = 0 volts.

[6] Error shown is the same as ±1/2LSB max error in % of FSR.

[7] See Table 1.

[8] For ±12V operation add "Z" to model number. Input range limited to a maximum of ±5V.

* Specifications same as AD ADC84.

Specifications subject to change without notice.

Typical Performance Curves

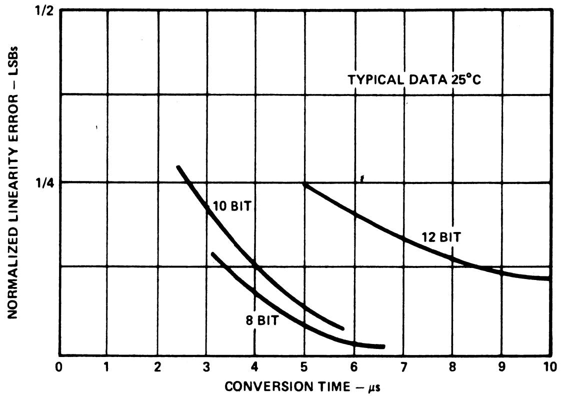


Figure 1. Linearity Error vs. Conversion Speed

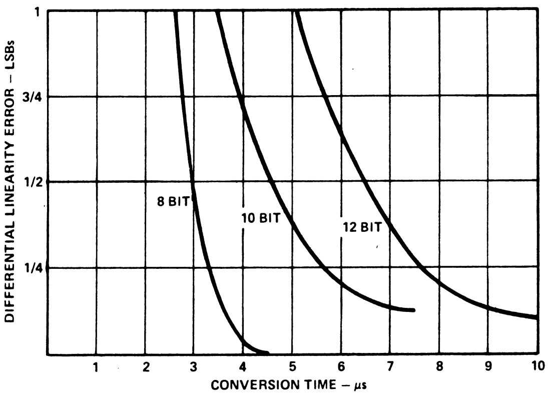


Figure 2. Change in Differential Linearity vs. Conversion Speed

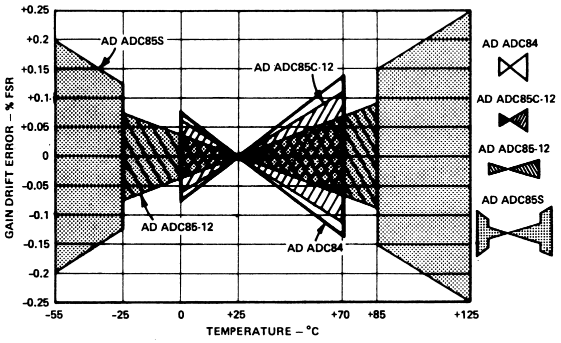


Figure 3. Gain Drift Error (%FSR) vs. Temperature

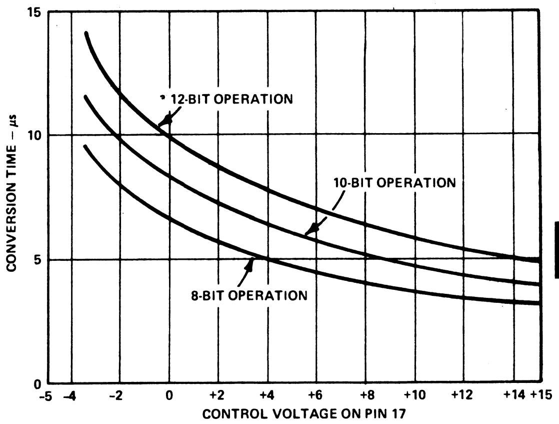


Figure 4. Conversion Speed vs. Control Voltage

The analog continuum is partitioned into 2^{12} discrete ranges for 12-bit conversion. All analog values within a given quantum are represented by the same digital code, usually assigned to the nominal midrange value. There is an inherent quantization uncertainty of ±1/2LSB, associated with the resolution, in addition to the actual conversion errors.

The actual conversion errors that are associated with A/D converters are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, reference error and power supply rejection. The matching and tracking errors in the converter have been minimized by the use of a monolithic DAC that includes the scaling network. The initial gain and offset errors are specified at ±0.1% FSR for gain and ±0.05% FSR for offset. These errors may be trimmed to zero by the use of the external trim circuits as shown in Figures 6 and 8. Linearity error is defined as the deviation from a true straight line transfer characteristic from a zero analog input which calls for a zero digital output to a point which is defined as full scale. The linearity error is unadjustable and is the most meaningful indication of A/D converter accuracy. Differential nonlinearity is a measure of the deviation in the staircase step width between codes from the ideal least significant bit step size (Figure 5).

Monotonic behavior requires that the differential linearity error be less than 1LSB, however a monotonic converter can have missing codes; the AD ADC84/AD ADC85 are specified as having no missing codes over the entire temperature range as specified on the data page.

There are three types of drift error over temperature: offset, gain and linearity. Offset drift causes a shift of the transfer characteristic left or right over the operating temperature range. Gain drift causes a rotation of the transfer characteristic about the zero or minus full scale point. The worst case accuracy drift is the summation of all three drift errors over temperature. Statistically, however, the drift error behaves as the root-sum-squared (RSS) and can be shown as:

$$RSS = \sqrt{\epsilon_G^2 + \epsilon_O^2 + \epsilon_L^2}$$

ϵ_G = Gain Drift Error (ppm/°C)

ϵ_O = Offset Drift Error (ppm of FSR/°C)

ϵ_L = Linearity Error (ppm of FSR/°C)

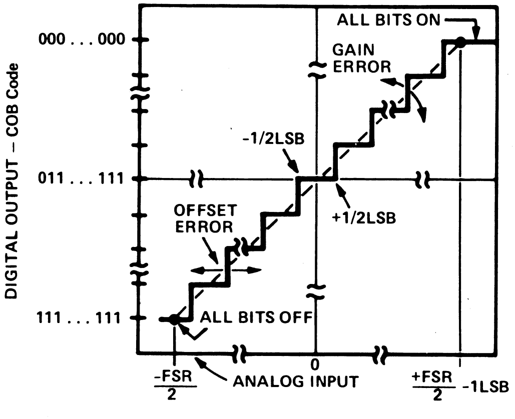


Figure 5. Transfer Characteristics for an Ideal Bipolar A/D

OFFSET ADJUSTMENT

The zero adjust circuit consists of a potentiometer connected across $\pm V_S$ with its slider connected through a 1.8MΩ resistor to Comparator Input pin 22 for all ranges. As shown in Figure 7 the tolerance of this fixed resistor is not critical, and a carbon composition type is generally adequate. Using a carbon composition resistor having a -1200ppm/°C tempco contributes a worst-case offset tempco of $8 \times 244 \times 10^{-6} \times 1200\text{ppm/°C} = 2.3\text{ppm/°C}$ of FSR, if the OFFSET ADJ potentiometer is set at either end of its adjustment range. Since the maximum offset adjustment required is typically no more than ±4LSB, use of a carbon composition offset summing resistor typically contributes no more than 1ppm/°C of FSR offset tempco.

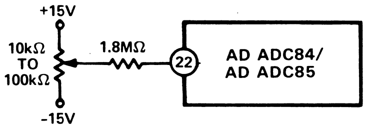


Figure 6. Offset Adjustment Circuit

An alternate offset adjust circuit, which contributes negligible offset tempco if metal film resistors (tempco <100 ppm/°C) are used, is shown in Figure 7.

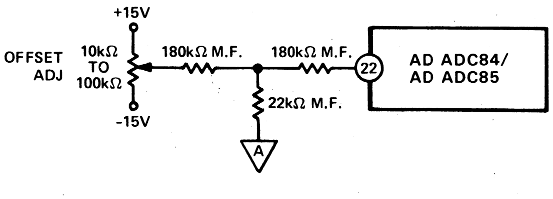


Figure 7. Low Tempco Zero Adjustment Circuit

In either zero adjust circuit, the fixed resistor connected to pin 22 should be located close to this pin to keep the pin connection runs short (Comparator Input pin 22 is quite sensitive to external noise pick-up).

GAIN ADJUSTMENT

The gain adjust circuit consists of a potentiometer connected across $\pm V_S$ with its slider connected through a 10MΩ resistor to the gain adjust pin 27 as shown in Figure 8.

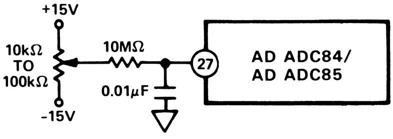


Figure 8. Gain Adjustment Circuit

An alternate gain adjust circuit which contributes negligible gain tempco if metal film resistors (tempco <100ppm/°C) are used is shown in Figure 9.

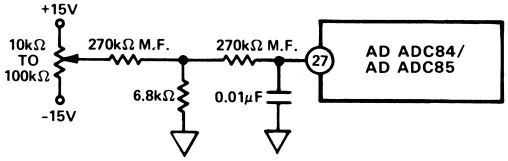


Figure 9. Low Tempco Gain Adjustment Circuit

THEORY OF OPERATION

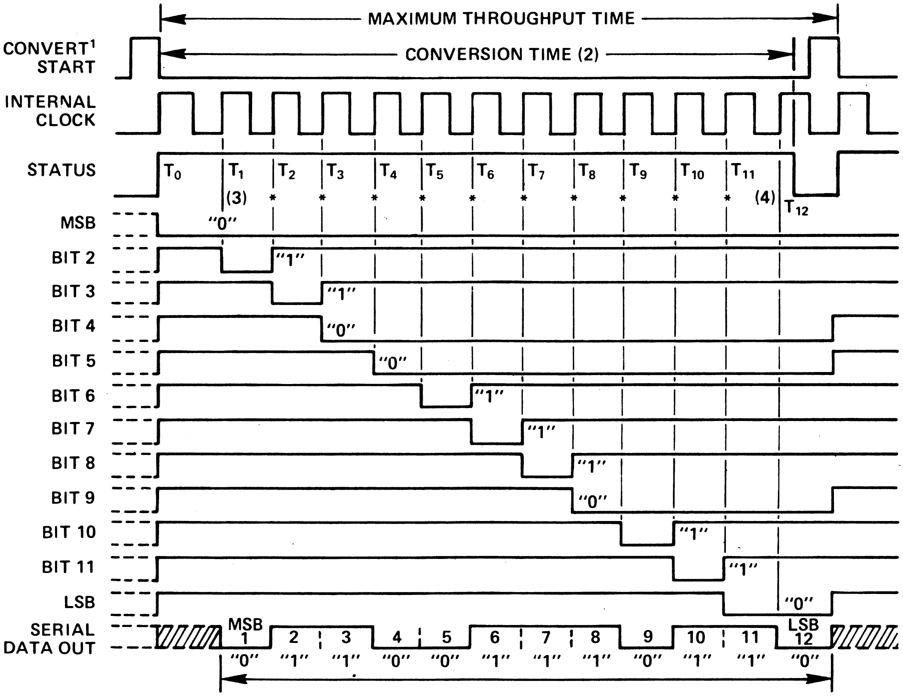
On receipt of a CONVERT START command, the AD ADC84/ AD ADC85 converts the voltage as its analog input into an equivalent 12-bit binary number. This conversion is accomplished as follows: the 12-bit successive-approximation register (SAR) has its 12-bit outputs connected both to the device bit output pins and to the corresponding bit inputs of the feedback DAC. The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

TIMING

The timing diagram is shown in Figure 10. Receipt of a CONVERT START signal sets the STATUS flag, indicating conversion in progress. This, in turn, removes the inhibit applied to the gated clock, permitting it to run through 13 cycles. All the SAR parallel bits, STATUS flip-flops, and the gated clock inhibit signal are initialized on the trailing edge of the CONVERT START signal. At time t_0, B_1 is reset and B_2 - B_{12} are set unconditionally. At t_1 the Bit 1 decision is made (keep) and Bit 2 is unconditionally reset. At t_2, the Bit 2 decision is made (keep) and Bit 3 is reset unconditionally. This sequence continues until the Bit 12 (LSB) decision (keep) is made at t_{12}. After a 40ns delay period, the STATUS flag is reset, indicating that the conversion is complete and that the parallel output data is valid. Resetting the STATUS flag restores the gated clock inhibit signal, forcing the clock output to the Logic "0" state.

Corresponding serial and parallel data bits become valid on the same positive-going clock edge. Serial data does not change and is guaranteed valid on negative-going clock edges, however; serial data can be transferred quite simply by clocking it into a receiving shift register on these edges (see Figure 10).

Incorporation of this 40ns delay guarantees that the parallel (and serial) data are valid at the Logic "1" to "0" transition of the STATUS flag, permitting parallel data transfer to be initiated by the trailing edge of the STATUS signal.



NOTES:
1. THE CONVERT START PULSE WIDTH IS 50ns MIN AND MUST REMAIN LOW DURING A CONVERSION. THE CONVERSION IS INITIATED BY THE "TRAILING EDGE" OF THE CONVERT COMMAND.
2. 10μs FOR 12 BITS AND 6μs FOR 10 BITS (MAX).
3. MSB DECISION
4. LSB DECISION 40ns PRIOR TO THE STATUS GOING LOW

*BIT DECISIONS

Figure 10. Timing Diagram (Binary Code 0 1 1 0 0 1 1 1 0 1 1 0)

DIGITAL OUTPUT DATA

Both parallel and serial data from TTL storage registers are in negative true form. Parallel data output coding is complementary binary for unipolar ranges and either complementary offset binary or complementary two's complement binary, depending on whether BIT 1 (pin 12) or its logical inverse $\overline{\text{BIT 1}}$ (pin 13) is used as the MSB. Parallel data becomes valid approximately 40ns before the STATUS flag returns to Logic "0", permitting parallel data transfer to be clocked on the "1" to "0" transition of the STATUS flag.

Serial data coding is complementary binary for unipolar input ranges and complementary offset binary for bipolar input ranges. Serial output is by bit (MSB first, LSB last) in NRZ (non-return-to-zero) format. Serial and parallel data outputs change state on positive-going clock edges. Serial data is guaranteed valid 200ns after the rising clock edges, permitting serial data to be clocked directly into a receiving register on the negative-going clock edges as shown in Figure 10. There are 13 negative-going clock edges in the complete 12-bit conversion cycle, as shown in Figure 10. The first edge shifts an invalid bit into the register, which is shifted out on the 13th negative-going clock edge. All serial data bits will have been correctly transferred and be in the receiving shift register locations shown at the completion of the conversion period.

Short Cycle Input: A Short Cycle Input, pin 14, permits the timing cycle shown in Figure 10 to be terminated after any number of desired bits has been converted, permitting somewhat shorter conversion times in applications not requiring full 12-bit resolution. When 12-bit resolution is required, pin 14 is connected to +5V (pin 16). When 10-bit resolution is desired, pin 14 is connected to Bit 11 output pin 2. The conversion cycle then terminates, and the STATUS flag resets after the Bit 10 decision (t_{10} +40ns in timing diagram of Figure 10). Short Cycle pin connections and associated maximum 12-, 10- and 8-bit conversion times are summarized in Table I.

Connect Short Cycle Pin 14 To Pin:	Connect Clock Rate Control Pin 17 To	Bits	Resolution (% FSR)	Maximum Conversion Time (μs)	Status Flag Reset
16	15	12	0.024	10	t_{12} +40ns
2	16	10	0.100	6	t_{10} +40ns
4	28	8	0.390	3.2	t_8 +40ns

Table I. Short Cycle Connections

INPUT SCALING

The AD ADC84/AD ADC85 inputs should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 11 for circuit details.

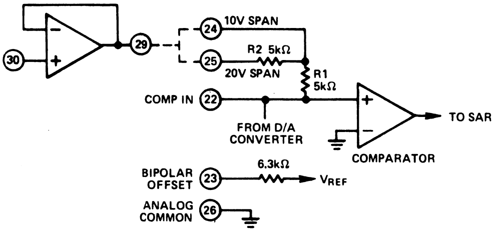


Figure 11. AD ADC84/AD ADC85 Input Scaling Circuit

Input Signal Range	Output Code	Connect Pin 23 To Pin	Connect Pin 25 To	For Direct Input Connect Input Signal To	For Buffered Input Pin 30 Connect Pin 29 To Pin
±10V	COB or CTC	22	Input Signal	25	25
±5V	COB or CTC	22	Open	24	24
±2.5V	COB or CTC	22	Pin 22	24	24
0V to +5V	CSB	26	Pin 22	24	24
0V to +10V	CSB	26	Open	24	24

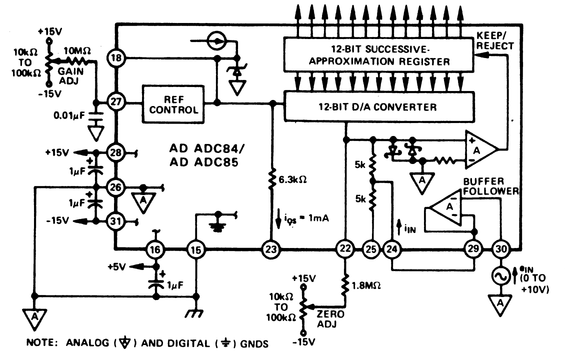
Table II. AD ADC84/AD ADC85 Input Scaling Connections

INPUT VOLTAGE RANGE AND LSB VALUES

Analog Input Voltage Range		±10V	±5V	±2.5V	0V to +10V	0V to +5V
Code Designation		COB* or CTC**	COB* or CTC**	COB* or CTC**	CSB***	CSB***
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$
	n = 8	78.13mV	39.06mV	19.53mV	39.06mV	19.53mV
	n = 10	19.53mV	9.77mV	4.88mV	9.77mV	4.88mV
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV
Transition Values MSB LSB						
000 . . . 000****	+Full Scale	+10V -3/2LSB	+5V -3/2LSB	+2.5V -3/2LSB	+10V -3/2LSB	+5V -3/2LSB
011 . . . 111	Mid Scale	0	0	0	+5V	+2.5V
111 . . . 110	-Full Scale	-10V +1/2LSB	-5V +1/2LSB	-2.5V +1/2LSB	0 + 1/2LSB	0 +1/2LSB

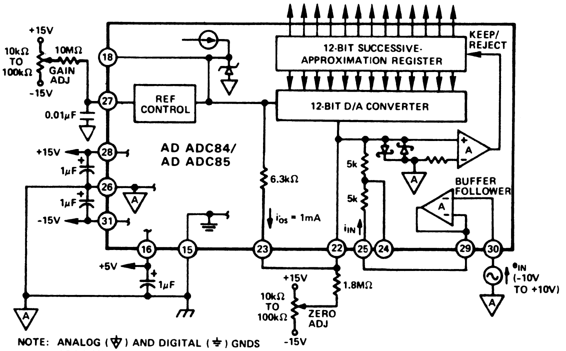
NOTES:
*COB = Complementary Offset Binary
**CTC = Complementary Two's complement–obtained by using the complement of the most significant bit ($\overline{\text{MSB}}$). $\overline{\text{MSB}}$ is available to pin 13.
***CSB = Complementary Straight Binary.
****Voltages given are the nominal value for transition to the code specified.

Table III. Input Voltages and Code Definition



NOTE: ANALOG (▽) AND DIGITAL (⏚) GNDS ARE NOT TIED INTERNALLY AND MUST BE CONNECTED EXTERNALLY.

Figure 12. Analog and Power Connections for Unipolar 0 to +10V Input Range with Buffer Follower



NOTE: ANALOG (▽) AND DIGITAL (⏚) GNDS ARE NOT TIED INTERNALLY AND MUST BE CONNECTED EXTERNALLY.

Figure 13. Analog and Power Connections for Bipolar -10V to +10V Input Range with Buffer Follower

CALIBRATION

External ZERO ADJ and GAIN ADJ potentiometers, connected as shown in Figures 12 and 13, are used for device calibration. To prevent interaction of these two adjustments, Zero is always adjusted first and then Gain. Zero is adjusted with the analog input near the most negative end of the analog range (0 for unipolar and -FS for bipolar input ranges). Gain is adjusted with the analog input near the most positive end of the analog range.

0 to +10V Range: Set analog input to +1LSB = +0.0024V. Adjust Zero for digital output = 111111111110. Zero is now calibrated. Set analog input to +FSR -2LSB = +9.9952V. Adjust Gain for 000000000001 digital output code; full-scale (Gain) is now calibrated. Half-scale calibration check: set analog input to +5.0000V; digital output code should be 011111111111.

-10V to +10V Range: Set analog input to -9.9951V; adjust Zero for 111111111110 digital output (complementary offset binary) code. Set analog input to +9.9902V; adjust Gain for 000000000001 digital output (complementary offset binary) code. Half-scale calibration check: set analog input to 0.0000V; digital output (complementary offset binary) code should be 0111111111111.

Other Ranges: Representative digital coding for 0 to +10V and -10V to +10V ranges is given above. Coding relationships and calibration points for 0 to +5V, -2.5V to +2.5V and -5V to +5V ranges can be found by halving the corresponding code equivalents listed for the 0 to +10V and -10V to +10V ranges, respectively.

Zero and full-scale calibration can be accomplished to a precision of approximately ±1/4LSB using the static adjustment procedure described above. By summing a small sine or triangular-wave voltage with the signal applied to the analog input, the output can be cycled through each of the calibration codes of interest to more accurately determine the center (or end points) of each discrete quantization level. A detailed description of this dynamic calibration technique is presented in "A/D Conversion Notes", D. Sheingold, Analog Devices, Inc., 1977, Part II, Chapter 4.

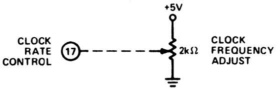
GROUNDING

Many data-acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return), and Analog Signal Ground. These grounds must be tied together at one point, usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the ground pin of the AD ADC84/AD ADC85. Separate ground returns should be provided to minimize the current flow in the path from sensitive points to the system ground point. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

Each of the AD ADC84/AD ADC85's supply terminals should be capacitively decoupled as close to the AD ADC84/ AD ADC85 as possible. A large value capacitor such as 1µF in parallel with a 0.1µF capacitor is usually sufficient. Analog supplies are bypassed to the Analog Power Return pin and the logic supply is bypassed to the Logic Power Return pin.

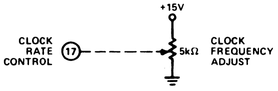
CLOCK RATE CONTROL ALTERNATE CONNECTIONS

If adjustment of the CLOCK RATE is desired for faster conversion speeds, the CLOCK RATE CONTROL may be connected to an external multi-turn trim potentiomer with a TCR of ±100ppm/°C or less as shown in Figures 14 and 15. If the potentiometer is connected to -15V, conversion time can be increased as shown in Figure 10. If these adjustments are used, delete the connections shown in Table I for pin 17. See Figure 1 for nonlinearity error vs. conversion speed and Figure 4 for the effect of the control voltage on clock speed.



(12-BIT RESOLUTION)
RANGE OF ADJUSTMENT IS 10 TO 7.5µs

Figure 14. 12-Bit Clock Rate Control Optional Fine Adjust



(8- OR 10-BIT RESOLUTION)
RANGE OF ADJUSTMENT IS 8 TO 4µs FOR
10-BIT AND 6.5 TO 3µs FOR 8-BIT RESOLUTIONS

Figure 15. 8-Bit Clock Rate Control Optional Fine Adjust

MICROPROCESSOR INTERFACING

The 10μs conversion time of the ADC84/ADC85 suggests several different methods of interface to microprocessors. In systems where the AD ADC84/AD ADC85 is used for high sampling rates on a single signal which is to be digitally processed, CPU-controlled conversion may be inefficient due to the slow cycle times of most microprocessors. It is generally preferable to perform conversions independently, inserting the resultant digital data directly into memory. This can be done using direct memory access (DMA) which is totally transparent to the CPU. Interface to user-designed DMA hardware is facilitated by the guaranteed data validity on the falling edge of the EOC signal.

Clearly, 12 bits of data must be broken up for interface to an 8-bit wide data bus. There are two possible formats: right-justified and left-justified. In a right-justified system, the least-significant 8 bits occupy one byte and the four MSB's reside in the low nybble of another byte. This format is useful when the data from the ADC is being treated as a binary number between 0 and 4095. The left-justified format supplies the eight most-significant bits in one byte and the 4LSB's in the high nybble of another byte. The data now represents the fractional binary number relating the analog signal to the full-scale voltage. An advantage to this organization is that the most-significant eight bits can be read by the processor as a coarse indication of the true signal value. The full 12-bit word can then be read only when all 12 bits are needed. This allows faster and more efficient control of a process.

Figure 16 shows a typical connection of an 8085-type bus, using a left-justified data format for unipolar inputs. Status polling is optional, and can be read simultaneously with the 4LSBs. If it is desired to right-justify the data, pins 1 through 12 of the AD ADC84/AD ADC85 should be reversed, as well as the connections to the data bus and high and low byte address signals.

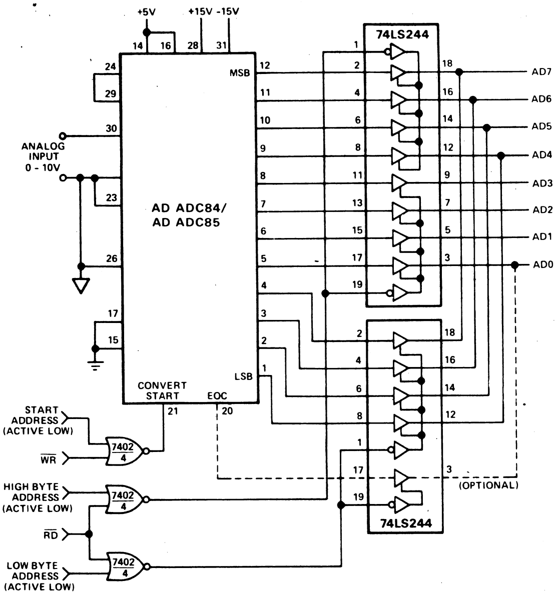


Figure 16. AD ADC84/AD ADC85-8085A Interface Connections

When dealing with bipolar inputs (±5V, ±10V ranges), using the MSB directly yields a complementary offset binary-coded output. If complementary two's complement coding is desired, it can be produced by substituting $\overline{\text{MSB}}$ (pin 13) for the MSB. This facilitates arithmetic operations which are subsequently performed on the ADC output data.

ORDERING GUIDE

Model[1]	Linearity	Temperature Range	Package	Gain T. C. – ppm/°C	Package Option[2]
AD ADC84-10	±0.048%	0 to +70°C	Ceramic	±30	HY32F
AD ADC84-12	±0.012%	0 to +70°C	Ceramic	±30	HY32F
AD ADC85C-10	±0.048%	0 to +70°C	Hermetic Ceramic	±40	HY32F
AD ADC85C-12	±0.012%	0 to +70°C	Hermetic Ceramic	±25	HY32F
AD ADC85-10	±0.048%	-25°C to +85°C	Hermetic Ceramic	±20	HY32F
AD ADC85-12	±0.012%	-25°C to +85°C	Hermetic Ceramic	±15	HY32F
AD ADC85S-10	±0.048%	-55°C to +125°C	Hermetic Ceramic	±25	HY32F
AD ADC85S-12	±0.012%	-55°C to +125°C	Hermetic Ceramic	±25	HY32F

[1] For complete model number suffixes must be added for "Z" option (±12V operation), linearity and military screening. The following guide shows the proper suffix order.
AD ADC(*)(**)-(***)/(****)

*Model Number
**"Z" Version Designator
***Linearity
****"883B" Versions

Typical Part Numbers
AD ADC84-12
AD ADC85SZ-12/883B

[2] See Section 20 for package outline information.

ANALOG DEVICES

14-Bit High Speed Analog-to-Digital Converters

ADC1130, ADC1131

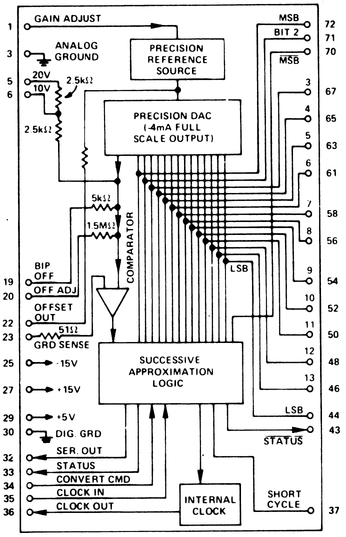
FEATURES

- **14-BIT Resolution and Accuracy**
- **Fast 12μs Conversion Time (ADC1131J/K)**
- **Low 10ppm/°C Maximum Gain TC**
- **User Choice of Input Range**
- **No Missing Codes**

APPLICATIONS

- **Wide Band Data Digitizing**
- **Multi-Channel Computer Interface**
- **High Accuracy Data Acquisition**
- **X-Ray Tomography**
- **Nuclear Accelerator Instrumentation**

ADC1130 AND ADC1131 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADC1130 and ADC1131 are high speed analog-to-digital converters packaged in a small 2" x 4" x 0.4" (51 x 102 x 10mm) module, which perform complete 14-bit conversions in 25μs and 12μs respectively. Using the successive approximations technique, they convert analog input voltages into natural binary, offset binary, or two's complement coded outputs. Data outputs are provided in both parallel and non-return-to-zero serial form.

Four analog input ranges are available: 0 to +20V, 0 to +10V, ±10V, ±5V. The user selects the desired range by making appropriate connections to the module terminals. The ADC1130 and ADC1131 can also be connected so as to perform conversions of less than 14 bit resolution with a proportionate decrease in conversion time.

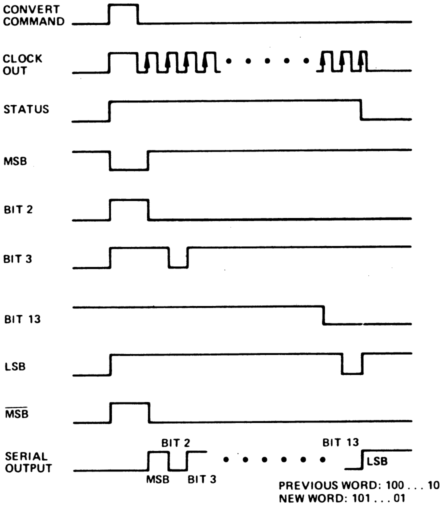
TIMING

As shown in Figure 1, the leading edge of the convert command set the MSB output to Logic "0" and the CLOCK OUT, STATUS, $\overline{\text{MSB}}$, and BIT 2 through BIT 12 outputs to Logic "1". Nothing further happens until the convert command returns to Logic "0", at which time the clock starts to run and the conversion proceeds.

With the MSB in the Logic "0" state, the internal digital-to-analog converter's output is compared with the analog input. If the D/A output is less than the analog input, the first "0" to "1" clock transition resets the MSB to Logic "1". If the D/A output is greater than the analog input, the MSB remains at Logic "0".

The first "0" to "1" clock transition also sets the BIT 2 output to Logic "0" and another comparison is made. This process continues through each successive bit until the BIT 14 (LSB) comparison is completed. At this point the STATUS and CLOCK OUT return to Logic "0" and the conversion cycle ends.

The serial data output is of the non-return-to-zero (NRZ) format. The data is available, MSB first, 20ns after each of the fourteen "0" to "1" clock transitions.



Timing Diagram

This two-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be found in Volume II, page 11-11.

SPECIFICATIONS (typical @ +25°C unless otherwise noted)

MODEL	HIGH SPEED 12µs ADC1131 J	K	MEDIUM SPEED 25µs ADC1130
RESOLUTION, BITS	14	14	14
CONVERSION TIME (max)	12µs	12µs	25µs
ACCURACY			
Integral Nonlinearity Error (LSB)	±1/2 (max)	*	*
Differential Nonlinearity Error (LSB)	±1/2 (1 max)	±1/2 (max)	±1/2 (1 max)
Missing Codes	No missing codes	*	*
TEMPERATURE COEFFICIENTS			
Gain ppm/°C	±12 (max)	±7 (+10 max)	±12 max
Unipolar Offset	±0.7 (±3 max)	*	*
Bipolar Offset	±3 (±7 max)	*	*
INPUT VOLTAGE RANGES	±5V, ±10V, +10V, +20V	*	*
INPUT IMPEDANCE (10V RANGE)	2500Ω	*	*
CONVERT COMMAND	Positive Pulse, 200ns min, 400ns max Leading Edge Resets, Trailing Edge Starts, TTL/DTL Compatible	*	*
PARALLEL DATA OUTPUT			
Unipolar	Positive True Binary	*	*
Bipolar	Positive True Offset Binary, Two's Complement	*	*
SERIAL DATA OUTPUT			
Unipolar	Positive True Binary	*	*
Bipolar	Positive True Offset Binary	*	*
STATUS OUTPUT	"1" During Conversion. Complement also available TTL/DTL Compatible.	*	*
LOGIC FANOUTS AND LOADINGS			
Convert Command Input	1TTL Unit Load	*	*
Clock Input	3TTL Unit Loads	*	*
Short Cycle Input	1TTL Unit Load	*	*
Parallel Data Outputs	3TTL Unit Loads/Bit	*	*
Serial Data Output	8TTL Unit Loads	*	*
STATUS Output	2TTL Unit Loads	*	*
$\overline{\text{STATUS}}$ Output	12TTL Unit Loads	*	*
Clock Output	4TTL Unit Loads	*	*
POWER REQUIREMENTS	+15V ±5% @ 40mA	*	*
	-15V ±5% @ 60mA	*	*
	+5V ±5% @ 250mA	*	*
POWER SUPPLY SENSITIVITY			
To ±15V Tracking Supplies			
Gain	±4.5ppm/%Δ V_S	*	*
Zero	±4.5ppm/%Δ V_S	*	*
To ±15V Non-Tracking Supplies			
Gain	±10ppm/%Δ V_S	*	*
Zero	±7ppm/%Δ V_S	*	*
TEMPERATURE RANGE			
Operating	0 to +70°C	*	*
Storage	-55°C to +85°C	*	*

*Same Specifications as ADC1131J.

NOTES:

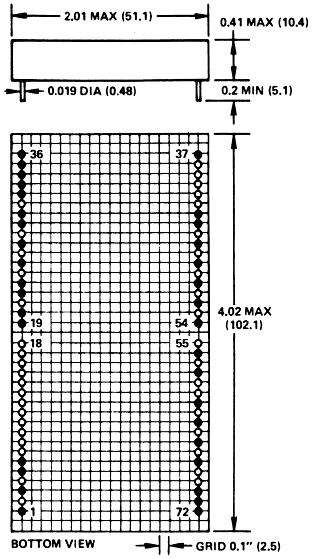
[1] Offset (zero) and gain errors are adjustable to zero by means of external potentiometers.

[2] Recommended power supply: Analog Devices model 923.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



NOTE:

Terminal pins installed only in shaded hole locations.

Module weight: 3.5 ounces (99.3 grams).

ANALOG DEVICES

Low Cost 16-Bit Analog-to-Digital Converter

ADC1140

FEATURES

Guaranteed Nonlinearity: ±0.003% FSR max
35μs Maximum Conversion Time
Small Size 2" X 2" X 0.4"
Wide Power Supply Operation: ±12V to ±17V
Low Cost

APPLICATIONS

Process Control Data Acquisition
Seismic Data Acquisition
Nuclear Instrumentation
Medical Instrumentation
Pulse Code Modulation Telemetry
Industrial Scales
Robotics

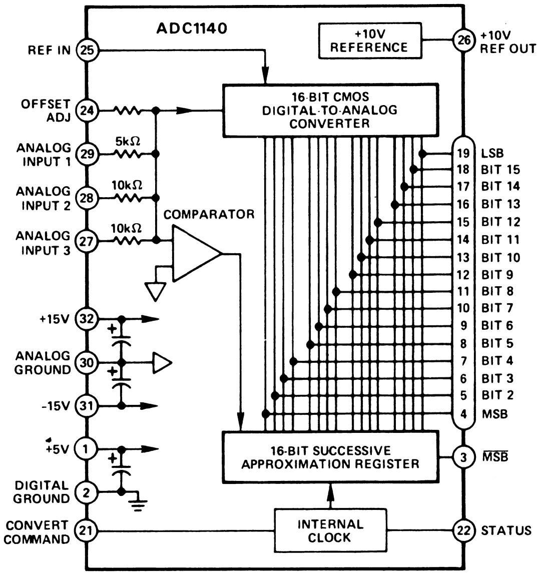
GENERAL DESCRIPTION

The ADC1140 is a low cost 16-bit successive-approximation analog-to-digital converter having a 35μs maximum conversion time. This converter provides high accuracy, high stability, and low power consumption all in a 2" X 2" X 0.4" module.

High accuracy performance such as integral, and differential nonlinearity of ±0.003% FSR max are both guaranteed. Guaranteed stability such as differential nonlinearity TC of ±2ppm/°C maximum, offset TC of ±30μV/°C maximum, gain TC of ±12ppm/°C maximum, and power supply sensitivity of ±0.002% of FSR/% V_S are also provided by the ADC1140.

The ADC1140 makes extensive use of both integrated circuit and thin-film components to obtain excellent performance, small size, and low cost. The internal 16-bit DAC incorporates Analog Devices proprietary thin-film resistor technology and proprietary CMOS current-steering switches. A low noise reference, low power comparator, and low power successive-approximation register are also used to optimize the ADC1140's design.

ADC1140 FUNCTIONAL BLOCK DIAGRAM



The ADC1140 can operate with power supplies ranging from ±12V to ±17V and has provisions for a user supplied external reference. Four analog input voltage ranges are selectable via pin programming: ±5V, ±10V, 0 to +5V and 0 to +10V. Bipolar coding is provided in the offset binary and two's complement formats with unipolar coding displayed in true binary.

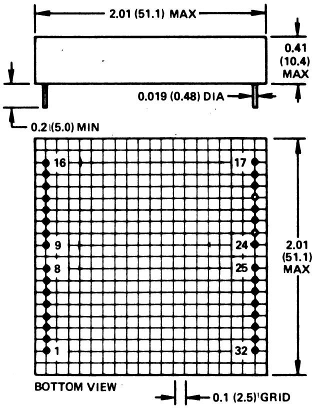
This two-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be found in Volume II, page 11-15.

SPECIFICATIONS (typical @ +25°C ±V_S = ±15V, V_{CC} = +5V, V_{REF} = +10.0V unless otherwise specified)

Model	ADC1140
RESOLUTION	16 Bits
CONVERSION TIME	35μs max
ACCURACY[1]	
Nonlinearity Error	±0.003% FSR[2] max
Differential Nonlinearity Error	±0.003% FSR[2] max
STABILITY	
Differential Nonlinearity	±2ppm/°C max
Gain (with internal reference)	±12ppm/°C max
(without internal reference)	±4ppm/°C max
Unipolar Offset	±30μV/°C max
Bipolar Offset	±7ppm/°C max
POWER SUPPLY SENSITIVITY	±0.002% FSR/% V_S
ANALOG INPUT	
Voltage Ranges	
Bipolar	±5V, ±10V
Unipolar	0 to +5V, 0 to +10V
Input Resistance	
0 to +5V	2.5kΩ
0 to +10V, ±5V	5.0kΩ
±10V	10.0kΩ
External Reference Input[3]	
Voltage Range	0 to +12V
Input Resistance	2.5kΩ
DIGITAL INPUT	
Convert Command	Positive Pulse, 100ns Width min Negative Edge Triggered
Logic Loading	1TTL Load
DIGITAL OUTPUT	
Parallel Output Data	
Unipolar	Binary (BIN)
Bipolar	Offset Binary (OBIN) Two's Complement
Output Drive	1TTL Load
Status	Logic "1" During Conversion
Output Drive	1TTL Load
INTERNAL REFERENCE VOLTAGE	+10V, ±0.3%
External Load Current (Rated Performance)	2mA max
Temperature Stability	±8.5ppm/°C max
POWER REQUIREMENTS[4]	
Voltage (Rated Performance)	±15V ±3%, +5V ±3%
Voltage (Operating)	±12V to ±17V, +4.75V to +5.25V
Supply Current Drain ±15V	±25mA
+5V	150mA
TEMPERATURE RANGE	
Specified	0 to +70°C
Operating	-25°C to +85°C
Storage	-55°C to +85°C
SIZE	2" X 2" X 0.4" (51 X 51 X 10.4mm)
Weight	1.2 oz (33g)

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



TERMINAL PINS INSTALLED ONLY IN SHADED HOLE LOCATIONS.

MATING PINS

AC1577 (2 REQUIRED)

PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	+5V	32	+15V
2	DIGITAL GROUND	31	-15V
3	$\overline{\text{MSB}}$	30	ANALOG GROUND
4	MSB	29	ANALOG IN 1
5	BIT 2	28	ANALOG IN 2
6	BIT 3	27	ANALOG IN 3
7	BIT 4	26	+10V REF OUT
8	BIT 5	25	REFERENCE IN
9	BIT 6	24	OFFSET ADJUST
10	BIT 7	23	NOT USED
11	BIT 8	22	STATUS
12	BIT 9	21	CONVERT COMMAND
13	BIT 10	20	NOT USED
14	BIT 11	19	LSB
15	BIT 12	18	BIT 15
16	BIT 13	17	BIT 14

---

[1] Offset and gain error are adjustable to zero by means of external potentiometers.

[2] FSR means Full Scale Range.

[3] Rated performance is specified with +10.0V reference.

[4] Recommended Power Supply: Analog Devices Model 923.

Specifications subject to change without notice.

ANALOG DEVICES

Ultra-Fast Hybrid Analog to Digital Converters

HAS-0802/1002/1202

FEATURES

- **Conversion Times as Low as 1.2μs**
- **Resolution: 8, 10 and 12 Bits**
- **Exceptional Accuracy, 0.012% of F.S.**
- **Low Power**
- **Contained in Glass or Metal 32-Pin DIP**
- **Adjustment-Free Operation**

APPLICATIONS

- **Waveform Analysis**
- **Fast Fourier Transforms**
- **Radar**

GENERAL DESCRIPTION

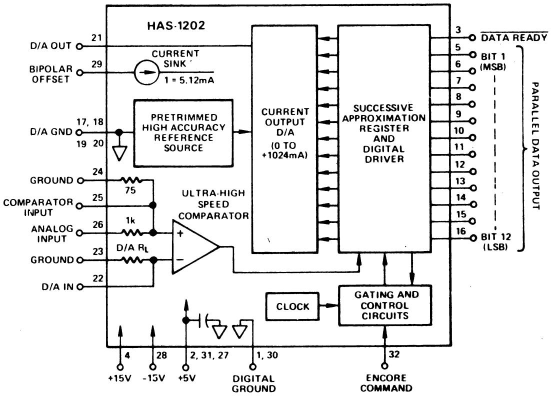
With a typical conversion time of only 2.2μs for complete 12-bit conversion, the Analog Devices' HAS series hybrid A/D converters are among the fastest, smallest, most complete successive-approximation A/D's available. Housed in 32-pin DIP packages, these converters feature laser trimming for accuracy and linearity surpassing the best modular competitive A/D's. This series offers a unique combination of flexibility and simplicity which allows them to be used as stand-alone A/D converters requiring no additional external potentiometers and needing only an analog input signal and encode command for operation.

The HAS-1202 A/D features an accuracy of 0.012% and when combined with an HTC-0300 track-and-hold, forms an A/D conversion system capable of up to 350kHz sampling rates.

The HAS series A/D's are ideally suited for applications requiring excellent performance characteristics, small size, low power consumption and adjustment-free operation. Some of these applications include radar, PCM, data-acquisition, and digital-signal-processing systems where FFT's and other digital processing techniques are to be performed on analog input data.

For the ultra-high reliability requirements of military and aerospace applications these A/D's are optionally available with hermetically sealed metal cases and with MIL-STD-883 processing.

HAS SERIES FUNCTIONAL BLOCK DIAGRAM



NOTES: 1. FUNCTIONAL CONFIGURATION SHOWN IS FOR THE HAS-1202. FOR THE HAS-1002 PINS 15 AND 16 ARE NOT CONNECTED INTERNALLY. FOR HAS-0802 PINS 13, 14, 15 AND 16 ARE NOT CONNECTED INTERNALLY.

2. FOR BIPOLAR OPERATION, CONNECT PINS 21, 22 AND 29. FOR UNIPOLAR OPERATION, CONNECT PIN 21 TO PIN 22 AND GROUND PIN 29.

Extreme care in circuit layout should be exercised when using these hybrids in order to obtain rated performance. In particular, input and output runs should be as short as possible, a ground plane should be used to tie all ground pins together, and power supplies should be bypassed as close to the hybrid circuit power supply pins as possible. Do not allow input or other analog signal lines to be in close proximity to or cross over any digital output line.

SPECIFICATIONS (typical @ +25°C with nominal voltages unless otherwise noted)

MODEL	UNITS	HAS-0802	HAS-1002	HAS-1202
RESOLUTION	BITS	8	10	12
LSB Weight	% Full Scale	0.4	0.1	0.025
	mV	40	10	2.5
RELATIVE ACCURACY (INCLUDING LINEARITY)	% Full Scale	0.05	0.025	0.012
Quantization Error	LSB	±1/2	*	*
LINEARITY VS. TEMPERATURE	ppm/°C	3 (No Missing Codes over Temperature Range)	*	*
INPUT OFFSET VOLTAGE				
Initial (Trimmable to Zero)	mV	10	*	*
Zero Offset vs. Temperature	μV/°C	15	*	*
Bipolar Offset vs. Temperature	μV/°C	100	*	*
GAIN ERROR				
Initial (Trimmable to Zero)	% Full Scale	0.1	*	*
Gain vs. Temperature	ppm/°C	30	*	*
INPUT				
Ranges (Full Scale)				
"Built-In" Standard Unipolar	V ±0.1%	+10.24	*	*
Bipolar	V ±0.05%	±5.12	*	*
Resistor Programmable (See Figure 3)	V, 0 to:	+5, +7.5, +15, +20, ±2.5, ±3.75, ±7.5, ±10		
Impedance	Ω min	1000	*	*
Overvoltage	V	Two Times Full Scale + or −		
CONVERSION TIME (COMPLETE CYCLE TIME)	μs max (typ)	1.5 (1.2)	1.7 (1.4)	2.8 (2.2)
CONVERSION RATE	kHz max	667	588	357
ENCODE COMMAND – TTL LOGIC INPUT				
Logic Levels (Positive Logic)	V	"0" = 0 to +0.4, "1" = +2 to +5		
Function[1]		Logic "1" Resets Converter Logic "0" Starts Conversion		
Loading		1 Standard TTL Load: "0" = −1.6mA, max "1" = 40μA, max		
Pulse Width	ns min	100	*	*
Repetition Rate		0 to Maximum Conversion Rate		
LOGIC OUTPUTS				
Data Ready ($\overline{DR}$)				
Function		Signals conversion is complete when low. After $\overline{DR}$ goes low, data is valid. A new conversion may be initiated at this time. $\overline{DR}$ may be used to strobe data into external register if adequate register setup time is allowed.		
Timing		See Figure 1		
Loading		5 Standard TTL Loads, max		
Parallel Data				
Format		8-, 10-, or 12-bits parallel data. Valid from time $\overline{DR}$ output goes low until 20ns after receipt of next encode command.		
Logic Levels		TTL Compatible: "0" = 0V to +0.4V "1" = +2.4V to +5V		
Loading		Will drive up to 5 Standard TTL Loads or 2 TTL "S" or "H" Loads.		
Coding[2]		Offset Binary (BIN) for Unipolar Inputs: +10.24V = 1 1 1 1 . . . . 1 0V = 0 0 0 0 . . . . 0 Offset Binary (OBN) for Bipolar Inputs: +5.12V = 1 1 1 1 . . . . 1 0V = 0 1 1 1 . . . . 1 −5.12V = 0 0 0 0 0		
POWER REQUIREMENTS				
+14.5V to +15.5V (+18V Absolute Max)	mA	40	*	*
−14.5V to −15.5V (−18V Absolute Max)	mA	15	*	*
+4.75V to +5.25V (+7V Absolute Max)	mA	200	*	*
TEMPERATURE RANGE				
Operating (Case)	°C	0 to +70	*	*
Storage	°C	−55 to +125	*	*
PACKAGE OPTION[3]	HY32A (glass package)		HY32C (metal package)	

NOTES:

[1] After converter is reset, all other logic signals, including clock, are internally generated.

[2] When HAS series A/D's are used with HTC-0300 track/hold, output coding is complementary binary (CBN) for unipolar inputs and complementary offset binary (COB) for bipolar inputs (see Table 1).

[3] See Section 20 for package outline information.

*Specifications same as model HAS-0802.
Specifications subject to change without notice.

*Table 1. Output Coding**

SCALE	INPUT OF HTC-0300	INPUT OF HAS-1202	DIGITAL OUTPUT
UNIPOLAR OPERATION			
FS-1LSB	-10.2375V	+10.2375V	111111111111
3/4 FS	- 7.6800V	+ 7.6800V	110000000000
1/2 FS	- 5.1200V	+ 5.1200V	100000000000
1/4 FS	- 2.5600V	+ 2.5600V	010000000000
+1LSB	- 0.0025V	+ 0.0025V	000000000001
0	0.0000V	0.0000V	000000000000
BIPOLAR OPERATION			
+FS-1LSB	- 5.1175V	+ 5.1175V	111111111111
0	0.0000V	0.0000V	100000000000
-FS+1LSB	+ 5.1175V	- 5.1175V	000000000001
-FS	+ 5.1200V	- 5.1200V	000000000000

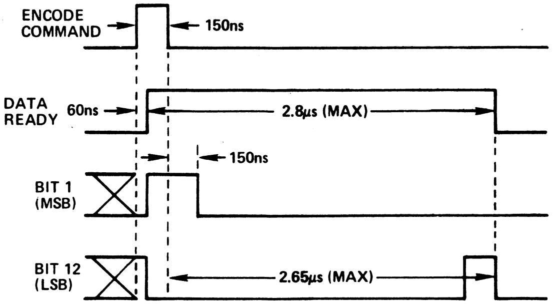
*Coding and input levels shown are for HAS-1202. For 8- and 10-bit A/D's the input levels are less by the values of the LSB weight for each type, and the digital output will show only 8 or 10 bits, respectively.

PIN DESIGNATIONS

HAS-1202*

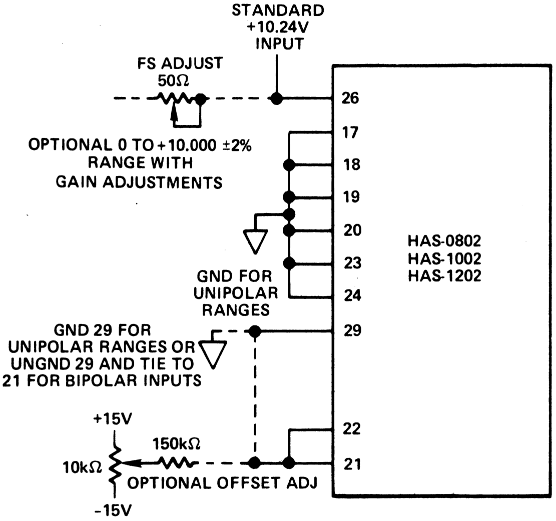
PIN	FUNCTION
1, 30	DIGITAL GROUND
2, 27, 31	+5V
3	DATA READY
4	+15V
5	BIT 1 OUTPUT (MSB)
6	BIT 2 OUTPUT
7	BIT 3 OUTPUT
8	BIT 4 OUTPUT
9	BIT 5 OUTPUT
10	BIT 6 OUTPUT
11	BIT 7 OUTPUT
12	BIT 8 OUTPUT
13	BIT 9 OUTPUT
14	BIT 10 OUTPUT
15	BIT 11 OUTPUT
16	BIT 12 OUTPUT (LSB)
17, 18, 19	ANALOG GROUND
20, 23, 24	ANALOG GROUND
21	D/A OUT
22	D/A IN
25	COMP INPUT
26	ANALOG INPUT
28	-15V
29	BIPOLAR OFFSET
32	ENCODE COMMAND

***HAS-1002, PINS 15 AND 16 ARE NOT CONNECTED INTERNALLY.
HAS-0802, PINS 13, 14, 15 AND 16 ARE NOT CONNECTED INTERNALLY.**



TIMING SHOWN FOR HAS-1202. TIMING IS SIMILAR FOR HAS-1002 AND HAS-0802 EXCEPT LSB IS BIT 10 AND 8, RESPECTIVELY, AND TOTAL TYPICAL CONVERSION TIME IS 1.4µs AND 1.2µs, RESPECTIVELY.

Figure 1. Timing Diagram (Typical)



NOTES:

1. THIS CIRCUIT SHOWN FOR UNIPOLAR (0 TO +10.24V) INPUT. 0V INPUT = 000000000000; +10.24 INPUT = 111111111111.
2. FOR BIPOLAR (±5.12V) INPUT, UNGROUND PIN 29 AND CONNECT PIN 29 TO PIN 21.
3. FOR EXTRA-PRECISE GAIN (FULL-SCALE) ADJUSTMENT, CONNECT A 50Ω VARIABLE RESISTANCE IN SERIES WITH PIN 26 OF HAS-1202. THIS WILL RESULT IN 0 TO +10.000V INPUT WITH ADJUSTMENT RANGE OF ±2% OF FULL SCALE.
4. FOR EXTRA-PRECISE ZERO OFFSET ADJUSTMENT, CONNECT 150k RESISTOR FROM PIN 21 TO THE TAP OF A 10k POTENTIOMETER. END TERMINATIONS OF POTENTIOMETER CONNECT TO +15V AND -15V. THIS ZERO OFFSET ADJUSTMENT WILL HAVE A RANGE OF APPROXIMATELY ±100mV.

Figure 2. Input Connections For Standard Input Ranges

INPUT RANGE	R1	R2	Z_{IN}	ABSOLUTE MAXIMUM SIGNAL
0 to +5V, ±2.5V	SHORT	800	500	±10V
0 to +7.5V, ±3.75V	SHORT	2500	750	±15V
0 to +15V, ±7.5V	500	OPEN	1500	±30V
0 to +20V, ±10V	1000	OPEN	2000	±40V

Input Connections For Optional Input Ranges

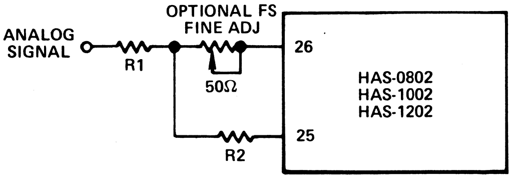


Figure 3. Full Scale Trim

APPLICATION CIRCUIT

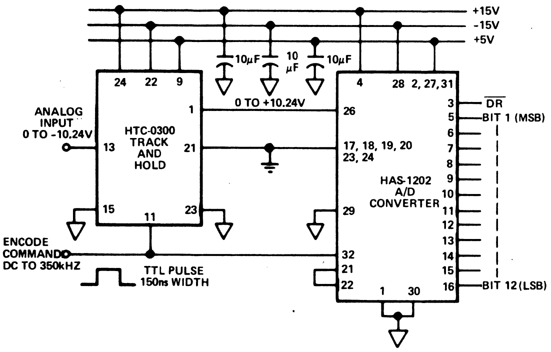


Figure 4. DC to 350kHz, 12-Bit, A/D Conversion System

ORDERING INFORMATION

Order model number HAS-0802, HAS-1002, or HAS-1202 for 8-, 10-, or 12-bit operation, respectively. Mating connector for the HAS series A/D's is model number HSA-2. Metal cased versions of this A/D with extended operating temperature range, and MIL-STD processing are also available. Consult the factory or nearest Analog Devices' sales office for further information.

ANALOG DEVICES

Ultra High Speed 8- and 10-Bit A/D Converters

MAH-0801, -1001

FEATURES

High Speed at Low Cost
8-Bits @ 750ns max
10-Bits @ 1μs max
Monotonic Over Temperature
Differential Nonlinearity ±1/4LSB typ
Parallel and Serial Outputs
Pin and Function Compatible with 4130, 4131

APPLICATIONS

High Speed Data Acquisition
Real Time Waveform Analysis
Radar Signal Processing
Analytical Instruments

GENERAL DESCRIPTION

The MAH series of high-speed analog-to-digital converters represent the latest "state-of-the-art" in high speed successive approximation technology. They are the fastest and most accurate complete converters of their type, featuring internal reference, clock, timing, encoding, and control logic functions. The MAH series A/Ds should be considered in applications where completeness of design function, ease of interface, and speed are required. These modules make maximum use of the latest monolithic and hybrid parts to minimize total parts complexity and increase reliability. They are designed to be form, fit, and function compatible with the T.P. 4130 and 4131, with advantages over the latter in overall accuracy without any sacrifice in speed.

In almost all applications, these A/Ds require the use of fast sample-and-hold. Depending upon the application, either the ADI THC or THS series of ultra-fast sample-and-holds are recommended.

ORDERING INFORMATION

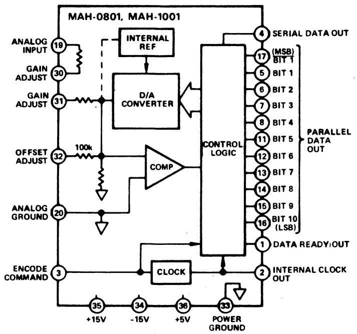
The 8- and 10-bit versions of the MAH series may be ordered with various options according to the chart below.

MAH-0801 -1

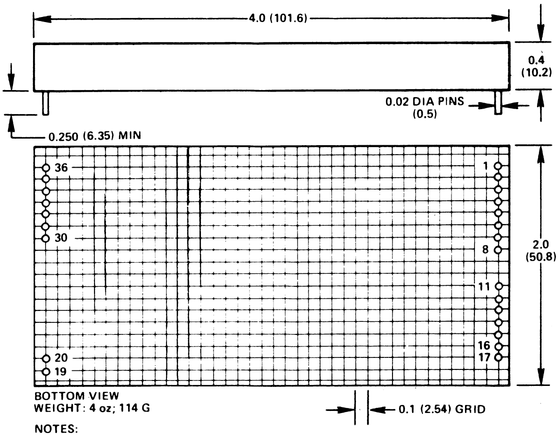
RESOLUTION AND ACCURACY	ANALOG INPUT RANGE
MAH-0801 = 8 Bits	-1 0 to -5V FS
MAH-1001 = 10 Bits	-2 0 to -10V FS
	-3 ±5V FS
	-4 ±10V FS
	-5 ±1.024V FS

This two-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be found in Volume II, page 11-19.

MAH-0801, MAH-1001 FUNCTIONAL BLOCK DIAGRAM



NOTES:
1. ON MODEL MAH-0801, PINS 15 AND 16 ARE UNUSED.
2. ANALOG AND POWER GROUNDS ARE CONNECTED TOGETHER INTERNALLY.



BOTTOM VIEW
WEIGHT: 4 oz; 114 G

NOTES:
SOME MODELS DO NOT USE ALL PIN OUTS. IN THESE CASES, UNUSED PINS ARE DELETED.
PINS ARE GOLD PLATED
DOT ON TOP INDICATES POSITION OF PIN 1

MATING CONNECTOR: MSA-1

SPECIFICATIONS (typical @ +25°C unless otherwise noted)

MODEL	UNITS	MAH-0801	MAH-1001
RESOLUTION FS @ Full Scale	Bits	8	10
ACCURACY (Relative to Full Scale)	±% FS	0.02	*
Quantization Error	LSB	±1/2	*
Nonlinearity	LSB (max)	±1/4	±1/2
Differential Nonlinearity	LSB (max)	±1/4	±1/2
	LSB (typ)	±1/8	±1/4
Missing Codes		No Missing Codes 0 to +70°C	
Monotonicity		Monotonic 0 to +70°C	
TEMPERATURE COEFFICIENTS			
Differential Nonlinearity	±ppm/°C	3	*
Gain	±ppm/°C	20	*
Zero Offset (Unipolar)	±µV/°C	10	*
Zero Offset (Bipolar)	±ppm/°C	15	*
INPUT			
Ranges (Full Scale)			
MAH-XXXX-1	V	0 to -5	*
MAH-XXXX-2	V	0 to -10	*
MAH-XXXX-3	V	±5	*
MAH-XXXX-4	V	±10	*
MAH-XXXX-5	V	±1.024	*
Impedance (Function of Option)	Ω/V	100	*
OVERVOLTAGE	V	To Twice Peak Input FS Without Damage.	
CONVERSION TIME[1]	ns max	750	1000
	ns typ	700	950
ENCODE COMMAND			
Logic Levels (1 Standard TTL Load)	V	"0" = 0 to +0.4, "1" = +2 to +5.5	
Function		Positive-going edge resets converter. Trailing edge starts conversion.	
Duration (Width)	ns min (max)	50 (150)	*
Rise and Fall Times	ns max	20	*
Repetition Rate	kHz max	1333	1000
LOGIC OUTPUTS			
Levels TTL (Same as Encode Command)			
Drive Capability		Data and Data Ready—10 Std TTL Loads, Clock—10 TTL Loads	
Parallel Data		8 or 10 lines of data held until start of next Encode Command	
Coding (Unipolar)		CBN	*
(Bipolar)		COB/C2SC	*
Serial Data		MSB first, successive pulse output during conversion, NRZ.	
Coding		Same as parallel output except 2SC not available.	
Clock		Pulse train of 9 or 11 internal clock pulses, gated on during the conversion period.	
POWER REQUIREMENTS			
+14.5V to +15.5V	mA max	50	*
-14.5V to -15.5V	mA max	30	*
+5V ±5%	mA max	250	*
TEMPERATURE RANGE			
Operating	°C	0 to +70	*
Storage	°C	-55 to +85	
PHYSICAL CHARACTERISTICS			
Case		Diallyl Phthalate per MIL-M-14 Type SDG-F	

NOTE:

[1] Total conversion time from leading edge of encode command pulse to trailing edge of data ready pulse with 50ns wide encode command.

*Specifications same as MAH-0801.

Specifications subject to change without notice.

ANALOG
DEVICES

Ultra High Speed 8-, 10-, and 12-Bit A/D Converters

MAS-0801, -1001, -1202

FEATURES

High Speed at Low Cost
- **8 Bits 1μs max**
- **10 Bits 1.5μs max**
- **12 Bits 2μs max**

No Missing Codes Over Temperature
Low Power
Industry Standard Pin Out
Parallel and Serial Outputs

APPLICATIONS

High Speed Data Acquisition
Real Time Waveform Analysis
Radar Signal Processing
Analytical Instruments

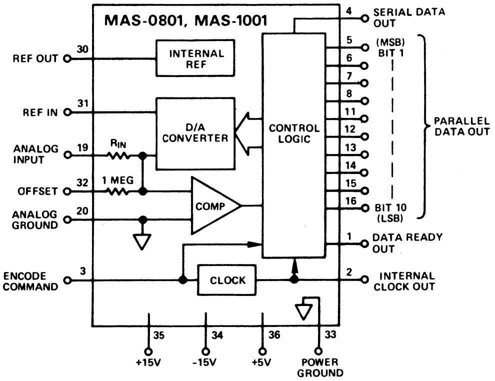
GENERAL DESCRIPTION

The MAS series of high speed analog to digital converters represent the "state of the art" in application of the successive approximation conversion technique by providing highest speed at lowest cost. With monotonicity guaranteed over temperature these reliable modules are form, fit and function compatible with popular industry standards from Datel and Philbrick (for new designs consider the HAS series of hybrid converters).

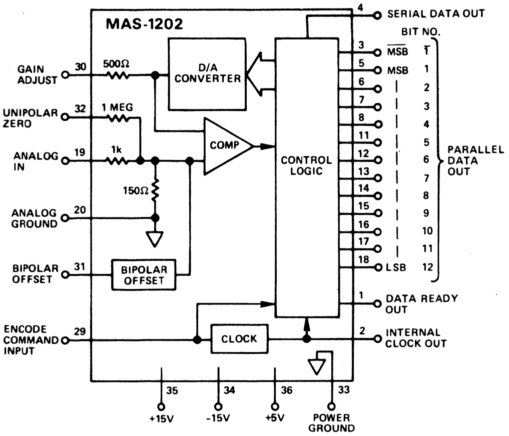
In most applications these A/Ds should be used with a fast sample hold such as the THS/THC series.

This two-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be found in Volume II, page 11-23.

MAS-0801, MAS-1001 FUNCTIONAL BLOCK DIAGRAM

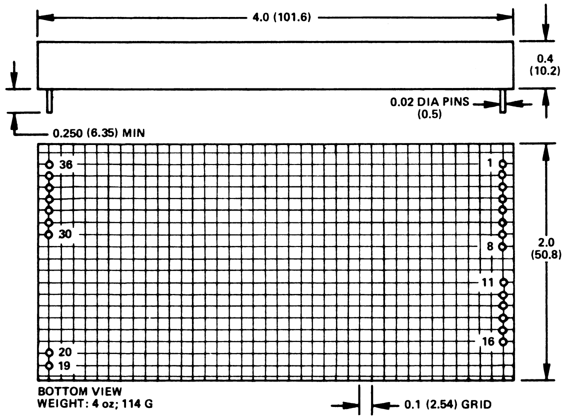


MAS-1202 FUNCTIONAL BLOCK DIAGRAM



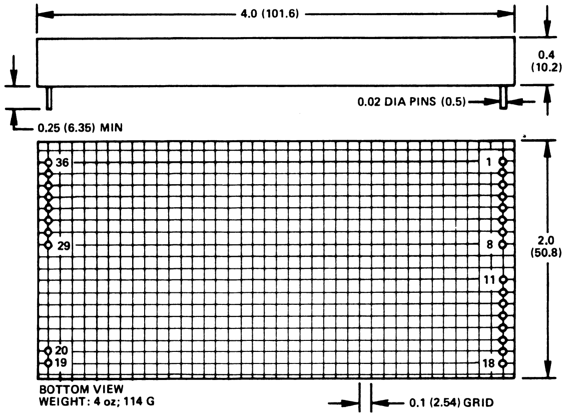
MAS-0801, MAS-1001 OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



MAS-1202 OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



SPECIFICATIONS (typical @ +25°C unless otherwise noted)

Model	Units	MAS-0801	MAS-1001	MAS-1202
RESOLUTION FS = Full Scale	Bits	8	10	12
ACCURACY (Relative to Full Scale)	±% FS	0.2	0.05	0.012
Quantization Error	LSB	±1/2	*	*
Nonlinearity	LSB (max)	±1/2	*	*
Differential Nonlinearity	LSB (max)	±1/2	*	*
Missing Codes		No Missing Codes 0 to +70°C		
TEMPERATURE COEFFICIENTS				
Differential Nonlinearity	±ppm/°C	3	*	*
Gain	±ppm/°C	20	*	30
Gain (Option-P)	±ppm/°C	5	*	NA
Zero Offset (Unipolar)	±μV/°C	10	*	100
Zero Offset (Bipolar)	±ppm/°C	15	*	*
Zero Offset (Option-P)	±ppm/°C	5	*	NA
INPUT				
Ranges (Full Scale)	Options MAS-0801 and MAS-1001 ONLY			STANDARD
MAS-XXXX-1	V	0 to -5	*	0 to +10/±5
MAS-XXXX-2	V	0 to -10	*	NA
MAS-XXXX-3	V	±5	*	NA
MAS-XXXX-4	V	±10	*	NA
MAS-XXXX-5	V	±1.024	*	NA
Impedance (Function of Option)	Ω/V	100	*	1150Ω
OVERVOLTAGE	V	To Twice Peak Input FS Without Damage.		
CONVERSION TIME[1]	μs max	1	1.5	2
	μs typ	0.8	1.3	1.8
ENCODE COMMAND				
Logic Levels (1 Standard TTL Load)	V	"0" = 0 to +0.4, "1" = +2 to +5.5		
Function		Positive-going edge resets converter, Trailing edge starts conversion for 8- and 10-bit versions.		
Duration (Width)	ns min	50	*	100
Rise and Fall Times	ns max	20	*	*
Repetition Rate	kHz max	1000	666	500
LOGIC OUTPUTS				
Levels TTL (Same as Encode Command)				
Drive Capability		Data and Data Ready – 4 Std TTL Loads, Clock – 6TTL Loads		
Parallel Data		8, 10 or 12 lines of data held until next Encode Command		
Coding (Unipolar)		CBN	*	BIN
(Bipolar)		COB/2SC	*	OBN/2SC
Serial Data		MSB first, successive pulse output during conversion, NRZ.		
Coding		Same as parallel output except 2SC not available.		
Clock		Pulse train of 9, 11 or 13 internal clock pulses, gated on during the conversion period.		
POWER REQUIREMENTS				
+14.5V to +15.5V	mA	70	*	80
-14.5V to -15.5V	mA	30	*	20
+5V ±5%	mA	150	*	*
TEMPERATURE RANGE				
Operating	°C	0 to +70	*	*
Storage	°C	-55 to +85	*	*
PHYSICAL CHARACTERISTICS				
Case		Diallyl Phthalate per MIL-M-14 Type SDC-F		

NOTE:

[1] Total conversion time from leading edge of encode command pulse to trailing edge of data ready pulse with 50ns wide encode command.

*Specifications same as MAS-0801.

Specifications subject to change without notice.

ANALOG DEVICES

8-Bit Video Analog-to-Digital Converter

MATV-0811, -0816, -0820

FEATURES

- 8-Bit Accuracy – Guaranteed Monotonic
- Ultra-High Speed – dc to 20MHz Word Rates
- Most Economical Video A/D
- Smallest Available Complete A/D – 5.5" X 4.38" X 0.85"
- Self Contained – Includes Input Buffer, Encoder, Reference, Timing, and Buffered Parallel Output

APPLICATIONS

- Digitize Color Television at Up to Three or Four Times NTSC or PAL Color Subcarrier Frequencies
- Video Time Base Correction and Frame Synchronization
- Radar Signal Processing
- Real Time Transient and Continuous Spectrum Analysis

GENERAL DESCRIPTION

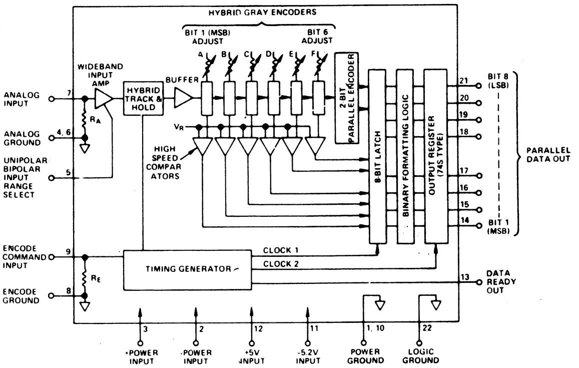
The Analog Devices' MATV series of A/D converters represent a major breakthrough in high-speed A/D technology. Providing conversion word rates from dc to 11MHz, 16MHz and 20MHz the MATV-0811, MATV-0816 and MATV-0820 are the lowest cost A/D converters in their performance class. As complete devices, they require only the addition of external power to accomplish precision video A/D conversion.

The use of internal hybrid microcircuit construction allows these modular A/D's to occupy a volume of only 21 cubic inches–about 1/5 the volume of available comparable devices. They are housed in metal cases which not only shield the circuits from external RF interference, but aid in efficient heat dissipation. A choice of analog input voltages is available, including the industry standard 0 to +1V at 75Ω. The encode command input, data ready output, and the digital bit outputs are all TTL compatible. Designed to operate from either ±12V or ±15V analog and +5V digital supplies (MATV-0811 and MATV-0816 also require -5.2V), the MATV series dissipate less than 8 watts. Their weight is < 10 ounces due to enclosure rather than encapsulation. This technique facilitates rapid, inexpensive factory repair and aids in reliable printed circuit board mounting by the customer without extensive mechanical constraints or system engineering.

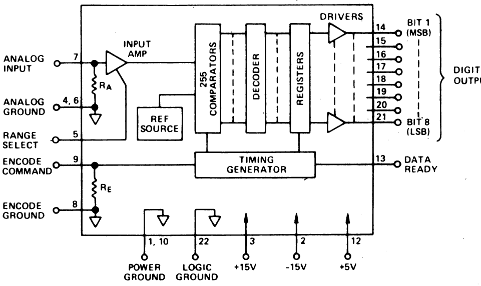
Relative dc accuracy is 0.2% of full scale ±1/2LSB when operating over the frequency range of dc to 20MHz. The MATV series is designed to digitize color television signals at rates up to 20MHz and is also ideally suited for other analog to digital conversion requirements, such as radar signal processing, laser pulse analysis, transient analysis, and medical electronics applications where real-time analysis and display of large quantities of information are required.

This two-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be found in Volume II, page 11-27.

MATV-0811, MATV-0816 FUNCTIONAL BLOCK DIAGRAM



MATV-0820 FUNCTIONAL BLOCK DIAGRAM



R_A AND R_E ARE DETERMINED BY THE ANALOG INPUT IMPEDANCE AND ENCODE COMMAND INPUT IMPEDANCE, RESPECTIVELY.

ORDERING INFORMATION

Each MATV series A/D converter will be calibrated at ±15V as a standard. Order by model number either MATV-0811, MATV-0816 or MATV-0820.

Optional Versions

The MATV series A/D's are available with a variety of options, including analog input range and impedance, encode command input impedance, encode word rate, power supply voltage calibration, etc. Any option other than what is shown on the data sheet will have longer delivery, since each non-standard device is built on a per order basis.

A complete listing of optional designators is available from either the factory or your local Analog Devices' sales office.

SPECIFICATIONS (typical @ +25°C and nominal power supply voltages unless otherwise noted)

MODEL	UNITS	MATV-0811	MATV-0816	MATV-0820
RESOLUTION (FS = Full Scale)	Bits/% FS	8/0.4	*	*
LSB Weight	% FS	0.4	*	*
ACCURACY (relative) at dc	typ	±0.15% ±1/2LSB	*[1]	*
	max	±0.2% ±1/2LSB	*[1]	*
Monotonicity		GUARANTEED	*	*
Differential Nonlinearity vs Temperature	% FS/°C	0.01	*	0.005
Linearity and Gain vs Temperature	% FS/°C	0.02	*	0.01
DYNAMIC CHARACTERISTICS				
AC Linearity @ Encode Rate[2]	MHz	11	15	20
Analog Input Frequency				
DC to 3.6MHz	Spurious Signals are > dB below FS	50	*	*
3.6MHz to 5.5MHz		45	*	*
Conversion Rate (Encode Word Rate)	MHz max	11	16[1]	20
Conversion Time[3]	ns	150±20	120±20	35 ±10 + l/Encode Rate
Aperture Uncertainty (Jitter)	ps max	±30	*	*
Aperture Time	ns	3	*	12
Signal to Noise Ratio				
(rms signal to rms noise)	dB min	48	*	*
(peak signal to rms noise)	dB min	58	*	*
Noise Power Ratio[4]	dB min	37	*	*
Transient Response[5]	ns	50	*	*
Overvoltage Recovery Time[6]	ns	60	*	*
Differential Gain[7]	%	3	*	*
Differential Phase	Degrees	1	*	*
Bandwidth				
Small Signal 3dB	MHz	20	*	*
Large Signal 3dB	MHz	15	*	*
Flat ±0.1dB, dc through	MHz	5.5	*	*
INPUT[8]				
Voltage Range				
Unipolar (Pin 5 Grounded)	V	0 to 1	*	*
Bipolar (Pin 5 open)	V	±0.5	*	*
Impedance (Terminated to Ground)	Ω	75	*	*
ENCODE COMMAND INPUT[8]				
Logic Levels, TTL Compatible		"0" = 0 to +0.4V	*	*
		"1" = +2.4V to +5V	*	*
Impedance (terminated to ground)	Ω	75 ±5%	*	*
Rise and Fall Times (10% to 90%) max	ns	10	*	*
Duration/Width 50% points (see timing diagram)	ns min	10	*	20
Frequency (random or periodic)	ns max	50% duty cycle	40	*
	dc to MHz	11	16	20
DIGITAL DATA OUTPUT[8]				
Format		Eight Parallel Bits NRZ		
Logic Levels, TTL		(Same as Encode Command)		
Drive Capability (not short circuit protected)	TTL Loads	10 Std	10 Schottky	
Time Skew	ns max	15	10	10
Coding		Straight Binary (BIN)		
DATA READY OUTPUT				
Format[9]		RZ	*	*
Logic Levels, TTL		(Same as Encode Command)		
Drive Capability		10 Std	10 Schottky	
Width	ns	40±10	35±5	25±5
POWER REQUIREMENTS[10]				
MATV-0811, MATV-0816/MATV-0820				
+15V ±2%/+11.8V to +15.5V	mA max	210	*	70
-15V ±2%/-11.8V to -15.5V	mA max	180	*	400
+5V ±5%/+5V +5%	mA max	450	540	200
-5.2V ±5%	mA max	280	*	N/A
TEMPERATURE RANGE				
Operating (case)	°C	0 to +70	*	*
Storage	°C	-55 to +85	*	*

*Same as MATV-0811.

NOTES:

[1] Applies to a customer specified operating frequency, ±10%. Outside this range, accuracy may degrade to ±0.3% ±1/2LSB.

[2] AC linearity expressed in terms of spurious in-band signals generated at specified encode rates.

[3] Pipeline delay not related to encode rate.

[4] DC to 5MHz while noise BW with slot frequency at 500kHz.

[5] Time to achieve 8-bit (0.2%) accuracy after F.S. step input.

[6] For signals not exceeding 10% overvoltage, the A/D will recover to 8-bit accuracy within 60ns after the signal returns to the specified range. Overvoltage inputs greater than 150% of F.S. may damage input circuits and should be avoided.

[7] At maximum encode rate, 20 IRE unit subcarrier, not including quantization effects.

[8] Consult factory for other voltage, impedance and logic level options.

[9] The leading edge of the data ready pulse occurs approximately 10ns before output data changes. The trailing edge is recommended for strobing data into external circuits.

[9] For MATV-0811, the leading edge of the Data Ready pulse occurs approximately 15ns before output data changes. The trailing edge is recommended for strobing data into external circuits.

For MATV-0816, the leading edge of the Data Ready pulse occurs approximately 10ns before output data changes. The trailing edge is recommended for strobing data into external circuits.

For MATV-0820, the leading edge of the Data Ready pulse occurs approximately simultaneously with output data changes. The trailing edge is recommended for strobing data into external circuits. This provides a minimum of 20ns set-up time for external registers.

[10] The A/D's are calibrated at the factory at either ±12V or ±15V as a no-cost option. Other operating voltages within this range may be specified by the user at slight additional cost.

Specifications subject to change without notice.

ANALOG DEVICES

10-Bit Video Analog to Digital Converter

MOD-1005

FEATURES

10 Bits @ 5MHz Word Rate
One-27 Sq. In. PC Board
Built-In Track-and-Hold – 25ps Aperture Uncertainty
20MHz Analog Input Bandwidth
TTL Compatible
Low (10-Watt) Power Dissipation
Signal-To-Noise Ratio Greater Than 58dB
Noise Power Ratio Greater Than 49dB
Completely Repairable

APPLICATIONS

Radar Digitizing
Digital Communications
Real Time Spectrum Analysis
High Resolution TV

GENERAL DESCRIPTION

Analog Devices' model MOD-1005 is a very high-speed A/D converter capable of digitizing video input signals to 10-bit accuracy at random or periodic word rates of dc through 5MHz. The MOD-1005 is truly a breakthrough in high-speed A/D technology. It is the most cost effective A/D in this speed category, combining small size and low power dissipation with low cost.

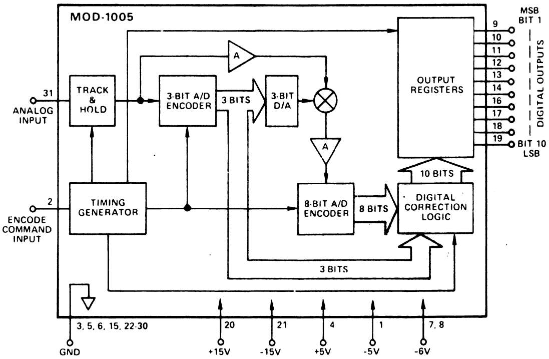
The MOD-1005 is constructed on a single printed circuit card which is intended for mounting on a system mother-board, and occupies only 27 square inches. Within this A/D is the required sample/track and hold amplifier, encoder, timing circuits and output latches for a true simultaneous, all-parallel digital output.

The encode command input and digital outputs are TTL compatible. The A/D requires only an external encode command pulse and external power supplies for operation. NO external parts are required. Gain and offset potentiometers are provided on the card. The A/D is fully repairable either at the factory or in the field.

The MOD-1005 is ideally suited for systems requiring the ultimate in conversion speed and accuracy. Such applications include radar digitizing, digital communications, spectrum analysis, and many others. Each MOD-1005 is backed by Analog Devices' limited one year warranty.

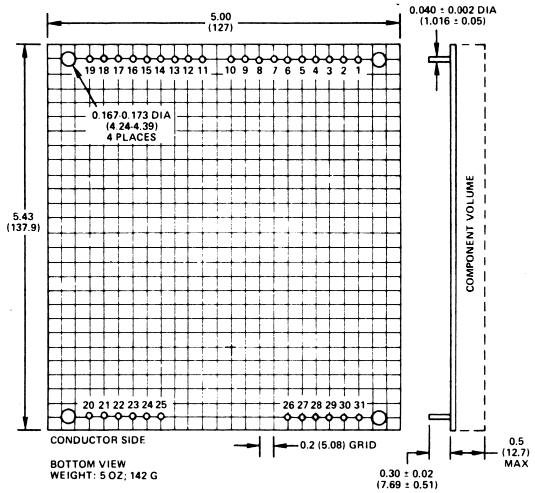
This two-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be found in Volume II, page 11-31.

MOD-1005 FUNCTIONAL BLOCK DIAGRAM



OUTLINE DIMENSIONS

Dimensions shown in inches (mm).



ORDERING INFORMATION

Order model number MOD-1005 A/D converter. Mating pin sockets for the MOD-1005 are model number MSB-2 (31 required per A/D).

SPECIFICATIONS (typical @ +25°C with nominal power supplies unless otherwise noted)

MODEL	MOD-1005
RESOLUTION (FS = FULL SCALE)	10 Bits (0.1% FS)
LSB WEIGHT	4mV
ACCURACY (INCLUDING LINEARITY) @ DC	±0.05% Full Scale ±1/2LSB
Monotonicity	Guaranteed
Differential Nonlinearity vs. Temperature	0.0005% of FS/°C
Gain vs. Temperature	0.01% of FS/°C
DYNAMIC CHARACTERISTICS	
AC Linearity[1]	Spurious Signals >59dB below FS
Conversion Time	See Text
Conversion Rate (Word Rate)	dc to 5MHz
Aperture Uncertainty (Jitter)	±25ps max
Aperture Time	45ns (±10ns from unit to unit)
Signal to Noise Ratio (rms signal to rms noise)	58dB min at 500kHz analog input
Noise Power Ratio[2]	49dB min
Transient Response (Full Scale Step Input)	10-Bit (0.05%) Accuracy within 50ns
Overvoltage Recovery Time Recovers to 10-bit accuracy after 2 X FS input overvoltage in	200ns
Input Bandwidth (small signal, 3dB)	20MHz min
Input Bandwidth (large signal, 3dB)	15MHz min flat within ±0.1dB, dc through 5MHz
INPUT	
Voltage Range	±2.048V FS ±4V Absolute max
Impedance	50Ω
Offset Voltage	Adjust to 0 with On Board Potentiometer
Offset vs. Temperature	0.01% Full Scale/°C
Bias Current	1nA max
ENCODE COMMAND INPUT	
Logic Levels, TTL Compatible	"0" = 0 to +0.4V "1" = +2.4V to +5V
Logic Loading	2 Standard TTL Gates
Rise and Fall Times	10ns max
Duration Min/Max	20ns/60% of Duty Cycle
Frequency (Random or Periodic)	dc to 5MHz
Sample Delay	45ns (unit to unit tolerance is ±10ns)
DIGITAL DATA OUTPUT	
Format	10 Parallel Bits, NRZ
Logic Levels, TTL Compatible	"0" = 0 to +0.4V "1" = +2.4V to +5V
Drive (Not Short Circuit Protected)	Up to 1 Schottky TTL or 2 Standard TTL Loads
Time Skew	10ns max
Coding	2's Complement (2SC)
Conversion Time	See Text on the Next Page
POWER REQUIREMENTS	typ/max
+15V ±5%	150/170mA
-15V ±5%	150/170mA
-6V ±4%	300/350mA
+5V ±5%	350/400mA
-5V ±5%	500/550mA
Power Consumption	10 Watts
TEMPERATURE RANGE	
Operating	0 to +70°C
Storage	-55°C to +85°C
Cooling Requirements	100 Linear Feet Per Min (LFPM)
PHYSICAL CHARACTERISTICS	
Construction	Single Printed Circuit Card

NOTES:

[1] AC linearity expressed in terms of spurious in-band signals generated as specified encode rates, with dc to 2.5MHz analog input.

[2] DC to 2.4MHz white noise BW with Slot frequency of 512kHz.

Specifications subject to change without notice.

ANALOG DEVICES

10-Bit Video Analog to Digital Converter

MOD-1020

FEATURES

10-Bits @ 20MHz Word Rates
One 35 Sq. In. PC Board
Built-In Track-and-Hold – 25ps Aperture
15MHz Large-Signal Input Bandwidth
ECL Compatible
Signal-to-Noise Ratio Greater Than 56dB
Noise Power Ratio Greater Than 45dB

APPLICATIONS

Television Digitizing
Radar Digitizing
Medical Instrumentation
Digital Communications
Spectrum Analysis
Sonar Digitizing

GENERAL DESCRIPTION

The Analog Devices' model MOD-1020 is an ultra-high-speed A/D converter capable of digitizing video input signals to 10-bit accuracy at word rates through 20MHz. The MOD-1020 is another in the series of state-of-the-art A/D converters from Analog Devices that employs the unique digital correcting subranging (DCS) conversion technique to virtually eliminate errors normally associated with subranging type A/D converters. No other A/D converter commercially available offers the user the speed and accuracy attainable with the MOD-1020.

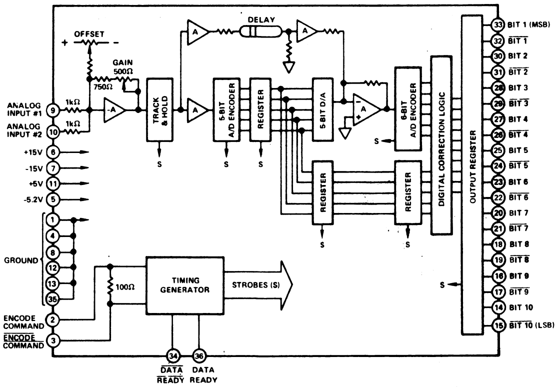
The MOD-1020 is constructed on a single printed circuit card which is intended for mounting on a system mother board and occupies only 35 square inches. The A/D is complete with internal track-and-hold, encoder, timing circuitry, references, and latched output. It produces a true all-parallel digital output.

The encode command input, digital outputs, and data ready output are balanced ECL compatible. The A/D requires only an external encode command input pulse and external power supplies for operation. The analog input impedance is at least 500Ω, so that the user can easily terminate the A/D with lower impedances in his system. Gain and offset potentiometers are provided on the card so that the A/D can be operated in either the unipolar or bipolar modes. The A/D is fully repairable.

The MOD-1020 is ideally suited for systems requiring the ultimate in conversion speed and accuracy. Such applications include radar digitizing, digital communications (baseband digitizing), composite color television digitizing, spectrum analysis, medical instrumentation, and many others. Each MOD-1020 is backed by Analog Devices' limited one-year warranty.

This two-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be found in Volume II, page 11–35.

MOD-1020 FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

IMPORTANT–THE ENCODE RATE OF THE MOD-1020 MUST BE SPECIFIED BY THE CUSTOMER AS SHOWN BELOW:

ORDER MODEL NUMBER: MOD-1020- "XXX", where "XXX" is to be specified by the customer. "XXX" represents the encode word rate in MHz with the decimal place assumed to be (but not shown) between the second and third places. Full 10-bit accuracy will be maintained within ±12% of this specified frequency, up to a maximum of 21MHz. For example, a device specified as MOD-1020-200 is for operation at 20.0MHz and will maintain accuracy from 17.6MHz to 21MHz.

For encode rates of 10MHz or less, the MOD-1020 will maintain full accuracy from dc to 10MHz. For encode frequencies of 10MHz or less, order MOD-1020-100.

Mating sockets for the MOD-1020 are model number MSB-2 (36 required per A/D).

SPECIFICATIONS (typical @ +25°C with nominal power supplies unless otherwise noted)

MODEL	MOD-1020
RESOLUTION (FS = FULL SCALE)	10 Bits (0.1% FS)
LSB WEIGHT	1mV or 2mV Depending on Analog Input Range
ACCURACY (INCLUDING LINEARITY) @ DC	±0.05% Full Scale ±1/2LSB
Monotonicity	Guaranteed 0 to +70°C
Nonlinearity vs. Temperature	0.0005% of FS/°C
Gain vs. Temperature	0.015% of FS/°C
DYNAMIC CHARACTERISTICS	
AC Linearity[1] (dc to 1MHz)	Spurious Signals ≥60dB below FS
(1MHz to 5MHz)	Spurious Signals ≥55dB below FS
(5MHz to 10MHz)	Spurious Signals ≥50dB below FS
Conversion Time	See Text and Timing Diagram
Conversion Rate[2]	dc to 20MHz (See Note and Ordering Information)
Aperture Uncertainty (Jitter)	±25ps max
Aperture Time (Delay)	5ns (±2ns unit-to-unit tolerance)
Signal to Noise Ratio[3]	56dB min
Signal to Noise Ratio[4]	65dB min
Noise Power Ratio[5]	45dB min, 47dB typ
Transient Response[6]	50ns
Overvoltage Recovery[7]	50ns
Input Bandwidth (small signal, 3dB)[8]	30MHz
Input Bandwidth (large signal, 3dB)[9]	15MHz; Flat within 0.2dB, dc to 10MHz
Two-Tone Linearity (@ Input Frequency);	
60kHz; 62kHz	In-Band Spurious Signals ≥60dB below FS
4.998MHz; 5.000MHz	In-Band Spurious Signals ≥55dB below FS
9.996MHz; 9.998MHz	In-Band Spurious Signals ≥50dB below FS
Differential Gain[10]	1% with 20 IRE Unit Reference
Differential Phase[10]	0.5° with 20 IRE Unit Reference
ANALOG INPUT	
Voltage Range	1V p-p or 2V p-p, Depending on Hook-Up Either Unipolar or Bipolar ±4V Absolute max Input
Impedance	1000Ω (2V Input Range) 500Ω (1V Input Range)
Offset	Adjustable to Zero with On-Card Potentiometer (R4)
Offset vs. Temperature	0.01%/°C
ENCODE COMMAND INPUT	
Logic Levels, ECL Compatible	"0" = -1.7V
(Balanced Input)	"1" = -0.9V
Impedance	100Ω Line-to-Line
Rise and Fall Times	5ns max
Duration (min/max)	10ns/70% of Duty Cycle
Frequency	Specified by Customer, dc to 20MHz (See Ordering Information)
DIGITAL OUTPUT DATA	
Format	10 Parallel Bits, NRZ
Logic Levels, ECL Compatible	"0" = -1.7V
(Balanced Outputs)	"1" = -0.9V
Drive	75Ω to 100Ω, Line-to-Line
Time Skew	5ns max
Coding	Binary (BIN); 2's Complement (2SC)
DATA READY OUTPUT	
Logic Level, ECL Compatible	"0" = -1.7V
(Balanced Output)	"1" = -0.9V
Rise and Fall Times	5ns max
Duration	25ns ±3ns
Conversion Time	Output data is valid two clock perios plus 185 ±20ns after the application of an initial Encode Command pulse—assuming that two pulses occur after the first. Use of the trailing edge of the Data Ready pulses are required to shift the data to the output. For example, with a 20MHz encode rate, data is valid 285 ±20ns after the application of the first Encode Command pulse—assuming that two pulses occur after the first. Use of the trailing edge of the Data Ready pulse is recommended for strobing output data into external registers.
POWER REQUIREMENTS	
+15V ±5%	200mA
-15V ±5%	200mA
+5V ±5%	100mA
-5.2V ±5%	2.7A
Power Consumption	21 Watts
TEMPERATURE RANGE	
Operating	0 to +70°C
Storage	-55°C to +85°C
Cooling Requirements	500 Linear Feet per Minute (LFPM)
PHYSICAL CHARACTERISTICS	
Construction	Single Printed Circuit Card

NOTES:

[1] AC linearity expressed in terms of spurious in-band signals generated at 20MHz encode rate at the analog frequencies ( ) shown.

[2] To be specified by the customer. See text and ordering information.

[3] RMS signal to rms noise ratio with 500kHz analog input.

[4] Peak-to-peak signal to rms noise ratio with 500kHz analog input.

[5] DC to 8.2MHz white noise bandwidth with slot frequency of 3.886MHz and an encode rate of 20MHz.

[6] Recovers to 10-bit accuracy after 2 X FS input overvoltage in time specified.

[7] For full-scale step input, attains 10-bit accuracy in time specified.

[8] With analog input signal 40dB below FS.

[9] With FS analog input.

[10] Applies to devices optimized for video applications. Differential gain and phase are measured and optimized for ADC's which have the following encode rate optional designators (see Ordering Information): "107" (3 X NTSC subcarrier); "133" (3 X PAL); "143" (4 X NTSC); "177" (4 X PAL).

Specifications subject to change without notice.

ANALOG DEVICES

12-Bit Video Analog to Digital Converter

MOD-1205

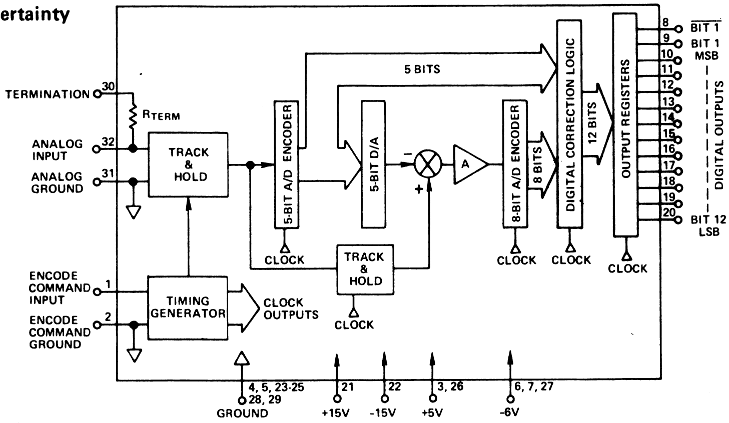
FEATURES

12 Bits @ 5MHz Word Rate
One-27 Sq. In. PC Board
Built-In Track-and-Hold – 25ps Aperture Uncertainty
15MHz Analog Input Bandwidth
TTL Compatible
Low (13-Watt) Power Dissipation
Signal-to-Noise Ratio Greater Than 66dB
Noise Power Ratio Greater Than 56dB
Completely Repairable

APPLICATIONS

Radar Digitizing
Digital Communications
Real Time Spectrum Analysis
Signature Analysis

MOD-1205 FUNCTIONAL BLOCK DIAGRAM



NOTE: WITH PIN 30 OPEN, ANALOG INPUT IMPEDANCE IS 400Ω. WITH PIN 30 GROUNDED, ANALOG IMPEDANCE IS 50Ω.

GENERAL DESCRIPTION

Analog Devices' model MOD-1205 is a very high-speed A/D converter capable of digitizing video input signals to 12-bit accuracy at random or periodic word rates of dc through 5MHz. The MOD-1205 is truly a breakthrough in high-speed A/D technology. It utilizes the latest state-of-the-art conversion technique called digital correcting subranging (DCS) to effectively eliminate errors normally associated with subranging type ADCs. It is the most cost effective A/D in this speed category, combining small size and low power dissipation with low cost.

The MOD-1205 is constructed on a single printed circuit card which is intended for mounting on a system mother board and occupies only 27 square inches. Within this A/D is the required sample/track-and-hold amplifier, encoder, timing circuits and output latches for a true simultaneous, all-parallel digital output.

The encode command input and digital outputs are TTL compatible. The A/D requires only an external encode command pulse and external power supplies for operation. NO external parts are required. Gain and offset potentiometers are provided on the card. The A/D is fully repairable either at the factory or in the field.

The MOD-1205 is ideally suited for systems requiring the ultimate in conversion speed and accuracy. Such applications include radar digitizing, digital communications, spectrum analysis, and many others. Each MOD-1205 is backed by Analog Devices' limited one year warranty.

PIN	FUNCTION	PIN	FUNCTION
1	ENCODE COMMAND	17	BIT 9
2	GND*	18	BIT 10
3	+5V	19	BIT 11
4	GND*	20	BIT 12 (LSB)
5	GND*	21	+15V
6	-6V	22	-15V
7	-6V	23	GND*
8	$\overline{\text{BIT 1}}$	24	GND*
9	BIT 1 (MSB)	25	GND*
10	BIT 2	26	+5V
11	BIT 3	27	-6V
12	BIT 4	28	GND*
13	BIT 5	29	GND*
14	BIT 6	30	TERMINATION
15	BIT 7	31	GND*
16	BIT 8	32	ANALOG INPUT

*ALL GROUND PINS ARE CONNECTED TOGETHER WITHIN THE MOD-1205

Pin Designations

ORDERING INFORMATION

Order model number MOD-1205 A/D converter. Mating pin sockets for the MOD-1205 are model number MSB-2 (32 required per A/D).

This two-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be found in Volume II, page 11-39.

SPECIFICATIONS (typical @ +25°C with nominal power supplies unless otherwise noted)

MODEL	MOD-1205
RESOLUTION (FS = FULL SCALE)	12 Bits (0.024% FS)
LSB WEIGHT	1mV
ACCURACY (INCLUDING LINEARITY) @ DC	±0.0125% Full Scale ±1/2LSB
Monotonicity	Guaranteed (0 to +70°C)
Nonlinearity vs. Temperature	0.0005% of FS/°C, max
Gain vs. Temperature	0.002% of FS/°C, typ; 0.005% of FS/°C, max
DYNAMIC CHARACTERISTICS	
AC Linearity[1] (dc to 1MHz)	Spurious Signals >70dB below FS, max
(1MHz to 2.5MHz)	Spurious Signals >65dB below FS, max; >68dB, typ
Conversion Time	See Text and Timing Diagram in Volume II
Conversion Rate (Word Rate)	dc to 5MHz
Aperture Uncertainty (Jitter)	±25ps max
Aperture Time	30ns (±10ns from unit to unit)
Signal to Noise Ratio[2]	66dB min; 68dB, typ
Noise Power Ratio[3]	56dB min, 58dB typ
Transient Response[4]	12-Bit (0.0125%) Accuracy within 200ns
Overvoltage Recovery Time[5]	200ns
Input Bandwidth (small signal, 3dB)	15MHz min
Input Bandwidth (large signal, 3dB)	10MHz min; flat within ±0.1dB, dc through 5MHz
ANALOG INPUT	
Voltage Range	±2.048V FS ±4V Absolute max
Impedance	400Ω with pin 30 open, 50Ω with pin 30 grounded
Offset Voltage	Adjust to 0 with On Board Potentiometer
Offset vs. Temperature	0.002% FS/°C, typ; 0.005% of FS/°C, max
Bias Current	1nA max
ENCODE COMMAND INPUT	
Logic Levels, TTL Compatible	"0" = 0 to +0.4V "1" = +2.4V to +5V
Logic Loading	2 Standard TTL Gates
Rise and Fall Times	10ns max
Duration min/max	25ns/50% of Duty Cycle
Frequency (Random or Periodic)	dc to 5MHz
DIGITAL DATA OUTPUT	
Format	12 Parallel Bits, NRZ
Logic Levels, TTL Compatible	"0" = 0 to +0.4V "1" = +2.4V to +5V
Drive (Not Short Circuit Protected)	Up to 1 Schottky TTL or 2 Standard TTL Loads
Time Skew	10ns max
Coding	Offset Binary (OBN) or 2's complement (2SC)
Conversion Time	See Text in Volume II
POWER REQUIREMENTS	
+15V ±5%	200mA
-15V ±5%	150mA
-6V ±4%	700mA
+5V ±5%	800mA
Power Consumption	13 Watts
TEMPERATURE RANGE	
Operating	0 to +70°C
Storage	-55°C to +85°C
Cooling Requirements	500 Linear Feet Per Min (LFPM) @ +70°C
PHYSICAL CHARACTERISTICS	
Construction	Single Printed Circuit Card

NOTES:

[1] AC linearity expressed in terms of spurious in-band signals generated at specified encode rates at analog input frequencies ( ).

[2] rms signal to rms noise at 500kHz analog input.

[3] dc to 2.4MHz white noise bandwidth with slot frequency of 512kHz.

[4] For full-scale step input, attains 12-bit accuracy in time specified.

[5] Recovers to 12-bit accuracy after 2 X FS input overvoltage in time specified.

Specifications subject to change without notice.

Voltage-to-Frequency & Frequency-to-Voltage Converters

Contents

	Page
Selection Guide	12-3
General Information; Factors in Choosing VFCs and FVCs	12-4
AD537 IC Voltage-to-Frequency Converter	12-7
•AD650J/K/S Voltage-to-Frequency and Frequency-to-Voltage Converter	12-15
•ADVFC32KN/BH/SH Voltage-to-Frequency and Frequency-to-Voltage Converter	12-17
451/453 Adjustable Frequency-to-Voltage Converter	12-21

•New product since the *1980 Data-Acquisition Components and Subsystems Catalog*

Selection Guide
Voltage-to-Frequency & Frequency-to-Voltage Converters

In this Selection Guide, V/F and F/V Converters are listed in separate tables, in order of increasing maximum frequency range. Complete descriptions, specifications, and applications information can be found in the data sheets. General information regarding VFCs and FVCs can be found in the following pages. Specifications are typical at rated supply voltage and load, and $T_A = +25°C$, except where noted.

VOLTAGE-TO-FREQUENCY CONVERTERS

Max F.S. Frequency	Model	Brief Description	Vol I Page	Vol II Page
10kHz	450	0.005% max nonlinearity, max tempcos: offset – 20μV/°C; gain – 25ppm/°C	–	12-7
10kHz	456	0.02% max nonlinearity, max tempcos: offset – 100μV/°C; gain – 80ppm/°C	–	12-7
20kHz	454	0.005% max nonlinearity, max tempcos: offset – 20μV/°C; gain – 25ppm/°C	–	12-7
100kHz	AD537	0.07% max nonlinearity, low power, max tempcos: offset – 1μV/°C (K); gain – 50ppm/°C (K)	12-7	–
100kHz	458	0.01% nonlinearity, max tempcos: offset – 30μV/°C; gain – 5ppm/°C	–	12-17
500kHz	ADVFC32	±0.01% of max nonlinearity, max tempcos: offset – 30μV/°C; gain – 100ppm/°C	12-17	–
1MHz	460	0.015% nonlinearity, max tempcos: offset – 30μV/°C; gain – 15ppm/°C	–	12-17
1MHz	AD650	±0.01% max nonlinearity, max tempcos: offset – 10μV/°C; gain – 100ppm/°C	12-15	–

FREQUENCY-TO-VOLTAGE CONVERTERS

Max F.S. Frequency	Model	Brief Description	Vol I Page	Vol II Page
100Hz-20kHz Adjustable	451	0.008% max nonlinearity, 30ms to full scale, max gain tempco – 50ppm/°C	12-21	12-11
1kHz-200kHz Adjustable	453	0.008% max nonlinearity, 4ms to full scale, max gain tempco – 50ppm/°C	12-21	12-11

Orientation

Voltage-to-Frequency & Frequency-to-Voltage Converters

VOLTAGE-TO-FREQUENCY CONVERTERS

Voltage-to-frequency converters (VFC's) convert analog voltage or current levels to pulse trains or square waves in a logic-compatible form (usually TTL) at frequencies that are accurately proportional to the analog quantity. The output continuously tracks the input signal, responding directly to changes in the input signal; external-clock synchronization is not required. V/f converters find applications in analog-to-digital converters with high resolution, long-term high-precision integrators, two-wire high-noise-immunity digital transmission, and digital voltmeters.

FREQUENCY-TO-VOLTAGE CONVERTERS

Frequency-to-voltage converters (FVC's) perform the inverse operation; they accept a wide variety of periodic waveforms and produce an analog output proportional to frequency. Combining adjustable threshold, gain, and output offset with low linearity-error, F/V converters offer economical solutions to a wide variety of applications where it is required to convert frequency to an analog voltage. Examples are motor-speed controllers, power-line frequency monitors, and VCO stabilization circuits. In analog-to-analog data transmission, they convert serially transmitted data in the form of pulse streams back to analog voltage.

Applications of both forms of conversion, as appropriate to specific device types, are illustrated with varying degrees of detail on the individual data sheets.

FACTORS IN CHOOSING VFC's AND FVC's

Voltage-to-frequency converters are available from Analog Devices in both pulse train and square wave outputs. The output of the change balance types, operate up to 1MHz F.S., is a train of pulses of constant height and width, with very low duty cycle for small analog inputs. The output of the AD537 is unique in that its output is square-wave, an advantage in some applications.

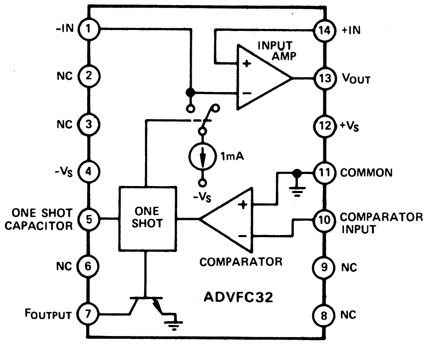


Figure 1. Block Diagram of the ADVFC32

The most-popular VFC designs (Figure 1) contain an integrator, which charges at a rate proportional to the value of the input signal. Each time the integrator's charge has been increased by a precisely metered increment, the threshold crossing produces a pulse of accurately known area. The pulse serves both as the output (via a buffer) and as a subtractive charge increment to reduce the integrator's net charge. The next pulse is triggered when the net integral has again reached the threshold. The relationship between the pulse rate and the input level is linear. The AD537* operates on a somewhat different principle (Figure 2): an input current charges a capacitor between 2 threshold levels, first in one direction, then in the other, in an emitter-coupled astable multivibrator circuit. Since the time required to reach the switching threshold is inversely proportional to the analog input, the frequency is directly proportional. For constant analog input, the charging rate and the discharge rate are equal, so the output is a square wave.

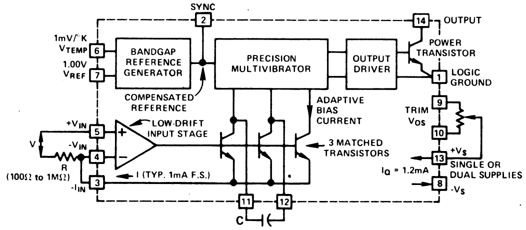
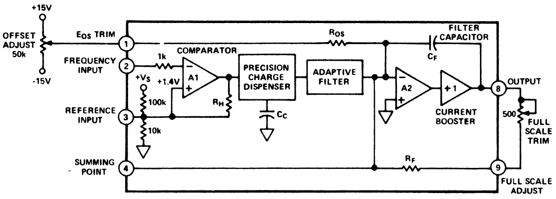


Figure 2. Block Diagram of the AD537

***A useful 20-page Application Note, "Applications of the AD537 IC Voltage-to-Frequency Converter", by Doug Grant, is available upon request.**



MODEL	C_F	R_{OS}	R_H	R_F
451	0.015μF	3.3MΩ	2.2MΩ	18kΩ
453	0.001μF	3.9MΩ	1.0MΩ	22kΩ

Figure 3. Block Diagram – Models 451 & 453 FVC's

Frequency-to-voltage converters (Figure 3) average a train of equal-area pulses that are generated internally by a precision charge dispenser, in response to each crossing of an input threshold. The analog output voltage is proportional to the sum of the pulse areas over a given period. F/V conversion can also be obtained by using the ADVFC32.

SPECIFICATIONS

The salient specifications for VFC's are *(non)linearity*, as a percentage of full-scale frequency; *frequency range*, the greater the frequency range, the greater the resolution for a given counting period; *full-scale-calibration error; gain-temperature coefficient*, in ppm of signal per °C, where "gain" is the ratio of full-scale frequency to full-scale voltage, *input-offset temperature coefficient; overrange capability*, within rated specifications, and *step response*, the worst-case time interval required for the frequency to respond to a full-scale-step input change.

For FVC's, important specs, in addition to accuracy specs corresponding to the above, include *output ripple* (for specified input frequencies), *threshold* (for recognition that another cycle has been initiated, and for versatility in interfacing various types of sensors directly), *hysteresis*, to provide a degree of insensitivity to noise superimposed on a slowly-varying input waveform, and *dynamic response* (important in motor control).

Definitions of some critical specifications, and the conditions for adjusting or measuring them, are detailed on individual data sheets.

ANALOG DEVICES

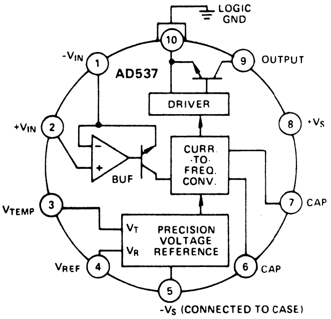
Integrated Circuit Voltage to Frequency Converter

AD537*

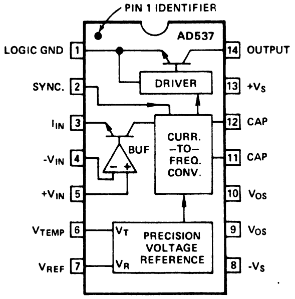
FEATURES

- **Low Cost A-D Conversion**
- **Versatile Input Amplifier**
  - **Positive or Negative Voltage Modes**
  - **Negative Current Mode**
  - **High Input Impedance, Low Drift**
- **Single Supply, 5 to 36 Volts**
- **Linearity: ±0.05% FS**
- **Low Power: 1.2mA Quiescent Current**
- **Full Scale Frequency up to 100kHz**
- **1.00 Volt Reference**
- **Thermometer Output (1mV/K)**
- **F-V Applications**

AD537 FUNCTIONAL BLOCK DIAGRAMS



TO-100
TOP VIEW



TO-116 STYLE
TOP VIEW

PRODUCT DESCRIPTION

The AD537 is a monolithic V-F converter consisting of an input amplifier, a precision oscillator system, an accurate internal reference generator and a high current output stage. Only a single external RC network is required to set up any full scale (F.S.) frequency up to 100kHz and any F.S. input voltage up to ±30V. Linearity error is as low as ±0.05% for 10kHz F.S., and operation is guaranteed over an 80dB dynamic range. The overall temperature coefficient (excluding the effects of external components) is typically ±30ppm/°C. The AD537 operates from a single supply of 5 to 36V and consumes only 1.2mA quiescent current.

A temperature-proportional output, scaled to 1.00mV/K, enables the circuit to be used as a reliable temperature-to-frequency converter; in combination with the fixed reference output of 1.00V, offset scales such as 0°C or 0°F can be generated.

The low drift (1µV/°C typ) input amplifier allows operation directly from small signals (e.g., thermocouples or strain gages) while offering a high (250MΩ) input resistance. Unlike most V-F converters, the AD537 provides a square-wave output, and can drive up to 12 TTL loads, LEDs, very long cables, etc.

The excellent temperature characteristics and long-term stability of the AD537 are guaranteed by the primary band-gap reference generator and the low T.C. silicon chromium thin film resistors used throughout.

The device is available in either a TO-116 ceramic DIP or a TO-100 metal can; both are hermetically sealed packages.

The AD537 is available in three performance/temperature grades; the J and K grades are specified for operation over the 0 to 70°C range while the AD537S is specified for operation over the full military temperature range, -55°C to +125°C. MIL-STD-883, Level B processing is available.

PRODUCT HIGHLIGHTS

1. The AD537 is a complete V-F converter requiring only an external RC timing network to set the desired full scale frequency and a selectable pull-up resistor for the open-collector output stage. Any full-scale input voltage range from 100mV to 10 volts (or greater, depending on $+V_S$) can be accommodated by proper selection of timing resistor. The full scale frequency is then set by the timing capacitor from the simple relationship, $f = V/10RC$.
2. The power supply requirements are minimal, only 1.2mA quiescent current is drawn from a single positive supply from 4.5 to 36 volts. In this mode, positive inputs can vary from 0 volts (ground) to $(+V_S - 4)$ volts. Negative inputs can easily be connected for below ground operation.
3. F-V converters with excellent characteristics are also easy to build by connecting the AD537 in a phase-locked loop. Application particulars are shown in Figure 8.
4. The versatile open-collector NPN output stage can sink up to 20mA with a saturation voltage less than 0.4 volts. The Logic Common terminal can be connected to any level between ground (or $-V_S$) and 4 volts below $+V_S$. This allows easy direct interface to any logic family with either positive or negative logic levels.

***Covered by Patent Numbers 3,887,863 and RE 30,586**

SPECIFICATIONS (typical @ +25°C with V_S (total) = 5 to 36V, unless otherwise noted)

MODEL	AD537JH	AD537JD	AD537K	AD537S[1]
CURRENT-TO-FREQUENCY CONVERTER				
Frequency Range	0 to 150kHz	*	*	*
Nonlinearity[2]				
f_{max} = 10kHz	0.15% max (0.1% typ)	*	0.07% max	**
f_{max} = 100kHz	0.25% max (0.15% typ)	*	0.1% max	**
Full Scale Calibration Error				
C = 0.01µF, I_{IN} = 1.000mA	±10% max	±7% max	±5% max	**
vs. Supply (f_{max} < 100kHz)	±0.1%/V max (0.01% typ)	*	*	*
vs. Temp. (T_{min} to T_{max})	±150ppm/°C max (50ppm typ)	*	50ppm/°C max (30ppm typ)[3]	150ppm/°C max
ANALOG INPUT AMPLIFIER (Voltage-to-Current Converter)				
Voltage Input Range				
Single Supply	0 to (+V_S - 4) Volts (min)	*	*	*
Dual Supply	-V_S to (+V_S - 4) Volts (min)	*	*	*
Input Bias Current (Either Input)	100nA	*	*	*
Input Resistance (Non-Inverting)	250MΩ	*	*	*
Input Offset Voltage (Trimmable in "D" Package Only)	5mV max	*	2mV max	**
vs. Supply	200µV/V max	100µV/V max	100µV/V max	**
vs. Temp. (T_{min} to T_{max})	5µV/°C	*	1µV/°C	10µV/°C max
Safe Input Voltage[4]	±V_S	*	*	*
REFERENCE OUTPUTS				
Voltage Reference				
Absolute Value	1.00 Volt ±5% max	*	*	*
vs. Temp. (T_{min} to T_{max})	50ppm/°C	*	100ppm/°C max[3]	**
vs. Supply	±0.03%/V max	*	*	*
Output Resistance[5]	380Ω	*	*	*
Absolute Temperature Reference[6]				
Nominal Output Level	1.00mV/K	*	*	*
Initial Calibration @ +25°C	298mV (±5mV)	*	298mV (±5mV max)	**
Slope Error from 1.00mV/K	±0.02mV/K	*	*	*
Slope Nonlinearity	±0.1K	*	*	*
Output Resistance[5]	900Ω	*	*	*
OUTPUT INTERFACE (Open Collector Output) (Symmetrical Square Wave)				
Output Sink Current in Logic "0" V_{OUT} = 0.4V max, T_{min} to T_{max})	10mA min	20mA min	20mA min	10mA min
Output Leakage Current in Logic "1" (T_{min} to T_{max})	200nA max	*	*	2µA max
Logic Common Level Range	-V_S to (+V_S - 4) Volts	*	*	*
Rise/Fall Times (C_T = 0.01µF)				
I_{IN} = 1mA	0.2µs	*	*	*
I_{IN} = 1µA	1µs	*	*	*
POWER SUPPLY				
Voltage, Rated Performance				
Single Supply	4.5V to 36V	*	*	*
Dual Supply	±5 to ±18V	*	*	*
Quiescent Current	1.2mA (2.5mA max)	*	*	*
TEMPERATURE RANGE				
Rated Performance	0 to +70°C	*	*	-55°C to +125°C
Storage	-65°C to +150°C	*	*	*
PACKAGE OPTIONS[7]				
"D" Package: TO-116 Style (D14A)	–	AD537JD	AD537KD	AD537SD
"H" Package: TO-100	AD537JH	–	AD537KH	AD537SH

*Specifications same as AD537JH.

**Specifications same as AD537K.

Specifications subject to change without notice.

[1] The AD537S is available inspected and processed to the full requirements of MIL-STD-883, Level B. A complete listing of the tests is available on request. Order part number AD537SD/883B or AD537SH/883B.

[2] Nonlinearity is specified for a current input level (I_{IN}) to the converter from 0.1 to 1000µA. Converter has 100% overrange capability up to I_{IN} = 2000µA with slightly reduced linearity. Nonlinearity is defined as deviation from a straight line from zero to full scale, expressed as a percentage of full scale.

[3] Guaranteed not tested.

[4] Maximum voltage input level is equal to the supply on either input terminal. However, large negative voltage levels can be applied to the negative terminal if the input is scaled to a nominal 1mA full scale through an appropriate value resistor (see Figure 2).

[5] Loading the 1.0 volt or 1mV/K outputs can cause a significant change in overall circuit performance, as indicated in the applications section. To maintain normal operation, these outputs should be operated into the internal buffer or an external amplifier.

[6] Temperature reference output performance is specified from 0 to +70°C for "J" and "K" devices, -55°C to +125°C for "S" model.

[7] See Section 20 for package outline information.

CIRCUIT OPERATION

A block diagram of the AD537 is shown on the first page. A versatile operational amplifier (BUF) serves as the input stage; its pupose is to convert and scale the input voltage signal to a drive current in the NPN follower. Optimum performance is achieved when, at the full scale input voltage, a 1mA drive current is delivered to the current-to-frequency converter. The drive current to the current-to-frequency converter (an astable multivibrator) provides both the bias levels and the charging current to the externally connected timing capacitor. This "adaptive" bias scheme allows the oscillator to provide low nonlinearity over the entire current input range of 0.1 to 2000μA. The square wave oscillator output goes to the output driver which provides a floating base drive to the NPN power transistor. This floating drive allows the logic interface to be referenced to a different level than $-V_S$. The "SYNC" input ("D" package only) allows the oscillator to be slaved to an external master oscillator; this input can also be used to shut off the oscillator.

The reference generator uses a band-gap circuit (this allows single-supply operation to 4.5 volts which is not possible with low T.C. zeners) to provide the reference and bias levels for the amplifier and oscillator stages. The reference generator also provides the precision, low T.C. 1.00 volt output and the V_{TEMP} output which tracks absolute temperature at 1mV/K.

V-F CONNECTION FOR POSITIVE INPUT VOLTAGES

The positive voltage input range is from $-V_S$ (ground in single supply operation) to 4 volts below the positive supply. The connection shown in Figure 1 provides a very high (250MΩ) input impedance. The input voltage is converted to the proper drive current at pin 3 by selecting a scaling resistor. The full scale current is 1mA, so, for example a 10 volt range would require a nominal 10kΩ resistor. The trim range required will depend on capacitor tolerance. Full scale currents other than 1mA can be chosen, but linearity will be reduced; 2mA is the maximum allowable drive.

As indicated by the scaling relationship in Figure 1, a 0.01μF timing capacitor will give a 10kHz full scale frequency, and 0.001μF will give 100kHz with a 1mA drive current. The maximum frequency is 150kHz. Polystyrene or NPO ceramic capacitors are preferred for T.C. and dielectric absorption; polycarbonate or mica are acceptable; other types will degrade linearity. The capacitor should be wired very close to the AD537.

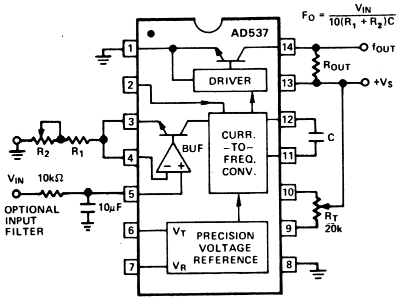


Figure 1. Standard V-F Connection for Positive Input Voltages

V-F CONNECTIONS FOR NEGATIVE INPUT VOLTAGE OR CURRENT

A wide range of negative input voltages can be accommodated with proper selection of the scaling resistor, as indicated in Figure 2. This connection, unlike the buffered positive connection, is not high impedance since the 1mA F.S. drive current must be supplied by the signal source. However, very large negative voltages beyond the supply can be handled easily; just modify the scaling resistors appropriately. Diode CR1 (HP5082-2811) is necessary for overload and latchup protection for current or voltage inputs.

If the input signal is a true current source, R_1 and R_2 are not used. Full scale calibration can be accomplished by connecting a 200kΩ pot in series with a fixed 27kΩ from pin 7 to $-V_S$ (see calibration section, below).

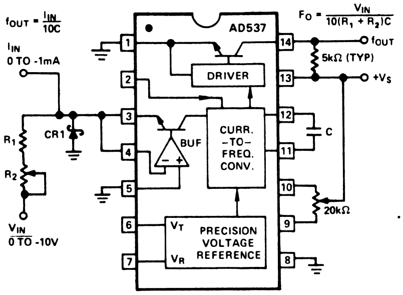


Figure 2. V-F Connections for Negative Input Voltage or Current

CALIBRATION

There are two independent adjustments: scale and offset. The first is trimmed by adjustment of the scaling resistor R and the second by the (optional) potentiometer connected to $+V_S$ and the V_{OS} pins ("D" package only). Precise calibration requires the use of an accurate voltage standard set to the desired FS value and a frequency meter; a scope is useful for monitoring output waveshape. Verification of linearity requires the availability of a switchable voltage source (or a DAC) having a linearity error below ±0.005%, and the use of long measurement intervals to minimize count uncertainties. *Every AD537 is automatically tested for linearity,* and it will not usually be necessary to perform this verification, which is both tedious and time-consuming.

Although drifts are small it is good practice to allow the operating environment to attain stable temperature and to ensure that the supply, source and load conditions are proper.

Begin by setting the input voltage to 1/10,000 of full scale. Adjust the offset pot until the output frequency is 1/10,000 of full scale (for example 1Hz for FS of 10kHz). This is most easily accomplished using a frequency meter connected to the output. Then apply the FS input voltage and adjust the gain pot until the desired FS frequency is indicated. In applications where the FS input is small, this adjustment will very slightly affect the offset voltage, due to the input bias current of the buffer amplifier. A change of 1kΩ in R will affect the input by approximately 100μV, which is as much as 0.1% of a 100mV FS range. Therefore, it may be necessary to repeat the offset and scale adjustments for the highest accuracy. The design of the input amplifier is such that the input voltage drift after offset nulling is typically below 1μV/°C.

In some cases the signal may be in the form of a negative current source. This can be handled in a similar way to a negative input voltage. However, the scaling resistor is no longer required, eliminating the capability of trimming full scale in this fashion. Since it will usually be impractical to vary the capacitance, an alternative calibration scheme is needed. This is shown in Figure 3. A resistor-potentiometer connected from the V_R output to $-V_S$ will alter the internal operating conditions in a predictable way, providing the necessary adjustment range. With the values shown, a range of ±4% is available; a larger range can be attained by reducing R1. This technique does not degrade the temperature-coefficient of the converter, and the linearity will be as for negative input voltages. The minimum supply voltage may be used.

Unless it is required to set the input node at exactly ground potential, no offset adjustment is needed. The capacitor C is selected to be 5% below the nominal value; with R2 in its mid-position the output frequency is given by

$$f = \frac{I}{10.5 \times C}$$

where f is in kHz, I is in mA and C is in μF. For example, for a FS frequency of 10kHz at a FS input of 1mA, C = 9500pF. Calibration is effected by applying the full-scale input and adjusting R2 for the correct reading.

This alternative adjustment scheme may also be used when it is desired to present an exact input resistance in the negative-voltage mode. The scaling relationship is then

$$f = \frac{V}{R_{exact}} \cdot \frac{1}{10.5\ C}$$

The calibration procedure is then similar to that used for positive input voltages, except that the scale adjustment is by means of R2.

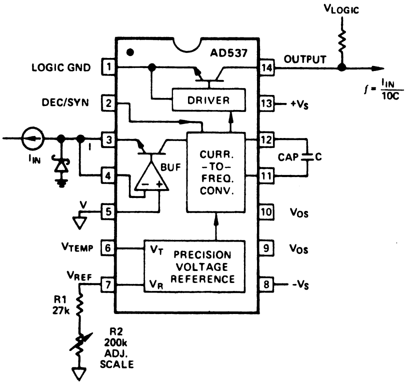


Figure 3. Scale Adjustment for Current Inputs

INPUT PROTECTION

The AD537 was designed to be used with a minimum of additional hardware. However, the successful application of a precision IC involves a good understanding of possible pitfalls and the use of suitable precautions.

The $-V_{IN}$, $+V_{IN}$ and I_{IN} pins should not be driven more than 300mV below $-V_S$. This would cause internal junctions to conduct, possibly damaging the IC. The AD537 can be protected from "below $-V_S$" inputs by a Schottky diode, CR1 (HP5082-2811) as shown in Figure 2. It is also desirable not to drive $+V_{IN}$, $-V_{IN}$ and I_{IN} above $+V_S$. In operation, the converter will become very nonlinear for inputs above ($+V_S$ -3.5V). Control currents above 2mA will also cause nonlinearity.

The 80dB dynamic range of the AD537 guarantees operation from a control current of 1mA (nominal FS) down to 100nA (equivalent to 1mV to 10V FS). Below 100nA improper operation of the oscillator may result, causing a false indication of input amplitude. In many cases this might be due to short-lived noise spikes which become added to the input. For example, when scaled to accept a FS input of 1V, the -80dB level is only 100μV, so when the mean input is only 60dB below FS (1mV), noise spikes of 0.9mV are sufficient to cause momentary malfunction.

This effect can be minimized by using a simple low-pass filter ahead of the converter. For a FS of 10kHz a single-pole filter with a time-constant of 100ms (Figure 1) will be suitable, but the optimum configuration will depend on the application and type of signal processing. Noise spikes are only likely to be a cause of error when the input current remains near its minimum value for long periods of time; above 100nA (1mV) full integration of additive input noise occurs.

The AD537 is somewhat susceptible to interference from other signals. The most sensitive nodes (besides the inputs) are the capacitor terminals and the SYNC pin. The timing capacitor should be located as close as possible to the AD537 to minimize signal pickup in the leads. In some cases, guard rings or shielding may be required. The SYNC pin should be decoupled through a 0.005μF (or larger) capacitor to pin 13 ($+V_S$). This minimizes the possibility that the AD537 will attempt to synchronize to a spurious signal. This precaution is unnecessary on the metal can package since the SYNC function is not brought out to a package pin and is thus not susceptible to pickup.

DECOUPLING

It is good engineering practice to use bypass capacitors on the supply-voltage pins and to insert small-valued resistors (10 to 100Ω) in the supply lines to provide a measure of decoupling between the various circuits in a system. Ceramic capacitors of 0.1μF to 1.0μF should be applied between the supply-voltage pins and analog signal ground for proper bypassing on the AD537.

A decoupling capacitor may also be useful from $+V_S$ to SYNC in those applications where very low cycle-to-cycle period variation (jitter) is demanded. By placing a capacitor across $+V_S$ and SYNC this noise is reduced. On the 10kHz FS range, a 6.8μF capacitor reduces the jitter to one in 20,000 which is adequate for most applications. A tantalum capacitor should be used to avoid errors due to dc leakage.

OPERATION WITH NON-ZERO TC

The good temperature stability of the AD537 can only be realized using stable timing components. However, compensation for timing components which yield a net negative full-scale frequency TC can be easily introduced by adding a resistor between the +1mV/K output and $-V_S$. The value should be selected from the curve given in Figure 4. Over this range of compensation the scale factor is only slightly affected; the error is about +0.03%/ppm/K in frequency (e.g., 150ppm shift would change the scale factor 4.5%).

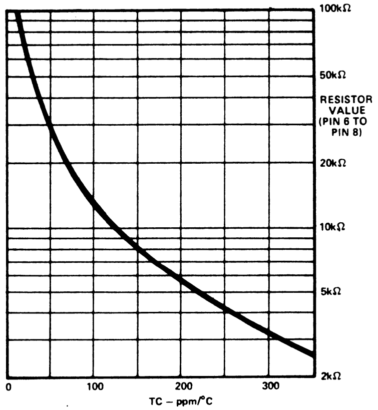


Figure 4. Positive T.C. Induced Versus Correction Resistance

NONLINEARITY SPECIFICATION

The preferred method for specifying linearity error is in terms of the maximum deviation from the ideal relationship after calibrating the converter at full scale and "zero". This error will vary with the full scale frequency and the mode of operation. The AD537 operates best at a 10kHz full scale frequency with a negative voltage input; the linearity is typically within ±0.05%. Operating at higher frequencies or with positive inputs will degrade the linearity as indicated in the specifications. The shape of a typical linearity plot is given in Figure 5.

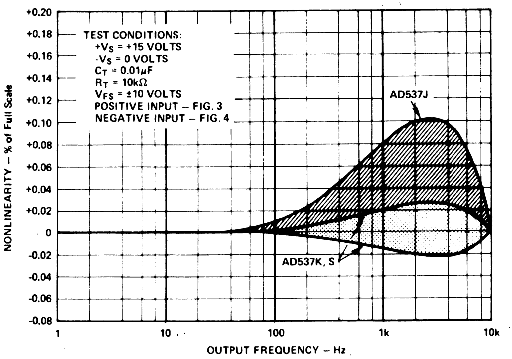


Figure 5a. Typical Nonlinearity Error Envelopes with 10kHz F.S. Output

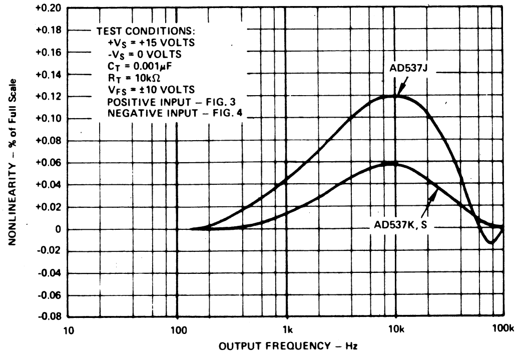
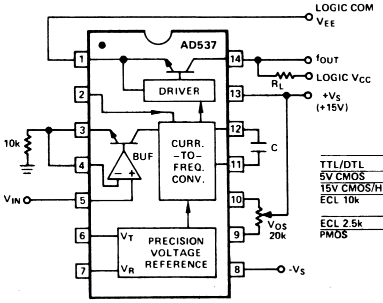


Figure 5b. Typical Nonlinearity Error with 100kHz F.S. Output

OUTPUT INTERFACING CONSIDERATIONS

The design of the output stage allows easy interfacing to all digital logic families. The collector and emitter of the output NPN transistor are both uncommitted; the emitter can be tied to any voltage between -V_S and 4 volts below +V_S. The open collector can be pulled up to a voltage 36 volts above the emitter regardless of +V_S. The high power output stage can supply up to 20mA (10mA for "H" package) at a maximum saturation voltage of 0.4 volts. The stage limits the output current at 25mA; it can handle this limit indefinitely without damaging the device.

Figure 6 shows the AD537 with a standard 0 to +10 volt input connection and the output stage connections. The value for the logic common voltage, pull-up resistor, positive logic level, and -V_S supply are given in the accompanying chart for several logic forms.



	V_{CC}	V_{EE}	R_L	-V_S
TTL/DTL	+5	GND	5k	GND
5V CMOS	+5	GND	20k	GND
15V CMOS/HNIL	+15	GND	10k	GND
ECL 10k	0	-8	5k	-8 to -15
ECL 2.5k	+1.3	-2	5k	-5
PMOS	0	-15	10k	-15

Figure 6. Interfacing Standard Logic Families

APPLICATIONS

The diagrams and descriptions of the following applications are provided to stimulate the discerning engineer with alternative circuit design ideas. "Applications of the AD537 IC Voltage-to-Frequency Converter", available from Analog Devices on request, covers a wider range of topics and concepts in data conversion and data transmission using voltage-to-frequency converters.

TRUE TWO-WIRE DATA TRANSMISSION

Figure 7 shows the AD537 in a true two-wire data transmission scheme. The twisted-pair transmission line serves the dual purpose of supplying power to the device and also carrying frequency data in the form of current modulation. The PNP circuit at the receiving end represents a fairly simple way for converting the current modulation back into a voltage square wave which will drive digital logic directly. The 0.6 volt square wave which will appear on the supply line at the device terminals does not affect the performance of the AD537 because of its excellent supply rejection. Also, note that the circuit operates at nearly constant average power regardless of frequency.

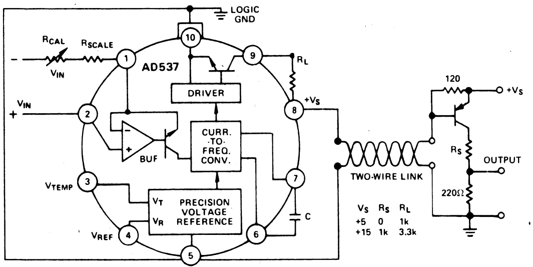


Figure 7. True Two-Wire Operation

F-V CONVERTERS

The AD537 can be used as a high linearity VCO in a phase-locked loop to accomplish frequency-to-voltage conversion. By operating the loop without a low-pass filter in the feedback path (first-order system), it can lock to any frequency from zero to an upper limit determined by the design, responding in three or four cycles to a step change of input frequency. In practice, the overall response time is determined by the characteristics of the averaging filter which follows the PLL.

Figure 8 shows a connection using a low-power TTL quad open-collector nand gate which serves as the phase comparator. The input signal should be a pulse train or square wave with characteristics similar to TTL or 5-volt CMOS outputs. Any duty cycle is acceptable, but the minimum pulse width is 40µs. The output voltage is one volt for a 10kHz input frequency. The output as shown here is at a fairly high impedance level; for many situations an additional buffer may be required.

Trimming is similar to V-F application trimming. First set the V_{OS} trimmer to mid-scale. Apply a 10kHz input frequency and trim the 2kΩ potentiometer for 1.00 volts out. Then apply a 10Hz waveform and trim the V_{OS} for 1mV out. Finally, retrim the full scale output at 10kHz. Other frequency scales can be obtained by appropriate scaling of timing components.

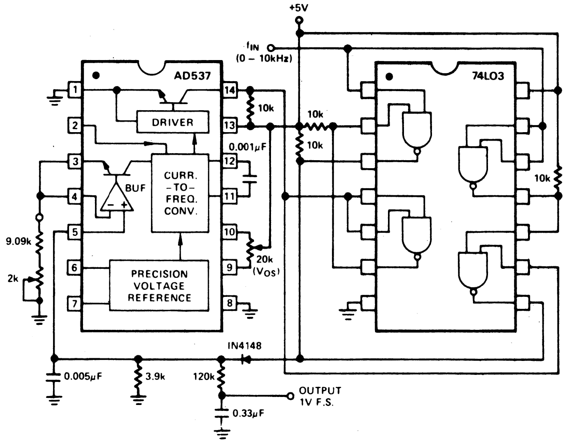


Figure 8. 10kHz F-V Converter

TEMPERATURE-TO-FREQUENCY CONVERSION

The linear temperature-proportional output of the AD537 can be used as shown in these applications to perform various direct temperature-to-frequency conversion functions; it can also be used with other external connections in a temperature sensing or compensation scheme. If the sensor output is used externally, it should be buffered through an op amp since loading that point will cause significant error in the sensor output as well as in the main V-F converter circuitry.

An absolute temperature (° Kelvin) -to-frequency converter is very easily accomplished, as shown in Figure 9. The 1mV per K output serves as the input to the buffer amplifier, which then scales the oscillator drive current to a nominal 298µA at +25°C (298K). Use of a 1000pF capacitor results in a corresponding frequency of 2.98kHz. Setting the single 2kΩ trimmer for the correct frequency at a well-defined temperature near +25°C will normally result in an accuracy of ±2°C from -55°C to +125°C (using an AD537S). An NPO ceramic capacitor is recommended to minimize nonlinearity due to capacitance drift.

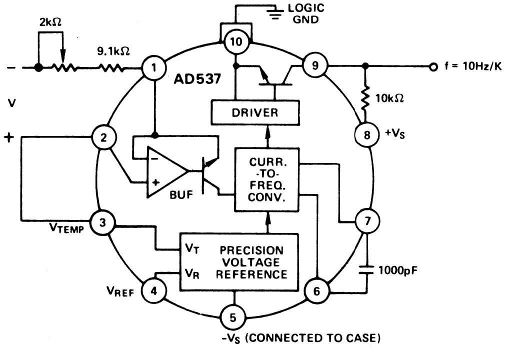


Figure 9. Absolute Temperature to Frequency Converter

OFFSET TEMPERATURE SCALES

Many other temperature scales can be set up by offsetting the temperature output with the voltage reference output. Such a scheme is shown by the Celsius-to-frequency converter in Figure 10. Corresponding component values for a Fahrenheit-to-frequency converter which give 10Hz/°F are given in parentheses.

A simple calibration procedure which will provide ±2°C accuracy requires substitution of a 7.27k resistor for the series combination of the 6.04k with the 2k trimmer; then simply set the 500Ω trimmer to give 250Hz at +25°C.

High accuracy calibration procedure:

1. Measure room temperature in K.
2. Measure temperature output at pin 6 at that temperature.
3. Calculate offset adjustment as follows:

$$\text{Offset Voltage (mV)} = \frac{V_{TEMP}\ \text{(pin 6) (mV)}}{\text{Room temp (K)}} \times 273.2$$

4. Temporarily disconnect 49Ω resistor (or 500Ω pot) and trim 2kΩ pot to give the offset voltage at the indicated node. Reconnect 49Ω resistor.
5. Adjust slope trimmer to give proper frequency at room temperature (+25°C = 250Hz).
   Adjustment for °F or any other scale is analogous.

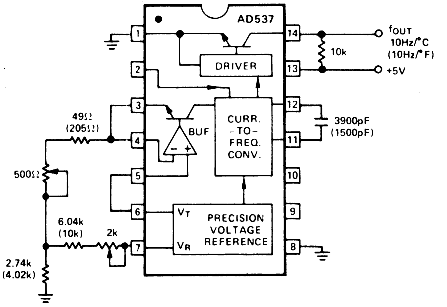


Figure 10. Offset Temperature Scale Converters-Centigrade and (Fahrenheit) to Frequency

SYNCHRONOUS OPERATION

The SYNC terminal at pin 2 of the DIP package can be used to synchronize a free running AD537 to a master oscillator, either at a multiple or a sub-multiple of the primary frequency. The preferred connection is shown in Figure 11. The diodes are used to produce the proper drive magnitude from high level signals. The SYNC terminal can also be used to shut off the oscillator. Shorting the terminal to $+V_S$ will stop the oscillator, and the output will go high (output NPN off).

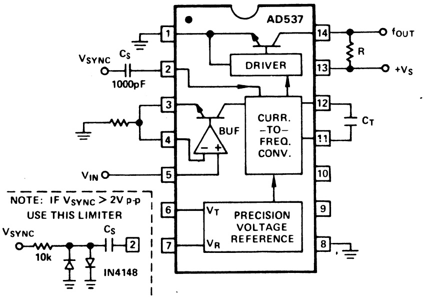


Figure 11. Connection for Synchronous Operation

Figure 12 shows the maximum pull-in range available at a given signal level; the optimum signal is a 0.8 to 1.0 volt square wave; signals below 0.1 volt will have no effect; signals above 2 volts p-p will disable the oscillator. The AD537 can normally be synchronized to a signal which forces it to a higher frequency up to 30% above the nominal free-running frequency, it can only be brought down about 1-2%.

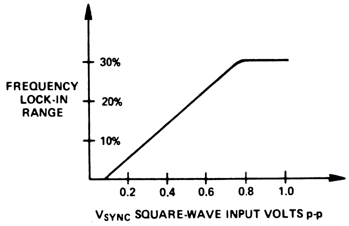


Figure 12. Maximum Frequency Lock-In Range Versus Sync. Signal

LINEAR PHASE LOCKED LOOP

The phase-locked-loop F/V circuit described earlier operates from an essentially noise-free binary input. PLL's are also used to extract frequency information from a noisy analog signal. To do this, the digital phase-comparator must be replaced by a linear multiplier. In the implementation shown in Figure 13, the triangular waveform appearing across the timing capacitor is used as one of the multiplier inputs; the signal provides the other input. It can be shown that the mean value of the multiplier output is zero when the two signals are in quadrature. In this condition, the ripple in the error signal is also quite small. Thus, the voltage at pin 5 is essentially zero, and the frequency is determined primarily by the current in the timing resistor, controlled either manually or by a control voltage.

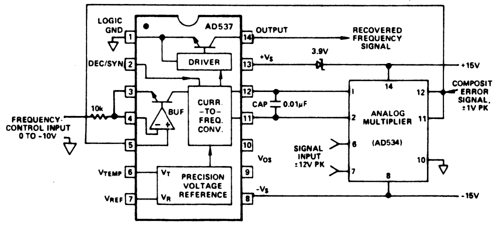


Figure 13. Linear Phase-Locked Loop

Noise on the input signal affects the loop operation only slightly; it appears as noise in the timing current, but this is averaged out by the timing capacitor. On the other hand, if the input frequency changes there is a net error voltage at pin 5 which acts to bring the oscillator back into quadrature. Thus, the output at pin 14 is a noise-free square-wave having exactly the same frequency as the input signal. The effectiveness of this circuit can be judged from Figure 14 which shows the response to an input of 1V rms 1kHz sinusoid plus 1V rms Gaussian noise. The positive supply to the AD537 is reduced by about 4V in order to keep the voltages at pins 11 and 12 within the common-mode range of the AD534.

Since this is also a first-order loop the circuit possesses a very wide capture range. However, even better noise-integrating properties can be achieved by adding a filter between the multiplier output and the VCO input. Details of suitable filter characteristics can be found in the standard texts on the subject.

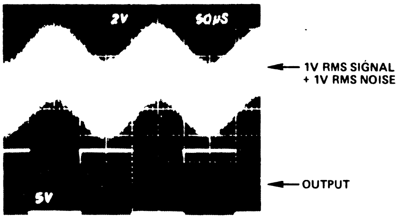


Figure 14. Performance of AD537 Linear Phase-Locked Loop

By connecting the multiplier output to the lower end of the timing resistor and moving the control input to pin 5, a high-resistance frequency-control input is made available. However, due to the reduced supply voltage, this input cannot exceed +6V.

TRANSDUCER INTERFACE

The AD537 was specifically designed to accept a broad range of input signals, particularly small voltage signals, which may be converted directly (unlike many V-F converters which require signal pre-conditioning). The 1.00V stable reference output is also useful in interfacing situations, and the high input resistance allows non-loading interfacing from a source of varying resistance, such as the slider of a potentiometer.

THERMOCOUPLE INPUT

The output of a Chromel-Constantan (Type E) thermocouple, using a reference junction at 0°C, varies from 0 to 53.14mV over the temperature range 0 to +700°C with a slope of 80.678µV/degree over most of its range and some nonlinearity over the range 0 to +200°C. For this example, we assume that it is desired to indicate temperature in Degrees Celsius using a counter/display with a 100ms gate width. Thus, the V-F converter must deliver an output of 7kHz for an input of 53.14mV. If very precise operation down to 0°C is imperative, some sort of linearizing is necessary (see, for example, Analog Devices' Nonlinear Circuits Handbook, pp92-97) but in many cases operation is only needed over part of the range.

The circuit shown in Figure 15 provides good accuracy from +300°C to +700°C. The extrapolation of the temperature-voltage curve back to 0°C shows that an offset of -3.34mV is required to fit the curve most exactly. This small amount of voltage can be introduced without an additional calibration step using the +1.00V output of the AD537. To adjust the scale, the thermocouple should be raised to a known reference temperature near 500°C and the frequency adjusted to value using R1. The error should be within ±0.2% over the range 400°C to 700°C.

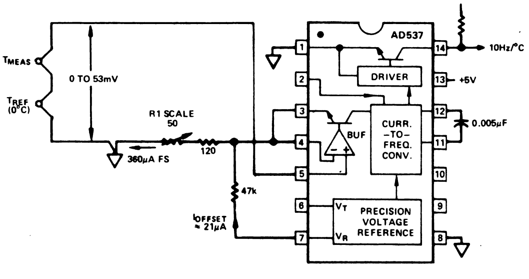


Figure 15. Thermocouple Interface with First-Order Linearization

ANALOG DEVICES

Voltage-to-Frequency and Frequency-to-Voltage Converter

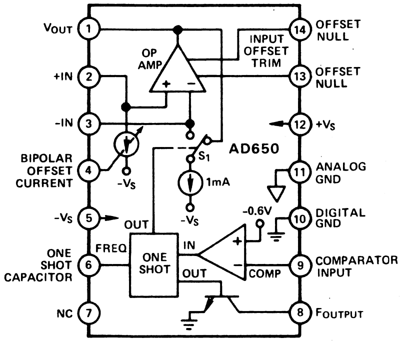
AD650

ADVANCE TECHNICAL DATA

FEATURES

- V/F Conversion to 1MHz
- Unipolar, Bipolar, or Differential V/F
- Very High Linearity
  - 0.002% typ at 10kHz
  - 0.005% typ at 100kHz
  - 0.1% max at 1MHz
- Input Offset Trimmable to Zero
- CMOS or TTL Compatible
- Reliable Monolithic Construction
- V/F or F/V Conversion

AD650 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD650 V/F/V (voltage to frequency or frequency to voltage) converter features both high linearity and ultra fast operation yet is priced in the same range as many lower performance devices. This is possible due to the AD650's sophisticated charge balancing circuit technique combined with completely diffused monolithic construction. Three other features that contribute to the AD650's flexibility are unipolar or bipolar input voltage ranges, input offset trim capability and separate analog and digital grounds.

At frequencies of 10kHz and lower, the AD650 outperforms all but the most expensive hybrids with a typical linearity error of 20ppm. Continuing up the frequency scale other V/Fs begin to experience serious linearity problems at 100kHz but the AD650 maintains very solid performance with 50ppm typical linearity error. And at 1MHz, linearity error is still only 1000ppm max.

Input offset voltage can be nulled out by using a 20kΩ adjustable resistor across pins 13 and 14 with the center tap connected to $+V_S$ through a 250kΩ resistor. This adjustment compensates for input offset by changing the collector bias current in the differential input transistor pair.

Two commercial grades are offered in both 16-pin plastic (N) and CERDIP (Q) dual-in line packages. The less expensive J grade is specified for operation up to 500kHz, while the premium K grade operates up to 1MHz. A -55°C to +125°C ceramic part (AD650SQ) with operation up to 1MHz is also available.

PRODUCT HIGHLIGHTS

1. In addition to very high linearity, the AD650 can operate at full scale output frequency up to 1MHz. The combination of these two features make the AD650 an inexpensive alternative in applications requiring high resolution monotonic A/D conversion.
2. An internal current source connected to the +IN terminal can be activated to allow bipolar or differential V/F conversion. With an extra 10V zener diode the differential mode input range can be expanded to ±10 volts common mode and ±10 volts differential.
3. TTL or CMOS compatibility is achieved using an open collector frequency output. The pullup resistor can be connected to voltages up to +30V, or +15V or +5V for conventional CMOS or TTL logic levels.
4. The maximum input voltage can be adjusted to accommodate a wide range by selecting the appropriate input resistor. Maximum input current should be set at 0.25mA.
5. The same components used for V/F conversion can also be used for F/V conversion by adding a simple logic biasing network and reconfiguring the AD650.
6. Separate analog and digital grounds make real world applications easier by preventing ground loops.

SPECIFICATIONS (typical @ +25°C with V_S = ±15V, unless otherwise noted)

MODEL	AD650J	AD650K	AD650S
DYNAMIC PERFORMANCE			
Minimum Frequency Range	0 to 500kHz	0 to 1MHz	0 to 1MHz
Maximum Nonlinearity[1] f_{max} = 10kHz	100ppm	*	*
100kHz	200ppm	*	*
500kHz	500ppm	*	1000ppm
1MHz	–	1000ppm	2000ppm
Full Scale Calibration Error			
(Adjustable to Zero)	±5%	*	*
vs. Supply[2]	±0.002% of FSR/% max	*	*
vs. Temp.	±150ppm/°C max	±100ppm/°C	*
BIPOLAR OFFSET CURRENT			
Activated by 1.25kΩ between pins 4 and 5	0.5mA ±10%	*	*
DYNAMIC RESPONSE			
Maximum Settling Time for Full Scale Step Input	1 Pulse of New Frequency Plus 1μs	*	*
Overload Recovery Time	1 Pulse of New Frequency Plus 1μs	*	*
ANALOG INPUT AMPLIFIER (V/F Conversion)			
Current Input Range	0 to +0.25mA	*	*
Voltage Input Range	-10 to 0	*	*
Differential Impedance	170kΩ‖10pF min	*	*
Common Mode Impedance	2.5MΩ‖10pF min	*	*
Input Bias Current			
Noninverting Input	40nA max	*	*
Inverting Input	8nA max	*	*
Input Offset Voltage			
(Trimmable to Zero)	4mV max	*	*
vs. Temp. (T_{min} to T_{max})	30μV/°C	*	*
Safe Input Voltage	±V_S	*	*
COMPARATOR (F/V Conversion)			
Logic "0" Level	$-V_S$ to -1V	*	*
Logic "1" Level	+1V to $+V_S$	*	*
Pulse Width Range	0.1μs to $(0.15/f_{max})$μs	*	*
Input Impedance	250kΩ	*	*
OPEN COLLECTOR OUTPUT (V/F Conversion)			
Output Sink Current in Logic "0" V_{OUT} = 0.4V max, T_{min} to T_{max}	8mA min	*	*
Output Leakage Current in Logic "1"	100nA max	*	*
Voltage Range	0 to 30V	*	*
AMPLIFIER OUTPUT (F/V Conversion)			
Voltage Range (1500Ω min load resistance)	0 to10V	*	*
Source Current (750Ω max load resistance)	+10mA min	*	*
Capacitive Load	100pF	*	*
POWER SUPPLY			
Voltage, Rated Performance			
Dual Supply	±9V to ±20V	*	*
Quiescent Current	6mA max	*	*
TEMPERATURE RANGE			
Rated Performance	0 to +70°C	*	-55°C to +125°C
Storage	-65°C to +150°C	*	*
PACKAGE OPTIONS[3]			
Plastic DIP – N14A	AD650JN	AD650KN	N/A
CERDIP – Q16A	AD650JQ	AD650KQ	AD650SQ

NOTES

[1] Nonlinearity is defined as deviation from a straight line from zero to full scale, expressed as a fraction of full scale.

[2] Power supply rejection measured at full scale output frequency of 10kHz.

[3] See Section 20 for package outline information.

*Specifications same as AD650J.

Specifications subject to change without notice.

ANALOG DEVICES

Voltage-to-Frequency and Frequency-to-Voltage Converter

ADVFC32

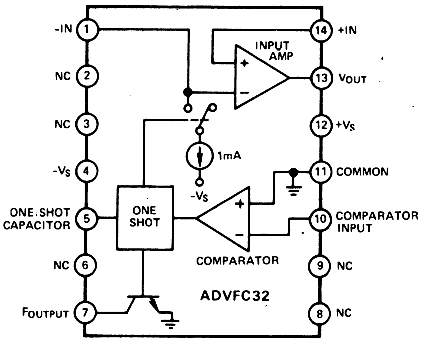
PRELIMINARY TECHNICAL DATA

FEATURES

High Linearity
- **±0.01% max at 10kHz FS**
- **±0.05% max at 100kHz FS**
- **±0.2% max at 0.5MHz FS**

Output DTL/TTL/CMOS Compatible
V/F or F/V Conversion
6 Decade Dynamic Range
Voltage or Current Input
Reliable Monolithic Construction
Low Cost

ADVFC32 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The industry standard ADVFC32 is a low cost monolithic voltage to frequency (V/F) converter or frequency to voltage (F/V) converter with good linearity (0.01% max error at 10kHz) and operating frequency up to 0.5MHz. In the V/F configuration, positive or negative input voltages or currents can be converted to a proportional frequency using external components. For F/V conversion, the same components are used with a simple biasing network to accommodate a wide range of input logic levels.

TTL or CMOS compatibility is achieved in the V/F operating mode using an open collector frequency output. The pullup resistor can be connected to voltages up to 30 volts, or to +15V or +5V for conventional CMOS or TTL logic levels. This resistor should be chosen to limit current through the open collector output to 8mA, or a larger resistance can be used if driving a high impedance load.

Input offset drift is only 3ppm of full scale per °C, and full scale calibration drift is held to a maximum of 100ppm/°C (ADVFC32BM) due to a low T.C. zener diode. Power supply rejection of ±0.002%/% keeps additional external error sources at a minimum.

The ADVFC32 is available in commercial, industrial, or military temperature grades. The commercial grade is packaged in a 14 pin epoxy DIP while the two wider temperature range parts are packaged in hermetically sealed TO-100 cans. 883B processing is also available on the -55°C to +125°C part.

PRODUCT HIGHLIGHTS

1. The ADVFC32 uses a charge balancing circuit technique (see Functional Block Diagram) which is well suited to higher accuracy voltage to frequency conversion. Another strong point of this technique is that capacitance changes in the integration capacitor due to temperature or other influences are subtracted out in the V/F conversion cycle and have no net effect.
2. Full scale frequency to 0.5MHz is possible using commonly available capacitors for one shot timing and integration. The maximum input voltage can also be adjusted to accommodate a wide range by selecting the appropriate input resistor. Maximum input current should be set at 0.25mA.
3. The same components used for V/F conversion can also be used for F/V conversion by adding a simple logic biasing network and reconfiguring the ADVFC32.
4. Inexpensive diffused monolithic construction and plastic packaging (ADVFC32KN) for a low cost to the end user.

SPECIFICATIONS (typical @ +25°C with $V_S = \pm15V$, unless otherwise noted)

Model	VFC32KN	VFC32BH	VFC32SH
DYNAMIC PERFORMANCE			
Minimum Frequency Range	0 to 500kHz	*	*
Maximum Nonlinearity[1]			
f_{max} = 10kHz	±0.01% max	*	*
f_{max} = 100kHz	±0.05% max	*	*
f_{max} = 0.5MHz	±0.2%	*	*
Full Scale Calibration Error (adjustable to zero)	±5%	*	*
vs. Supply[2]	±0.002% of FSR/% max	*	*
vs. Temperature	±150ppm/°C max	±100ppm/°C	*
DYNAMIC RESPONSE			
Max Settling Time for Full Scale Step Input	1 Pulse of New Frequency Plus 1μs	*	*
Overload Recovery Time	1 Pulse of New Frequency Plus 1μs	*	*
ANALOG INPUT AMPLIFIER (V/F Conversion)			
Current Input Range	0 to +0.25mA	*	*
Voltage Input Range	-10 to 0, 0 to 0.25mA X R1	*	*
Differential Impedance	170k$\Omega | $10pF min	*	*
Common Mode Impedance	2.5M$\Omega | $10pF min	*	*
Input Bias Current			
Noninverting Input	40nA max	*	*
Inverting Input	8nA max	*	*
Input Offset Voltage (trimmable to zero)	4mV max	*	*
vs. Temperature (T_{min} to T_{max})	30μV/°C	*	*
Safe Input Voltage	$\pm V_S$	*	*
COMPARATOR (F/V Conversion)			
Logic "0" Level	$-V_S$ to -0.6V	*	*
Logic "1" Level	+1V to $+V_S$	*	*
Pulse Width Range	0.1μs to $(0.15/f_{max_{in\ Hz}})\mu s$	*	*
Input Impedance	250kΩ	*	*
OPEN COLLECTOR OUTPUT (V/F Conversion)			
Output Sink Current in Logic "0" V_{OUT} = 0.4V max (T_{min} to T_{max})	8mA min	*	*
Output Leakage Current in Logic "1"	100nA max	*	*
Voltage Range	0 to +30V	*	*
Fall Times (Load = 500pF and I_{OUT} = -5mA)	400ns	*	*
AMPLIFIER OUTPUT (F/V Conversion)			
Voltage Range	0 to 10V (1500Ω min)	*	*
Source Current	+10mA min (max Load Resistance of 750Ω)	*	*
Capacitive Load	100pF	*	*
POWER SUPPLY			
Voltage, Rated Performance			
Dual Supply	±9V to ±20V	*	*
Quiescent Current	6mA max	*	*
TEMPERATURE RANGE			
Rated Performance	0 to +70°C	-25°C to +85°C	-55°C to +125°C
Storage	-65°C to +150°C	*	*
PACKAGE OPTIONS[3]			
Plastic DIP (N14A)	ADVFC32KN	N/A	N/A
TO-100	N/A	ADVFC32BH	ADVFC32SH

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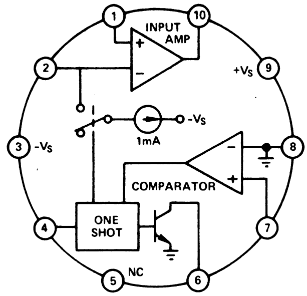
[1] Nonlinearity is defined as deviation from a straight line from zero to full scale, expressed as a percentage of full scale.

[2] Power supply rejection measured at full scale output frequency of 10kHz.

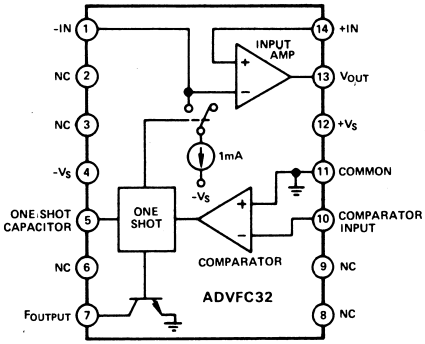
[3] See Section 20 for package outline information.

*Specifications same as VFC32KN.

Specifications subject to change without notice.



"H" PACKAGE – TO-100



"N" PACKAGE – N14A

ORDERING GUIDE

Part Number	Gain Tempco ppm/°C	Temp Range °C	Package
ADVFC32KN	150	0 to +70	N14A (Plastic DIP)
ADVFC32BH	100	-25 to +85	TO-100
ADVFC32SH*	150	-55 to +125	TO-100

*Order ADVFC32SH/883B for 883B processing.

UNIPOLAR V/F, POSITIVE INPUT VOLTAGE

When operated as a V/F converter, the transformation from voltage to frequency is based on a comparison of input signal magnitude to the 1mA internal current source. To illustrate this, consider one full cycle: the one shot output has just gone low disconnecting the 1mA current source from the inverting input, so that the only current flowing into the integrator is V_{IN}/R_{IN}. This current charges the integration capacitor (C2), forcing the integrator output down until the comparator triggers the one shot. During the active one shot period, the 1mA current source discharges the integration capacitor causing the integrator to ramp back up. The end of the one shot time period marks the end of the cycle and the integrator output voltage will be at the same level as at the beginning of the cycle. Some thought will show that this loop is self stabilizing, and will converge to a unique frequency.

Throughout the entire cycle (including the one shot time period) the input current (V_{IN}/R_{IN}) flows into the summing junction. The resulting voltage developed across the integration capacitor is discharged during the one shot time period through the 1mA current source. Since the integrator voltage ended up at the same level, the two (current X time) products must be equal.

Mathematically,

$$1\text{mA} \times t_{\text{one shot}} = \frac{V_{IN}}{R_{IN}} \times \frac{1}{\text{Frequency}}$$

or reformulated, frequency is directly proportional to input voltage:

$$\text{Frequency} = \frac{V_{IN}}{1\text{mA} \times t_{\text{one shot}} \times R_{IN}}$$

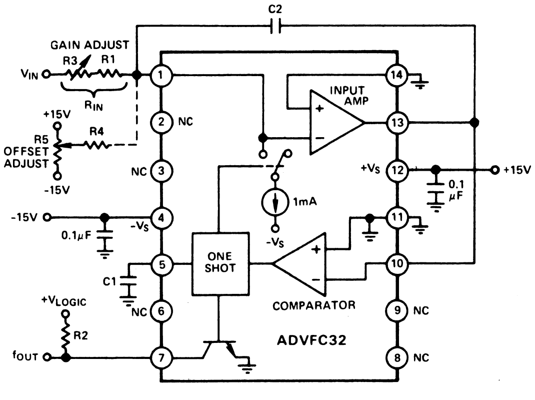


Figure 2. Connection Diagram for V/F Conversion, Positive Input Voltage

Components should be selected to optimize performance over the desired input voltage and output frequency range using the equation listed below.

$$C_1 = \frac{3.3 \times 10^{-5}}{F_{max}} - 3.0 \times 10^{-11} \text{ Farads}$$

$$C_2 = \frac{10^{-4}}{F_{max}} \text{ Farads (1000pF minimum)}$$

$$R_{IN} = \frac{V_{IN} \text{ max}}{0.25} \text{ k}\Omega$$

$$R_2 \geqslant \frac{+V_{LOGIC}}{8} \text{ k}\Omega$$

(maximum sink current of 8mA)

Both R_{IN} and C1 should have very low temperature coefficients as changes in their values will result in a proportionate change in the V/F transfer function. Other component values and temperature coefficients are not critical.

Input resistance R_{IN} is composed of a fixed resistor (R1) and a variable resistor (R3) to allow for initial gain error compensation. To cover all possible situations, R3 should be 20% of R_{IN}, and R1 should be 90% of R_{IN}. This allows a ±10% gain compensation. If more accurate initial offset is required, the circuit of R4 and R5 can be added. R5 can have a value between 10kΩ and 100kΩ but must have a temperature coefficient of <100ppm/°C. The tolerance and temperature coefficient of R4 are not critical as long as it has a nominal value of 10MΩ.

BIPOLAR V/F

By adding another resistor from pin 1 (pin 2 of TO-100 can) to a stable positive voltage, the ADVFC32 can be operated with a bipolar input voltage. For example, an 80kΩ resistor to +10V causes an additional current of 0.125mA to flow into the integrator so that the net current flow to the integrator is positive even for negative input voltages. At negative full scale input voltage, -0.125mA will flow into the integrator from V_{IN} cancelling out the 0.125mA from the offset resistor, resulting in an output frequency of zero. At positive full scale, the sum of the two currents will be 0.25mA and the output will be at its maximum frequency.

UNIPOLAR V/F, NEGATIVE INPUT VOLTAGE

Figure 3 shows the connection diagram for V/F conversion of negative input voltages. In this configuration full scale output frequency occurs at negative full scale input, and zero output frequency corresponds with zero input voltage.

A very high impedance signal source may be used since it only drives the noninverting integrator input. Typical input impedance at this terminal is 250kΩ or higher. For V/F conversion of positive input signals the signal generator must be able to source 0.25mA to properly drive the ADVFC32, but for negative V/F conversion the 0.25mA integration current is drawn from ground through R1 and R3.

Circuit operation for negative input voltages is very similar to positive input unipolar conversion described in a previous section. For best operating results use component equations listed in that section.

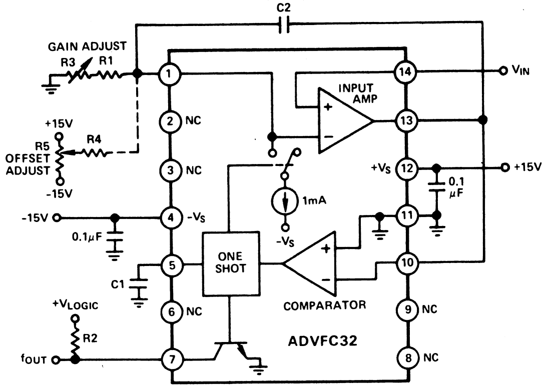


Figure 3. Connection Diagram for V/F Conversion, Negative Input Voltage

F/V CONVERSION

Although the mathematics of F/V conversion can be very complex, the basic principle is easy to understand. Figure 4 shows the connection diagram for F/V conversion with TTL input logic levels. Each time the input signal crosses the comparator threshold going negative, the one shot is activated and switches 1mA into the integrator input for a measured time period (determined by C1). As the frequency increases, the amount of charge injected into the integration capacitor increases proportionately. The voltage across the integration capacitor is stabilized when the leakage current through R1 and R3 equals the average current being switched into the integrator. The net result of these two effects is an average output voltage which is proportional to the input frequency. Optimum performance can be obtained by selecting components using the same guidelines and equations listed in the V/F conversion section.

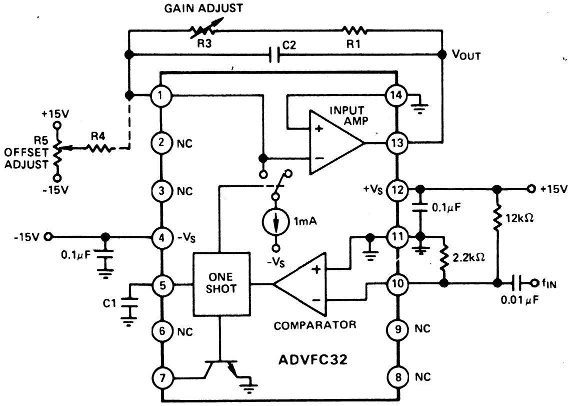


Figure 4. Connection Diagram for F/V Conversion, TTL Input

ANALOG DEVICES

Low-Cost, Versatile, 10/100kHz Frequency to Voltage Converters

MODELS 451, 453

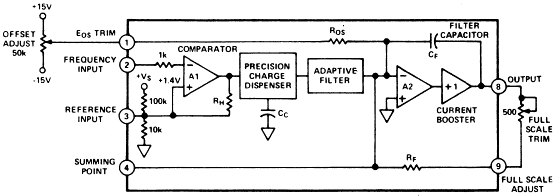
FEATURES

- Low Cost
- Versatility: Adjustable Threshold, Gain & Output Offset
- Guaranteed Low Nonlinearity: 80ppm Max, 451L and 453L
- Accepts TTL, CMOS, HNIL, Sinewave, Pulse, Squarewave and Triangle Wave Input Signals
- No External Components to Meet Rated Performance
- +20mA Output to Operate Relays and Meters
- Low Profile Package, 0.4" Case Height
- Meet MIL-STD-202E Environmental Testing

APPLICATIONS

- Motor Control and Speed Monitor
- Line Frequency Monitor and Alarm Indicator
- Fluid Flow Measurements and Control
- FM Demodulation and VCO Stabilization
- Frequency vs. Amplitude Response Measurements

MODEL 451, 453 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

Models 451 and 453 are low cost 10kHz and 100kHz frequency to voltage converters that feature excellent low nonlinearity to less than 80ppm, output current of +20mA and the capability of interfacing with TTL, HNIL, CMOS, sinewave, squarewave, pulse and triangular input signals. External components are not required to achieve rated performance, however, extreme versatility is maintained by allowing access to all critical points of the design. This versatility allows programmable input threshold, gain, and output offset voltage.

Both models 451 and 453 are available in three selections, each offering guaranteed maximum nonlinearity error as well as maximum gain drift error. Models 451J and 453J offer 0.03% max nonlinearity and 100ppm/°C max gain drift. Models 451K and 453K offer 0.015% max nonlinearity and 50ppm/°C max gain drift. Models 451L and 453L offer 0.008% max nonlinearity and 50ppm/°C max gain drift.

WHERE TO USE FREQUENCY TO VOLTAGE CONVERTERS

Pin compatible with existing popular models, these versatile new designs offer economical solutions to a wide variety of applications where it is required to convert frequency to an analog voltage.

Process Control Systems: For motor speed controllers, power line frequency monitoring and fluid flow measurements where flow transducers, such as variable reluctance magnetic pickups, provide pulse train outputs as a linear function of flow rate.

Audio and Accoustic Systems: For wow and flutter measurements with tape recorders and turntables, FM demodulation and speaker response measurements.

Test Instrumentation: For VCO stabilization, analog readout frequency meter, vibrational analysis and frequency versus amplitude X-Y plots where the vertical axis presents the normal amplitude signal and the horizontal axis presents the output signal from the F/V converter.

Data Acquisition Systems: For converting serially transmitted data back to analog voltages.

DESIGN FEATURES AND USER BENEFITS

The combination of low cost and high performance provided by models 451 and 453 offers exceptional quality and value to the OEM designer. These compact modules have been designed to provide maximum versatility, thereby increasing their utility in a broad scope of applications.

Adjustable Input Threshold: Threshold level is externally resistor programmable from 0 to ±12V, permitting simple, direct interface with low level signals, e.g. 10mV p-p, as well as with high level inputs such as CMOS and HNIL logic levels, e.g. 0 to +12V.

Adjustable Gain: Model 451 can be adjusted to provide full scale output voltage for any input frequency from 1kHz to 20kHz. Model 453 can be adjusted to provide full scale output voltage for any input frequency from 1kHz to 200kHz. This adjustable gain feature enables the user to easily match the maximum frequency output from a wide class of frequency transducers to the +10V full scale output from models 451 and 453. Increased signal conversion sensitivity with higher resolution results.

Adjustable Output Offset Voltage: The output offset is adjustable from -10V to +10V, enabling bipolar outputs or expanded scale measurements or setting the input frequency where zero output voltage occurs.

This two-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be found in Volume II, page 12-11.

SPECIFICATIONS (typical @ +25°C and V_S = ±15V dc unless otherwise noted)

MODEL	10kHz FULL SCALE			100kHz FULL SCALE		
	451			453		
	J	K	L	J	K	L
TRANSFER FUNCTION	$E_O = (10^{-3}\,V/Hz)(F_{IN})$			$E_O = (10^{-4}\,V/Hz)(F_{IN})$		
FREQUENCY INPUT						
Frequency Range	dc to 10kHz min			dc to 100kHz min		
Overrange	10% min			10% min		
Waveforms	Sine, Square, Triangle, Pulse Train			Sine, Square, Triangle, Pulse Train		
Pulse Width (Pulse Train Input)	20μs min			2μs min		
Threshold	+1.4V			+1.4V		
With External Adjustment	0V to ±12V			0V to ±12V		
Hysteresis	±50mV			±100mV		
Levels (TTL Compatible) High	+1.45V to +12V			+1.5V to +12V		
Low	-12V to +1.35V			-12V to +1.3V		
Max Safe Input Voltage[1]	$\pm V_S$			$\pm V_S$		
Impedance	10MΩ‖10pF			10MΩ‖10pF		
ACCURACY						
Warm-Up Time	one minute			one minute		
Nonlinearity[2]						
F_{IN} = 1Hz to 11kHz	±0.03% max	±0.015% max	±0.008% max	–	–	–
F_{IN} = 1Hz to 110kHz	–	–	–	±0.03% max	±0.015% max	±0.008% max
Gain vs. Temperature[3] (0 to +70°C)	±100ppm/°C max	±50ppm/°C max	±50ppm/°C max	±100ppm/°C max	±50ppm/°C max	±50ppm/°C max
vs. Supply Voltage	±300ppm/%			±350ppm/%		
vs. Time	±30ppm/month			±30ppm/month		
RESPONSE						
Step Response to ±0.5% of Final Value						
F_{IN} = dc to Full Scale	4ms			0.8ms		
F_{IN} = Full Scale to dc	30ms			4ms		
Internal Filter Time Constant	200μs			24μs		
External Filter Time Constant	20ms/μF			20ms/μF		
OUTPUT[4]						
Voltage (F_{IN} = Full Scale)[5]	+9.85V min; +9.95V max			+9.85V min; +9.95V max		
Current (E_O = +10V, -10V)	(+20, -2)mA min			(+20, -2)mA min		
Offset Voltage[6] @ +25°C	±7.5mV max			±7.5mV max		
vs. Temperature (0 to +70°C)	±30μV/°C max			±30μV/°C max		
vs. Supply Voltage	±100μV/% max			±50μV/% max		
vs. Time	±100μV/month			±100μV/month		
Ripple						
F_{IN} = 1Hz	3mV p-p			55mV p-p		
F_{IN} = 10kHz	80mV rms			35mV rms		
F_{IN} = 100kHz	–			35mV rms		
Impedance	0.1Ω			0.1Ω		
Offset Scale Factor[7]	-56μA/V			-45μA/V		
POWER SUPPLY[8]						
Voltage, Rated Performance	±15V dc			±15V dc		
Voltage, Operating	±(12 to 18)V dc			±(12 to 18)V dc		
Current, Quiescent	(+10, -8)mA			(+10, -8)mA		
TEMPERATURE RANGE						
Rated Performance	0 to +70°C			0 to +70°C		
Operating	-25°C to +85°C			-25°C to +85°C		
Storage	-55°C to +85°C			-55°C to +125°C		
MECHANICAL						
Case Size	1.5" x 1.5" x 0.4"			1.5" x 1.5" x 0.4"		
Weight	25 grams			25 grams		

[1] F_{IN} and REF terminals can be shorted to $\pm V_S$ indefinitely without damage.
[2] Nonlinearity error is specified as a percentage of 10V full scale output level.
[3] Gain temperature drift is specified in ppm of output signal level.
[4] OUT terminal can be shorted indefinitely to $\pm V_S$ and ground without damage.
[5] Adjustable to +10.000V using FULL SCALE ADJUST trim pot.
[6] Adjustable to zero using 50kΩ OFFSET ADJUST trim pot.
[7] Current into the SUM PT terminal to offset the output voltage positive.
[8] Recommended power supply, ADI model 904, ±15V @ 50mA output.

Specifications subject to change without notice.

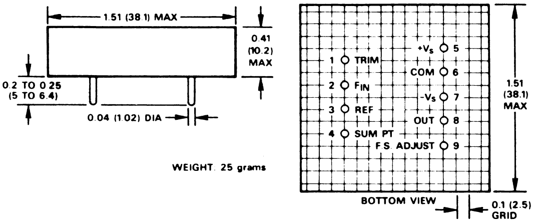
All Units Meet the Requirements of
MIL-STD-202E as Outlined Below

TEST	METHOD	CONDITION
High Temperature Storage	108A	D (Non-Operating)
Moisture Resistance	106D	(10 Days)
Solderability	208C	
Thermal Shock	107D	A (5 Cycles)
Terminal Strength	211A	A (Pull Test, 10 lbs)
Temperature Cycling	102A	D (-55°C/+85°C)
Vibration	204C	B (15g Peak)
Barometric Pressure	105C	B (50,000 Feet)

TABLE 1. Environmental Specifications

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm)



Synchro & Resolver Converters

Contents

Page

Selection Guide 13–2

General Information and Definitions of Devices 13–4

●SDC/RDC1740/1741/1742 12- and 14-Bit Hybrid Synchro/Resolver to Digital Converters 13–5

●New product since *1980 Data-Acquisition Components and Subsystems Catalog*

Selection Guide
Synchro & Resolver Converters

The products in this section are generally concerned with angular measurements. They include the following classes of device:

- Digital Angle to Trigonometric (sine-cosine) Analog Voltage
- Digital-to-Resolver Converters
- Digital-to-Synchro Converters
- Inductosyn™-to-Digital Converters
- Resolver-to-Analog Voltage Converters
- Resolver-to-Digital Converters
- Resolver-to-Digital Display (Angular-Position Indicators)
- Synchro-to-Analog Voltage Converters
- Synchro-to-Digital Converters
- Synchro-to-Digital Display (Angular-Position Indicators)

Complete descriptions, specifications, and applications information on the products in this section can be found in the data sheets. Brief general information can be found overleaf.

The Selection Guide is provided to ease the job of finding the right unit to do your job. Devices are listed in the Selection Guide vertically, by model number, in alphabetic, then numeric order, as well as by function and type of input. Salient characteristics are listed horizontally. A bullet is placed at each intersection that is appropriate for each device.

			ANALOG I/O				DIGITAL I/O								
								BCD			RESOLUTION (BITS)				
			SYNCHRO	RESOLVER	INDUCTOSYN™	LINEAR	BINARY	0 to ±180°	0 to 360°	PULSE TRAIN	18	16	14	12	10
SYNCHRO RESOLVER INPUT	Angle Position Indicator	API1620	●	●			●		●			●			
		API1718	●	●			●		●			●			
DIGITAL INPUT	Digital to Synchro Resolver	DSC1705	●	●			●						●		
		DSC1706	●	●			●							●	
	Digital to Trig. (Analog)	DTM1716				●							●		
		DTM1717				●								●	
INDUCTOSYN	Inductosyn/ Resolver to Digital	IRDC1730		●	●		●							●	
		IRDC1731		●	●					●				●	
RESOLVER INPUT	Resolver to Digital Converters	RDC1727		●			●				●				
		RDC1740		●			●						●		
		RDC1741		●			●							●	
		RDC1742		●			●							●	
	Sync/Resolver Analog	SAC1763	●	●		●									
	Synchro or Resolver to BCD Converters	SBCD1752	●	●				●					●[1]		
		SBCD1753	●	●				●					●[2]		
		SBCD1756	●	●					●				●[1]		
		SBCD1757	●	●					●				●[2]		
	Synchro or Resolver to Binary	SDC1700	●	●			●							●	
		SDC1702	●	●			●								●
		SDC1704	●	●			●						●		
		SDC1725	●	●			●							●	
		SDC1726	●	●			●								●
SYNCHRO INPUT	Synchro to Digital	SDC1727	●				●				●				
		SDC1740	●				●						●		
		SDC1741	●				●							●	
		SDC1742	●				●							●	

[1] 13 Bit BCD plus sign.

[2] 14 Bits BCD.

Inductosyn is a registered trademark of Farrand Industries Inc.

Here's an example of its use: if you were looking for a 14-bit resolver-to-digital converter with the highest accuracy in the smallest package, you night start at the 14-bit column; you would see that there are two resolver families that have 14-bit resolution and error less than 5 arc-minutes: RDC1740 and SDC1704; the RDC1740 is a hybrid, and the SDC1704 is in a 0.4"H module. Thus, you would be quickly led to look at the SDC/RDC1740 data sheet and be guided to its location by the page number at the right.

In addition to the devices listed in the chart, data sheets for the following accessory products are also to be found in this section:

Resolver and Synchro 5VA Output Transformers, models RTM/STM1686/1696/1736/1687/1697/1737	Volume II, Page 13-27
Synchro/Resolver 5VA-Output Power Amplifier, model SPA1695	Volume II, Page 13-57
Two-Speed Processor for Coarse/Fine Synchro/Resolver Systems, model TSL1612	Volume II, Page 13-59

	ACCURACY (arc-min)					ASSEMBLY/PACKAGE TECHNOLOGY					PAGE		
							MODULE						
	≤1	≤5	≤10	≤20	≥20	HYBRID	≤0.4"H	0.4"H	≥0.4"H	INSTRUMENT	VOLUME I	VOLUME II	
		●								●	–	13-5	API1620
		●								●	–	13-5	API1718
		●							●		–	13-9	DSC1705
			●						●		–	13-9	DSC1706
		●						●			–	13-13	DTM1716
		●						●			–	13-13	DTM1717
				●				●			–	13-17	IRDC1730
				●				●			–	13-23	IRDC1731
	●								●		–	13-49	RDC1727
		●				●					13-5	13-53	RDC1740
				●		●					13-5	13-53	RDC1741
			●			●					13-5	13-53	RDC1742
				●					●		–	13-31	SAC1763
				●					●		–	13-35	SBCD1752
				●					●		–	13-35	SBCD1753
				●					●		–	13-35	SBCD1756
				●					●		–	13-35	SBCD1757
			●					●			–	13-39	SDC1700
					●			●			–	13-39	SDC1702
		●						●			–	13-39	SDC1704
		●					●				–	13-45	SDC1725
				●			●				–	13-45	SDC1726
	●								●		–	13-49	SDC1727
		●				●					13-5	13-53	SDC1740
				●		●					13-5	13-53	SDC1741
			●			●					13-5	13-53	SDC1742

Orientation

Synchro & Resolver Converters

These products constitute a complete line of devices for the digital measurement and control of angular and linear displacements by means of synchros, resolvers, and Inductosyns. In addition to modules and hybrid circuits that perform the appropriate conversions, the line also includes modules that perform purely algebraic or logical functions; in some cases, solid-state circuitry emulates the functions of electromechanical devices.

The range of synchro processing modules now available covers a wide area of application. They are widely used in military and radar applications, but there are additional fields in which they could be used to advantage because of the proven ruggedness and high precision of the electromechanical hardware, their standardized specifications, and their low cost. They have a number of advantages over potentiometers and optical systems.

In this introductory section, there will be provided a brief set of device definitions. Detailed data and applications information is given in the data sheets. For a complete introduction to synchro/digital conversion, Analog Devices has available a 208-page book, *Synchro and Resolver Conversion*, edited by G. Boyes (1980), $11.50.

In this section, and in much of the text, the word "Synchro" appears frequently. In many cases, the word "Resolver" could be used in its place. The modules make use of angular data in resolver form; if the input data is in three-wire synchro form, transformers in "Scott T" configuration convert it to resolver form; analog outputs are available in both forms. There are a number of voltage and frequency options.

REPRESENTATION OF ANGLES IN DIGITAL FORM

Binary

The most commonly used method of representing angles in digital form is simple natural binary weighting, where the most-significant bit (MSB) represents 180°, the next represents 90°, etc. The table shows the bit weights in degrees, degrees-and-minutes, and radians for this coding method.

BCD

When angular measures have to be displayed in visual form, BCD coding is used, through the use of binary-to-BCD converters, such as the BDM1615, which provides the necessary scaling and conversion, e.g., from 10100000000000 (180° + 45°) to 10 0010 0101.0000 000 (or 225.00°).

TYPICAL S/D/S DEVICES

Binary-to-Binary-Coded-Digital Converter (BDM1615/16/17)

A device that accepts angular data in binary form and converts it to BCD form, with fractional degrees in decimal fractions of 1° (1615, 1617) or minutes and seconds (1616). The BCD output is modulo 360°.

Bit No.	Degrees	Degrees, minutes		Radians
1	180	180	0	3.141593
2	90	90	0	1.570796
3	45	45	0	0.785398
4	22.5	22	30	0.392699
5	11.25	11	15	0.196349
6	5.625	5	37.5	0.098175
7	2.8125	2	48.75	0.049087
8	1.40625	1	24.38	0.024544
9	0.70312	0	42.19	0.012272
10	0.35156	0	21.09	0.006136
11	0.17578	0	10.55	0.003068
12	0.08789	0	5.27	0.001534
13	0.04395	0	2.64	0.000767
14	0.02197	0	1.32	0.000383
15	0.01099	0	0.66	0.000192
16	0.00549	0	0.33	0.000096

Digital-to-Synchro Converters (DSC1705/06)

Devices that accept parallel binary digital inputs (14 or 12 bits) and an ac reference signal, and provide outputs in 3-wire synchro form.

Inductosyn/Resolver-to-Digital Converter (IRDC1730)

A device that produces a digital output capable of resolving (to 12 bits) intermediate distances within a single track-pitch of a Farrand linear-Inductosyn stator in displacement- and angle-measuring Inductosyn systems. The moving element is used as though it were a resolver input; hence the device will also convert resolver information to digital.

Synchro-to-Digital Converter

A device that accepts either 3-wire synchro- or 4-wire resolver inputs, together with a 2-wire ac reference, and outputs angular binary data in a continuously tracking mode, employing a Type 2 servo loop. The inputs may be from either remote synchros or from electrically simulated synchros (e.g., DSC's).

Digital Converter and Processor for Two-Speed Synchros (TSL1612)

A two-speed processor takes as inputs two sets of digital information, representing the angles from coarse and fine synchros, and combines them to produce a single 19-bit word representing the actual angle of the "coarse" shaft. The TSL consists of the processing logic alone—it can be used with a pair of SDC's, which provide the two sets of digital information.

ANALOG DEVICES

12 and 14 Bit Hybrid Synchro/ Resolver to Digital Converters

SDC/RDC1740/1741/1742

FEATURES

Internal Isolating Transformers
14-Bit or 12-Bit Resolution
Three Accuracy Options
Three-State Latched Output
Continuous Tracking – Even During Data Transfer
Simple Data Transfer
Laser Trimmed – No External Adjustments
MIL Spec/Hi Rel Options Available
Hermetically Sealed

APPLICATIONS

Avionic Systems
Servo Mechanisms
Coordinate Conversion
Axis Transformation
Antenna Monitoring
Artillery Fire Control Systems
Engine Controllers

GENERAL DESCRIPTION

The SDC1740, SDC1741 and SDC1742 are hybrid, continuous tracking synchro or resolver to digital converters which employ a type 2 servo loop and contain three-state latches on the digital outputs.

The input signals can either be 3 wire synchro plus reference or 4 wire resolver format plus reference depending on the option; and the outputs are presented in TTL compatible parallel natural binary buffered by three-state latches.

The three state output facility, which has separate $\overline{\text{ENABLE}}$ inputs for the most significant 8 bits and the least significant 4 bits (or 6 bits in the case of the SDC1740), not only simplifies multiplexing of more than one device onto a single data bus, but also enables the $\overline{\text{INHIBIT}}$ to be used without opening the internal converter loop.

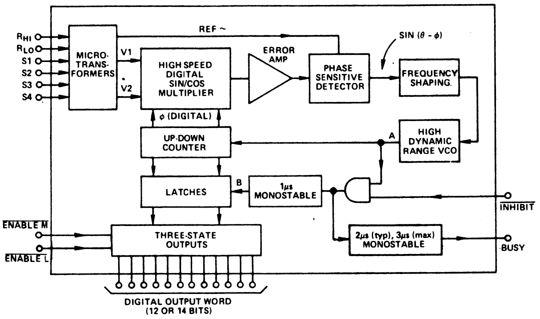
An outstanding feature of these converters is that although the profile height is only 0.28 inches (7.1mm) they contain internal transformers which provide for true isolation on the signal and reference inputs.

The converters are hermetically sealed in a metal 32-pin dual in line package.

To ensure a level of reliability consistent with the performance, each converter receives a stringent pre-cap visual inspection, high temperature storage and temperature cycling, fine and gross leak testing, acceleration testing and operating burn-in.

The converters are also available processed in accordance with MIL-STD-883, Method 5008, Class B.

SDC/RDC1740/1741/1742 FUNCTIONAL BLOCK DIAGRAM



MODELS AVAILABLE

The three synchro/resolver to digital converters described in this data sheet differ primarily in the areas of resolution, accuracy and dynamic performance as follows:

Model SDC1740XYZ is a 14-bit converter with an overall accuracy of ±4 arc-minutes and a resolution of 1.3 arc-minutes.

Model SDC1741XYZ is a 12-bit converter with an accuracy of ±15.3 arc-minutes and a resolution of 5.3 arc-minutes.

Model SDC1742XYZ is a 12-bit converter with an accuracy of ±8.5 arc-minutes and a resolution of 5.3 arc-minutes.

The XYZ code defines the option as follows: (X) signifies the operating temperature range, (Y) signifies the reference frequency, (Z) signifies the signal and reference voltage and whether it will accept synchro or resolver format.

More information about the option code is given under the heading of "Ordering Information".

THEORY OF OPERATION

If the unit is a Synchro to Digital Converter the 3 wire synchro output will be connected to S1, S2 and S3 on the unit and the Scott T transformer pair will convert these signals into resolver format.

i.e., $V_1 = K\,E_O \text{ Sin } \omega t \text{ Sin } \theta$

$V_2 = K\,E_O \text{ Sin } \omega t \text{ Cos } \theta$

Where θ is the angle of the synchro shaft.

SPECIFICATIONS (typical @ +25°C unless otherwise specified)

Models	SDC/RDC1742	SDC/RDC1741	SDC/RDC1740
ACCURACY[1] (Max Error on all Options)	±8.5 arc-minutes	±15.3 arc-minutes	±4 arc-minutes
RESOLUTION	12 Bits (1LSB = 5.3 arc-minutes)	*	14 Bits (1LSB = 1.3 arc-minutes)
OUTPUT	12 Bits Parallel Natural Binary	*	14 Bits Parallel Natural Binary
SIGNAL AND REFERENCE FREQUENCY	400Hz or 2.6kHz	*	*
SIGNAL VOLTAGE (Line to Line)	90V, 26V or 11.8V rms	*	*
SIGNAL IMPEDANCE			
90 Volt Signal	200kΩ (Resistive)	*	*
26V Signal	57.7kΩ (Resistive)	*	*
11.8V Volt Signal	26kΩ (Resistive)	*	*
REFERENCE VOLTAGE	115V, 26V or 11.8V rms	*	*
REFERENCE IMPEDANCE			
115 Volt Reference	120kΩ (Resistive)	*	*
26 Volt Reference	27kΩ (Resistive)	*	*
11.8 Volt Reference	12.3kΩ (Resistive)	*	*
TRANSFORMER ISOLATION	350V dc	*	*
TRACKING RATE (Minimum)	18 Revolutions Per Second	*	12 Revolutions Per Second
ACCELERATION			
Constant K_a	$66,000/sec^2$	*	$36,000/sec^2$
STEP RESPONSE (179° Step for Settling to 1LSB of Error)	150ms	*	*
POWER LINES			
+15V	19mA (typ) 23mA (max)	*	23mA (typ) 30mA (max)
-15V	19mA (typ) 23mA (max)	*	23mA (typ) 30mA (max)
+5V	45mA (typ) 110mA (max)	*	150mA (typ) 180mA (max)
POWER DISSIPATION	0.8 Watts (typ) 1.3 Watts (max)	*	1.44 Watts (typ) 1.8 Watts (max)
DATA LOGIC OUTPUTS[2]	6TTL Loads	*	*
BUSY LOGIC OUTPUT LOADING[2]	2TTL Loads	*	*
BUSY LOGIC OUTPUT WIDTH	3μs (max)	*	*
INHIBIT INPUT (TO INHIBIT)	Logic "0" 1TTL Load	*	*
ENABLE INPUTS (TO ENABLE)[3]	Logic "0" 1TTL Load	*	*
TEMPERATURE RANGE			
Operating	-55°C to +125°C	*	*
Storage	-65°C to +150°C	*	*
PACKAGE OPTION[4]			
Hermetic DIP	HY32B	*	*
WEIGHT	0.8 ozs (23 G)	*	*

*Specifications the same as for SDC/RDC1742.

NOTES

[1] Specified over the appropriate operating temperature range and for: (a) ±10% signal and reference amplitude variation; (b) 10% signal and reference harmonic distortion; (c) ±5% power supply variation; and (d) ±10% variation in reference frequency.

[2] Schottky logic loading rules apply.

[3] ENABLE M enable most significant 8 bits.
ENABLE L enable least significant 4 bits (or 6 bits for the SDC/RDC1740).

[4] See Section 20 for package outline information.

Specifications subject to change without notice.

If the unit is a Resolver to Digital Converter, the 4 wire resolver output will be connected to S1, S2, S3 and S4 on the unit and the transformers will act purely as isolators.

To understand the conversion process, assume that the current word state of the up-down counter is ϕ.

Then V_1 is multiplied by Cos ϕ and V_2 is multiplied by Sin ϕ to give:

$$K E_O \sin \omega t \sin \theta \cos \phi$$

and

$$K E_O \sin \omega t \cos \theta \sin \phi$$

These signals are subtracted by the error amplifier to give:

$$K E_O \sin \omega t (\sin \theta \cos \phi - \cos \theta \sin \phi)$$

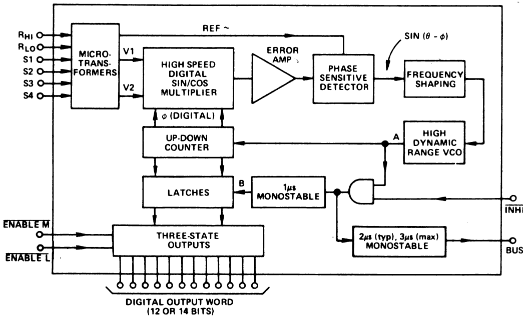
or

$$K E_O \sin \omega t \sin (\theta - \phi)$$

A phase sensitive detector, integrator and voltage controlled oscillator (VCO) form a closed loop system which seeks to null Sin $(\theta - \phi)$.

When this is accomplished, the word state of the up-down counter (ϕ) equals, within the rated accuracy of the converter, the synchro shaft angle θ.

Assuming that the "$\overline{\text{INHIBIT}}$" is at a logic high state, then the digital word ϕ will be strobed into the latches 1µs after the up-down counter has been updated. If the three state "$\overline{\text{ENABLE}}$" is at a logic low, then the digital output word will be presented to the output pins of the unit.



Functional Diagram of the SDC/RDC1740, SDC/RDC1741 and the SDC/RDC1742

DATA TRANSFER

Data transfer from the converters is straightforward.

Consider the timing sequence shown in the timing diagram which assumes that the input to the converter is changing.

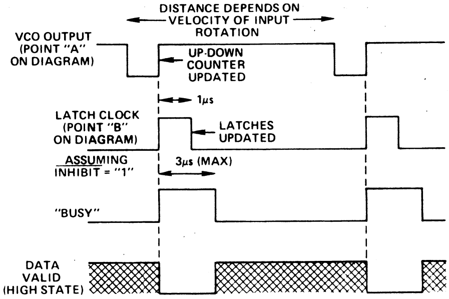
From this diagram, it can be seen that there are two ways to transfer data.

One method is to detect the state of the BUSY signal, which is high for up to 2.0 microseconds (typical) while the up-down counters and latches are settling, and transfer data when it is in a low state.

An alternative method is to use the "$\overline{\text{INHIBIT}}$" input. As can be seen from the functional diagram, application of the "$\overline{\text{INHIBIT}}$" prevents the two monostables being triggered and consequently the latches being updated. Therefore, it follows that data will always be valid after 3µs has elapsed from the application of the $\overline{\text{INHIBIT}}$ (i.e. taken to logic low). It can also be seen that this method of data transfer is valid regardless of when the $\overline{\text{INHIBIT}}$ is applied.

The three-state $\overline{\text{ENABLE}}$ can be used at any time in order to present the data in the latches to the output pins. $\overline{\text{ENABLE M}}$ enables the most significant 8 bits while $\overline{\text{ENABLE L}}$ enables the least significant 4 bits (6 bits in the SDC/RDC1740).

Note that the operation of the internal converter loop cannot be affected in any way by the logic state present on the INHIBIT and ENABLE pins.


DISTANCE DEPENDS ON VELOCITY OF INPUT ROTATION
VCO OUTPUT (POINT "A" ON DIAGRAM)
UP-DOWN COUNTER UPDATED
1µs
LATCH CLOCK (POINT "B" ON DIAGRAM)
LATCHES UPDATED
ASSUMING INHIBIT = "1"
3µs (MAX)
"BUSY"
DATA VALID (HIGH STATE)

Timing Diagram

Bit Number	Weight in Degrees
1 (MSB)	180.0000°
2	90.0000
3	45.0000
4	22.5000
5	11.2500
6	5.6250
7	2.8125
8	1.4063
9	0.7031
10	0.3516
11	0.1758
12 (LSB) For 1741/1742	0.0879
13	0.0439
14 (LSB For 1740	0.0220

Bit Weight Table

CONNECTING THE CONVERTER

The electrical connections to the converter are straightforward. The power lines, which must not be reversed, should be connected to the "+15V", "–15V" and "+5V" pins with the common connection to the ground pin "GND". It is suggested that a parallel combination of a 0.1µF and a 6.8µF capacitor is placed in each of the three positions from "+15V" to "GND", from "–15V" to "GND" and from "+5V" to "GND".

The pin marked "case" is connected electrically to the case and should be taken to a convenient zero volt potential in the system.

The digital output is taken from Pin "1" through to "12" for the SDC/RDC1742 and SDC/RDC1741 and "1" through to "14" for the SDC/RDC1740, where Pin "1" is the MSB.

The reference connections are made to "R_{HI}" and "R_{LO}".

In the case of a Synchro, the signals are connected to "S1", "S2" and "S3" according to the following convention:

$$E_{S1-S3} = E_{RLO-RHI} \sin \omega t \sin \theta$$

$$E_{S3-S2} = E_{RLO-RHI} \sin \omega t \sin (\theta + 120^\circ)$$

$$E_{S2-S1} = E_{RLO-RHI} \sin \omega t \sin (\theta + 240^\circ)$$

For a resolver, the signals are connected to "S1", "S2", "S3" and "S4" according to the following convention:

$$E_{S1-S3} = E_{RLO-RHI} \text{ Sin } \omega t \text{ Sin } \theta$$
$$E_{S2-S4} = E_{RHI-RLO} \text{ Sin } \omega t \text{ Cos } \theta$$

The "BUSY", "$\overline{\text{INHIBIT}}$" and "$\overline{\text{ENABLE}}$" pins should be connected as described under the heading "Data Transfer".

RESISTIVE SCALING OF INPUTS

A feature of these converters is that the signal and reference inputs can be resistively scaled to accommodate any range of input signal and reference voltages.

This means that a standard converter can be used with a personality card in systems where a wide range of input and reference voltages are encountered.

To calculate the values of the external scaling resistors in the case of a Synchro Converter, add 1.11kΩ per extra volt of signal in series with "S1", "S2" and "S3", and 1kΩ per extra volt of reference in series with "R_{HI}".

In the case of a Resolver to Digital Converter, add 2.22kΩ in series with "S1" and "S2" per extra volt of signal and 1kΩ per extra volt of reference in series with "R_{HI}".

MEAN TIME BETWEEN FAILURES (MTBF)

The reliability of these products is very high due to the extensive use of custom chip circuitry. For details of MTBF figures under particular conditions please consult the factory.

ORDERING INFORMATION

When ordering, the converter part numbers should be suffixed by an option code in order to fully define them. All the standard options and their option codes are shown below. For options not shown, please consult the factory.

SDC 1740 X Y Z

SDC = Synchro to Digital Converter
RDC = Resolver to Digital Converter

Z = 1	Signal	11.8V	Reference	26V	Synchro
Z = 2	Signal	90V	Reference	115V	Synchro
Z = 3	Signal	11.8V	Reference	11.8V	Resolver
Z = 4	Signal	26V	Reference	26V	Resolver
Z = 8	Signal	11.8V	Reference	26V	Resolver

1740 = 14-bit resolution, ±4 arc-min accuracy
1741 = 12-bit resolution, ±15.3 arc-min accuracy
1742 = 12-bit resolution, ±8.5 arc-min accuracy

Y = 1 400Hz Reference Frequency
Y = 4 2.6kHz Reference Frequency

X = 4 -55°C to +125°C Operating Temperature Range

Sample/Track-Hold Amplifiers

Contents

Page

Selection Guide 14–3
General Information and Definitions of Key Specifications 14–4
•AD346JD/SD High-Speed Sample-and-Hold Amplifier 14–7
AD582K/S Monolithic IC Sample-Hold Amplifier, Low Cost 14–9
AD583K Monolithic IC Sample-Hold Amplifier, High Speed 14–13
•ADSHC-85 Fast 0.01% Track/Sample-Hold Amplifiers 14–17
•ADSHM-5/5K Ultra Fast 0.01% Track/Sample-Hold Amplifiers 14–21
HTS/HTC Hybrid High-Speed Track-Hold Amplifier Series 14–23
SHA1144 High-Resolution Sample-Hold Amplifier 14–29

•New product since *1980 Data-Acquisition Components and Subsystems Catalog*

Selection Guide
Sample/Track-Hold Amplifiers

1. GENERAL PURPOSE

Model	Acquisition Time	Characteristics	Vol I Page	Vol II Page
AD583K	4μs to ±0.1% (C = 50pF)	Aperture time 50ns, 10pC charge transfer	14–13	–
AD582K/S	6μs to ±0.1% (C = 100pF)	Aperture time 150ns, nonlinearity ±0.01%, low cost	14–9	–

2. HIGH SPEED

Model	Acquisition Time	Characteristics	Vol I Page	Vol II Page
AD346	2μs to ±0.01%	Aperture time 60ns, low droop 0.5mV/μs	14–7	–
ADSHC-85	4.5μs to ±0.01%	Aperture time 25ns, low droop 0.2mV/μs	14–17	–

3. VERY HIGH SPEED

Model	Acquisition Time	Characteristics	Vol I Page	Vol II Page
HTS-0025	20ns to 1%	Aperture jitter 20ps, 0.01% nonlinearity	14–23	–
THS-0025	20ns to 1%	Aperture jitter 20ps, 0.01% nonlinearity	–	14–15
THS-0060	75ns to 1%	Aperture jitter 20ps, 0.01% nonlinearity	–	14–15
THS-0225	300ns to 1%	Aperture jitter 20ps, 0.01% nonlinearity	–	14–15
HTC-0300	100ns to 0.1%	Aperture jitter 100ps, max, 0.01% nonlinearity	14–23	–
THC-0300	100ns to 0.1%	Aperture jitter 100ps, max, 0.01% nonlinearity	–	14–15
THC-0750	300ns to 0.1%	Aperture jitter 100ps, max, 0.01% nonlinearity	–	14–15
THC-1500	1000ns to 0.1%	Aperture jitter 100ps, max, 0.01% nonlinearity	–	14–15
ADSHM-5	350ns to 0.01%	Low droop 20μV/μs, 0.005% nonlinearity	14–21	14–7
ADSHM-5K	250ns to 0.01%	Low droop 12μV/μs, 0.005% nonlinearity	14–21	14–7

4. HIGH RESOLUTION

Model	Acquisition Time	Characteristics	Vol I Page	Vol II Page
SHA1144	8μs max to 0.003%	Aperture jitter 500ps, gain nonlinearity ±0.001%	14–29	14–11

Orientation
Sample/Track-Hold Amplifiers

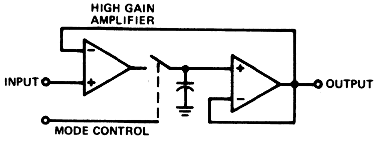
The principal application for sample/track-hold amplifiers is to maintain an analog-to-digital converter's input constant during conversion, at a value representing the analog input as of a certain precisely known time. The characteristics of the SHA are crucial to system accuracy and the reliability of the digital data, especially in 12-bit and/or high-throughput-rate applications.

A sample/track-hold amplifier (s/h or SHA), as its name indicates, has two modes of operation, programmed by a digital control-input. In the *track*— or *sample*—mode, the output follows the input, usually with a gain of +1. When the mode-input switches to *hold*, the output of the SHA ideally retains the last value it had when the command to hold was given, and it retains that value until the logic input dictates *track (sample)*, at which time the output ideally jumps to the input value and follows the input until the next *hold* command is given.

Analog Devices *track-holds* and *sample-holds* are functionally identical; they are designed to acquire input signals for either immediate hold or for a possibly extended period of tracking. They should not be confused with ac devices termed "sample-hold" that can *only* obtain quick samples and cannot track the input continuously.

SHA CIRCUITRY AND HARDWARE

A sample-hold amplifier usually consists of a storage capacitor, input- and output buffer-amplifiers, and a switch and its drive-circuitry. During *sample*, the circuit is connected to promote rapid charging of the capacitor. During *hold*, the capacitor is disconnected from its charging source and—ideally— retains its charge. The figure below shows a typical feedback configuration (AD583): the input buffer is a high-gain differential amplifier with a current output that charges the capacitor through the logic-controlled switch. The capacitor is unloaded by a unity-gain buffer-follower. The output is fed back to the negative input (as in an op-amp follower configuration), and thus, in *sample*, the charge on the capacitor is compelled to follow the input. In *hold*, the input amplifier no longer drives the capacitor; it retains its charge, unloaded by the output follower. In another popular configuration, the capacitor is used as the feedback element of an inside-the-loop integrator (AD582, SHA1144, HTC-0300). The highest-speed devices (HTS-0025) usually run open-loop.

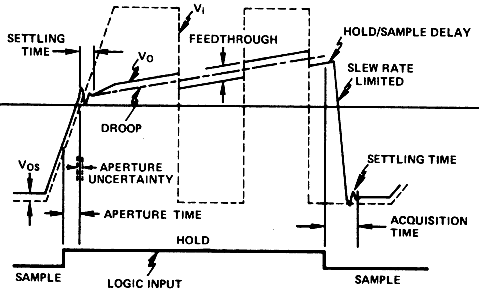


Since drive current is finite, and leakage current in *hold* is not zero, the capacitance—if large—limits the slewing rate in *sample* and—if small—converts leakage current to "droop" in *hold*. In s/h *hybrids*, the capacitance is usually fixed, and the properties of the complete device are optimized for one condition— and so specified. In s/h *monolithic ICs*, the capacitor is omitted, and furnished by the user (both for flexibility and because good capacitors for this purpose are hard to integrate). The optimum capacitance can be selected for the specific application. Design curves of performance vs. capacitance, given on the IC data sheets (AD582 and AD583) facilitate this process. In some types, the gain connections are external, like those of an op amp (AD582, AD583, SHA1144), permitting gains other than +1.

PERFORMANCE

In the *sample* mode, it is useful to consider that a SHA's performance can be characterized by specifications similar to those of a closed-loop operational amplifier (offset, drift, nonlinearity, gain error, bias current, etc.), but with somewhat slower response (gain-bandwidth, slewing rate, settling time) because of the need to charge the storage capacitor.

However, during the *sample-to-hold, hold,* and *hold-to-sample* states, the dynamic nature of the mode-switching introduces a number of specifications that are peculiar to SHAs. The most-important of these are defined below and illustrated in the adjoining figure. They include the *aperture time* and its *uncertainty*, the *sample-to-hold step, feedthrough* and *droop* (in hold), and *acquisition time.*



DEFINITIONS

Acquisition Time is the time required by the output of the device to reach its final value, within a specified error band, after the *sample* command has been given. Included are switch-delay time, the slewing interval, and settling time for a specified output-voltage change.

Aperture (Delay) Time is the time required after the *hold* command for the switch to open fully. The sample is, in effect, delayed by this interval, and the *hold* command would have to be advanced by this amount for precise timing.

Aperture Uncertainty—or *Aperture (Delay) Jitter*—is the range of variation in the *aperture time*. If the *aperture time* is "tuned out" by advancing the *hold* command a suitable amount, this spec establishes the ultimate timing error, hence, the maximum sampling frequency to a given resolution.

Charge Transfer (or *offset step*), the principal component of *sample-to-hold* offset (or *pedestal*), is the charge transferred to the storage capacitor via stray capacitance when switching to the *hold* mode. It can sometimes be reduced by lightly coupling an appropriate-polarity version of the *hold* signal to the capacitor for cancellation. The associated voltage error ($\Delta Q/C$) can be reduced by using greater capacitance for storage; but this increases response time.

Droop is the change of the output voltage during *hold* as a result of leakage or bias currents flowing through the storage capacitor. Its polarity depends on the sources of leakage current within a given device. In ICs, it is specified as a *(droop* or *drift)* current, in modules, a dV/dt. (Note: $I = CdV/dt$.)

Feedthrough is the fraction of the input signal variation or ac input waveform that appears at the output in *hold*. It is caused by stray capacitive coupling from the input to the storage capacitor, principally across the open switch.

Sample-to-Hold Offset, a shift in level between the last value in *sample* and the value settled-to in *hold*, is the residual step error after the *charge transfer* is accounted for and/or cancelled. Since it is unpredictable in magnitude and may be a function of the signal, it is also known as *offset nonlinearity.*

ANALOG DEVICES

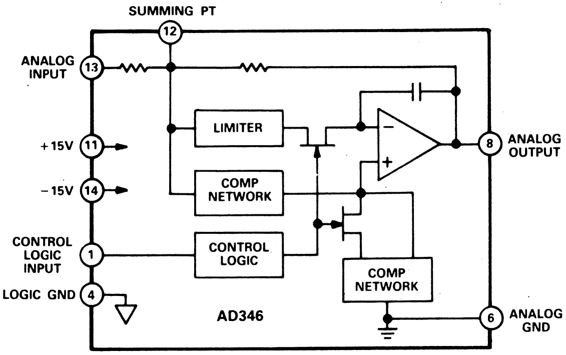
High Speed Sample and Hold Amplifier

AD346

FEATURES

Fast 2.0µs Acquisition Time to ±0.01%
Low Droop Rate: 0.5mV/ms
Low Offset
Low Glitch: <40mV
Aperture Jitter: 400ps
Military Temperature Range: −55°C to +125°C
Internal Hold Capacitor

AD346 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD346 is a high speed (2µs to 0.01%), adjustment free sample and hold amplifier designed for high throughput rate data acquisition applications. The fast acquisition time (2µs to 0.01%) and low aperture jitter (400ps) make it suitable for use with fast A/D converters to digitize signals up to 97kHz.

The AD346 is complete with an internal hold capacitor and it incorporates a compensation network which minimizes the sample to hold charge offset. The AD346 is also laser trimmed to eliminate the need for external trimming potentiometers.

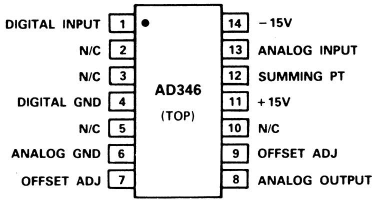
Typical applications for the AD346 include sampled data systems, D/A deglitchers, peak hold functions, strobed measurement systems and simultaneous sampling converter systems.

The device is available in two versions: the "J" specified for operation over the 0 to +70°C commercial temperature range and the "S" specified over the full military temperature range, −55°C to +125°C with processing to MIL-STD-883, Level B screening available.

PRODUCT HIGHLIGHTS

1. The AD346 is an improved second source for other sample and holds of the same pin configuration.
2. The AD346 provides separate analog and digital grounds, thus improving the device's immunity to ground and switching transients.
3. The droop rate is only 0.5mV/ms so that it may be used in slower high accuracy systems without the loss of accuracy.
4. The fast acquisition time and low aperture make it suitable for very high speed data acquisition systems.

PIN CONFIGURATIONS



PIN OUT

SPECIFICATIONS (typical @ +25°C, V_S = ±15V unless otherwise noted)

Model	AD346JD	AD346SD	Units
ANALOG INPUT			
Voltage Range	±10.0	*	Volts
Input Impedance	3.0	*	kΩ
DIGITAL INPUT			
"0" Input Threshold Voltage (Hold)	+0.8 max	*	Volts
"1" Input Threshold Voltage (Sample)	2.0 min	*	Volts
"0" Input Current	50.0	*	μA
"1" Input Current	1.0	*	μA
TRANSFER CHARACTERISTICS			
Gain	−1.0	*	
Gain Error	±0.02 max (±0.01 typ)	*	% FSR
Gain Error, $T_{min} - T_{max}$	±0.05 max (±0.03 typ)	*	% FSR
Offset Voltage	±3 max (±1 typ)	*	mV
Offset Voltage, $T_{min} - T_{max}$	±20 max (±6 typ)	*	mV
Pedestal	±4 max (±2 typ)	*	mV
Pedestal, $T_{min} - T_{max}$	±20 max (±8 typ)	±20 max (±10 typ)	mV
Droop Rate	0.5 max (0.1 typ)	*	mV/μs
Droop Rate, $T_{min} - T_{max}$	60 max (20 typ)	700 max (200 typ)	mV/μs
DYNAMIC CHARACTERISTICS			
Full Power Bandwidth			
V_{OUT} = +10V, −3dB	1.4	*	MHz
Output Slew Rate	50	*	V/μs
Acquisition Time			
To ±0.01% 10V Step	2.0 max (1.0 typ)	*	μs
To ±0.01% 20V Step	2.5 max (1.6 typ)	*	μs
Aperture Delay	60 max (30 typ)	*	ns
Settling Time			
Sample Mode (10V Step)	2.0 max (1.0 typ)	*	μs
Sample to Hold	500 max (150 typ)	*	ns
Feedthrough (Hold Mode)			
at 1kHz	0.02 max (0.005 typ)	*	% FSR
Transient Peak Amplitude			
Sample/Hold/Sample	40	*	mV
ANALOG OUTPUT			
Output Voltage Swing[1]	±10.0 min	*	Volts
Output Current	3.0	*	mA
POWER REQUIREMENTS			
Operating Voltage Range	±12 to ±18	*	Volts
Supply Current			
+V	18 max (9 typ)	*	mA
−V	−10 max (−3 typ)	*	mA
Power Supply Rejection Ratio	100	*	μV/V
Power Consumption	500 max (200 typ)	*	mW
PACKAGE OPTION[2]			
14 Pin DIP	HY14C	*	

[1] Maximum output swing is 4V less than $+V_S$.
[2] See Section 20 for package outline information.
*Specifications same as AD346JD.
Specifications subject to change without notice.

ANALOG DEVICES

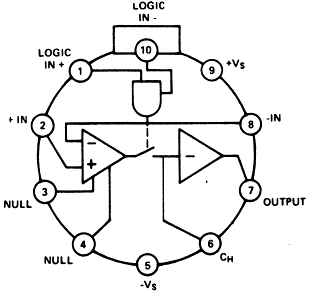
Low Cost Sample/Hold Amplifier

AD582

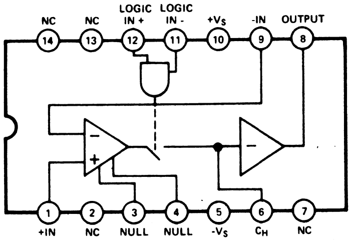
FEATURES

- Low Cost
- Suitable for 12-Bit Applications
- High Sample/Hold Current Ratio: 10^7
- Low Acquisition Time: 6μs to 0.1%
- Low Charge Transfer: <2pC
- High Input Impedance in Sample and Hold Modes
- Connect in Any Op Amp Configuration
- Differential Logic Inputs

AD582 PIN CONFIGURATION AND FUNCTIONAL BLOCK DIAGRAM



10-PIN TO-100 TOP VIEW



14-PIN TO-116 TOP VIEW

PRODUCT DESCRIPTION

The AD582 is a low cost integrated circuit sample and hold amplifier consisting of a high performance operational amplifier, a low leakage analog switch and a JFET integrating amplifier – all fabricated on a single monolithic chip. An external holding capacitor, connected to the device, completes the sample and hold function.

With the analog switch closed, the AD582 functions like a standard op amp; any feedback network may be connected around the device to control gain and frequency response. With the switch open, the capacitor holds the output at its last level, regardless of input voltage.

Typical applications for the AD582 include sampled data systems, D/A deglitchers, analog de-multiplexers, auto null systems, strobed measurement systems and A/D speed enhancement.

The device is available in two versions: the "K" specified for operation over the 0 to +70°C commercial temperature range and the "S" specified over the full military temperature range, -55°C to +125°C with processing to MIL-STD-883, Class B available. All versions may be obtained in either the hermetically sealed, TO-100 can or the TO-116 DIP.

PRODUCT HIGHLIGHTS

1. The monolithic AD582 is the lowest cost sample and hold amplifier available. Until recently, quality sample and hold circuits could only be fabricated with costly discrete or hybrid components.
2. The specially designed input stage presents a high impedance to the signal source in both sample and hold modes (up to ±12V). Even with signal levels up to $\pm V_S$, no undesirable signal inversion, peaking or loss of hold voltage occurs.
3. The AD582 may be connected in any standard op amp configuration to control gain or frequency response and provide signal inversion, etc.
4. The AD582 offers a high, sample-to-hold current ratio: 10^7 The ratio of the available charging current to the holding leakage current is often used as a figure of merit for a sample and hold circuit.
5. The AD582 has a typical charge transfer less than 2pC. A low charge transfer produces less offset error and permits the use of smaller hold capacitors for faster signal acquisition.
6. The AD582 provides separate analog and digital grounds, thus improving the device's immunity to ground and switching transients.

SPECIFICATIONS (typical @ +25°C, V_S = ±15V and C_H = 1000pF, A = +1 unless otherwise specified)

MODEL	AD582K	AD582S (AD582S/883B)
SAMPLE/HOLD CHARACTERISTICS		
Acquisition Time, 10V Step to 0.1%, C_H = 100pF	6μs	•
Acquisition Time, 10V Step to 0.01%, C_H = 1000pF	25μs	•
Aperture Time, 20V p-p Input, Hold 0V	150ns	•
Aperture Jitter, 20V p-p Input, Hold 0V	15ns	•
Settling Time, 20V p-p Input, Hold 0V, to 0.01%	0.5μs	•
Droop Current, Steady State, ±10V_{OUT}	100pA max	•
Droop Current, T_{min} to T_{max}	1nA	150nA max
Charge Transfer	5pC max (1.5pC typ)	•
Sample to Hold Offset	0.5mV	•
Feedthrough Capacitance 20V p-p, 10kHz Input	0.05pF	•
TRANSFER CHARACTERISTICS		
Open Loop Gain V_{OUT} = 20V p-p, R_L = 2k	25k min (50k typ)	•
Common Mode Rejection V_{CM} = 20V p-p, F = 50Hz	60dB min (70dB typ)	•
Small Signal Gain Bandwidth V_{OUT} = 100mV p-p, C_H = 200pF	1.5MHz	•
Full Power Bandwidth V_{OUT} = 20V p-p, C_H = 200pF	70kHz	•
Slew Rate V_{OUT} = 20V p-p, C_H = 200pF	3V/μs	•
Output Resistance Hold Mode, I_{OUT} = ±5mA	12Ω	•
Linearity V_{OUT} = 20V p-p, R_L = 2k	±0.01%	•
Output Short Circuit Current	±25mA	•
ANALOG INPUT CHARACTERISTICS		
Offset Voltage	6mV max (2mV typ)	•
Offset Voltage, T_{min} to T_{max}	4mV	8mV max (5mV typ)
Bias Current	3μA max (1.5μA typ)	•
Offset Current	300nA max (75nA typ)	•
Offset Current, T_{min} to T_{max}	100nA	400nA max (100nA typ)
Input Capacitance, f = 1MHz	2pF	•
Input Resistance, Sample or Hold 20V p-p Input, A = +1	30MΩ	•
Absolute Max Diff Input Voltage	30V	•
Absolute Max Input Voltage, Either Input	$\pm V_S$	•
DIGITAL INPUT CHARACTERISTICS		
+Logic Input Voltage		
Hold Mode, T_{min} to T_{max}, -Logic @ 0V	+2V min	•
Sample Mode, T_{min} to T_{max}, -Logic @ 0V	+0.8V max	•
+Logic Input Current		
Hold Mode, +Logic @ +5V, -Logic @ 0V	1.5μA	•
Sample Mode, +Logic @ 0V, -Logic @ 0V	1nA	•
-Logic Input Current		
Hold Mode, +Logic @ +5V, -Logic @ 0V	24μA	•
Sample Mode, +Logic @ 0V, -Logic @ 0V	4μA	•
Absolute Max Diff Input Voltage, +L to -L	+15V/-6V	•
Absolute Max Input Voltage, Either Input	$\pm V_S$	•
POWER SUPPLY CHARACTERISTICS		
Operating Voltage Range	±9V to ±18V	±9V to ±22V
Supply Current, $R_L = \infty$	4.5mA max (3mA typ)	•
Power Supply Rejection, ΔV_S = 5V, Sample Mode (see next page)	60dB min (75dB typ)	•
TEMPERATURE RANGE		
Specified Performance	0 to +70°C	-55°C to +125°C
Operating	-25°C to +85°C	-55°C to +125°C
Storage	-65°C to +150°C	•
Lead Temperature (Soldering, 15 sec)	+300°C	•
PACKAGE OPTION[1]		
"H" Package: TO-100	AD582KH	AD582SH
"D" Package: TO-116 Style (D14A)	AD582KD	AD582SD

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[1] See Section 20 for package outline information.

•Specifications same as AD582K.

Specifications subject to change without notice.

APPLYING THE AD582

Both the inverting and non-inverting inputs are brought out to allow op amp type versatility in connecting and using the AD582. Figure 1 shows the basic non-inverting unity gain connection requiring only an external hold capacitor and the usual power supply bypass capacitors. An offset null pot can be added for more critical applications.

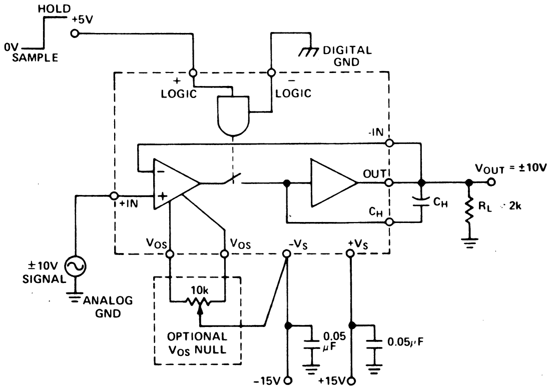


Figure 1. Sample and Hold with A = +1

Figure 2 shows a non-inverting configuration where voltage gain, A_V, is set by a pair of external resistors. Frequency shaping or non-linear networks can also be used for special applications.

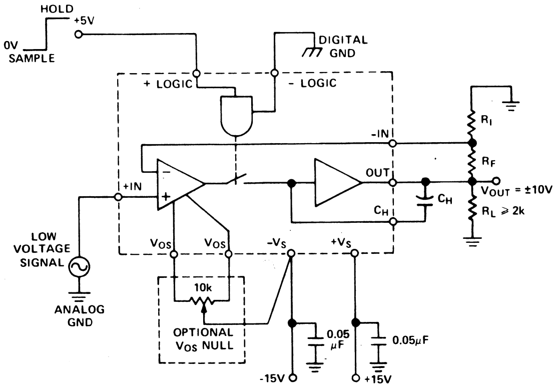


Figure 2. Sample and Hold with A = (1 + R_F/R_I)

The hold capacitor, C_H, should be a high quality polystyrene (for temperatures below +85°C) or Teflon type with low dielectric absorption. For high speed, limited accuracy applications, capacitors as small as 100pF may be used. Larger values are required for accuracies of 12 bits and above in order to minimize feedthrough, sample to hold offset and droop errors (see Figure 6). Care should be taken in the circuit layout to minimize coupling between the hold capacitor and the digital or signal inputs.

In the hold mode, the output voltage will follow any change in the $-V_S$ supply. Consequently, this supply should be well regulated and filtered.

Biasing the +Logic Input anywhere between -6V to +0.8V with respect to the -Logic will set the sample mode. The hold mode will result from any bias between +2.0V and ($+V_S$ - 3V). The sample and hold modes will be controlled differentially with the absolute voltage at either logic input ranging from $-V_S$ to within 3V of $+V_S$ (V_S - 3V). Figure 3 illustrates some examples of the flexibility of this feature.

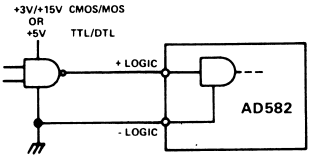


Figure 3A. Standard Logic Connection

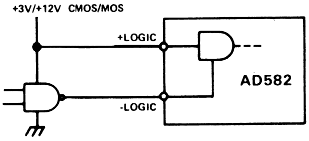


Figure 3B. Inverted Logic Sense Connection

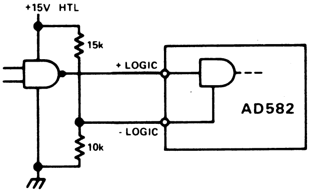


Figure 3C. High Threshold Logic Connection

DEFINITION OF TERMS

Figure 4 illustrates various dynamic characteristics of the AD582.

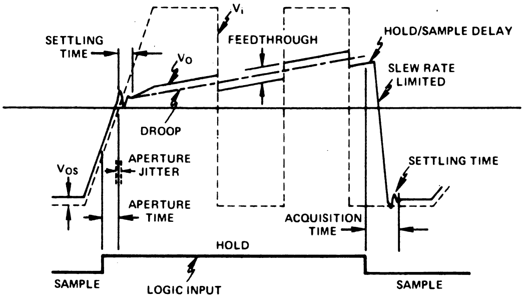


Figure 4. Pictorial Showing Various S/H Characteristics

Aperture Time is the time required after the "hold" command until the switch is fully open and produces a delay in the effective sample timing. Figure 5 is a plot giving the maximum frequency at which the AD582 can sample an input with a given accuracy (lower curve).

Aperture Jitter is the uncertainty in Aperture Time. If the Aperture Time is "tuned out" by advancing the sample-to-hold command 150ns with respect to the input signal, the Aperture Jitter now determines the maximum sampling frequency (upper curve of Figure 5).

Acquisition Time is the time required by the device to reach its final value within a given error band after the sample command has been given. This includes switch delay time, slewing time and settling time for a given output voltage change.

Droop is the change in the output voltage from the "held" value as a result of device leakage. In the AD582, droop can be in either the positive or negative direction. Droop rate may be calculated from droop current using the following formula:

$$\frac{\Delta V}{\Delta T}\ (\text{Volts/sec}) = \frac{I(\text{pA})}{C_H(\text{pF})}$$

(See also Figure 6.)

Feedthrough is that component of the output which follows the input signal *after* the switch is open. As a percentage of the input, feedthrough is determined as the ratio of the feedthrough capacitance to the hold capacitance (C_F/C_H).

Charge Transfer is the charge transferred to the holding capacitor from the interelectrode capacitance of the switch when the unit is switched to the hold mode. The charge transfer generates a sample-to-hold offset where:

$$\text{S/H Offset (V)} = \frac{\text{Charge (pC)}}{C_H(\text{pF})}$$

(See also Figure 6.)

Sample to Hold Offset is that component of D.C. offset independent of C_H (see Figure 6). This offset may be nulled using a null pot, however, the offset will then appear during the sampling mode.

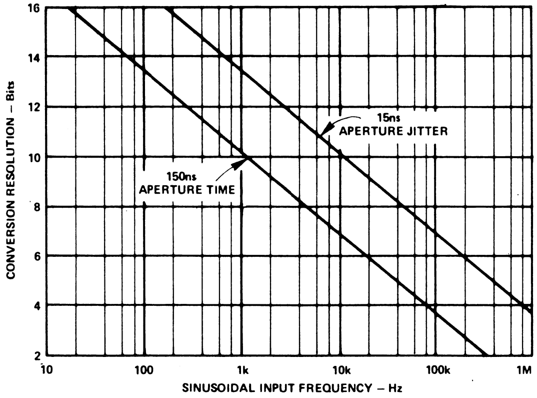


Figure 5. Maximum Frequency of Input Signal for ½LSB Sampling Accuracy

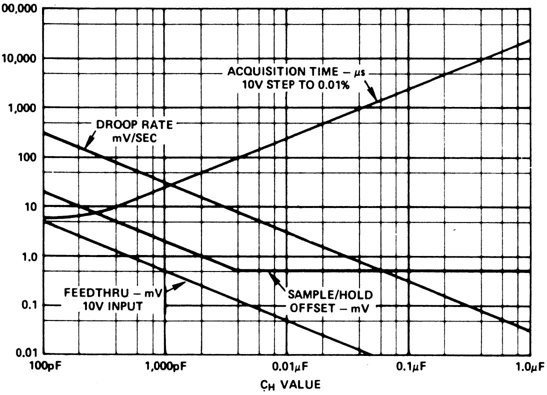


Figure 6. Sample and Hold Performance as a Function of Hold Capacitance

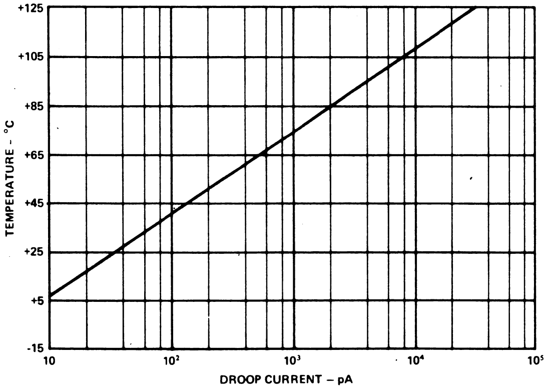


Figure 7. Droop Current vs. Temperature

ANALOG DEVICES

IC Sample and Hold Gated Op Amp

AD583

FEATURES

High Sample-to-Hold Current Ratio: 10^6
High Slew Rate: 5V/µs
High Bandwidth: 2MHz
Low Aperture Time: 50ns
Low Charge Transfer: 10pC
DTL/TTL Compatible
May Be Used as Gated Op Amp

PRODUCT DESCRIPTION

The AD583 is a monolithic sample and hold circuit consisting of a high performance operational amplifier in series with an ultra-low leakage analog switch and unity gain amplifier. An external holding capacitor, connected to the switch output, completes the sample-and-hold or track-and-hold function.

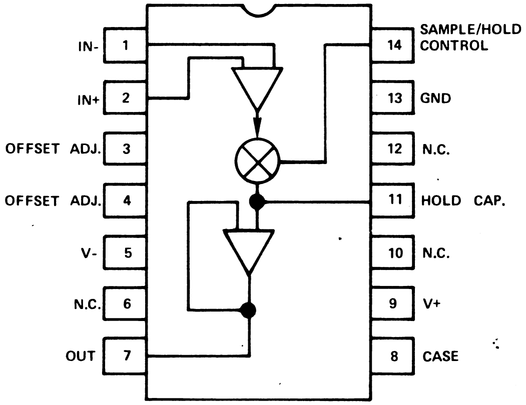
With the analog switch closed, the AD583 functions like a standard op amp; any feedback network may be connected around the device to control gain and frequency response. With the switch open the capacitor holds the output at its previous level.

The AD583 may also be used as a versatile operational amplifier with a gated output for applications such as analog switches, peak holding circuits, etc.

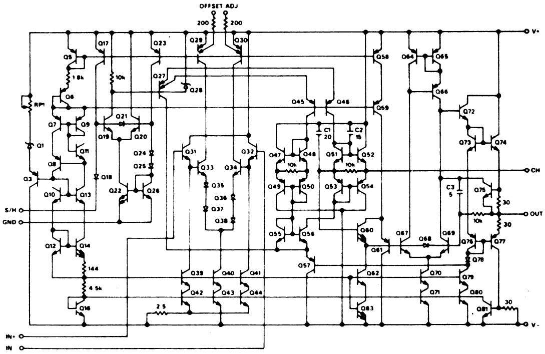
PRODUCT HIGHLIGHTS

1. Sample-and-hold operation is obtained with the addition of one external capacitor.
2. Low charge transfer (10pC) and high sample-to-hold current ratio insure accurate tracking.
3. Any gain or frequency response is available using standard op amp feedback networks.
4. High slew rate and low aperture time permit sampling of rapidly changing signals.
5. Output, gated through a low leakage analog switch, also makes the AD583 useful for applications such as analog switches, peak holding circuits, etc.

AD583 FUNCTIONAL BLOCK DIAGRAM



TO-116



Schematic Diagram

SPECIFICATIONS (typical @ +25°C and ±15V dc unless otherwise specified)

MODEL	AD583KD
OPEN LOOP GAIN R_L = 2kΩ, T_{min} to T_{max}	25k min (50k typ)
OUTPUT VOLTAGE SWING R_L = 2kΩ, T_{min} to T_{max}	±10V min
OUTPUT CURRENT	±10mA min
OUTPUT RESISTANCE	5Ω
OFFSET VOLTAGE	6mV max (3mV typ)
T_{min} to T_{max}	8mV max (4mV typ)
BIAS CURRENT	200nA max (50nA typ)
T_{min} to T_{max}	400nA max
OFFSET CURRENT	50nA max (10nA typ)
T_{min} to T_{max}	100nA max
INPUT RESISTANCE	5MΩ min (10MΩ typ)
COMMON MODE RANGE	±10V min
COMMON MODE REJECTION T_{min} to T_{max}	74dB min (90dB typ)
GAIN BANDWIDTH PRODUCT	2MHz
SLEW RATE Av = +1, R_L = 2kΩ, C_L = 50pF, V_{out} = ±10V p-p	5V/μs
RISE TIME Av = +1, R_L = 2kΩ, C_L = 50pF, V_{out} = 400mV p-p	100ns
OVERSHOOT Av = +1, R_L = 2kΩ, C_L = 50pF, V_{out} = 400mV p-p	20%
DIGITAL INPUT CURRENT	
V_{in} = 0, T_{min} to T_{max}	0.8mA max (Logic "Sample")
V_{in} = +5.0V, T_{min} to T_{max}	20μA max (Logic "Hold")
DIGITAL INPUT VOLTAGE	
Low T_{min} to T_{max}	0.8V max
High T_{min} to T_{max}	2.0V min
ACQUISITION TIME Av = +1, R_L = 2kΩ, C_L = 50pF	
to 0.1% of final value:	4μs
to 0.01% of final value:	5μs
APERTURE TIME	50ns
APERTURE JITTER	5ns
DRIFT CURRENT	50pA max (5pA typ)
T_{min} to T_{max}	1.0nA max (0.05nA typ)
CHARGE TRANSFER	20pC max (10pC typ)
SUPPLY CURRENT	5.0mA max (2.5mA typ)
POWER SUPPLY REJECTION	74dB min (90dB typ)
OPERATING TEMP	0 to +70°C
STORAGE TEMP	-65°C to +150°C
PACKAGE STYLE[1]: TO-116 Style	(D14A)

Specifications subject to change without notice.

[1] See Section 20 for package outline information.

ABSOLUTE MAXIMUM RATINGS

Voltage between V+ and V- Terminals	40V
Differential Input Voltage	±30V
Digital Voltage (Pin 14)	+8V, -15V
Output Current	Short Circuit Protected
Internal Power Dissipation	30mW (Derate power dissipation by 4.3mW/°C above +150°C ambient temperature)

APPLYING THE AD583

Figure 1 shows the AD583 connected in a simple sample and hold configuration with unity gain and offset nulling. Any other standard op amp gain and frequency response configuration may also be used. Note that the holding capacitor, C_H, should have extremely high insulation resistance and low dielectric absorption. Polystyrene (below +85°C), teflon or Mica types are recommended.

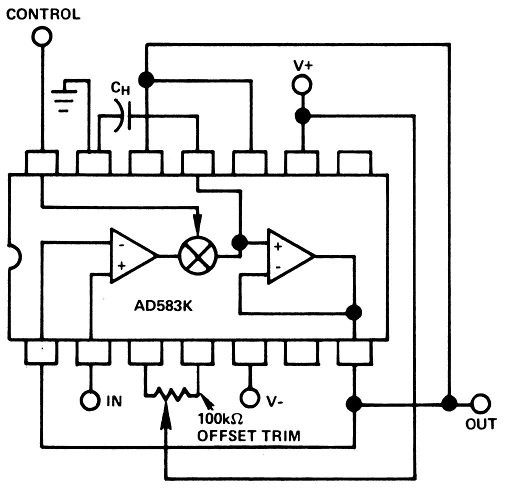


Figure 1. Basic Track-and-Hold/Sample-and-Hold

Figure 2 shows the guard ring used to reduce leakage paths between the pc board and the package. This minimizes drift during the hold command.

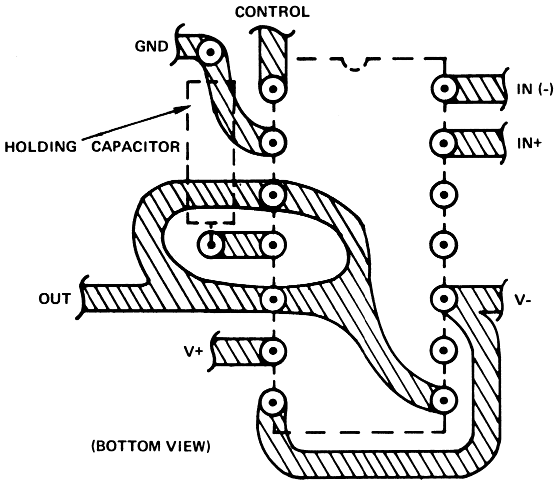


Figure 2. Guard Ring Layout

Also note that the input amplifier of the AD583 may be used as a gated amplifier by utilizing Pin 11 as the output. This amplifier has excellent drive capabilities along with exceptionally low switch leakage.

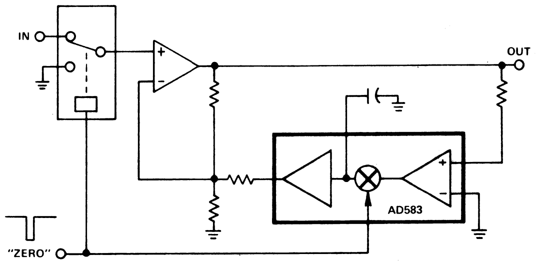


Figure 3. Automatic Offset Zeroing

The circuit of Figure 3 illustrates how the AD583 may be used to automatically zero a high gain amplifier. Basically, the input is periodically grounded and the output offset is then sampled and fed back to cancel the error. This technique is useful in A/D conversion, instrumentation, DVM's to eliminate offset drift errors by periodically rezeroing the system.

Care should be taken to assure that the zeroing loop is dynamically stable. A second sample-and-hold could be added in series with the output to remove the output discontinuity.

DEFINITION OF TERMS

Acquisition Time:

Acquisition Time is the time required by the device to reach its final value within ±0.1% after the sample command has been given. This includes switch delay time, slewing time, and settling time and is the minimum sample time required to obtain a given accuracy.

Charge Transfer:

Charge Transfer is the small charge transferred to the holding capacitor from the interelectrode capacitance of the switch when the unit is switched to the sample mode. Sample-to-hold offset error is directly proportional to this charge, where:

$$\text{Offset Error (V)} = \frac{\text{Charge (pC)}}{C_H\text{(pF)}}$$

Aperture Time:

The time required after the "hold" command until the switch is fully open. This delays the effective sample timing with rapidly changing input signals.

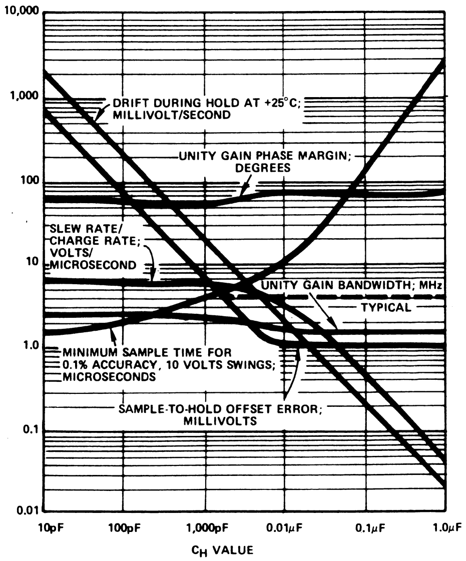
Drift Current:

Leakage currents from the holding capacitor during the hold mode cause the output voltage to drift. Drift rate (or droop rate) is calculated from drift current values using the formula:

$$\frac{\Delta V}{\Delta T}\ \text{(Volts/sec)} = \frac{I\text{(pA)}}{C_H\text{(pF)}}$$

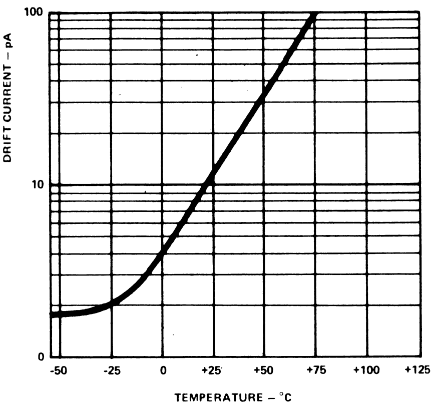
Performance Curves

V_{SUPPLY} = ±15V dc, T_A = +25°C, C_H = 1,000pF unless otherwise specified

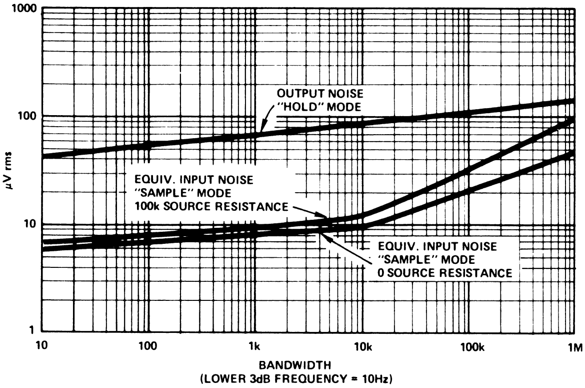


Typical Sample-and-Hold Performance as a Function of Holding Capacitance

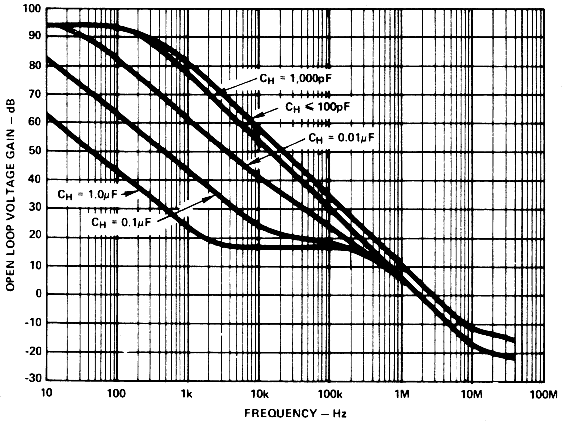
DRIFT CURRENT VS. TEMPERATURE



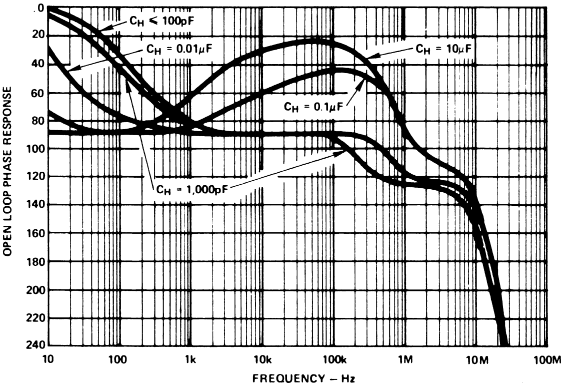
Drift Current vs. Temperature



Broadband Noise Characteristics



Open Loop Frequency Response



Open Loop Phase Response

ANALOG DEVICES

Fast 0.01% Track/Sample-Hold Amplifiers

ADSHC–85

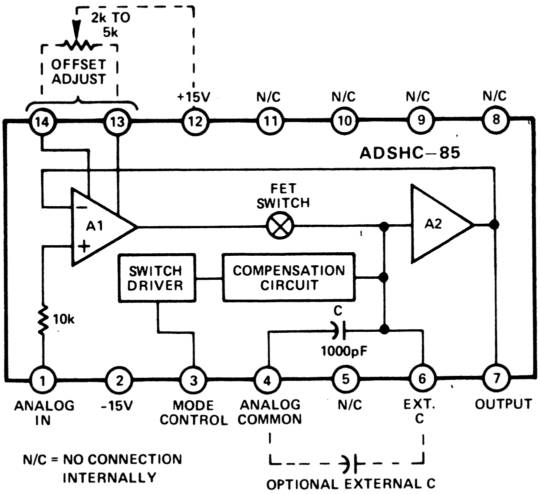
FEATURES

Improved SHC-85 Replacement
500ns Sample-to-Hold Transient
50μV rms Noise
Low Droop Rate of 0.2mV/ms

APPLICATIONS

Data Acquisition Systems
Data Distribution Systems
Analog Delay and Storage
Peak Amplitude Measurements

ADSHC-85 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADSHC-85 Sample/Hold amplifier combines fast acquisition time and linear performance with low cost to provide an economical solution for a variety of applications.

The unit is an improved second source for the SHC-85, featuring faster sample-to-hold settling, and lower noise. It is pin-for-pin compatible with other 14-pin DIP packages of this type; designed to acquire and hold analog signals as large as ± 10V dc.

Accuracies of ±0.01% can be achieved in 4.5μs for 10-volt input steps, and in only 5μs for 20-volt steps.

Both commercial temperature ranges and extended temperature ranges are available, respectively, in the ADSHC-85 and the ADSHC-85ET. In addition, the ADSHC-85ET can be processed per the requirements of MIL-STD-883, Method 5008.

TRACK-AND-HOLD (T/H) MODE

When operated in the T/H mode, the ADSHC-85 "tracks" all changes in analog input as they occur, functioning like a unity gain amplifier. The "hold" mode is initiated by the user and causes the output of the T/H unit to be "frozen".

A logic "1" at Pin 3 causes the unit to be in a "track" (or sample) mode; a logic "0" puts the output in "hold".

SPECIFICATIONS (typical @ +25°C, 1,000pF internal capacitance, and nominal supply voltages unless otherwise noted)

MODEL	UNITS	ADSHC-85	ADSHC-85ET
ANALOG INPUT			
Voltage Range	V	±10	*
Overvoltage, no damage	V max	±15	*
Impedance	Ohms	10^{11}	*
Capacitance	pF	10	*
Bias Current	nA, max	0.5	*
Initial Offset Voltage	mV, max	±2, adjustable to zero	*
DIGITAL INPUT (TTL Compatible)			
Mode Control	Voltage	Current	
"Sample/Track" Logic "1"	+2.0V to +5.5V	50nA max	
"Hold" Logic "0"	0V to +0.8V	−50μA max	
ANALOG OUTPUT			
Voltage	V	±10	*
Current	mA	±10	*
Impedance	Ohms max	1	*
Capacitive Load	pF	1,000	*
Noise			
@ 100kHz	μV rms	50	*
@ 1.0MHz	μV rms	150	*
DC ACCURACY/STABILITY			
Gain	V/V	+1	*
Gain Error	%	±0.01	*
Gain Nonlinearity	%	±0.01	*
Gain Temperature Coefficient	ppm/°C	±2	*
Input Offset vs. Temperature	μV/°C	±25	*
SAMPLE (TRACK) MODE DYNAMICS			
Frequency Response			
Small Signal (−3dB)	MHz	3	*
Full Power (−3dB)	kHz	200	*
Slew Rate	V/μs	15	*
SAMPLE (TRACK)-TO-HOLD SWITCHING			
Aperture Time	ns	25	*
Aperture Uncertainty (Jitter)	ns	0.5	*
Offset Step (Pedestal)	mV	1.0	*
Switching Transient			
Amplitude	mV	325	*
Settling to 1mV	μs, max	0.5	*
HOLD MODE DYNAMICS			
Droop Rate			
Typical (Maximum)	mV/ms	0.2 (0.5)	*
Variation with Temperature		Doubles/10°C Change	*
Feedthrough Rejection			
(20V p-p @ 1kHz)	dB	80	*
HOLD-TO-SAMPLE (TRACK) DYNAMICS			
Acquisition Time (to ±0.01%)			
10V Step	μs, max	4.5	*
20V Step	μs, max	5.0	*
POWER REQUIREMENTS[1]			
Nominal Voltages	V (%)	±15 (±3)	*
Current	mA, typ (max)	±18 (±20)	*
Power Supply Rejection			
(dc − 50kHz)	μV/V	100	*
TEMPERATURE RANGE			
Operating (Case)	°C	0 to +70	−55 to +125
Storage	°C	−55 to +125	*
MTBF[2]			
Mean Time Between Failures	hours	466,797	*
PACKAGE OPTION[3]	HY14D		

*Specifications same as Model ADSHC-85.

[1] Recommended power supply ADI Model 902-2 ±15V @ ±100mA

[2] Calculated using MIL-HNBK-217; Ground; Fixed; +70°C case

[3] See Section 20 for package outline information.

Specifications subject to change without notice.

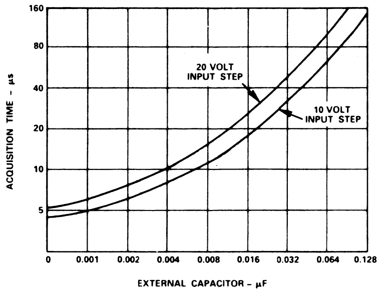


Figure 1.

As shown in Figure 2, two different intervals of time can affect the point on the analog input which is sampled when the T/H is switched from "track" to "hold". One of these, aperture time, is a constant and, therefore, should not be regarded as an error source. The other, aperture uncertainty (or "jitter"), may vary from one "hold" command to the next and qualifies as a valid error source.

This "jitter" is the result of noise signals of various kinds which modulate the phase of the hold command and are manifested as sample-to-sample variations in the value of the analog input which is being "frozen". The aperture error which results from this jitter is directly related to the dV/dt of the analog input.

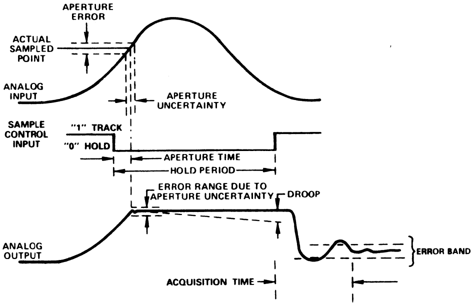


Figure 2. Track-and-Hold Operation

Another phenomenon associated with the hold period which can contribute to error is feedthrough. High feedthrough rejection is important in a track-and-hold to prevent leakage from input to output during the hold interval.

Acquisition time is the interval required for the T/H to reestablish accurate tracking of the analog input signal after the "hold" period has ended.

Longer intervals will be required for greater accuracy; but the interval is also affected by the rate of change of the input. Nyquist sampling is the most stringent tracking requirement.

SAMPLE-AND-HOLD (S/H)MODE

In the S/H mode, the output of the ADSHC-85 is left in the "hold" mode most of the time, but is switched to the "sample" (track) mode for brief intervals.

The width of the sample pulse at the MODE CONTROL input is dictated by (1) the acquisition time of the ADSHC-85, in combination with (2) the desired accuracy of the sampled output.

A third factor which affects the accuracy is the amount of change which has occurred since the preceding sample; this is analogous to the situation which happens between successive "hold" commands when operating as a T/H.

OPTIONAL EXTERNAL CAPACITOR

The droop, charge offset, and acquisition time of the ADSHC-85 are determined by the holding capacitor.

(Charge offset is caused by the transfer of charge to the holding capacitor via the gate capacitance of the switching FET when switching into "hold". The charge is essentially restored by a compensation circuit inside the ADSHC-85 when the unit goes into the "hold" mode.)

The droop rate can be reduced with the use of an external capacitor, but this technique is not an unmixed blessing, since additional capacitance which improves droop rate characteristics also adds to settling time.

Figure 1 approximates the relationship of acquisition time and added external capacitance. The droop rate is determined by:

$$\text{Droop} = \frac{dV}{dt} = \frac{0.5 \times 10^{-9}}{1{,}000\text{pF} + C_{ext}}$$

OFFSET ADJUSTMENT

Offset in the Functional Diagram should be adjusted with the analog input grounded, and with the sample/hold switching continuously between the "sample" and "hold" modes.

Output offset error is adjusted to zero when the unit is in the "hold" mode. This will compensate for both charge offset (see above) and amplifier offset.

APPLICATIONS

The most common application for a track-and-hold is to place it ahead of a converter to allow digitizing of signals with bandwidths higher than the converter alone can handle.

For these kinds of applications, the ADSHC-85 series can reduce system aperture to 500 picoseconds or less.

Their ability to be operated as either track-and-hold or sample-and-hold devices adds to their flexibility, and makes them appropriate for multiple uses.

OPERATION WITH A/D CONVERTER

Figure 3 shows in simplified form the use of an ADSHC-85 as a track-and-hold in combination with a converter.

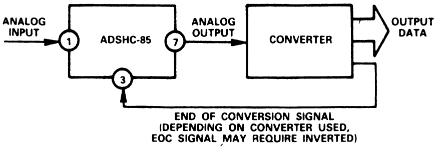

ANALOG INPUT
1
ADSHC-85
7
ANALOG OUTPUT
CONVERTER
OUTPUT DATA
3
END OF CONVERSION SIGNAL (DEPENDING ON CONVERTER USED, EOC SIGNAL MAY REQUIRE INVERTED)

Figure 3.

The maximum value of input signal frequency that can be acquired and digitized using this combination is influenced by the bandwidth of the T/H, but is also dictated by:

A. The aperture uncertainty (jitter) of the ADSHC-85
and

B. The desired accuracy, and corresponding resolution of the converter (the larger the number of bits, the lower the maximum instantaneous input frequency).

If the desired accuracy of digitizing were 0.1% to a tolerance of ± 1/2LSB, the maximum value of input signal frequency which can be digitized is determined by:

$$F\max = \frac{2^{-N}}{2\pi T_a} = \frac{1}{2\pi \cdot 1{,}024 \cdot 5 \times 10^{-10}} = 310.8\text{kHz}$$

where 0.1% is 10 bits; and aperture uncertainty of the ADSHC-85 is 0.5ns.

For this situation, the converter in Figure 3 could be either the Analog Devices Model HAS-1002, or the Analog Devices Model AD579.

Either of these units and the ADSHC-85 could acquire and digitize an analog input frequency of slightly less than 311kHz.

The maximum throughput rate of each of these combinations would be different, however.

When using an ADSHC-85 with HAS-1002, throughput would be 169k samples per second (a period of 4.5μs plus 1.4μs). Using the AD579 results in 154k (4.5μs plus 2.0μs). NOTE: These update rates are based on using the ADSHC-85 without external capacitance; none is required because droop is insignificant during the conversion time.

Without violating the Nyquist sampling theorem, the HAS-1002 could be used for input frequencies from dc through 84kHz; the AD579 for inputs from dc through 77kHz. Input frequencies higher than these (up to the maximum of 311kHz) would result in "undersampling" of the input signal. Signals up to 311kHz could be processed if their bandwidth is less than one-half the sample frequency (example: IF signals).

SIMULTANEOUS SAMPLE/HOLD

The ADSHC-85 can be used for time correlation of sampled data signals by using one sample/hold for each analog signal. The outputs of the units are then applied to the input of an analog multiplexer.

The worst-case droop error of the sample/hold in the last channel to be sampled is determined by the maximum "Hold" time of the system. This maximum hold time, in turn, is established by the A/D conversion rate, and the number of data channels.

Droop error is computed by:

MAX DROOP ERROR (for Channel N) = (T × n) (Droop Rate)

$$\text{where } T = \frac{1}{\text{A/D Conversion Rate}}$$

and n = number of multiplexer data channels

Figure 4 shows an 8-channel system using ADSHC-85 units for simultaneous sampling. Their outputs are applied to either a Model AD7501 or Model AD7503 CMOS analog multiplexer; the output of the MUX is then applied through an amplifier to a Model HAS-1202.

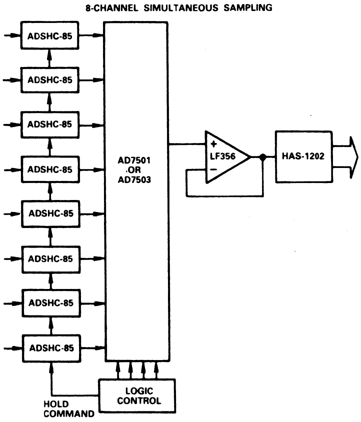


Figure 4.

When the input signal range is ± 10 volts, this 12-bit system will have a value for the Least Significant Bit (LSB) of slightly less than 5mV (4.88mV).

If the system is going to maintain 12-bit integrity, the droop rate must be appreciably less than 1/2LSB. In this example, if one assumes a system sample rate of 20kHz, the computed droop error of the last channel meets that requirement:

$$\text{Droop} = \left(\frac{1}{\text{System Sample Rate}}\right)(\text{max T/H droop})$$

$$\text{Droop} = \left(\frac{1}{20 \times 10^3}\right)(0.5\text{mV/ms}) = 25\mu\text{V}$$

The computed droop error is negligible; therefore, no external capacitance need be added to the ADSHC-85s. This should hold true for all except the very slowest A/Ds which might be substituted for the HAS-1202.

RECOMMENDED CONVERTERS

The application notes above offer suggestions on converters from the Analog Devices product line which are candidates for use with the ADSHC-85 Sample/Hold units.

Depending on the application and desired resolution, a number of units should be considered.

They include:

ADC84
ADC85
AD578
AD579
HAS-0802
HAS-1002
HAS-1202
MAH-0801
MAH-1001
MAS-0801
MAS-1001
MAS-1202

ANALOG DEVICES

Ultra Fast 0.01% Track/Sample-Hold Amplifiers

ADSHM-5/ADSHM-5K

FEATURES

ADSHM-5
- 2nd Source—Replaces all SHM-5 Series
- Fast 350ns Acquisition Time to ±0.01%
- Aperture Uncertainty 250ps

ADSHM-5K
- Ultra Fast 250ns Acquisition Time to ±0.01%
- 100ns Acquisition Time to ±0.1%
- Wide 12MHz Bandwidth
- 300V/µs Slew Rate
- Super Low 2nA Input Bias Current

APPLICATIONS
- Fast Data Acquisition
- Data Distribution Systems
- Peak Measurement
- Simultaneous Sample & Hold
- Analog Delay & Storage

GENERAL DESCRIPTION

The ADSHM-5 is a new ultra-fast (350ns to 0.01%) sample-hold amplifier designed for use with high-speed 10- and 12-bit analog-to-digital converters, such as Analog Devices' MAH, MAS, and HAS Series, as well as other manufacturers' types.

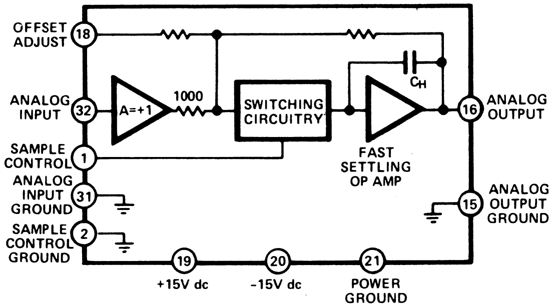
Designed specifically to second source other SHM-5's, the ADSHM-5 is a fit, form and function equivalent for these modules.

When used in a 12-bit data acquisition system, the ADSHM-5 acquires to within 12 bits (±0.01%) in 350ns for a 10V step change. For systems requiring 10-bit performance, the ADSHM-5 acquires to within ±0.1% in just 200ns max.

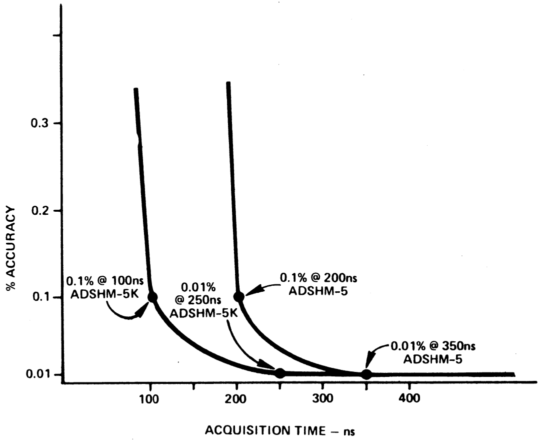
Other salient features of the ADSHM-5 include 0.005% max Tracking Nonlinearity and a Small Signal Bandwidth of 5MHz.

To upgrade system performance one need only to look at the new ADSHM-5K. While sharing the same pinout and package of the ADSHM-5, this all new module utilizes the latest "state-of-the-art" hybrid techniques to offer the user the optimum in specifications. The ADSHM-5K features a maximum 12-bit acquisition time of only 250ns and 10-bit acquisition time of an astonishing 100ns max. Another improvement is in acquisition time where the input buffer must also respond to a 10V step change, such as in multiplexed applications. The total acquisition time in this application is only 350ns max. Further, the Small Signal Bandwidth has been improved from 5MHz to 12MHz.

ADSHM-5, ADSHM-5K FUNCTIONAL BLOCK DIAGRAM



Both units are packaged in a 2" X 2" X 0.4" case. The operating temperature range is 0 to +70°C, and the power requirements are ±15V dc @ 75mA max.



Acquisition Time vs. Settling Accuracy

This two-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be found in Volume II, page 14-7.

SPECIFICATIONS (typical @ +25°C and ±15V dc power supplies unless otherwise noted)

MODEL	UNITS	ADSHM-5	ADSHM-5K
ANALOG INPUT			
Input Voltage Range	V min	±10	*
Input Overvoltage, No Damage	V max	±15	*
Input Impedance	Ω	100M	1000
Input Bias Current	nA max	250	2
Offset Adjustment Range	mV	±300	*
SAMPLE CONTROL INPUT			
Sample Mode: Logic "1", TTL[1]	V	+2.0 to +5.5	*
Hold Mode: Logic "0", TTL	V	0 to +0.8	*
Loading	mA	+1	*
ANALOG OUTPUT			
Output Voltage Range	V min	±10	*
Output Current, S.C. Protected	mA	±40	±50
Output Impedance	Ω max	0.1	*
Noise (dc to 2.5MHz)	µV	100	*
ACCURACY/STABILITY DC			
Gain[2]	V/V	-1.000 ±0.1%	*
Gain vs. Temperature	ppm/°C	±10	*
Output Offset vs. Temperature	µV/°C max	±30	*
Output Offset vs. Supply	mV/V	1	*
Tracking Nonlinearity	% max	±0.005	*
Output Offset Voltage, Sample Mode	mV max	±50	*
DYNAMIC RESPONSE[3]			
Acquisition Time[4], 10V to 0.1%	ns max	200	100
Acquisition Time[4], 10V to 0.01%	ns max	350	250
Acquisition Time[5], 10V to 0.01%	ns typ	1,000	300
Bandwidth, Tracking, -3dB	MHz	5	12
Slew Rate, Tracking	V/µs	25	300
Aperture Delay Time[6]	ns	20	*
Aperture Uncertainty Time	ps	250	100
Hold Mode Droop	µV/µs max	20	12
Hold Mode Feedthrough, dc to 500kHz	dB	70	*
Sample to Hold Offset Error	mV max	±5	*
POWER REQUIREMENT			
Power Supply Voltage	V dc	±15 ±0.5	*
Quiescent Current	mA max	75	*
PHYSICAL–ENVIRONMENTAL			
Operating	°C	0 to +70	*
Storage	°C	-55 to +125	*
Relative Humidity	%	Up to 100%, noncondensing	*
Case Size	"	2.0 X 2.0 X 0.4	*
Case Material	N/A	Diallyl Phthalate per MIL-M-14 Type SDG-f	
Pins	N/A	0.020" round, gold plated; 0.25" long min	

NOTES

[1] TTL compatible. Schottky Pull Up (74S132 or equivalent) recommended to supply the 1mA required.

[2] The Gain Error of ±0.1% can be adjusted out most easily by using the Gain Adjust of the companion A/D converter.

[3] When switched into Hold, about 50ns is required for switching transients to settle. This time should be allowed before initiating the first conversion.

[4] From Tracking Mode.

[5] From Input Buffer.

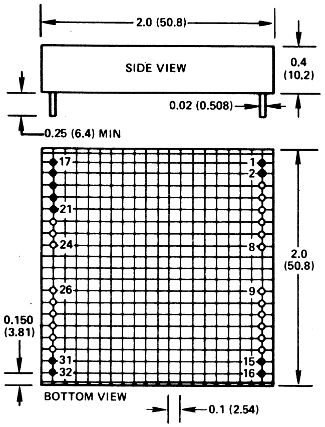
[6] The Analog Signal Delay from the input to the Sampling Switch is approximately 32ns. Aperture Delay time is 20ns.

*Specifications same as ADSHM-5.

Specifications and prices subject to change without notice.

MECHANICAL DIMENSIONS

Dimensions shown in inches and (mm).



NOTES: PINS ARE GOLD PLATED
DOT ON TOP INDICATES POSITION OF PIN 1

PIN DESIGNATIONS

PIN	FUNCTION
1	SAMPLE CONTROL
2	SAMPLE CONTROL GND
15	ANALOG OUTPUT GND
16	ANALOG OUTPUT
17	NC
18	OFFSET ADJUST
19	+15V POWER
20	-15V POWER
21	POWER GROUND
31	ANALOG INPUT GND
32	ANALOG INPUT

ANALOG DEVICES

Ultra High Speed Hybrid Track-and-Hold Amplifiers

HTS-0025, HTC-0300

FEATURES

Aperture Times to 20ps
Acquisition Times to 20ns
Linearity 0.01%
$10^{10}\Omega$ Input Z (HTS-0025)
±50mA Output Current

APPLICATIONS

Data Acquisition Systems
Data Distribution Systems
Peak Measurement Systems
Simultaneous Sample & Hold
Analog Delay & Storage

GENERAL DESCRIPTION

The HTS-0025 and HTC-0300 represent "state of the art" in the ability of an analog device to capture and hold rapidly changing transient or continuous waveforms. The user can choose between them by making engineering trade-offs between maximum speed/bandwidth capability, precision gain, feedthrough rejection, input impedance, hold time, harmonic distortion, output swing, logic type, power requirements and price. With an aperture uncertainty of only 20ps and an acquisition/settling time of 20ns, the HTS-0025 is the fastest hybrid sample/track-and-hold amplifier available.

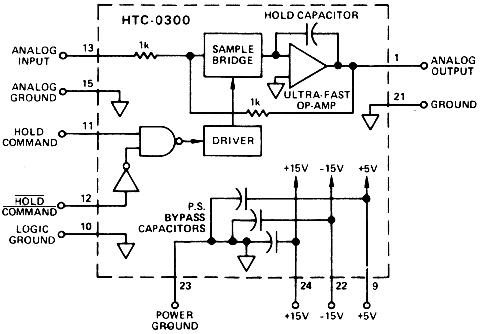
It achieves this performance with a dc coupled Schottky diode sampling bridge driven by a $10^{10}\Omega$ input impedance FET amplifier and followed by a low impedance – 10Ω max – output amplifier.

The HTC-0300 provides 100ps aperture uncertainty and 170ns acquisition/settling time to 0.1% for a 10 volt input-output swing (less than 300ns for 12-bit settling). It achieves this speed and precision gain (-1.00 ±0.1%) with high speed op amps and diode switches. These techniques also improve feedthrough rejection, output swing, linearity, harmonic distortion and droop rate.

APPLICATIONS

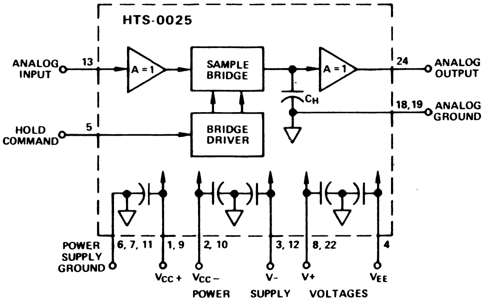
The most common use for a sample/track-and-hold is to place it ahead of an A/D converter to allow digitizing of signals with bandwidths higher than the digitizer alone can handle. The use of the HTS-0025 can allow a reduction of system aperture to 20ps. These sample/track-and-hold amplifiers are also used for peak holding functions, simultaneous sampling A/D's (with appropriate analog multiplexing), and other high-speed analog signal processing applications. These hybrids have been used to construct A/D converters of up to 12 bits of resolution with word rates as high as 20MHz. The HTC-0300 is designed to be used with Analog Devices' HAS Series hybrid A/D converters.

HTC-0300 FUNCTIONAL BLOCK DIAGRAM



NOTE: PIN 12 SHOULD BE GROUNDED IF NOT USED.

HTS-0025 FUNCTIONAL BLOCK DIAGRAM



SPECIFICATIONS (typical at +25°C and nominal power supply voltages unless otherwise noted)

MODEL	UNITS	HTS-0025	HTS-0025M	HTC-0300	HTC-0300M
DYNAMIC CHARACTERISTICS					
Acquisition Time (See Figure 1)					
to 1% for 1V Output Step	ns typ (max)	20 (30)	*	N/A	**
to 0.1% for 10V Output Step	ns typ (max)	N/A	*	170 (200)	170 (200)
Sample Rate[1]	MHz max	30	*	5	**
Aperture Time	ns min (typ) (max)	6 (10) (20)	*	*	*
Settling Time	ns typ (max)	20 (30)	*	100 (120)	**
Bandwidth (3dB 2V p-p Input)	MHz min	30	20	N/A	**
(3dB Small Signal Input)	MHz min	N/A	*	8	**
Slew Rate	V/µs typ (min)	400 (200)	*	250 (120)	250 (100)
Aperture Uncertainty	ps (rms) max	20	*	100	**
Harmonic Distortion (See Figure 6 and Output Loading)	dB typ (max)	65 (60)	*	75 (62)	**
Feedthrough Rejection (2V p-p, 10MHz Input)	dB min	70	*	N/A	**
(dc to 2.5MHz)	dB min	N/A	*	70	**
Droop Rate	mV/µs typ (max)	0.2 (4)[2]	0.2 (30)	0.005 (0.007)	0.005 (0.1)
Pedestal During Hold (See Figure 1)	mV typ (max)	2 (20)	*	5 (50)	**
Transients (See Figure 1)	mV typ (max)	30 (100)	*	N/A	**
ACCURACY/STABILITY DC					
Gain	V/V	+0.92 min	*	-1.00 ±0.1%	**
Gain vs. Temperature	ppm/°C typ (max)	20 (40)	*	10 (50)	**
Zero Offset Voltage	mV typ (max)	2 (20)	*	2 (20)	**
Offset vs. Temperature	typ (max)	50 (150)µV/°C	*	40 (75)ppm/°C	**
Linearity	% max	0.01	*	*	*
INPUT					
Voltage Range	V max	±2	*	±10	**
60dB Feedthrough Rejection	V p-p max	3	*	N/A	**
Impedance	Ω typ (min)	10^{10} (10^{9})	10^{10} (10^{8})	1000	**
Bias Current	nA max	15	100	15µA	**
OUTPUT					
Voltage	V max	±2	*	±10	**
Current (not short circuit protected)	mA max	±50	*	*	*
Impedance	Ω typ (max)	3 (10)	*	0.1 (dc)	**
Loading – Harmonic					
Distortion for 2V p-p 50dB	Ω min	50	*	N/A	**
Signal and Specified R_L 60dB	Ω min	100	*	N/A	**
65dB	Ω min	200	*	N/A	**
Noise[3]	mV rms	0.1 (max)	0.2 (max)	0.1	**
HOLD COMMAND (DIGITAL INPUT)					
Logic Compatible		ECL	*	TTL	**
"0" = Track/"1" = Hold[4]	V	-1.5 to -1.4/-0.7 to -1.05	*	N/A	**
"Hold" Input, "0" = Track/"1" = Hold	V	N/A	*	0 to +0.4/+2.4 to +5	**
"$\overline{\text{Hold}}$" Input, "0" = Hold/"1" = Track	V	N/A	*	0 to +0.4/+2.4 to +5	**
POWER REQUIREMENTS – HTS					
V+ = +15V ±0.5V (Pins 8 and 22)	mA max	40	*	N/A	**
V- = -15V ±0.5V (Pins 3 and 12)	mA max	40	*	N/A	**
$V_{CC}+$ = +4.4V to +15.5V (Pins 1 and 9)[5]	mA max	15	*	N/A	**
V_{CC}^{-} = -4.95V to -15.5V (Pins 2 and 10)[5]	mA max	15	*	N/A	**
V_{EE} = -5.2V ±0.25V (Pin 4)	mA max	40	*	N/A	**
POWER REQUIREMENTS – HTC					
±12V to ±18V	mA max	N/A	*	25	**
+5V to ±0.25V	mA max	N/A	*	25	**
Power Supply Rejection Ratio	mV/V	N/A	*	10	**
TEMPERATURE RANGE					
Operating (Case)	°C	0 to +70	-55 to +100	0 to +70	-55 to +100
Storage	°C	-55 to +125	*	*	*

NOTES:

[1] Sample rates shown are a guide only, and are based on system acquisition times – not logic speed. These rates can be exceeded with acquisition time trade-offs.

[2] Droop rate for case temperatures up to 50°C is 1mV/µs max.

[3] Noise level measured in track mode is 5MHz bandwidth. Noise level increases when high duty cycle repetitive hold command is applied. A 50% duty cycle hold command results in approximately 0.3mV (rms) total noise output.

[4] One ECL-10k Gate, no pulldown resistor.

[5] $V_{CC}+$ may be tied to V^{+}. $V_{CC}-$ may be tied to V^{-} or V_{EE}. However, for proper operation, $V_{CC}+$ and $V_{CC}-$ must have the same numerical value.

*Specifications same as model HTS-0025.
**Specifications same as model HTC-0300.

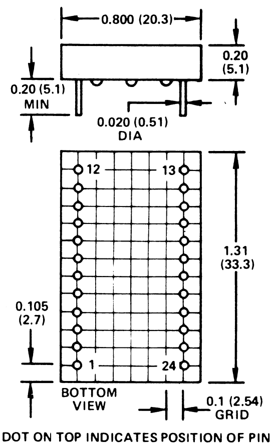
Specifications subject to change without notice.

Specifications in parenthesis ( ) indicate max/min over entire specified operating temperature range.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm)

HTC-0300 (Only)
GLASS PACKAGE



PIN DESIGNATIONS

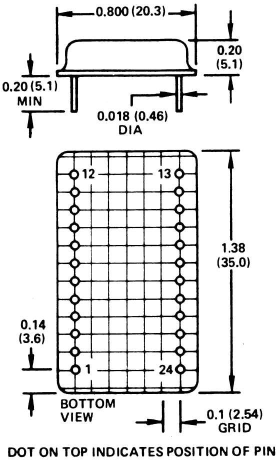
PIN	FUNCTION (HTC-0300)	FUNCTION (HTS-0025)
1	ANALOG OUTPUT	$V_{CC}+$ [+5V to +15.5V]*
2	N/A	$V_{CC}-$ [-5V to -15.5V]*
3	N/A	V- [-15V]
4	N/A	V_{EE} [-5.2V]
5	N/A	HOLD COMMAND
6	N/A	GROUND
7	N/A	GROUND
8	N/A	V+ [+15V]
9	+5V	$V_{CC}+$ [+5V to +15.5V]*
10	GROUND	$V_{CC}-$ [-5V to -15.5V]*
11	HOLD	GROUND
12	$\overline{\text{HOLD}}$	V- [-15V]
13	ANALOG INPUT	ANALOG INPUT
15	INPUT GROUND	N/A
18	N/A	ANALOG GROUND
19	N/A	ANALOG GROUND
21	GROUND	N/A
22	-15V	V+ [+15V]
23	GROUND	N/A
24	+15V	ANALOG OUTPUT

*FOR PROPER OPERATION, $V_{CC}-$ SHOULD HAVE THE SAME NUMERICAL VALUE.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm)

HTS-0025, HTS-0025M, HTC-0300M
METAL PACKAGE



TRACK-AND-HOLD (T/H) MODE

When operated in the T/H mode, these devices are allowed to "track" the input signal for a period of time prior to initiating a "hold command". During the track period, the output follows the input, and the devices function as operational amplifiers. The HTS-0025 operates as a precision follower with a gain of +1, the HTC-0300, -1.

When a Logic "1" is applied to the "hold command" input of the unit, its output is frozen. This output level is held until the track mode is reestablished by a Logic "0" at the hold command input. This operation is shown graphically in Figure 1. The held output level is the voltage value at the input at the instant (plus the aperture time) the hold command is applied.

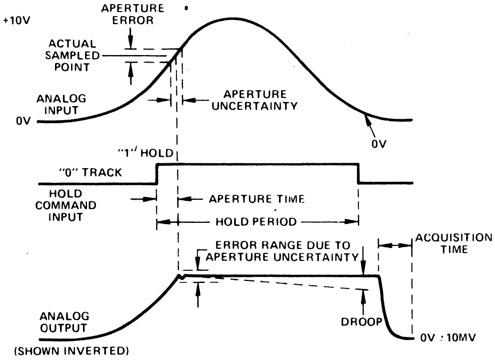


Figure 1a. Track/Hold Waveforms – HTC-0300

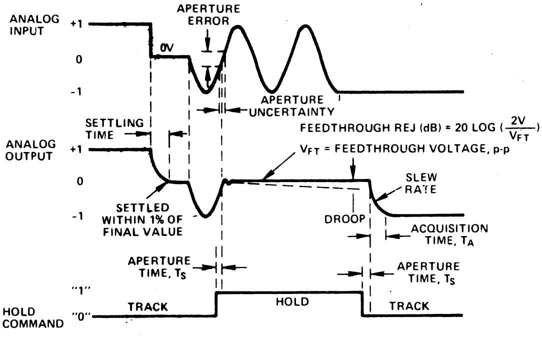


Figure 1b. Track/Hold Waveforms – HTS-0025

The HTC-0300 provides a $\overline{\text{hold}}$ input for use if the hold command is inverted, that is if the user wishes to use a "0" for the hold condition and a "1" for the track mode. Performance of the unit is identical with either type of input.

Variations in the instants of sampling are called aperture uncertainty. It appears as jitter in the sampling point and can cause significant errors when very high dV/dt inputs are sampled. During the hold period, feedthrough and droop rate can introduce errors at the output. It is important that a track-and-hold have high feedthrough rejection to prevent input-to-output leakage during the hold period. The droop rate is the amount the output changes during the hold period as a result of loading on the internal hold capacitor.

When the hold command input returns to the track condition, the amount of time required for the track-and-hold output to reestablish accurate tracking of the input signal is called the acquisition time.

SAMPLE-AND-HOLD (S/H) MODE

In the S/H mode of operation, the devices are normally left in the hold condition. A very short sample pulse is applied to the hold command input when a new sample needs to be obtained at the output. The sample pulse width is dictated by the acquisition time. For small sample-to-sample variations, a pulse width as narrow as 20 to 80ns may be used. In general, however, the pulse width should be 100 to 300ns (see Figure 4).

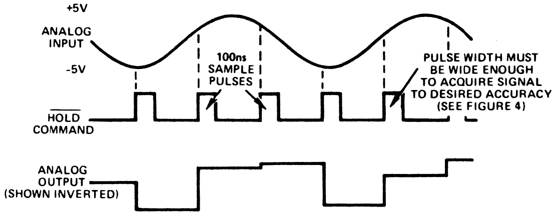

+5V
ANALOG INPUT
-5V
100ns SAMPLE PULSES
PULSE WIDTH MUST BE WIDE ENOUGH TO ACQUIRE SIGNAL TO DESIRED ACCURACY (SEE FIGURE 4)
HOLD COMMAND
ANALOG OUTPUT (SHOWN INVERTED)

Figure 2. Sample/Hold Operation – HTC-0300

The HTC-0300 hybrid track-and-hold amplifier has been designed to operate without external trimming potentiometers and "compensation" devices required in most modular units. Active laser trimming is used on the HTC-0300 to "null" the pedestal (the offset during "HOLD" times), set the dc offset to zero, and adjust the gain of the device to unity. Internal frequency compensating elements are incorporated to make the HTC-0300 unconditionally stable and to optimize the frequency response of the internal operational amplifier for this application. Unlike other microcircuit T/H amplifiers, the HTC has a high drive capability (±50mA) and a very low output impedance which allows it to drive directly virtually all types of A/D converters (even the "current-bucking" input types which will produce a degraded A/D conversion without sufficient T/H output drive) and those with low input impedance.

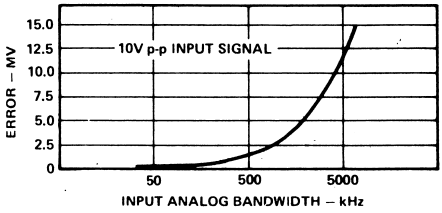


Figure 3. HTC-0300 Error Due to Aperture Uncertainty

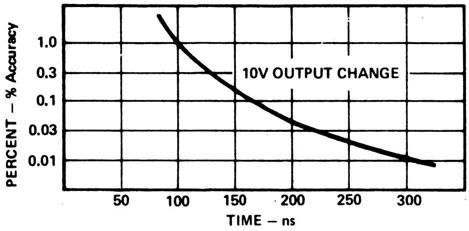


Figure 4a. Settling Accuracy vs. Acquisition Time – HTC-0300

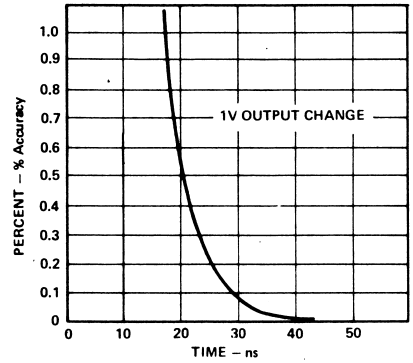


Figure 4b. Settling Accuracy vs. Acquisition Time – HTS-0025

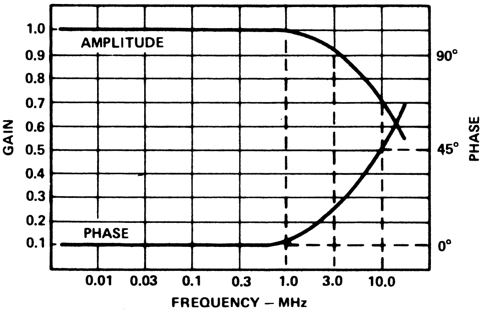


Figure 5. Amplitude and Phase Response – HTC-0300

INPUT: 2V, p-p, 4MHz
LOAD: 1kΩ

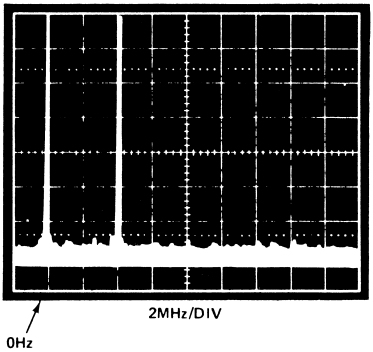


Figure 6a. Harmonic Distortion – Track Mode

RATE: 15MHz
INPUT: 2V, p-p, 3MHz
LOAD: 1kΩ

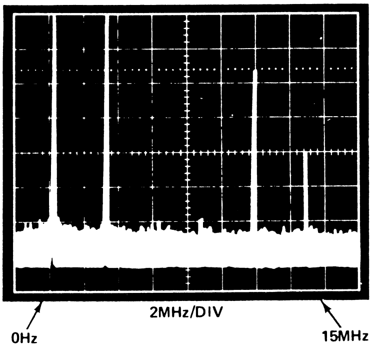


Figure 6b. Frequency Domain Outputs

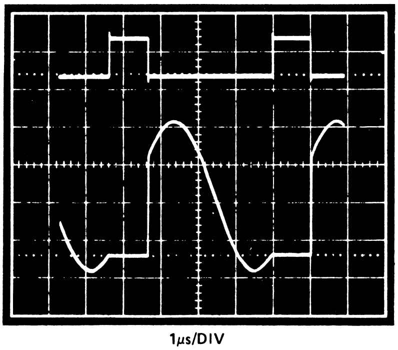
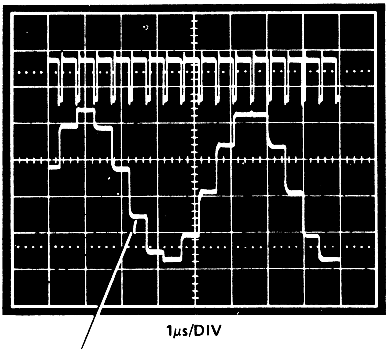


Figure 7a. Track/Hold Operation



PORTION OF SINE WAVE
APPEARS WHEN IN TRACK

Figure 7b. Sample/Hold Operation

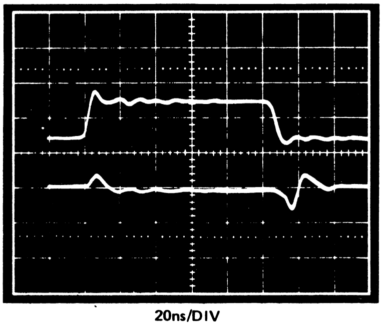


Figure 7c. Expanded View of Output Signal Showing Switching Transients and Pedestal with DC Input

A/D CONVERSION SYSTEM WITH 300kHz CONTINUOUS SAMPLING RATE AND 12-BIT BINARY OUTPUT

The circuit below illustrates a typical application of the HTC-0300 as a sample/hold amplifier preceding a successive-approximation type of A/D converter. During the conversion interval, the input voltage to the A/D must be held constant. To the extent that this input signal is not absolutely constant, an error results in the digitized output of the A/D. However, with the excellent feedthrough-rejection and droop-rate specifications of the HTC-0300, very little error in the A/D conversion process will be due to the T/H circuit. In addition, the very fast acquisition time of this hybrid microcircuit means that the A/D can be operated at very near its maximum sample rate since very little of the conversion cycle time is required for the T/H to acquire each successive signal sample.

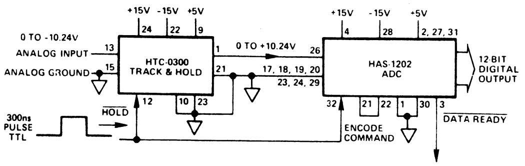


Figure 8. A/D Conversion System

Sample Rate	Approximately 300kHz
Analog Input	Digital Output
0V	000000000000
-10V	111111111111

Table 1. Performance Parameters For This A/D System

ORDERING INFORMATION

Order Model Number HTS-0025 or Model Number HTC-0300 for 0 to +70°C operation. For operation from -55°C to +100°C order Model HTS-0025M or HTC-0300M in metal cases. For units processed to MIL-STD-883, consult the factory or the nearest Analog Devices' sales office.

ANALOG DEVICES

High Resolution 14-Bit Sample and Hold Amplifier

SHA1144

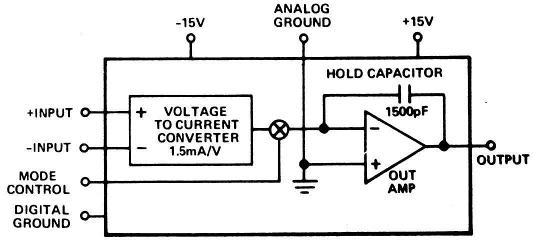
FEATURES

- ±10V min Input/Output Range
- 50ns Aperture Delay
- 0.5ns Aperture Jitter
- 6μs Settling Time
- ±0.001% Max Gain Linearity Error
- Complete with Input Buffer

APPLICATIONS

- Track and Hold
- Peak Measurement Systems
- Data Acquisition Systems
- Simultaneous Sample-and-Hold

SHA1144 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The SHA1144 is a fast sample-hold amplifier module with accuracy and dynamic performance appropriate for applications with fast 14-bit A/D converters. In the "sample" mode, it acts as a fast amplifier, tracking the input signal. When switched to the "hold" mode, the output is held at a level corresponding to the input signal voltage at the instant of switching. The droop rate in "hold" is appropriate to allow accurate conversion by 14-bit A/D converters having conversion times of up to 150μs.

DYNAMIC PERFORMANCE

The SHA1144 was designed to be compatible with fast 14-bit A/D converters such as the Analog Devices' ADC1130 and ADC1131 series, which convert 14 bits in 25μs and 12μs, respectively. Maximum acquisition time of 8μs for the SHA1144 permits high sampling rates for 14-bit conversions. The SHA1144 is guaranteed to have a maximum gain nonlinearity of ±0.001% of full scale to insure 1/2LSB accuracy in 14-bit systems. When in the "hold" mode, the droop rate is 1μV/μs, so the SHA1144 will hold an input signal to ±0.003% of full scale (20V p-p) for over 600μs.

PRINCIPLE OF OPERATION

The SHA1144 consists basically of two high speed operational amplifiers, a storage capacitor, and a digitally controlled switch. It differs from typical sample-and-hold modules in one important respect; application versatility. The user completes the SHA1144 feedback circuit external to the module. Therefore, the module may be used in inverting or noninverting configurations and can easily be arranged to provide circuit gain of more than unity to simplify signal conditioning in a subsystem.

FEEDBACK CONNECTIONS

The input section acts as a voltage-to-current converter, providing the current needed to charge the "hold" capacitor. The output amplifier isolates the "hold" capacitor and provides low output impedance for driving the load. Since feedback is not hard-wired in the module, both inverting and noninverting input terminals are available, and the SHA1144 can be connected as a follower with unity gain or potentiometric gain, as well as inverter or even a differential amplifier. Since the unity gain follower mode will be the most frequent application, performance data listed in the specification table is based on this operating mode.

This two-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be found in Volume II, page 14–11.

SPECIFICATIONS (typical @ +25°C, gain = +1V/V and nominal supply voltages unless otherwise noted)

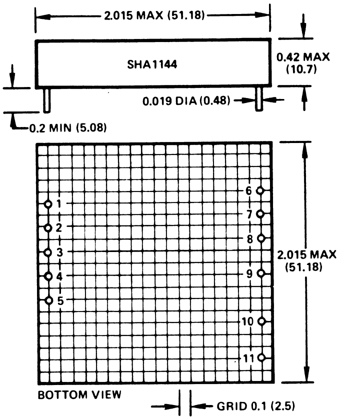
MODEL	SHA1144
ACCURACY	
Gain	+1V/V
Gain Error	±0.005%
Gain Nonlinearity	±0.0005% (±0.001% max)
Gain Temperature Coefficient (0 to +70°C)	±1ppm/°C (±2ppm/°C max)
INPUT CHARACTERISTICS	
Input Voltage Range	±10V
Impedance	$10^{11}\ \Omega \parallel 10pF$
Bias Current	0.5nA max
Initial Offset Voltage	Adjustable to Zero
Offset vs. Temperature (0 to +70°C)	±30μV/°C max
OUTPUT CHARACTERISTICS	
Voltage	±10V min
Current	±20mA min
Resistance	<1Ω
Capacitive load	350pF
Noise @ 100kHz Bandwidth	70μV p-p
@ 1MHz Bandwidth	175μV p-p
SAMPLE MODE DYNAMICS	
Frequency Response	
Small Signal (-3dB)	1MHz
Full Power	50kHz
Slew Rate	3V/μs
SAMPLE-TO-HOLD SWITCHING	
Aperture Delay Time	50ns
Aperture Uncertainty	0.5ns
Offset Step	1mV
Offset Nonlinearity	160μV
Switching Transient	
Amplitude	50mV
Settling Time to ±0.003%	1μs
HOLD MODE DYNAMICS	
Droop Rate	1μV/μs (2μV/μs max)
Variation with Temperature	double every +10°C
Feedthrough (for 20V p-p Input @ 1kHz)	-80dB
HOLD-TO-SAMPLE SWITCHING	
Acquisition Time to ±0.003% (20V Step)	6μs (8μs max)
(10V Step)	5μs
±0.01% (20V Step)	5μs
(10V Step)	4μs
DIGITAL INPUT	
Sample Mode (Logic "1")	+2V<Logic "1"<+5.5V @ 15nA max
Hold Mode (Logic "0")	0V<Logic "0"<+0.8V @ 5μA (20μA max)
POWER REQUIRED[1]	+15V ±3% @ 60mA -15V ±3% @ 45mA
TEMPERATURE RANGE	
Operating	0 to +70°C
Storage	-55°C to +85°C

[1] Recommended Power Supply ADI Model 902-2, ±15V @ ±100mA output.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

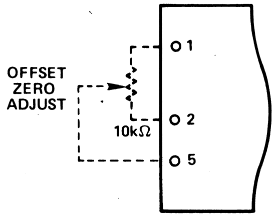
Dimensions shown in inches and (mm).



PIN DESIGNATIONS

1. TRIM
2. TRIM
3. +INPUT
4. -INPUT
5. TRIM
6. +15V
7. ANALOG GROUND
8. -15V
9. ANALOG OUTPUT
10. MODE CONTROL
11. DIGITAL GROUND

OFFSET ZERO ADJUST (OPTIONAL)



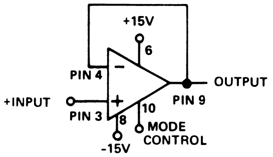


Figure 1. Unity Gain Follower

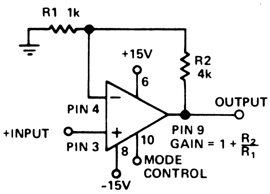


Figure 2. Noninverting Operation

Data-Acquisition Subsystems

Contents

Page

Selection Guide 15-3
AD362 Hybrid-IC 16-to-8-Channel DAS Front End, for User-Chosen A/D Converter 15-5
AD363 Hybrid-IC 16-to-8-Channel 12-Bit Complete DAS 15-13
AD364 Hybrid-IC 16-to-8-Channel 12-Bit Complete µP-Compatible DAS 15-25
DAS1128 16/8-Channel 12-Bit Data-Acquisition System 15-37
●DAS1152/1153 14-Bit and 15-Bit Sampling Analog-to-Digital Converters 15-39
●DAS1155/1156 14-Bit and 15-Bit Low Level Data-Acquisition Systems 15-41

●New product since the *1980 Data-Acquisition Components and Subsystems Catalog*

Selection Guide
Data-Acquisition Subsystems

The products to be found in this section are high-performance modules and hybrid A/D conversion circuits that also provide sample-hold and/or multiplexing. In addition, some types have programmable-gain amplifiers, microprocessor interface logic, and switching for applications involving both differential and single-ended inputs.

In addition to the devices listed in the Selection Guide, there are a number of other devices, to be found in this Volume, which perform data-acquisition functions, including MACSYM, the µMAC-4000 Intelligent Measurement-and-Control Subsystem, Microcomputer Interface Boards, Digital Panel Meters, and A/D Converters (including, for example, the 12-bit 5MHz MOD-1205, with on-board track-hold amplifier).

Of especial note are the AD2036, AD2037, and AD2038 scanning digital panel instruments (to be found in the Digital Panel Instrument Section), which provide complete six-channel data-acquisition (including power supply) for measurement of temperature or voltage and have BCD data outputs for system input. Also of note (and to be found in Volume I) is the monolithic AD7581 data-acquisition-system-on-a-chip, which continuously converts 8 channels of analog information, stores stores them in dual-port RAM, and continuously makes all eight available by direct memory read instructions to the appropriate channel.

The data sheets provide complete descriptions, specifications, and application information. Additional general information pertaining to portions of the subsystems may be found in the appropriate sections of this Databook (e.g., A/D Converters, Sample/Track-Hold Amplifiers). Basic general information can be found in *Analog-Digital Conversion Notes*, a 246-page book published by Analog Devices, Inc. It is available at $5.95 from P.O. Box 796, Norwood, MA 02062.

		SINGLE CHANNEL				MULTI-CHANNEL				
		DAS1152	DAS1153	DAS1155	DAS1156	AD7581	AD363[1,2]	AD364[1,2]	AD362[1,3]	DAS1128[1]
Resolution	8 Bits					●				
	12 Bits						●	●		●
	14 Bits	●		●						
	15 Bits		●		●					
Input Structure	Sample/Hold	●	●	●	●		●	●	●	●
	Single Ended	●	●			●	●	●	●	
	Differential			●	●		●	●	●	●
	Amplifier									
	Differential Amplifier			●	●		●	●	●	●
	Resistor Programmable Gain			●	●					
	Channels									
	One	●	●	●	●					
	Eight					●	●	●	●	●
	Sixteen						●	●	●	●
Internal Reference		●	●	●	●		●	●	●	●
µP Bus Compatible		●	●	●	●	●		●		
Operating Temperature Ranges	0 to +70°C	●	●	●	●	●	●	●	●	●
	-25°C to +85°C	●	●	●	●	●				
	-55°C to +125°C						●	●	●	
Output	Digital	●	●	●	●	●	●	●		●
	Analog								●	
Logic Compatible	TTL	●	●	●	●	●	●	●	●	●
	CMOS					●				
Volume I Page		15-39	15-39	15-41	15-41	11-121	15-13	15-25	15-5	15-37
Volume II Page		15-25	15-25	15-29	15-29	–	15-9	15-13	15-5	15-17

[1] 8 channels differential input, 16 channels single ended.
[2] Two DIP packages.
[3] DAS Analog Input Section.

ANALOG DEVICES

Precision Sample-and-Hold with 16-Channel Multiplexer

AD362

FEATURES

- **16 Single-Ended or 8 Differential Channels with Switchable Mode Control**
- **True 12-Bit Precision: Nonlinearity ≤±0.005%**
- **High Speed: 10μs Acquisition Time to 0.01%**
- **Complete and Calibrated: No Additional Parts Required**
- **Small, Reliable: 32 Pin Hermetic Metal DIP**
- **Versatile: Simple Interface to Popular Analog to Digital Converters**
- **High Differential Input Impedance ($10^{10}\Omega$) and Common Mode Rejection (80dB)**
- **Fully Protected Multiplexer Inputs**

PRODUCT DESCRIPTION

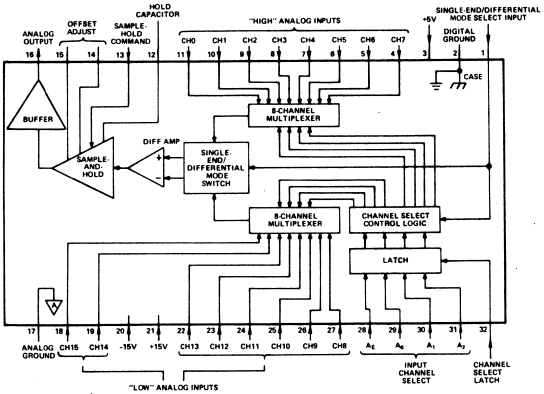
The AD362 is a complete, precision 16-channel data acquisition system analog input section in hybrid integrated circuit form. Large-scale linear integrated circuitry, thick- and thin-film technology and active laser trimming gives the AD362 extensive applications versatility along with full 12-bit accuracy.

The AD362 contains two 9-channel multiplexers, a differential amplifier, a sample-and-hold with high-speed output amplifier, a channel address latch and control logic. The multiplexers may be connected to the differential amplifier in either an 8-channel differential or 16-channel single-ended configuration. A unique feature of the AD362 is an internal user-controllable analog switch that connects the multiplexers in either a single-ended or differential mode. This allows a single device to perform in either mode without hard-wire programming and permits a mixture of single-ended and differential sources to be interfaced by dynamically switching the input mode control.

The sample-and-hold mode control is designed to connect directly to the "Status" output of an analog to digital converter so that a convert command to the ADC will automatically put the sample-and-hold into the "Hold" mode. A precision hold capacitor is included with each AD362. The AD362 output amplifier is capable of driving the unbuffered analog input of most high-speed, 12-bit successive-approximation ADCs. Interface is thereby reduced to two simple connections with no additional components required.

When used with a 12-bit, 25-microsecond ADC such as the AD572, AD574 or AD ADC80, system throughput rate is as high as 30kHz at full rated accuracy. The AD362KD is specified for operation over a 0 to +70°C temperature range while the AD362SD operates to specification from -55°C to +125°C. Processing to MIL-STD-883, Class B is available for the AD362SD. Both grades are packaged in a hermetic, electrostatically shielded 32-pin metal dual-in-line package.

AD362 FUNCTIONAL BLOCK DIAGRAM



32-PIN DIP

PRODUCT HIGHLIGHTS

1. The AD362, when used with a precision analog to digital converter, forms a complete, accurate, high-speed data acquisition system.
2. The 16-input channels may be configured in single-ended, differential or a mixture of both modes. Mode switching is provided by a user-controllable internal analog switch.
3. Multiplexers, differential amplifier, sample-and-hold and high-speed output buffer provide complete analog interfacing capabilities.
4. Internal channel address latches are provided to facilitate interfacing the AD362 to data, address or control buses.
5. All grades of the AD362 are hermetically sealed in rugged metal DIP packages.
6. A precision hold capacitor is provided with each AD362.
7. The AD362SD is specified over the entire military temperature range, -55°C to +125°C. Processing to MIL-STD-883, Class B is available.

SPECIFICATIONS (typical @ +25°C, ±15V and +5V with 2000pF hold capacitor as provided unless otherwise noted)

MODEL	AD362KD	AD362SD/AD362SD-883B[1]
ANALOG INPUTS		
Number of Inputs	16 Single-Ended or 8 Differential (Electronically Selectable)	*
Input Voltage Range, Linear T_{min} to T_{max}	±10V min	*
Input (Bias) Current, Per Channel	±50nA max	*
Input Impedance		
On Channel	$10^{10}\Omega$, 100pF	*
Off Channel	$10^{10}\Omega$, 10pF	*
Input Fault Current (Power Off or On)	20mA, max, Internally Limited	*
Common Mode Rejection		
Differential Mode	70dB min (80dB typ) @ 1kHz, 20V p-p	*
Mux Crosstalk (Interchannel, Any Off Channel to Any On Channel)	-80dB max (-90dB typ) @ 1kHz, 20V p-p	*
Offset, Channel to Channel	±2.5mV max	*
ACCURACY		
Gain Error, T_{min} to T_{max}	±0.02% FSR, max	*
Offset Error, T_{min} to T_{max}	±4mV	*
Linearity Error	±0.005% max	*
T_{min} to T_{max}	±0.01% max	*
Noise Error	1mV p-p, 0.1 to 1MHz, max	*
T_{min} to T_{max}	2mV p-p, 0.1 to 1MHz, max	*
TEMPERATURE COEFFICIENTS		
Gain, T_{min} to T_{max}	±4ppm/°C max	±2ppm/°C max
Offset, ±10V Range, T_{min} to T_{max}	±2ppm/°C max	±1.5ppm/°C max
SAMPLE AND HOLD DYNAMICS		
Aperture Delay	100ns max (50ns typ)	*
Aperture Uncertainty	500ps max (100ps typ)	*
Acquisition Time, for 20V Step to ±0.01% of Final Value	18μs max (10μs typ)	*
Feedthrough	-70dB max (-80dB typ) @ 1kHz	*
Droop Rate	2mV/ms max (1mV/ms typ)	*
DIGITAL INPUT SIGNALS[2]		
Input Channel Select (Pins 28-31)	4-Bit Binary, Channel Address	*
	1LS TTL Load	*
Channel Select Latch (Pin 32)	"1": Latch Transparent	*
	"0": Latched	*
	8LS TTL Loads	*
Single Ended/Differential Mode Select (Pin 1)	"0": Single-Ended Mode	*
	"1": Differential Mode	*
	3TTL Loads	*
Sample and Hold Command (Pin 13)	"0": Sample Mode	*
	"1": Hold Mode	*
	1TTL Load	*
POWER REQUIREMENTS		
Supply Voltages/Currents	+15V, ±5% @ 30mA max	*
	-15V, ±5% @ 30mA max	*
	+5V, ±5% @ 40mA max	*
Total Power Dissipation	1.1 Watts max	*
TEMPERATURE RANGE		
Specification	0 to +70°C	-55°C to +125°C
Storage	-55°C to +85°C[3]	-55°C to +150°C

NOTES:

[1] The AD362 is available processed and screened to the requirements of MIL-STD-883, Class B. When ordering, specify "AD362SD/883B".

[2] One TTL Load is defined as $I_{IL} = -1.6mA$ max @ $V_{IL} = 0.4V$, $I_{IH} = 40\mu A$ max @ $V_{IH} = 2.4V$. One LS TTL Load is defined as $I_{IL} = -0.36mA$ max @ $V_{IL} = 0.4V$, $I_{IH} = 20\mu A$ max @ $V_{IH} = 2.7V$.

[3] AD362KD External Hold Capacitor is limited to +85°C; AD362 device itself may be stored at up to +150°C.

*Specifications same as AD362KD.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS
(ALL MODELS)

+V, Digital Supply	+5.5V
+V, Analog Supply	+16V
-V, Analog Supply	-16V
V_{IN}, Signal	±V, Analog Supply
V_{IN}, Digital	0 to +V, Digital Supply
A_{GND} to D_{GND}	±1V

AD362 ORDERING GUIDE

Model	Specification Temp Range	Max Gain TC	Package Option[1]
AD362KD	0 to +70°C	±4ppm/°C	HY32D
AD362SD	-55°C to +125°C	±2ppm/°C	HY32D
AD362SD/ 883B	-55°C to +125°C	±2ppm/°C	HY32D

NOTE: D Suffix = Dual-In-Line package designator.

[1] See Section 20 for package outline information.

AD362 PIN FUNCTION DESCRIPTION

Pin Number	Function
1	Single-End/Differential Mode Select "0": Single-Ended Mode "1": Differential Mode
2	Digital Ground
3	Positive Digital Power Supply, +5V
4	"High" Analog Input, Channel 7
5	"High" Analog Input, Channel 6
6	"High" Analog Input, Channel 5
7	"High" Analog Input, Channel 4
8	"High" Analog Input, Channel 3
9	"High" Analog Input, Channel 2
10	"High" Analog Input, Channel 1
11	"High" Analog Input, Channel 0
12	Hold Capacitor (Provided)
13	Sample-Hold Command "0": Sample Mode "1": Hold Mode Normally Connected to ADC Status
14	Offset Adjust (See Figure 5)
15	Offset Adjust (See Figure 5)
16	Analog Output Normally Connected to ADC "Analog In"
17	Analog Ground
18	"High" ("Low") Analog Input, Channel 15 (7)
19	"High" ("Low") Analog Input, Channel 14 (6)
20	Negative Analog Power Supply, -15V
21	Positive Analog Power Supply, +15V
22	"High" ("Low") Analog Input, Channel 13 (5)
23	"High" ("Low") Analog Input, Channel 12 (4)
24	"High" ("Low") Analog Input, Channel 11 (3)
25	"High" ("Low") Analog Input, Channel 10 (2)
26	"High" ("Low") Analog Input, Channel 9 (1)
27	"High" ("Low") Analog Input, Channel 8 (0)
28	Input Channel Select, Address Bit AE
29	Input Channel Select, Address Bit A0
30	Input Channel Select, Address Bit A1
31	Input Channel Select, Address Bit A2
32	Input Channel Select Latch "0": Latched "1": Latch Transparent

AD362 DESIGN

The AD362 consists of two 8-channel multiplexers, a differential amplifier, a sample-and-hold with high-speed output buffer, channel address latches and control logic as shown in Figure 1. The multiplexers can be connected to the differential amplifier in either an 8-channel differential or 16-channel single-ended configuration. A unique feature of the AD362 is an internal analog switch controlled by a digital input that performs switching between single-ended and differential modes. This feature allows a single AD362 to perform in either mode without external hard-wire interconnections. Of more significance is the ability to serve a mixture of both single-ended and differential sources with a single AD362 by dynamically switching the input mode control.

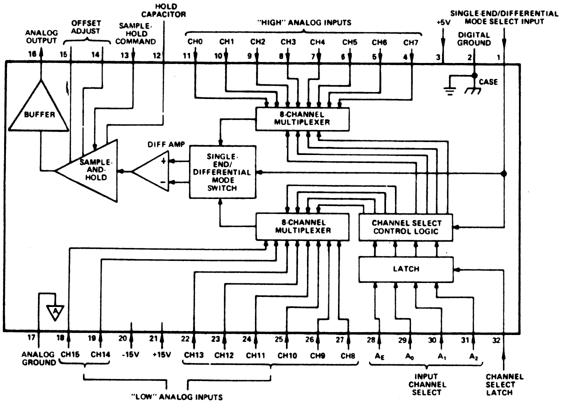


Figure 1. AD362 Analog Input Section Functional Block Diagram and Pinout

Multiplexer channel address inputs are interfaced through a level-triggered ("transparent") input register. With a Logic "1" at the Channel Select Latch input, the address signals feed through the register to directly select the appropriate input channel. This address information can be held in the register by placing a Logic "0" on the Channel Select Latch input. Internal logic monitors the status of the Single-Ended/Differential Mode input and addresses the multiplexers accordingly.

A differential amplifier buffers the multiplexer outputs while providing high input impedance in both differential and single-ended modes. Amplifier gain and common mode rejection are actively laser-trimmed.

The sample-and-hold is a high speed monolithic device that can also function as a gated operational amplifier. Its uncommitted differential inputs allow it to serve a second role as the output subtractor in the differential amplifier. This eliminates one amplifier and decreases drift, settling time and power consumption. A Logic "1" on the Sample-and-Hold Command input will cause the sample-and-hold to "freeze" the analog signal while the ADC performs the conversion. Normally the Sample-and-Hold Command is connected to the ADC Status output which is at Logic "1" during conversion and Logic "0" between conversions. For slowly-changing inputs, throughput speed may be increased by grounding the Sample-and-Hold Command input instead of connecting it to the ADC status.

A Polystyrene hold capacitor is provided with each commercial temperature range device (AD362KD) while a Teflon capacitor is provided with units intended for operation at temperatures up to 125°C (AD362SD). Use of an external capacitor allows the user to make his own speed/accuracy tradeoff; a smaller capacitor will allow faster sample-and-hold response but will decrease accuracy while a larger capacitor will increase accuracy at slower conversion rates.

The output buffer is a high speed amplifier whose output impedance remains low and constant at high frequencies. Therefore, the AD362 may drive a fast, unbuffered, precision ADC without loss of accuracy.

The AD362 is constructed on a substrate that includes thick-film resistors for non-critical applications such as input protection and biasing. A separately-mounted laser-trimmed thin-film resistor network is used to establish accurate gain and high common-mode rejection. The metal package affords electromagnetic and electrostatic shielding and is hermetically welded at low temperatures. Welding eliminates the possibility of contamination from solder particles or flux while low temperature sealing maintains the accuracy of the laser-trimmed thin-film resistors.

THEORY OF OPERATION

Concept

The AD362 is intended to be used in conjunction with a high-speed precision analog-to-digital converter to form a complete data acquisition system (DAS) in microcircuit form. Figure 2 shows a general AD362-with-ADC DAS application.

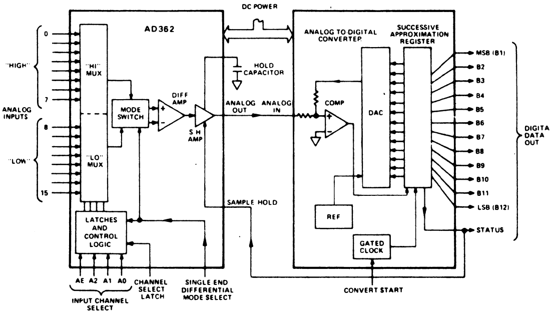


Figure 2. AD362 with ADC as a Complete Data Acquisition System

By dividing the data acquisition task into two sections, several important advantages are realized. Performance of each design is optimized for its specific function. Production yields are increased thus decreasing costs. Furthermore, the standard configuration packages plug into standard sockets and are easier to handle than larger packages with higher pin counts.

System Timing

Figure 3 is a timing diagram for the AD362 connected as shown in Figure 2 and operating at maximum conversion rate. The ADC is assumed to be a conventional 12 bit type such as the AD572 or AD ADC80.

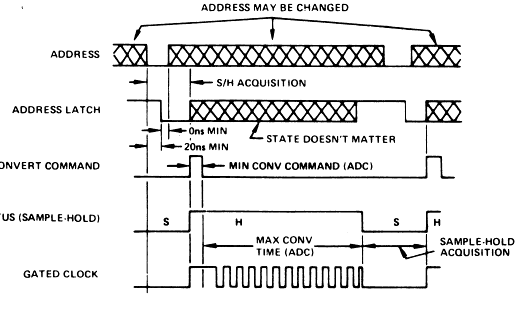


Figure 3. DAS Timing Diagram

The normal sequence of events is as follows:

1. The appropriate Channel Select Address is latched into the address register. Time is allowed for the multiplexers to settle.
2. A Convert Start command is issued to the ADC which, in response, indicates that it is "busy" by placing a Logic "1" on its Status line.
3. The ADC Status controls the sample-and-hold. When the ADC is "busy", the sample-and-hold is in the Hold mode.
4. The ADC goes into its conversion routine. Since the sample-and-hold is holding the proper analog value, the address may be updated during conversion. Thus multiplexer settling time can coincide with conversion and need not affect throughput rate.
5. The ADC indicates completion of its conversion by returning Status to Logic "0". The sample-and-hold returns to the Sample mode.
6. If the input signal has changed full-scale (different channels may have widely-varying data) the sample-and-hold will typically require 10 microseconds to "acquire" the next input to sufficient accuracy for 12-bit conversion.

After allowing a suitable interval for the sample-and-hold to stabilize at its new value, another Convert Start command may be issued to the ADC.

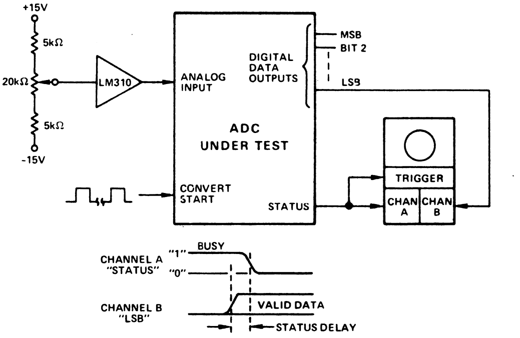


Figure 4. ADC Status Valid Test

NOTE:

Valid Output Data

Not all ADCs have all data bits available when Status indicates that the conversion is complete. Successive approximation ADCs based on the 2502/3/4 type of register must have a Status delay built in or the final data bit will lag Status by approximately 50ns. This will result in two problems:

1. The sample-and-hold will return to Sample, disturbing the analog input to the ADC as it is attempting to convert the least significant bit. This may result in an error.
2. If the falling edge of Status is being used to load the data into a register, the least significant bit will not be valid when loaded.

An external 100ns delay or use of an ADC with a valid Status output is necessary to prevent this problem. The applications shown in this data sheet ensure that all data bits will be valid.

The following test may be made to determine if the ADC Status timing is correct:

1. Connect the ADC under test as shown in Figure 4.
2. Trigger the oscilloscope on Status. Delay the display such that Status is mid-screen.
3. Observe the LSB data output of the ADC.
4. Vary the analog input control to confirm that the LSB transition precedes the Status transition.

Single-Ended/Differential Mode Control

The AD362 features an internal analog switch that configures the Analog Input Section in either a 16-channel single-ended or 8-channel differential mode. This switch is controlled by a TTL logic input applied to pin 1 of the Analog Input Section:

"0": Single-Ended (16 channels)
"1": Differential (8 channels)

When in the differential mode, a differential source may be applied between corresponding "High" and "Low" analog input channels.

It is possible to mix SE and DIFF inputs by using the mode control to command the appropriate mode. In this case, four microseconds must be allowed for the output of the Analog Input Section to settle to within ±0.01% of its final value, but if the mode is switched concurrent with changing the channel address, no significant additional delay is introduced. The effect of this delay may be eliminated by changing modes while a conversion is in progress (with the sample-and-hold in the "Hold" mode). When SE and DIFF signals are being processed concurrently, the DIFF signals must be applied between corresponding "High" and "Low" analog input channels. Another application of this feature is the capability of measuring 16 sources individually and/or measuring differences between pairs of those sources.

Input Channel Addressing

Table 1 is the truth table for input channel addressing in both the single-ended and differential modes. The 16 single-ended channels may be addressed by applying the corresponding digital number to the four Input Channel Select address bits, AE, A0, A1, A2 (pins 28–31). In the differential mode, the eight channels are addressed by applying the appropriate digital code to A0, A1 and A2; AE must be enabled with a Logic "1". Internal logic monitors the status of the SE/DIFF Mode input and addresses the multiplexers singularly or in pairs as required.

ADDRESS				ON CHANNEL (Pin Number)		
					Differential	
AE	A2	A1	A0	Single Ended	"Hi"	"Lo"
0	0	0	0	0 (11)	None	
0	0	0	1	1 (10)	None	
0	0	1	0	2 (9)	None	
0	0	1	1	3 (8)	None	
0	1	0	0	4 (7)	None	
0	1	0	1	5 (6)	None	
0	1	1	0	6 (5)	None	
0	1	1	1	7 (4)	None	
1	0	0	0	8 (27)	0 (11)	0 (27)
1	0	0	1	9 (26)	1 (10)	1 (26)
1	0	1	0	10 (25)	2 (9)	2 (25)
1	0	1	1	11 (24)	3 (8)	3 (24)
1	1	0	0	12 (23)	4 (7)	5 (23)
1	1	0	1	13 (22)	5 (6)	5 (22)
1	1	1	0	14 (19)	6 (5)	6 (19)
1	1	1	1	15 (18)	7 (4)	7 (18)

Table 1. Input Channel Addressing Truth Table

When the channel address is changed, six microseconds must be allowed for the Analog Input Section to settle to within ±0.01% of its final output (including settling times of all elements in the signal path). The effect of this delay may be eliminated by performing the address change while a conversion is in progress (with the sample-and-hold in the "Hold" mode).

Input Channel Address Latch

The AD362 is equipped with a latch for the Input Channel Select address bits. If the Latch Control pin (pin 32) is at Logic "1", input channel select address information is passed through to the multiplexers. A Logic "0" "freezes" the input channel address present at the inputs at the "1"-to-"0" transition (level-triggered).

This feature is useful when input channel address information is provided from an address, data or control bus that may be required to service many devices. The ability to latch an address is helpful whenever the user has no control of when address information may change.

Sample-and-Hold Mode Control

The Sample-and-Hold Mode Control input (pin 13) is normally connected to the Status output (pin 20) from an analog to digital converter. When a conversion is initiated by applying a Convert Start command to the ADC, Status goes to Logic "1", putting the sample-and-hold into the "Hold" mode. This "freezes" the information to be digitized for the period of conversion. When the conversion is complete, Status returns to Logic "0" and the sample-and-hold returns to the "Sample" mode. Eighteen microseconds must be allowed for the sample-and-hold to acquire ("catch up" to) the analog input to within ±0.01% of the final value before a new Convert Start command is issued.

The purpose of a sample-and-hold is to "stop" fast changing input signals long enough to be converted. In this application, it also allows the user to change channels and/or SE/ DIFF mode while a conversion is in progress thus eliminating the effects of multiplexer, analog switch and differential amplifier settling times. If maximum throughput rate is required for slowly changing signals, the Sample-and-Hold Mode Control may be wired to ground (Logic "0") rather than to ADC Status thus leaving the sample-and-hold in a continuous Sample mode.

Hold Capacitor

A 2000pF capacitor is provided with each AD362. One side of this capacitor is wired to pin 12, the other to analog ground as close to pin 17 as possible. The capacitor provided with the AD362KD is Polystyrene while the wider operating temperature range of the AD362SD requires a Teflon capacitor (supplied).

Smaller capacitors will allow slightly faster operation, but only with increased noise and decreased precision. 1000pF will typically allow acquisition to 0.1% in four microseconds.

Larger capacitors may be substituted to reduce noise, and sample-to-hold offset, but acquisition time of the sample-and-hold will be extended. If less than 12 bits of accuracy is required, a smaller capacitor may be used. This will shorten the S/H acquisition time. In all cases, the proper capacitor dielectric must be used; i.e., Polystyrene (AD326KD only) or Teflon (AD362KD or SD). Other types of capacitors may have higher dielectric absorption (memory) and will cause errors. CAUTION: Polystyrene capacitors will be destroyed if subjected to temperatures above +85° C. No capacitor is required if the sample-and-hold is not used.

Analog Input Section Offset Adjust Circuit

Although the offset voltage of the AD362 may be adjusted, that adjustment is normally performed at the ADC. In some special applications, however, it may be helpful to adjust the offset of the Analog Input Section. An example of such a case would be if the input signals were small (<10mV) relative to AD362 voltage offset and gain was to be inserted between the AD362 and the ADC. To adjust the offset of the AD362, the circuit shown in Figure 5 is recommended.

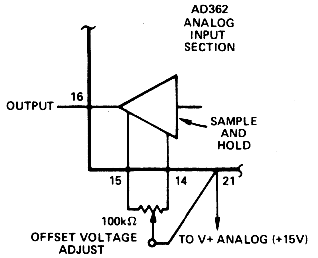


Figure 5. AD362 Offset Voltage Adjustment

Under normal conditions, all calibration is performed at the ADC Section.

Other Considerations

Grounding: Analog and digital signal grounds should be kept separate where possible to prevent digital signals from flowing in the analog ground circuit and inducing spurious analog signal noise. Analog Ground (pin 17) and Digital Ground (pin 2) are not connected internally; these pins must be connected externally for the system to operate properly. Preferably, this connection is made at only one point, as close to the AD362 as possible. The case is connected internally to Digital Ground to provide good electrostatic shielding. If the grounds are not tied common on the same card with the AD362, the digital and analog grounds should be connected locally with back-to-back general-purpose diodes as shown in Figure 6. This will protect the AD362 from possible damage caused by voltages in excess of ±1 volt between the ground systems which could occur if the key grounding card should be removed from the overall system. The device will operate properly with as much as ±200mV between grounds, however this difference will be reflected directly as an input offset voltage.

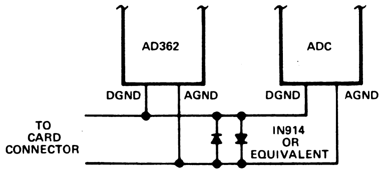


Figure 6. Ground-Fault Protection Diodes

Power Supply Bypassing: The ±15V and +5V power leads should be capacitively bypassed to Analog Ground and Digital Ground respectively for optimum device performance. 1μF tantalum types are recommended; these capacitors should be located close to the system. It is not necessary to shunt these capacitors with disc capacitors to provide additional high frequency power supply decoupling since each power lead is bypassed internally with a 0.039μF ceramic capacitor.

Interfacing to Popular Analog to Digital Converters

The AD362 has been designed to interface directly to most analog to digital converters; often no additional components are required and only two interconnections must be made. The direct interface requirements for the ADC are as follows:

1. The ADC Status output must be positive-true Logic ("1" during conversion).
2. Transition from "0" to "1" must occur at least 200ns before the most significant bit decision is made (successive approximation ADC) or before input integration starts (integrating type ADC).
3. Status must not return to "0" before the LSB decision is made.
4. If Status is being used to latch output data, it must not return to Logic "0" until all output data bits are valid and available.

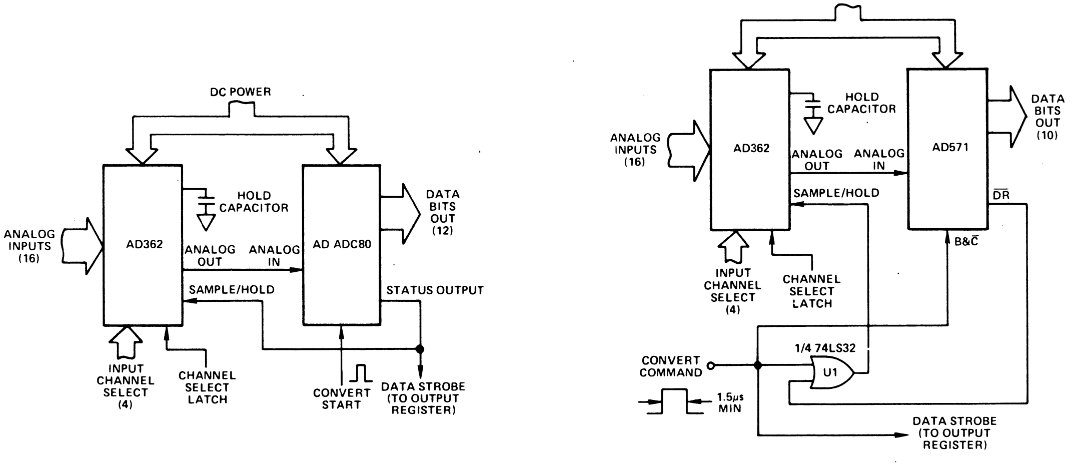
Complete system throughput performance is determined by combining the worst-case specifications of the AD362 and the ADC. If guaranteed system performance is required, the AD363 and AD364 are recommended. The AD363 includes an AD362 and an AD572 12-bit, 25-microsecond precision ADC. The AD364 consists of an AD362 and an AD574 12-bit, microprocessor-compatible, low cost ADC. Each is specified as a complete, two-package system; data sheets are available upon request.

Figure 7a shows the AD362 driving an AD ADC80. The AD ADC80 is a 12-bit, 25-microsecond, low-cost ADC that meets all of the requirements listed above. Throughput rate is typically 30kHz with no missing codes over the operating temperature range.

Figure 7b shows a 10-bit application based on the AD362 and the AD571, a complete low cost 10-bit, 25-microsecond ADC. In this case, two of the above requirements are not met:

1. $\overline{\text{DR}}$ ($\overline{\text{DATA READY}}$), as Status, is positive-true but. . .
2. $\overline{\text{DR}}$ does not indicate that a conversion is in progress until 1.5μs after conversion starts.
3. $\overline{\text{DR}}$ does indicate conversion complete after the LSB decision is made, but. . .
4. $\overline{\text{DR}}$ precedes the enabling of the AD571 output 3-state gates by 500ns.

The gating provided by U1 allows the applied convert command (CC) to initiate input hold at the AD362. CC must last for more than 1.5μs so that $\overline{\text{DR}}$ may then assume control of Hold. If conversion is continuous (consistent with multichannel operation), the next convert command can be used to load the previously-converted data into an output register. For single conversion operation, a 1μs delay of the falling edge of $\overline{\text{DR}}$ may be used to signify valid data.



a. 12-Bit DAS Using AD362 and AD ADC80

b. 10-Bit DAS Using AD362 and AD571

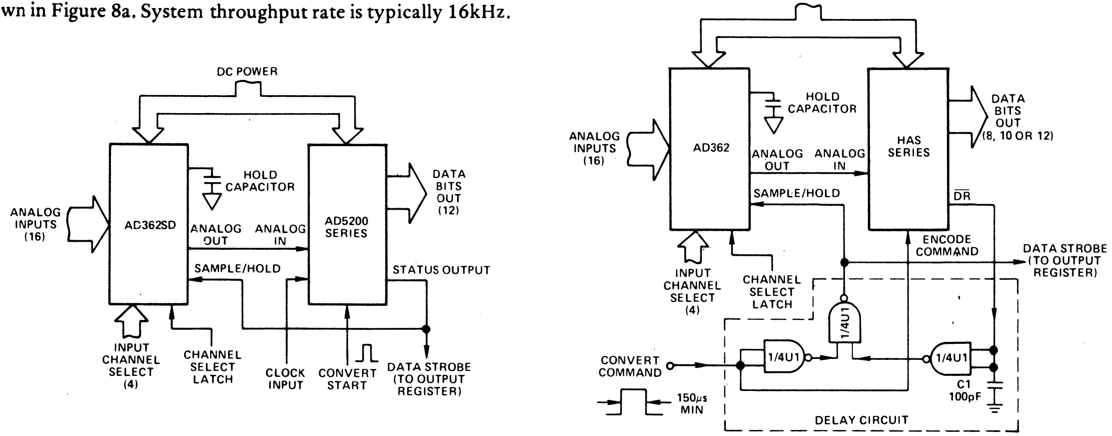
Figure 7. Data Acquisition Systems Based on the AD362 and Popular ADC's

Interfacing to Special Purpose ADCs

The AD5200 series of ADCs perform a 12-bit conversion in 50 microseconds and feature totally adjustment-free operation, high accuracy, and a small hermetically-sealed 24-pin package.

These ADCs are often used in high-reliability applications and, like the AD362SD (which operates over the -55°C to +125°C temperature range) are available processed to MIL-STD-883, Class B. The AD5200 series meets all of the interfacing requirements for direct connection to the AD362 as shown in Figure 8a. System throughput rate is typically 16kHz.

The HAS series of ultra-fast ADCs are 8-bit (HAS0801), 10-bit (HAS1001) and 12-bit (HAS1202) devices that convert in 1.5, 1.7, and 2.8 microseconds (maximum) respectively. These devices are hybrid IC's, packaged in 32-pin DIPs. Since the Data Ready signal from the HAS precedes the LSB decision, $\overline{\text{DR}}$ must be delayed. Figure 8b shows the appropriate circuitry to provide that delay. Throughput rate for the 12-bit system is typically 80kHz.



a. 12-Bit High Accuracy and Reliability DAS Using AD362 and AD5200

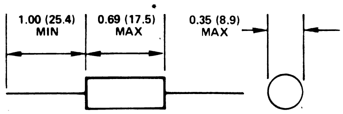
b. High-Speed DAS Using AD362 and HAS

Figure 8. Data Acquisition Systems Based on the AD362 and Purpose ADCs

CAPACITOR OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

HOLD CAPACITOR



*THIS DIMENSION IS FOR POLYSTYRENE CAPACITOR SUPPLIED WITH AD362KD

MAX BODY LENGTH OF TEFLON CAPACITOR SUPPLIED WITH AD362SD IS 1.00".

ANALOG DEVICES

Complete 16-Channel 12-Bit Integrated Circuit Data Acquisition System

AD363

FEATURES

Versatility
- **Complete System in Reliable IC Form**
- **Small Size**
- **16 Single-Ended or 8 Differential Channels with Switchable Mode Control**
- **Military/Aerospace Temperature Range: -55°C to +125°C (AD363S) MIL-STD-883B Processing Available**
- **Versatile Input/Output/Control Format**
- **Short-Cycle Capability**

Performance
- **True 12-Bit Operation: Nonlinearity ⩽±0.012%**
- **Guaranteed No Missing Codes Over Temperature Range**
- **High Throughput Rate: 30kHz**
- **Low Power: 1.7W**

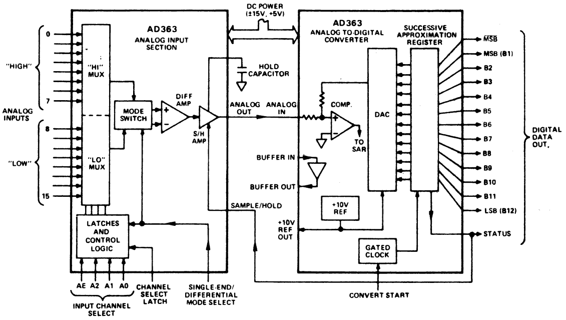
Value
- **Complete: No Additional Parts Required**
- **Reliable: Hybrid IC Construction, Hermetically Sealed. All Inputs Fully Protected**
- **Precision +10.0 ±0.005 Volt Reference for External Application**
- **Fast Precision Buffer Amplifier for External Application**
- **Low Cost**

PRODUCT DESCRIPTION

The AD363 is a complete 16 channel, 12-bit data acquisition system in integrated circuit form. By applying large-scale linear and digital integrated circuitry, thick and thin film hybrid technology and active laser trimming, the AD363 equals or exceeds the performance and versatility of previous modular designs.

The AD363 consists of two separate functional blocks. Each in hermetically-sealed 32 pin dual-in-line packages. The analog input section contains two eight-channel multiplexers, a differential amplifier, a sample-and-hold, a channel address register and control logic. The multiplexers may be connected to the differential amplifier in either an 8-channel differential or 16-channel single-ended configuration. A unique feature of the AD363 is an internal user-controllable analog switch that connects the multiplexers in either a single-ended or differential mode. This allows a single device to perform in either mode without hard-wire programming and permits a mixture of single-ended and differential sources to be interfaced to an AD363 by dynamically switching the input mode control.

AD363 FUNCTIONAL BLOCK DIAGRAM



TWO-32 PIN DIPS

The Analog-to-Digital Converter Section contains a complete 12-bit successive approximation analog-to-digital converter, including internal clock, precision 10 volt reference, comparator, buffer amplifier and a proprietary-design 12-bit D/A converter. Active laser trimming of the reference and D/A converter results in maximum linearity errors of ±0.012% while performing a 12-bit conversion in 25 microseconds.

Analog input voltage ranges of ±2.5, ±5.0, ±10, 0 to +5 and 0 to +10 volts are user-selectable. Adding flexibility and value are the precision 10 volt reference (active-trimmed to a tolerance of ±5mV) and the internal buffer amplifier, both of which may be used for external applications. All digital signals are TTL/DTL compatible and output data is positive-true in parallel and serial form.

System throughput rate is as high as 30kHz at full rated accuracy. The AD363K is specified for operation over a 0 to +70°C temperature range while the AD363S operates to specification from -55°C to +125°C. Processing to MIL-STD-883B is available for the AD363S. Both device grades are guaranteed to have no missing codes over their specified temperature ranges.

SPECIFICATIONS

(typical @ +25°C, ±15V and +5V with 2000pF hold capacitor as provided unless otherwise noted)

MODEL	AD363K	AD363S
ANALOG INPUTS		
Number of Inputs	16 Single-Ended or 8 Differential (Electronically Selectable)	*
Input Voltage Ranges		
Bipolar	±2.5V, ±5.0V, ±10.0V	*
Unipolar	0 to +5V, 0 to +10V	*
Input (Bias) Current, Per Channel	±50nA max	*
Input Impedance		
On Channel	$10^{10}\Omega$, 100pF	*
Off Channel	$10^{10}\Omega$, 10pF	*
Input Fault Current (Power Off or On)	20mA, max, Internally Limited	*
Common Mode Rejection		
Differential Mode	70dB min (80dB typ) @ 1kHz, 20V p-p	*
Mux Crosstalk (Interchannel, Any Off Channel to Any On Channel)	-80dB max (-90dB typ) @ 1kHz, 20V p-p	*
RESOLUTION	12 BITS	*
ACCURACY		
Gain Error[1]	±0.05% FSR (Adj. to Zero)	*
Unipolar Offset Error	±10mV (Adj to Zero)	*
Bipolar Offset Error	±20mV (Adj to Zero)	*
Linearity Error	±½LSB max	*
Differential Linearity Error	±1LSB max (±½LSB typ)	*
Relative Accuracy	±0.025% FSR	*
Noise Error	1mV p-p, 0 to 1MHz	*
TEMPERATURE COEFFICIENTS		
Gain	±30ppm/°C max (±10ppm/°C typ)	±25ppm/°C max (±15ppm/°C typ)
Offset, ±10V Range	±10ppm/°C max (±5ppm/°C typ)	±8ppm/°C max (±5ppm/°C typ)
Differential Linearity	No Missing Codes Over Temperature Range	*
SIGNAL DYNAMICS		
Conversion Time[2]	25μs max (22μs typ)	*
Throughput Rate, Full Rated Accuracy	25kHz min (30kHz typ)	*
Sample and Hold		
Aperture Delay	100ns max (50ns typ)	*
Aperture Uncertainty	500ps max (100ps typ)	*
Acquisition Time		
To ±0.01% of Final Value for Full Scale Step	18μs max (10μs, typ)	*
Feedthrough	-70dB max (-80dB typ) @ 1kHz	*
Droop Rate	2mV/ms max (1mV/ms typ)	*
DIGITAL INPUT SIGNALS[3]		
Convert Command (to ADC Section, Pin 21)	Positive Pulse, 200ns min Width. Leading Edge ("0" to "1") Resets Register, Trailing Edge ("1" to "0") Starts Conversion. 1TTL Load	* *
Input Channel Select (To Analog Input Section, Pins 28-31)	4 Bit Binary, Channel Address. 1LS TTL Load	* *
Channel Select Latch (To Analog Input Section, Pin 32)	"1" Latch Transparent "0" Latched 4LS TTL Loads	* * *

MODEL	AD363K	AD363S
DIGITAL INPUT SIGNALS, cont.		
Sample-Hold Command (To Analog Input Section Pin 13 Normally Connected To ADC "Status", Pin 20)	"0" Sample Mode	*
	"1" Hold Mode	*
	2LS TTL Loads	*
Short Cycle (To ADC Section Pin 14)	Connect to +5V for 12 Bits Resolution.	*
	Connect to Output Bit n + 1 For n Bits Resolution.	*
	1TTL Load	*
Single Ended/Differential Mode Select (To Analog Input Section, Pin 1)	"0": Single-Ended Mode	*
	"1": Differential Mode	*
	3TTL Loads	*
DIGITAL OUTPUT SIGNALS[3] **(All Codes Positive True)**		
Parallel Data		
Unipolar Code	Binary	*
Bipolar Code	Offset Binary/Two's Complement	*
Output Drive	2TTL Loads	*
Serial Data (NRZ Format)		
Unipolar Code	Binary	*
Bipolar Code	Offset Binary	*
Output Drive	2TTL Loads	*
Status ($\overline{\text{Status}}$)	Logic "1" ("0") During Conversion	*
Output Drive	2TTL Loads	*
Internal Clock		
Output Drive	2TTL Loads	*
Frequency	500kHz	*
INTERNAL REFERENCE VOLTAGE	+10.00V, ±10mV	*
Max External Current	±1mA	*
Voltage Temp. Coefficient	±20ppm/°C, max	*
POWER REQUIREMENTS		
Supply Voltages/Currents	+15V, ±5% @ +45mA max (+38mA typ)	*
	-15V, ±5% @ -45mA max (-38mA typ)	*
	+5V, ±5% @ +136mA max (+113mA typ)	*
Total Power Dissipation	2 watts max (1.7 watts typ)	*
TEMPERATURE RANGE		
Specification	0 to +70°C	-55°C to +125°C
Storage	-55°C to +85°C[4]	-55°C to +150°C

NOTES:

[1] With 50Ω, 1% fixed resistor in place of Gain Adjust pot; see Figures 7 and 8.

[2] Conversion time of ADC Section.

[3] One TTL Load is defined as $I_{IL} = -1.6mA$ max @ $V_{IL} = 0.4V$, $I_{IH} = 40\mu A$ max @ $V_{IH} = 2.4V$.
One LS TTL Load is defined as $I_{IL} = -0.36mA$ max @ $V_{IL} = 0.4V$, $I_{IH} = 20\mu A$ max @ $V_{IH} = 2.7V$.

[4] AD363K External Hold Capacitor is limited to +85°C; Analog Input Section and ADC Section may be stored at up to +150°C.

*Specifications same as AD363K.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS
(ALL MODELS)

+V, Digital Supply	+5.5V
+V, Analog Supply	+16V
-V, Analog Supply	-16V
V_{IN}, Signal	±V, Analog Supply
V_{IN}, Digital	0 to +V, Digital Supply
A_{GND} to D_{GND}	±1V

PIN FUNCTION DESCRIPTION

ANALOG INPUT SECTION

Pin Number	Function
1	Single-End/Differential Mode Select "0": Single-Ended Mode "1": Differential Mode
2	Digital Ground
3	Positive Digital Power Supply, +5V
4	"High" Analog Input, Channel 7
5	"High" Analog Input, Channel 6
6	"High" Analog Input, Channel 5
7	"High" Analog Input, Channel 4
8	"High" Analog Input, Channel 3
9	"High" Analog Input, Channel 2
10	"High" Analog Input, Channel 1
11	"High" Analog Input, Channel 0
12	Hold Capacitor (Provided, See Figure 1)
13	Sample-Hold Command "0": Sample Mode "1": Hold Mode Normally Connected to ADC Pin 20
14	Offset Adjust (See Figure 6)
15	Offset Adjust (See Figure 6)
16	Analog Output Normally Connected to ADC "Analog In" (See Figure 1)
17	Analog Ground
18	"High" ("Low") Analog Input, Channel 15 (7)
19	"High" ("Low") Analog Input, Channel 14 (6)
20	Negative Analog Power Supply, -15V
21	Positive Analog Power Supply, +15V
22	"High" ("Low") Analog Input, Channel 13 (5)
23	"High" ("Low") Analog Input, Channel 12 (4)
24	"High" ("Low") Analog Input, Channel 11 (3)
25	"High" ("Low") Analog Input, Channel 10 (2)
26	"High" ("Low") Analog Input, Channel 9 (1)
27	"High" ("Low") Analog Input, Channel 8 (0)
28	Input Channel Select, Address Bit AE
29	Input Channel Select, Address Bit A0
30	Input Channel Select, Address Bit A1
31	Input Channel Select, Address Bit A2
32	Input Channel Select Latch "0": Latched "1": Latch "Transparent"

ANALOG TO DIGITAL CONVERTER SECTION

Pin Number	Function
1	Data Bit 12 (Least Significant Bit) Out
2	Data Bit 11 Out
3	Data Bit 10 Out
4	Data Bit 9 Out
5	Data Bit 8 Out
6	Data Bit 7 Out
7	Data Bit 6 Out
8	Data Bit 5 Out
9	Data Bit 4 Out
10	Data Bit 3 Out
11	Data Bit 2 Out
12	Data Bit 1 (Most Significant Bit) Out
13	$\overline{\text{Data Bit 1}}$ ($\overline{\text{MSB}}$) Out
14	Short Cycle Control Connect to +5V for 12 Bits Connect to Bit (n+1) Out for n Bits
15	Digital Ground
16	Positive Digital Power Supply, +5V
17	$\overline{\text{Status}}$ Out "0": Conversion in Progress (Parallel Data Not Valid) "1": Conversion Complete (Parallel Data Valid)
18	+10Volt Reference Out (See Figures 3, 7, 8, 11)
19	Clock Out (Runs During Conversion)
20	Status Out "0": Conversion Complete (Parallel Data Valid) "1": Conversion in Progress (Parallel Data Not Valid)
21	Convert Start In Reset Logic : ___↑‾‾‾ Start Convert : ‾‾‾↓___
22	Comparator In (See Figures 3, 7, 8)
23	Bipolar Offset Open for Unipolar Inputs Connect to ADC Pin 22 for Bipolar Inputs (See Figure 8)
24	10V Span R In (See Figure 7)
25	20V Span R In (See Figure 8)
26	Analog Ground
27	Gain Adjust (See Figures 7 and 8)
28	Positive Analog Power Supply, +15V
29	Buffer Out (For External Use)
30	Buffer In (For External Use)
31	Negative Analog Power Supply, -15V
32	Serial Data Out Each Bit Valid On Trailing (‾‾↓__) Edge Clock Out, ADC Pin 19

AD363 DESIGN

Concept

The AD363 consists of two separate functional blocks as shown in Figure 1.

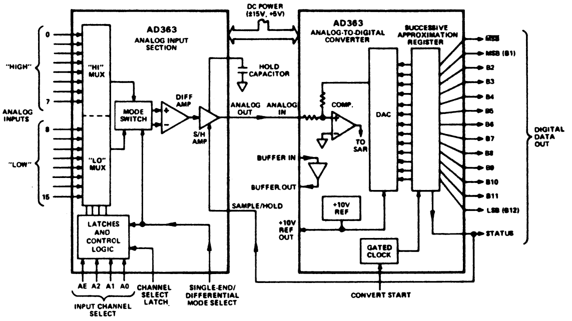


Figure 1. AD363 Functional Block Diagram

The Analog Input Section contains multiplexers, a differential amplifier, a sample-and-hold, a channel address register and control logic. Analog-to-digital conversion is provided by a 12 bit, 25 microsecond "ADC" which is also available separately as the AD572.

By dividing the data acquisition task into two sections, several important advantages are realized. Performance of each design is optimized for its specific function. Production yields are increased thus decreasing costs. Furthermore, the standard configuration 32 pin packages plug into standard sockets and are easier to handle than larger packages with higher pin counts.

Analog Input Section Design

Figure 2 is a block diagram of the AD363 Analog Input Section (AIS).

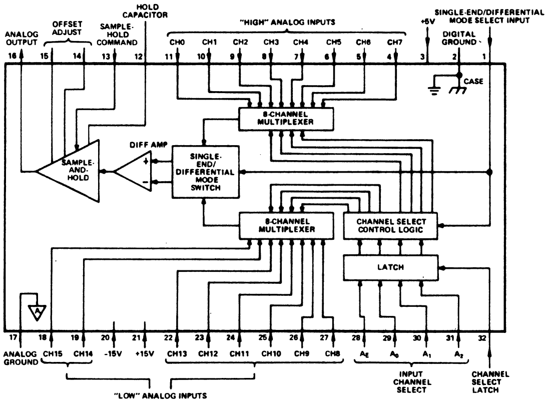


Figure 2. AD363 Analog Input Section Functional Block Diagram and Pinout

The AIS consists of two 8-channel multiplexers, a differential amplifier, a sample-and-hold, channel address latches and control logic. The multiplexers can be connected to the differential amplifier in either an 8-channel differential or 16-channel single-ended configuration. A unique feature of the AD363 is an internal analog switch controlled by a digital input that performs switching between single-ended and differential modes. This feature allows a single product to perform in either mode without external hard-wire interconnections. Of more significance is the ability to serve a mixture of both single-ended and differential sources with a single AD363 by dynamically switching the input mode control.

Multiplexer channel address inputs are interfaced through a level-triggered ("transparent") input register. With a Logic "1" at the Channel Select Latch input, the address signals feed through the register to directly select the appropriate input channel. This address information can be held in the register by placing a Logic "0" on the Channel Select Latch input. Internal logic monitors the status of the Single-Ended/Differential Mode input and addresses the multiplexers accordingly.

A differential amplifier buffers the multiplexer outputs while providing high input impedance in both differential and single-ended modes. Amplifier gain and common mode rejection are actively laser-trimmed.

The sample-and-hold is a high speed monolithic device that can also function as a gated operational amplifier. Its uncommitted differential inputs allow it to serve a second role as the output subtractor in the differential amplifier. This eliminates one amplifier and decreases drift, settling time and power consumption. A Logic "1" on the Sample-and-Hold Command input will cause the sample-and-hold to "freeze" the analog signal while the ADC performs the conversion. Normally the Sample-and-Hold Command is connected to the ADC Status output which is at Logic "1" during conversion and Logic "0" between conversions. For slowly-changing inputs, throughput speed may be increased by grounding the Sample-and-Hold Command input instead of connecting it to the ADC status.

A Polystyrene hold capacitor is provided with each commercial temperature range system (AD363K) while a Teflon capacitor is provided with units intended for operation at temperatures up to 125°C (AD363S). Use of an external capacitor allows the user to make his own speed/accuracy tradeoff; a smaller capacitor will allow faster sample-and-hold response but will decrease accuracy while a larger capacitor will increase accuracy at slower conversion rates.

The Analog Input Section is constructed on a substrate that includes thick-film resistors for non-critical applications such as input protection and biasing. A separately-mounted laser-trimmed thin-film resistor network is used to establish accurate gain and high common-mode rejection.

Analog-to-Digital Converter Design

Figure 3 is a block diagram of the Analog-to-Digital Converter Section (ADC) of the AD363.

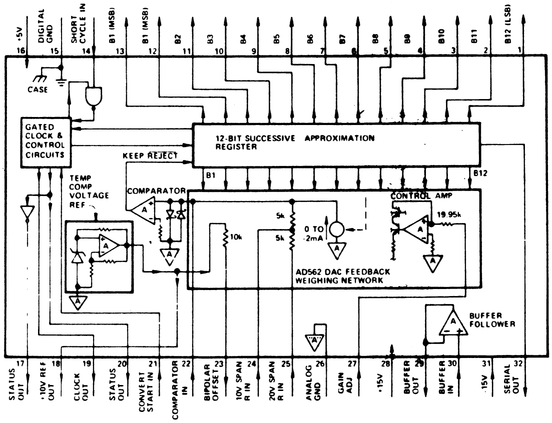


Figure 3. AD363 ADC Section (AD572) Functional Diagram and Pinout

Available separately as the AD572, the ADC is a 12-bit, 25 microsecond device that includes an internal clock, reference, comparator and buffer amplifier.

The +10V reference is derived from a low T.C. zener reference diode which has its zener voltage amplified and buffered by an op amp. The reference voltage is calibrated to +10V, ±10mV by active laser-trimming of the thin-film resistors which determine the closed-loop gain of the op amp. 1mA of current is available for external use.

The DAC chip uses 12 precision, high speed bipolar current steering switches, control amplifier and a laser-trimmed thin film resistor network to produce a very fast, high accuracy analog output current. This ladder network is active laser-trimmed to calibrate all bit ratio scale factors to a precision of 0.005% of FSR (full-scale range) to guarantee no missing codes over the operating temperature range. The design of the ADC includes scaling resistors that provide user-selectable analog input signal ranges of ±2.5, ±5, ±10, 0 to +5, or 0 to +10 volts.

Other useful features include true binary output for unipolar inputs, offset binary and two's complement output for bipolar inputs, serial output, short-cycle capability for lower resolution, higher speed measurements, and an available high input impedance buffer amplifier which may be used elsewhere in the system.

THEORY OF OPERATION

System Timing

Figure 4 is a timing diagram for the AD363 connected as shown shown in Figure 1 and operating at maximum conversion rate.

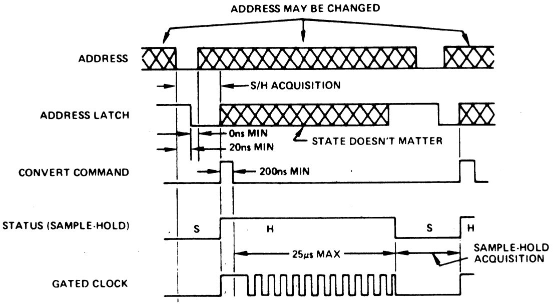


Figure 4. AD363 Timing Diagram

The normal sequence of events is as follows:

1. The appropriate Channel Select Address is latched into the address register. Time is allowed for the multiplexers to settle.
2. A Convert Start command is issued to the ADC which indicates that it is "busy" by placing a Logic "1" on its Status line.
3. The ADC Status controls the sample-and-hold. When the ADC is "busy" the sample-and-hold is in the hold mode.
4. The ADC goes into its 25 microsecond conversion routine. Since the sample-and-hold is holding the proper analog value, the address may be updated during conversion. Thus multiplexer settling time can coincide with conversion and need not effect throughput rate.
5. The ADC indicates completion of its conversion by returning Status to Logic "0". The sample-and-hold returns to the sample mode.
6. If the input signal has changed full-scale (different channels may have widely-varying data) the sample-and-hold will typically require 10 microseconds to "acquire" the next input to sufficient accuracy for 12-bit conversion.

After allowing a suitable interval for the sample-and-hold to stabilize at its new value, another Convert Start command may be issued to the ADC.

ADC Operation

On receipt of a Convert Start command, the analog-to-digital converter converts the voltage at its analog input into an equivalent 12-bit binary number. This conversion is accomplished as follows:

The 12-bit successive-approximation register (SAR) has its 12-bit outputs connected both to the respective device bit output pins and to the corresponding bit inputs of the feedback DAC.

The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

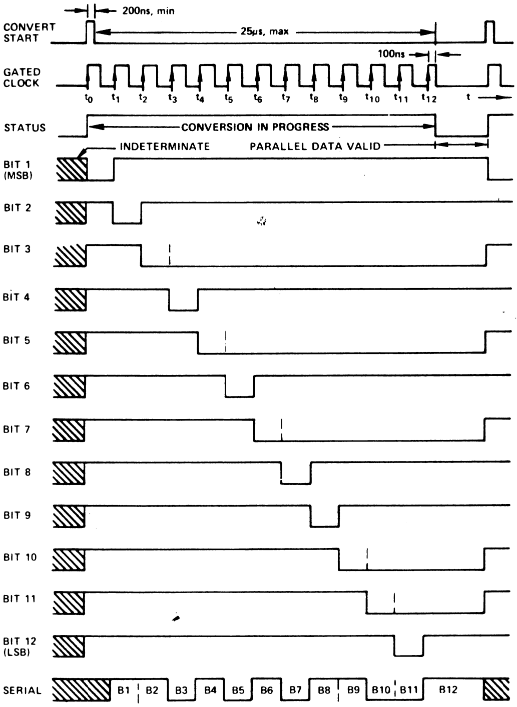


Figure 5. ADC Timing Diagram (Binary Code 110101011001)

The timing diagram is shown in Figure 5. Receipt of a Convert Start signal sets the Status flag, indicating conversion in progress. This, in turn, removes the inhibit applied to the gated clock, permitting it to run through 13 cycles. All SAR parallel bit and Status flip-flops are initialized on the leading edge, and the gated clock inhibit signal removed on the trailing edge of the Convert Start signal. At time t0, B1 is reset and B2-B12 are set unconditionally. At t1 the Bit 1 decision is made (keep) and Bit 2 is unconditionally reset. At t2, the Bit 2 decision is made (keep) and Bit 3 is reset unconditionally. This sequence continues until the Bit 12 (LSB) decision (keep) is made at t12. After 100ns delay period, the Status flag is reset, indicating that the conversion is complete and that the parallel output data is valid. Resetting the Status flag restores the gated clock inhibit signal, forcing the clock output to the Logic "0" state.

Corresponding serial and parallel data bits become valid on the same positive-going clock edge. Serial data does not change and is guaranteed valid on negative-going clock edges, however; serial data can be transferred quite simply by clocking it into a receiving shift register on these edges.

Incorporation of the 100ns delay period guarantees that the parallel (and serial) data are valid at the Logic "1" to "0" transition of the Status flag, permitting parallel data transfer to be initiated by the trailing edge of the Status signal.

The versatility and completeness of the AD363 concept results in a large number of user-selectable configurations. This allows optimization of most systems applications.

Single-Ended/Differential Mode Control

The 363 features an internal analog switch that configures the Analog Input Section in either a 16-channel single-ended or 8-channel differential mode. This switch is controlled by a TTL logic input applied to pin 1 of the Analog Input Section:

"0": Single-Ended (16 channels)
"1": Differential (8 channels)

When in the differential mode, a differential source may be applied between corresponding "High" and "Low" analog input channels.

It is possible to mix SE and DIFF inputs by using the mode control to command the appropriate mode. Figure 11 illustrates an example of a "mixed" application. In this case, four microseconds must be allowed for the output of the Analog Input Section to settle to within ±0.01% of its final value, but if the mode is switched concurrent with changing the channel address, no significant additional delay is introduced. The effect of this delay may be eliminated by changing modes while a conversion is in progress (with the sample-and-hold in the "hold mode"). When SE and DIFF signals are being processed concurrently, the DIFF signals must be applied between corresponding "High" and "Low" analog input channels. Another application of this feature is the capability of measuring 16 sources individually and/or measuring differences between pairs of those sources.

Input Channel Addressing

Table 1 is the truth table for input channel addressing in both the single-ended and differential modes. The 16 single-ended channels may be addressed by applying the corresponding digital number to the four Input Channel Select address bits, AE, A0, A1, A2 (Analog Input Section, pins 28–31). In the differential mode, the eight channels are addressed by applying the appropriate digital code to A0, A1 and A2; AE must be enabled with a Logic "1". Internal logic monitors the status of the SE/DIFF Mode input and addresses the multiplexes singly or in pairs as required.

ADDRESS				ON CHANNEL (Pin Number)		
					Differential	
AE	A2	A1	A0	Single Ended	"Hi"	"Lo"
0	0	0	0	0 (11)	None	
0	0	0	1	1 (10)	None	
0	0	1	0	2 (9)	None	
0	0	1	1	3 (8)	None	
0	1	0	0	4 (7)	None	
0	1	0	1	5 (6)	None	
0	1	1	0	6 (5)	None	
0	1	1	1	7 (4)	None	
1	0	0	0	8 (27)	0 (11)	0 (27)
1	0	0	1	9 (26)	1 (10)	1 (26)
1	0	1	0	10 (25)	2 (9)	2 (25)
1	0	1	1	11 (24)	3 (8)	3 (24)
1	1	0	0	12 (23)	4 (7)	5 (23)
1	1	0	1	13 (22)	5 (6)	5 (22)
1	1	1	0	14 (19)	6 (5)	6 (19)
1	1	1	1	15 (18)	7 (4)	7 (18)

Table 1. Input Channel Addressing Truth Table

When the channel address is changed, six microseconds must be allowed for the Analog Input Section to settle to within ±0.01% of its final output (including settling times of all elements in the signal path). The effect of this delay may be eliminated by performing the address change while a conversion is in progress (with the sample-and-hold in the "hold" mode).

Input Channel Address Latch

The AD363 is equipped with a latch for the Input Channel Select address bits. If the Latch Control pin (pin 32 of the Analog Input Section) is at Logic "1", input channel select address information is passed through to the multiplexers. A Logic "0" "freezes" the input channel address present at the inputs at the time of the "1" to "0" transition.

This feature is useful when input channel address information is provided from an address, data or control bus that may be required to service many devices. The ability to latch an address is helpful whenever the user has no control of when address information may change.

Sample-and-Hold Mode Control

The Sample-and-Hold Mode Control input (Analog Input Section, pin 13) is normally connected to the Status output (pin 20) from the ADC section. When a conversion is initiated by applying a Convert Start command to the ADC (pin 21), Status goes to Logic "1", putting the sample-and-hold into the "hold" mode. This "freezes" the information to be digitized for the period of conversion. When the conversion is complete, Status returns to Logic "0" and the sample-and-hold returns to the sample mode. Eighteen microseconds must be allowed for the sample-and-hold to acquire ("catch up" to) the analog input to within ±0.01% of the final value before a new Convert Start command is issued.

The purpose of a sample-and-hold is to "stop" fast changing input signals long enough to be converted. In this application, it also allows the user to change channels and/or SE/ DIFF mode while a conversion is in progress thus eliminating the effects of multiplexer, analog switch and differential amplifier settling times. If maximum throughput rate is required for slowly changing signals, the Sample-and-Hold Mode Control may be wired to ground (Logic "0") rather than to ADC Status thus leaving the sample-and-hold in a continuous sample mode.

Hold Capacitor

A 2000pF capacitor is provided with each AD363. One side of this capacitor is wired to the Analog Input Section pin 12, the other to analog ground as close to pin 17 as possible. The capacitor provided with the AD363K is Polystyrene while the wider operating temperature range of the AD363S demands a Teflon capacitor (supplied).

Larger capacitors may be substituted to minimize noise, but acquisition time of the sample-and-hold will be extended. If less than 12 bits of accuracy is required, a smaller capacitor may be used. This will shorten the S/H acquisition time. In all cases, the proper capacitor dielectric must be used; i.e., Polystyrene (AD363K only) or Teflon (AD363K or S). Other types of capacitors may have higher dielectric absorption (memory) and will cause errors. CAUTION: Polystyrene capacitors will be destroyed if subjected to temperatures above +85°C. No capacitor is required if the sample-and-hold is not used.

Short Cycle Control

A Short Cycle Control (ADC Section, pin 14) permits the timing cycle shown in Figure 5 to be terminated after any number of desired bits has been converted, permitting somewhat shorter conversion times in applications not requiring full 12-bit resolution. When 12-bit resolution is required, pin 14 is connected to +5V (ADC Section, pin 10). When 10-bit resolution is desired, pin 14 is connected to Bit 11 output pin 2. The conversion cycle then terminates, and the Status flag resets after the Bit 10 decision (t10 + 100ns in timing diagram of Figure 2). Short Cycle pin connections and associated maximum 12-, 10- and 8-bit conversion times are summarized in Table 2.

Connect Short Cycle Pin 14 to Pin:	Bits	Resolution (% FSR)	Maximum Conversion Time (µs)	Status Flag Reset at: (Figure 5)
16	12	0.024	25	t_{12} +100ns
2	10	0.10	21	t_{10} +100ns
4	8	0.39	17	t_8 +100ns

Table 2. Short Cycle Connections

One should note that the calibration voltages listed in Table 4 are for 12-bit resolution only, and are not those corresponding to the center of each discrete quantization interval at reduced bit resolution.

Digital Output Data Format

Both parallel and serial data are in positive-true form and outputted from TTL storage registers. Parallel data output coding is binary for unipolar ranges and either offset binary or two's complement binary, depending on whether Bit 1 (ADC Section pin 12) or its logical inverse $\overline{\text{Bit}}$ 1 (pin 13) is used as the MSB. Parallel data becomes valid approximately 200ns before the Status flag returns to Logic "0", permitting parallel data transfer to be clocked on the "1" to "0" transition of the Status flag.

Serial data coding is binary for unipolar input ranges and offset binary for bipolar input ranges. Serial output is by bit (MSB first, LSB last) in NRZ (non-return-to-zero) format. Serial and parallel data outputs change state on positive-going clock edges. Serial data is guaranteed valid on all negative-going clock edges, permitting serial data to be clocked directly into a receiving register on these edges. There are 13 negative-going clock edges in the complete 12-bit conversion cycle, as shown in Figure 5. The first edge shifts an invalid bit into the register, which is shifted out on the 13th negative-going clock edge. All serial data bits will have been correctly transferred at the completion of the conversion period.

Analog Input Voltage Range Format

The AD363 may be configured for any of 3 bipolar or 2 unipolar input voltage ranges as shown in Table 3.

Range	Connect Analog Input To ADC Pin:	Connect ADC Span Pin:	Connect Bipolar ADC Pin 23 To:
0 to +5V	24	25 to 22	——
0 to +10V	24	——	
-2.5V to +2.5V	24	25 to 22	22
-5V to +5V	24	——	
-10V to +10V	25	——	

Table 3. Analog Input Voltage Range Pin Connections

Analog Input - Volts (Center of Quantization Interval)			Input Normalized to FSR		Digital Output Code (Binary for Unipolar Ranges; Offset Binary for Bipolar Ranges)
0 to +10V Range	-5V to +5V Range	-10V to +10V Range	Unipolar Ranges	Bipolar Ranges	B1 (MSB) B12 (LSB)
+9.9976	+4.9976	+9.9951	+FSR-1 LSB	+½FSR-1 LSB	1 1 1 1 1 1 1 1 1 1 1 1
+9.9952	+4.9952	+9.9902	+FSR-2 LSB	+½FSR-2 LSB	1 1 1 1 1 1 1 1 1 1 1 0
⋮	⋮	⋮	⋮	⋮	⋮
+5.0024	+0.0024	+0.0049	+½FSR+1 LSB	+1 LSB	1 0 0 0 0 0 0 0 0 0 0 1
+5.0000	+0.0000	+0.0000	+½FSR	ZERO	1 0 0 0 0 0 0 0 0 0 0 0
⋮	⋮	⋮	⋮	⋮	⋮
+0.0024	-4.9976	-9.9951	+1 LSB	-½FSR+1 LSB	0 0 0 0 0 0 0 0 0 0 0 1
+0.0000	-5.0000	-10.0000	ZERO	-½FSR	0 0 0 0 0 0 0 0 0 0 0 0

Table 4. Digital Output Codes vs Analog Input For Unipolar and Bipolar Ranges

The resulting input-output transfer functions are given by Table 4.

Analog Input Section Offset Adjust Circuit

The offset voltage of the AD363 may be adjusted at either the Analog Input Section or the ADC Section. Normally the adjustment is performed at the ADC but in some special applications, it may be helpful to adjust the offset of the Analog Input Section. An example of such a case would be if the input signals were small (<10mV) relative to Analog Input Section voltage offset and gain was inserted between the Analog Input Section and the ADC. To adjust the offset of the Analog Input Section, the circuit shown in Figure 6 is recommended.

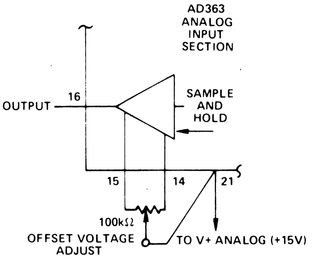
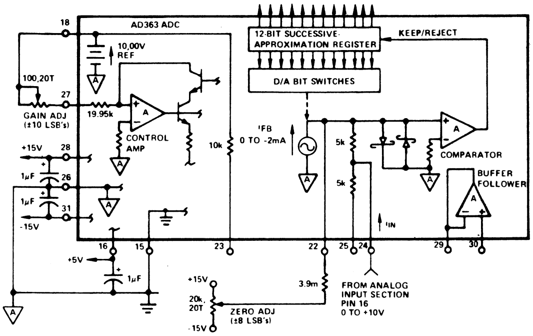


Figure 6. Analog Input Section Offset Voltage Adjustment

Under normal conditions, all calibration is performed at the ADC Section.

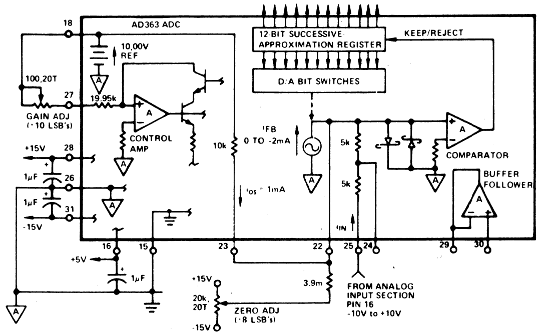
ADC Offset Adjust Circuit

Analog and power connections for 0 to +10V unipolar and -10V to +10V bipolar input ranges are shown in Figures 7 and 8, respectively. The Bipolar Offset, ADC pin 23 is open-circuited for all unipolar input ranges, and connected to Comparator input (ADC pin 22) for all bipolar input ranges. The zero adjust circuit consists of a potentiometer connected across $\pm V_S$ with its slider connected through a 3.9MΩ resistor to Comparator input (ADC pin 22) for all ranges. The tolerance of this fixed resistor is not critical, and a carbon composition type is generally adequate. Using a carbon composition resistor having a -1200ppm/°C tempco contributes a worst-case offset tempco of $8 \times 244 \times 10^{-6} \times 1200\text{ppm}/^\circ\text{C} = 2.3\text{ppm}/^\circ\text{C}$ of FSR, if the OFFSET ADJ potentiometer is set at either end of its adjustment range. Since the maximum offset adjustment required is typically no more than ±4LSB, use of a carbon composition offset summing resistor normally contributes no more than 1ppm/°C of FSR offset tempco.



NOTE: ANALOG (A) AND DIGITAL (⏚) GNDS ARE NOT TIED INTERNALLY AND MUST BE CONNECTED EXTERNALLY.

Figure 7. ADC Analog and Power Connections for Unipolar 0 to +10V Input Range



NOTE: ANALOG (A) AND DIGITAL (⏚) GNDS ARE NOT TIED INTERNALLY AND MUST BE CONNECTED EXTERNALLY.

Figure 8. ADC Analog and Power Connections for Bipolar -10V to +10V Input Range

An alternate offset adjust circuit, which contributes negligible offset tempco if metal film resistors (tempco <100 ppm/°C) are used, is shown in Figure 9.

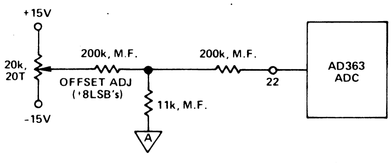


Figure 9. Low Tempco Zero Adj Circuit

In either zero adjust circuit, the fixed resistor connected to ADC pin 22 should be located close to this pin to keep the connection runs short, since the Comparator input (ADC pin 22) is quite sensitive to external noise pick-up.

Gain Adjust

The gain adjust circuit consists of a 100Ω potentiometer connected between +10V Reference Output pin 18 and Gain Adjust Input (ADC pin 27) for all ranges. Both GAIN and ZERO ADJ potentiometers should be multi-turn, low tempco types; 20T cermet (tempco = 100ppm/°C max) types are recommended. If the 100Ω GAIN ADJ potentiometer is replaced by a fixed 50Ω resistor, absolute gain calibration to ±0.1% of FSR is guaranteed.

Calibration

Calibration of the AD363 consists of adjusting offset and gain. Relative accuracy (linearity) is not affected by these adjustments, so if absolute zero and gain error is not important in a given application, or if system intelligence can correct for such errors, calibration may be unnecessary.

External ZERO ADJ and GAIN ADJ potentiometers, connected as shown in Figures 7, 8, and 9, are used for device calibration. To prevent interaction of these two adjustments, Zero is always adjusted first and then Gain. Zero is adjusted with the analog input near the most negative end of the analog range (0 for unipolar and -½FSR for bipolar input ranges). Gain is adjusted with the analog input near the most positive end of the analog range.

0 to +10V Range: Set analog input to +1LSB = +0.0024V. Adjust Zero for digital output = 000000000001; Zero is now calibrated. Set analog input to +FSR -2LSB = +9.9952V. Adjust Gain for 111111111110 digital output code; full-scale (Gain) is now calibrated. Half-scale calibration check: set analog input to +5.0000V; digital output code should be 100000000000.

-10V to +10V Range: Set analog input to -9.9951V; adjust Zero for 000000000001 digital output (offset binary) code. Set analog input to +9.9902V; adjust Gain for 111111111110 digital output (offset binary) code. Half-scale calibration check: set analog input to 0.0000V; digital output (offset binary) code should be 100000000000.

Other Ranges: Representative digital coding for 0 to +10V, -5V to +5V, and -10V to +10V ranges is shown in Table 4. Coding relationships are calibration points for 0 to +5V and -2.5V to +2.5V ranges can be found by halving the corresponding code equivalents listed for the 0 to +10V and -5V to +5V ranges, respectively.

Zero and full-scale calibration can be accomplished to a precision of approximately ±¼LSB using the static adjustment procedure described above. By summing a small sine or triangular-wave voltage with the signal applied to the analog input, the output can be cycled through each of the calibration codes of interest to more accurately determine the center (or end points) of each discrete quantization level. A detailed description of this dynamic calibration technique is presented in "A/D Conversion Notes", D. Sheingold, Analog Devices, Inc., 1977, Part II, Chapter II-4.

Other Considerations

Grounding: Analog and digital signal grounds should be kept separate where possible to prevent digital signals from flowing in the analog ground circuit and inducing spurious analog signal noise. Analog Ground (Analog Input Section pin 17, ADC Section pin 26) and Digital Ground (Analog Input Section pin 2 and ADC Section pin 15) are not connected internally; these pins must be connected externally for the system to operate properly. Preferably, this connection is made at only one point, as close to the system as possible. The cases are connected internally to Digital Ground to provide good electrostatic shielding. If the grounds are not tied common on the same card with both system packages, the digital and analog grounds should be connected locally with back-to-back general-purpose diodes as shown in Figure 10. This will protect the AD363 from possible damage caused by voltages in excess of ±1 volt between the ground systems which could occur if the key grounding card should be removed from the overall system. The system will operate properly with as much as ±200mV between grounds, however this difference will be reflected directly as an input offset voltage.

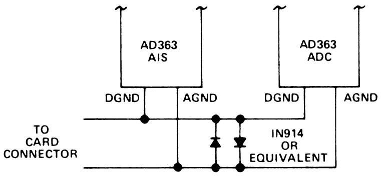


Figure 10. Ground-Fault Protection Diodes

Power Supply Bypassing: The ±15V and +5V power leads should be capacitively bypassed to Analog Ground and Digital Ground respectively for optimum device performance. 1μF tantalum types are recommended; these capacitors should be located close to the system. It is not necessary to shunt these capacitors with disc capacitors to provide additional high frequency power supply decoupling since each power lead is bypassed internally with a 0.039μF ceramic capacitor.

Applications

The AD363 contains several unique features that contribute to its application versatility. The more significant features include a precision +10V reference, an uncommitted buffer amplifier, the dynamic single-ended/differential mode switch and simple, uncommitted digital interfaces.

Transducer Interfacing

The precision +10V reference, buffer amplifier and mode switch can simplify transducer interfacing. Figure 11 illustrates how these features may be used to advantage.

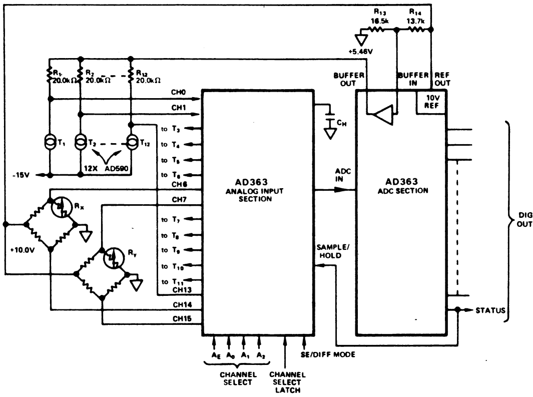


Figure 11. AD363 Transducer Interface Application

The AD590 is a temperature transducer that can be considered an ideal two-terminal current source with an output of one microamp per degree Kelvin ($1\mu A/^\circ K$). With an offsetting current of $273\mu A$ sourced from the +5.46 volt buffered reference through $20k\Omega$ resistors (R1-R12) each of the 12 AD590 circuits develop $-20mV/^\circ C$. The outputs are monitored with the AD363 front-end in the single-ended mode (Logic "0" on the Mode Control input). The +5.46 volt reference is derived from the ADC +10 volt precision reference and voltage divider R13, R14. Low output impedance for this +5.46 volt reference is provided by the ADC internal buffer amplifier. (The $10\mu V/^\circ C$ offset voltage drift of the buffer amplifier contributes negligible errors.) At $0^\circ C$, each temperature transducer circuit delivers a 0 volt output. At $125^\circ C$, the output is -2.5V; at $-55^\circ C$, the output is +1.10V. By using the two's complement ADC output (complemented MSB or sign bit), the negative voltage versus temperature function is inverted and digital reading proportional to temperature in degrees centigrade is provided. Resolution is $0.061^\circ C$ per least significant bit.

The precision +10 volt reference is also used to power several bridge circuits that require differential read-out. When addressing these bridge transducers, a Logic "1" at the mode control input will switch the AD363 to the differential mode. In many cases, this feature will eliminate the requirement for a differential amplifier for each bridge transducer.

Microprocessor Interfacing

Digital interfacing to the AD363 has been deliberately left uncommitted; every processor system and application has different interface requirements and designing for one specific processor could complicate other applications.

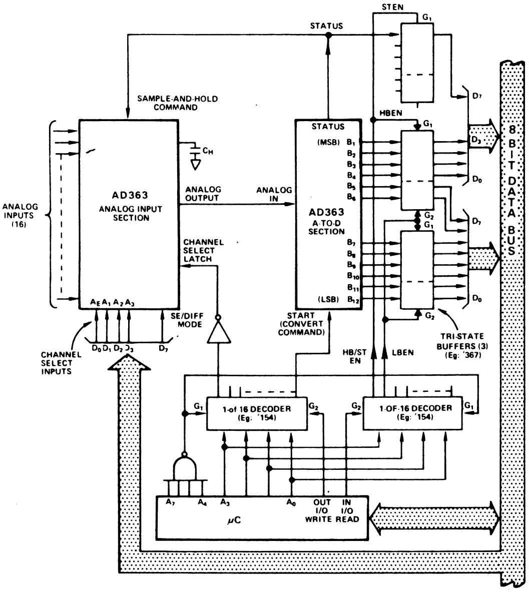


Figure 12. AD363 Microprocessor Interface Application

The addition of a small amount of hardware will satisfy most interface requirements; an example based on 8080-type architecture is shown in Figure 12.

In this system the data bus is used to transmit multiplexer channel selection and convert and read commands to the AD363. It is also possible to address the AD363 as memory using the address bus to perform channel selection, convert and read operations.

The address lines can be decoded to provide channel selection, ADC convert start, status and ADC data (2 bytes) locations. These are accessed with I/O read/write instructions.

The ADC outputs are buffered with tri-state drivers. Figure 12 shows the 4 most significant ADC data bits and status as one byte

FF_H:	STATUS	—	—	—	B1 (MSB)	B2	B3	B4
	D7							D0

and the 8 least significant ADC data bits as the second byte.

FE_H:	B5	B6	B7	B8	B9	B10	B11	B12 (LSB)
	D7							D0

Internal tri-state buffering is not provided because in many applications it would be better to have the first byte contain the 8 most significant bits. To accomodate both left and right justified formats would require more package pins and increase complexity.

The operating sequence for this system is as follows:

1	MVI	80_H	puts the address for channel 0 (including SE/DIFF mode) into accumulator
2	OUT	FF_H	puts 80_H on data bus and FF_H on address bus. Pulses I/O WRITE. OUT FF_H is decoded as a "LOAD ADDRESS" command to the channel select latches.
3	OUT	FO_H	puts FO_H on address bus and pulses I/O WRITE. This is decoded to issue a "CONVERSION START" to the ADC. Accumulator contents are of no significance.
4	IN	FF_H	puts FF_H on address bus and pulses I/O READ. This is decoded to enable the appropriate tri-states, thus putting status and the 4 most significant bits on the data bus.

The status may be examined for "0" (conversion complete). In that case, the 4 MSB's would be read.

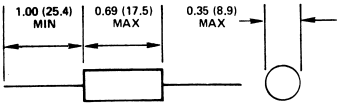
5	IN	FE_H	puts FE_H on address bus and pulses I/O READ. This is decoded to enable the appropriate tri-states, thus putting the 8 least significant bits on the data bus.

At this point, the multiplexer channel selection may be changed and another channel processed with the same instruction set (steps 2 through 5).

CAPACITOR OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

HOLD CAPACITOR



*THIS DIMENSION IS FOR POLYSTYRENE CAPACITOR SUPPLIED WITH K GRADE.

MAX BODY LENGTH OF TEFLON CAPACITOR SUPPLIED WITH S GRADE IS 1.00"

AD363 ORDERING GUIDE

					Package Styles[1]	
Model	Specification Temp Range	Max Gain T.C.	Max Reference T.C.	Guaranteed Temp Range No Missing Codes	Analog Input Section	ADC Section
AD363KD	0 to +70°C	±30ppm/°C	±20ppm/°C	0 to +70°C	HY32D	HY32G
AD363SD	-55°C to +125°C	±25ppm/°C	±20ppm/°C	-55°C to +125°C	HY32D	HY32G
AD363SD/ 883B		Meets all AD363SD specifications after processing to the requirements of MIL-STD-883B, Method 5008.				

NOTE: D Suffix = Dual-In-Line package designator.

[1] See Section 20 for package outline information.

ANALOG DEVICES Fast, Complete, 16-Channel µP Compatible 12-Bit Data Acquisition System

AD364

ADVANCED TECHNICAL DATA

FEATURES

Complete Data Acquisition System in 2-Package IC Form
Full 8- or 16-Bit Microprocessor Bus Interface
16 Single-Ended or 8 Differential Channels with Switchable Mode Control
True 12-Bit Operation: Nonlinearity ⩽±0.012%
Guaranteed No Missing Codes Over Specified Temperature Range
High Throughput Rate: 20kHz
Fast Successive Approximation Conversion: 25µs
Buried Zener Reference for Long-Term Stability and Low Gain TC
Small Size: Requires Only 2.8 Square Inches
Short-Cycle Capability
Low Power: 1.4 Watts
Military/Aerospace Temperature Range: -55°C to +125°C
MIL-STD-883 Class B Processing Available

PRODUCT DESCRIPTION

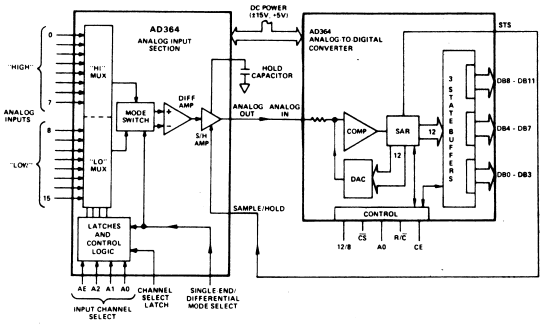
The AD364 is a complete 16 channel, microprocessor compatible, 12-bit data acquisition system in integrated circuit form. The AD364 design is implemented with linear compatible LSI chips, active laser trimming and hybrid technology resulting in maximum performance and flexibility.

The AD364 consists of two separate functional blocks, each in a hermetically sealed dual-in-line package. The analog input section contains two eight-channel multiplexers, a differential amplifier, a sample-and-hold, a channel address register and control logic. The multiplexers may be connected to the differential amplifier in either an 8-channel differential or 16-channel single-ended configuration. A unique feature of the AD364 is an internal user-controllable analog switch that connects the multiplexers in either a single-ended or differential mode. This allows a single device to perform in either mode without hard-wire programming and permits a mixture of single-ended and differential sources to be interfaced to an AD364 by dynamically switching the input mode control.

The ADC section contains a complete 12-bit successive approximation ADC, including internal clock, precision 10 volt reference, comparator and bus interface. The ADC uses the newly-developed LCI (Linear-Compatible Integrated Injection Logic) process to provide the low power logic necessary to make a high speed 12-bit ADC and 3-state output buffer circuitry for direct interface to an 8-, 12- or 16-bit microprocessor bus.

The AD364 is available in 4 different grades. The AD364J and K grades are specified for operation over the 0 to +70°C temperature range. The AD364S, T are specified for the -55°C to +125°C range.

AD364 FUNCTIONAL BLOCK DIAGRAM



TWO DUAL IN-LINE PACKAGES

PRODUCT HIGHLIGHTS

1. The precision laser-trimmed scaling and bipolar offset resistors provide three calibrated ranges; 0 to +10 volts unipolar, or -5 to +5 and -10 to +10 volts bipolar. Typical bipolar offset and full scale calibration errors of ±0.05% can be trimmed to zero each with one external component.

2. The internal buried zener reference is trimmed to 10.00 volts with a ±1% maximum error and 15ppm/°C typical TC. The reference is available externally and can drive up to 1.5mA beyond that required for the reference and bipolar offset resistors.

3. The AD364 interfaces to most popular microprocessors with an 8-, 12-, or 16-bit bus without external buffers or peripheral interface controllers. Multiple-mode three-state output buffers connect directly to the data bus while the read and convert commands are taken from the control bus. The 12 bits of output data can be read either as one 12-bit word or as two 8-bit bytes (one with 8 data bits, the other with 4 data bits and 4 trailing zeros).

SPECIFICATIONS

(typical @ +25°C, ±15V and +5V with 2000pF hold capacitor as provided unless otherwise noted)

PARAMETER	AD364J	AD364K	AD364S	AD364T	UNITS
ANALOG INPUTS					
Number of Inputs	16 Single-Ended or 8 Differential (Electronically Selectable)				
Input Voltage Range					
T_{min} to T_{max}	±10	*	*	*	V
Input (Bias) Current per Channel	±50	*	*	*	nA max
Input Impedance ON Channel	10^{10}/100	*	*	*	Ω/pF
OFF Channel	10^{10}/10	*	*	*	Ω/pF
Input Fault Current	20	*	*	*	mA max
(Power ON or OFF)					(Internally
Common Mode Rejection					Limited)
Differential Mode 1kHz 20Vp-p	70 min (80 typ)	*	*	*	dB
Mux Cross Talk (Any OFF Channel to Any ON Channel) 1kHz 20V p-p	-80 max (-90 typ)	*	*	*	dB
Offset, Channel to Channel	±5	*	*	*	mV max
ACCURACY					
Gain Error[1]	0.3	*	*	*	% of FSR
Unipolar Offset Error[2]	±10	±8	*	**	mV
Bipolar Offset Error[2]	±50	±20	*	**	mV
Linearity Error	0.024	0.012	*	**	% of FSR max
T_{min} to T_{max}	0.024	0.012	*	*	% of FSR max
Differential Linearity Error	0.024	0.012	*	**	% of FSR max
T_{min} to T_{max}	0.024	0.012	*	*	% of FSR max
Noise Error	1mV p-p 0.1Hz to 1MHz	*	*	*	
TEMPERATURE COEFFICIENTS					
Gain	54	31	*	**	ppm/°C
Offset (±10V Range)	12	7	*	**	ppm/°C
Operating Temperature Range	0 to +70°C	*	−55°C to +125°C	***	ppm/°C
SIGNAL DYNAMICS					
Conversion Time	32 max (25 typ)	*	*	*	μs
Throughput Rate, Full Accuracy	20 min (25 typ)	*	*	*	kHz
Sample Hold					
Aperture Delay	100 max (50 typ)	*	*	*	ns
Aperture Uncertainty	500 max (100 typ)	*	*	*	ps
Acquisition Time To 0.01% of Final Value For Full Scale Step	18 max (10 typ)	*	*	*	μs
Feedthrough at 1kHz	-70 max (-80 typ)	*	*	*	dB
Droop Rate	2 max (1 typ)	*	*	*	mV/ms
DIGITAL INPUT SIGNALS					
Analog Input Section					
Input Channel Select	4 Bit Binary Address	*	*	*	
	1 LS TTL Load	*	*	*	
Channel Select Latch	"1" Latch Transparent	*	*	*	
	"0" Latched	*	*	*	
	4 LS TTL Loads	*	*	*	
Single Ended/Differential	"0" Single Ended	*	*	*	
Mode Select	"1" Differential	*	*	*	
	3TTL Loads	*	*	*	
Sample and Hold Command	"0" Sample Mode	*	*	*	
	"1" Hold Mode	*	*	*	
	1TTL Load	*	*	*	
ADC Section[3] $4.5 \leqslant V_L \leqslant 5.5$					
Logic Input Threshold					
T_{min} to T_{max}					
Logic "1"	2.0	*	*	*	V min
Logic "0"	0.8	*	*	*	V max
Logic Input Current					
T_{min} to T_{max}					
Logic "1"	10	*	*	*	μA max
Logic "0"	10	*	*	*	μA max

PARAMETER	AD364J	AD364K	AD364S	AD364T	UNITS
DIGITAL OUTPUT SIGNALS					
Logic Outputs T_{min} to T_{max}					
Sink Current $V_{OUT} = 0.4V$	1.6	*	*	*	mA min
Source Current $V_{OUT} = 2.4V$	0.5	*	*	*	mA min
Output Leakage When In Three State	±40	*	*	*	µA max
Output Coding					
Unipolar	Positive True Binary	*	*	*	
Bipolar	Positive True Offset Binary	*	*	*	
POWER REQUIREMENTS					
Supply Voltages/Currents	+15V, ±5% @ 36mA max	*	*	*	
	-15V, ±5% @ 65mA max	*	*	*	
	+5V, ±5% @ 75mA max	*	*	*	

[1] With 50Ω resistor from REF IN to REF OUT. Adjustable to zero.
[2] Adjustable to zero.
[3] 12/$\overline{8}$ line must be hard wired to V_{LOGIC} or digital common.
*Specifications same as AD364J.
**Specifications same as AD364K.
***Specifications same as AD364S.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS (ALL MODELS)

+V, Digital Supply	+5.5V
+V, Analog Supply	+16V
-V, Analog Supply	-16V
V_{IN}, Signal	±V, Analog Supply
V_{IN}, Digital	0 to +V, Digital Supply
A_{GND} to D_{GND}	±1V

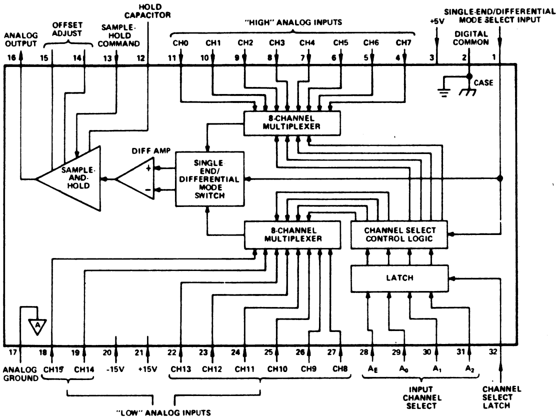


Figure 1. AD364 Analog Input Section Functional Block Diagram and Pinout

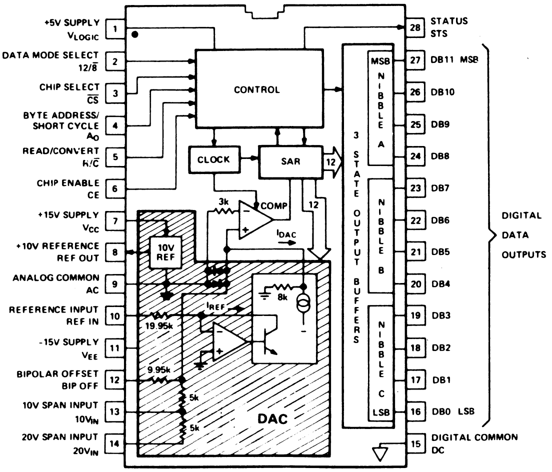


Figure 2. ADC Section Functional Block Diagram and Pinout

PIN FUNCTION DESCRIPTION

ANALOG INPUT SECTION	
Pin Number	Function
1	Single-End/Differential Mode Select "0": Single-Ended Mode "1": Differential Mode
2	Digital Common
3	Positive Digital Power Supply, +5V
4	"High" Analog Input, Channel 7
5	"High" Analog Input, Channel 6
6	"High" Analog Input, Channel 5
7	"High" Analog Input, Channel 4
8	"High" Analog Input, Channel 3
9	"High" Analog Input, Channel 2
10	"High" Analog Input, Channel 1
11	"High" Analog Input, Channel 0
12	Hold Capacitor (Provided, See Figure 3)
13	Sample-Hold Command "0": Sample Mode "1": Hold Mode Normally Connected to ADC Pin 28
14	Offset Adjust (See Figure 7)
15	Offset Adjust (See Figure 7)
16	Analog Output Normally Connected to ADC "Analog In" (See Figure 3)
17	Analog Common
18	"High" ("Low") Analog Input, Channel 15 (7)
19	"High" ("Low") Analog Input, Channel 14 (6)
20	Negative Analog Power Supply, -15V
21	Positive Analog Power Supply, +15V
22	"High" ("Low") Analog Input, Channel 13 (5)
23	"High" ("Low") Analog Input, Channel 12 (4)
24	"High" ("Low") Analog Input, Channel 11 (3)
25	"High" ("Low") Analog Input, Channel 10 (2)
26	"High" ("Low") Analog Input, Channel 9 (1)
27	"High" ("Low") Analog Input, Channel 8 (0)
28	Input Channel Select, Address Bit AE
29	Input Channel Select, Address Bit A0
30	Input Channel Select, Address Bit A1
31	Input Channel Select, Address Bit A2
32	Input Channel Select Latch "0": Latched "1": Latch "Transparent"

ANALOG TO DIGITAL CONVERTER SECTION	
Pin Number	Function
1	Logic Power Supply, +5V
2	Data Mode Select (12/$\overline{8}$) "0": 8 Upper Bits or 4 Lower Bits as Selected by Byte Select (A_0)
3	Chip Select ($\overline{CS}$) "0": Device Selected "1": Device Inhibited
4	Byte Address/Short Cycle (A_0) "0": Upper 8 Bits Enabled (12/$\overline{8}$ "0")/ 12 Bit Cycle "1": Lower 4 Bits Enabled (12/$\overline{8}$ "1")/ 8 Bit Cycle
5	Read Convert (R/$\overline{C}$) "0": Convert Start "1": Read Enable
6	Chip Enable (CE) ↑: R/$\overline{C}$ "0", $\overline{CS}$ "0" Initiates Conversion ↑: R/$\overline{C}$ "1", $\overline{CS}$ "0" Initiates Read "0": Device Disabled "1": Device Enabled
7	Analog Power Supply, +15V (V_{CC})
8	Reference Out, +10V
9	Analog Common (AC)
10	Reference In
11	Analog Power Supply, -15V (V_{EE})
12	Bipolar Offset
13	10 Volt Span Input
14	20 Volt Span Input
15	Digital Common (DC)
16	Data Bit 0
17	Data Bit 1
18	Data Bit 2
19	Data Bit 3
20	Data Bit 4
21	Data Bit 5
22	Data Bit 6
23	Data Bit 7
24	Data Bit 8
25	Data Bit 9
26	Data Bit 10
27	Data Bit 11
28	Status Out

AD364 DESIGN

Concept

The AD364 consists of two separate functional blocks as shown in Figure 3; each is packaged in a hermetically-sealed DIP.

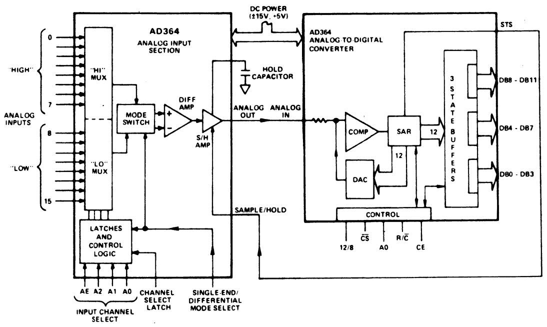


Figure 3. AD364 Functional Block Diagram

The Analog Input Section contains multiplexers, a differential amplifier, a sample-and-hold, a channel address latch and control logic. Analog-to-digital conversion is provided by a 12 bit, 35 microsecond "ADC" which is also available separately as the AD574.

By dividing the data acquisition task into two sections, several important advantages are realized. Performance of each design is optimized for its specific function. Production yields are increased thus decreasing costs. Furthermore, the standard configuration 28 and 32 pin packages plug into standard sockets and are easier to handle than larger packages with higher pin counts.

Analog Input Section Design

The AIS consists of two 8-channel multiplexers, a differential amplifier, a sample-and-hold, channel address latches and control logic. The multiplexers can be connected to the differential amplifier in either an 8-channel differential or 16-channel single-ended configuration. A unique feature of the AD364 is an internal analog switch controlled by a digital input that performs switching between single-ended and differential modes. This feature allows a single product to perform in either mode without external hard-wire interconnections. Of more significance is the ability to serve a mixture of both single-ended and differential sources with a single AD364 by dynamically switching the input mode control.

Multiplexer channel address inputs are interfaced through a level-triggered ("transparent") input register. With a Logic "1" at the Channel Select Latch input, the address signals feed through the register to directly select the appropriate input channel. This address information can be held in the register by placing a Logic "0" on the Channel Select Latch input. Internal logic monitors the status of the Single-Ended/Differential Mode input and addresses the multiplexers accordingly.

A differential amplifier buffers the multiplexer outputs while providing high input impedance in both differential and single-ended modes. Amplifier gain and common mode rejection are actively laser-trimmed.

The sample-and-hold is a high speed monolithic device that can also function as a gated operational amplifier. Its uncommitted differential inputs allow it to serve a second role as the output subtractor in the differential amplifier. This eliminates one amplifier and decreases drift, settling time and power consumption. A Logic "1" on the Sample-and-Hold Command input will cause the sample-and-hold to "freeze" the analog signal while the ADC performs the conversion. Normally the Sample-and-Hold Command is connected to the ADC Status output which is at Logic "1" during conversion and Logic "0" between conversions. For slowly-changing inputs, throughput speed may be increased by grounding the Sample-and-Hold Command input instead of connecting it to the ADC status.

A Polystyrene hold capacitor is provided with each commercial temperature range system (AD364J, K) while a Teflon capacitor is provided with units intended for operation at temperatures up to 125°C (AD364S, T). Use of an external capacitor allows the user to make his own speed/accuracy tradeoff; a smaller capacitor will allow faster sample-and-hold response but will decrease accuracy while a larger capacitor will increase accuracy at slower conversion rates.

The Analog Input Section is constructed on a substrate that includes thick-film resistors for non-critical applications such as input protection and biasing. A separately-mounted laser-trimmed thin-film resistor network is used to establish accurate gain and high common-mode rejection. The metal package affords electromagnetic and electrostatic shielding and is hermetically welded at low temperatures. Welding eliminates the possibility of contamination from solder particles or flux while low temperature sealing maintains the accuracy of the laser-trimmed thin-film resistors.

"ADC" Section

The ADC Section is a complete 12-bit A/D converter which requires no external components to provide the complete successive-approximation analog-to-digital conversion function. A block diagram of the ADC is shown in Figure 2. The device consists of two chips, one containing the precision 12-bit DAC with voltage reference, the other containing the comparator, successive-approximation register, clock, output buffers and control circuitry.

When the control section is commanded to initiate a conversion (as described later), it then enables the clock and resets the successive-approximation register (SAR) to all zeros. (Once a conversion cycle has begun, it cannot be stopped or re-started and data is not available from the output buffers). The SAR, timed by the clock, will then sequence through the conversion cycle and return an end-of-convert flag to the control section. The control section will then disable the clock, bring the output status flag low, and enable control functions to allow data read functions by external command.

During the conversion cycle, the internal 12-bit current output DAC is sequenced by the SAR from the most-significant-bit (MSB) to least-significant-bit (LSB) to provide an output current which accurately balances the input signal current through the 5kΩ (or 10kΩ) input resistor. The comparator determines whether the addition of each successively-weighted bit current causes the DAC current sum to be greater or less than the input current; if the sum is less, the bit is left on; if more, the bit is turned off. After testing all the bits, the SAR contains a 12-bit binary code which accurately represents the input signal to within ±1/2LSB.

The temperature-compensated buried Zener reference provides the primary voltage reference to the DAC and guarantees excellent stability with both time and temperature. The reference is trimmed to 10.00 volts ±1%; it is buffered and can supply up to 1.5mA to an external load in addition to that required to drive the reference input resistor (0.5mA) and bipolar offset resistor (1mA). The thin film application resistors are trimmed to match the full scale output current of the DAC. There are two 5kΩ input scaling resistors to allow either a 10 volt or 20 volt span. The 10kΩ bipolar offset resistor is grounded for unipolar operation or connected to the 10 volt reference for bipolar operation.

THEORY OF OPERATION

System Timing

Figure 4 is a timing diagram for the AD364 connected as shown in Figure 3 and operating at maximum conversion rate.

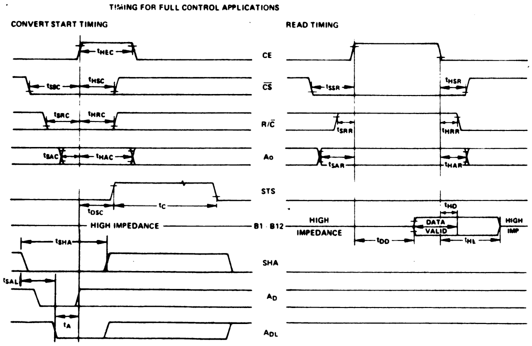


Figure 4. AD364 Timing Diagram

The normal sequence of events is as follows:

1. The appropriate Channel Select Address is latched into the address register. Time is allowed for the multiplexers to settle.
2. A Convert Start Control sequence is issued to the ADC which indicates that it is "busy" by placing a Logic "1" on its Status Line.
3. The ADC Status controls the sample-and-hold. When the ADC is "busy" the sample-and-hold is in the hold mode.
4. The ADC goes into its 35 microsecond conversion routine. Since the sample-and-hold is holding the proper analog value, the address may be updated during conversion. Thus multiplexer settling time can coincide with conversion and need not effect throughput rate.
5. The ADC indicates completion of its conversion by returning Status to Logic "0". The sample-and-hold returns to the sample mode.
6. If the input signal has changed full-scale (different channels may have widely-varying data) the sample-and-hold will typically require 10 microseconds to "acquire" the next input to sufficient accuracy for 12-bit conversion.

After allowing a suitable interval for the sample-and-hold to stabilize at its new value, another Convert Start control sequence may be issued to the ADC.

ADC Operation

There are two sets of control pins on the ADC: the general control inputs (CE, $\overline{CS}$, and R/$\overline{C}$), and the internal register control inputs (12/$\overline{8}$ and A_O). The general control pins function similarly to those on most A/D converters, performing device timing, addressing, cycle initiation and read enable functions. The internal register control inputs, which are not found on most A/D converters, select output data format and conversion cycle length.

The two major control functions, convert start and read enable, are controlled by CE, $\overline{CS}$, R/$\overline{C}$. Although all three inputs must be in the correct state to perform the function (for convert start, CE = 1, $\overline{CS}$ = 0, R/$\overline{C}$ = 0; for read enable, CE = 1, $\overline{CS}$ = 0, R/$\overline{C}$ = 1), the sequence does not matter. For large systems, typically microprocessor controlled, standard operation for convert start would be to first set R/$\overline{C}$ = 0 (from R/$\overline{W}$ line); address the chip with $\overline{CS}$ = 0, then apply a positive start pulse to CE. A read would be done similarly but with R/$\overline{C}$ = 1.

The A_O (byte select) and 12/$\overline{8}$ (data format) inputs work together to control the output data and conversion cycle. In almost all situations 12/$\overline{8}$ is hard-wired "high" (to V_{LOGIC}) or "low" (to Digital Common). If it is wired high, all 12 data lines will be enabled when the read function is called by the general control inputs. For an 8-bit bus interface, 12/$\overline{8}$ will be wired low. In this mode, only the 8 upper bits or the 4 lower bits can be enabled at once, as addressed by A_O. For these applications, the 4LSB's (pins 16–19) should be hard-wired to the 4MSB's (pins 24-27). Thus, during a read, when A_O is low, the upper 8 bits are enabled and present data on pins 20 through 27. When A_O goes high, the upper 8 data bits are disabled, the 4LSB's then present data to pins 24 to 27, and the 4 middle bits are overridden so that zeros are presented to pins 20 and 23.

The A_O input performs an additional function of controlling conversion length. If A_O is held low prior to cycle initiation, a full 12-bit, 25μs cycle will result; if A_O is held high prior to cycle initiation a shortened 8-bit, 16μs cycle will result. The A_O line must be set prior to cycle initiation and held in the desired position at least until STS goes high. Thus, for microprocessor interface applications, the A_O line must be properly controlled during both the convert start and read functions.

STANDARD FULL CONTROL INTERFACE

The timing for the standard full control interface is shown in Figure 4. In this operating mode, $\overline{CS}$ is used as the address input which selects the particular device, R/$\overline{C}$ selects between the read data and start conversion functions, and CE is used to time the actual functions.

The left side of the figure shows the conversion start control. $\overline{CS}$ and R/$\overline{C}$ are brought low (their sequence does not matter), then the start pulse is applied to CE. The timing diagram shows a time delay for $\overline{CS}$ and R/$\overline{C}$ prior to the start pulse at CE. If less time than this is allowed, the conversion will still be started, but an appropriately longer pulse will be needed at CE. However, if the hold times for $\overline{CS}$ and R/$\overline{C}$ after the rising edge of the start pulse at CE are not followed, the conversion may not be initiated.

The A_O line determines the conversion cycle length, and must be selected prior to conversion initiation. If A_O is low, a 12-bit cycle results; if A_O is high, an 8-bit short cycle results. Minimum set-up and hold times are shown. The status line goes high to indicate conversion in progress. The analog input signal is allowed to vary until the STS goes high. It must then be held steady until STATUS again goes low at the end of conversion.

The data read function operates in a similar fashion except that R/$\overline{C}$ is now held high. The data is stored in the output register and can be recalled at will until a new conversion cycle is commanded. In addition, if the converter is arranged in the 8-bit data mode, the A_O line now functions as the byte select address, with set-up and hold times as shown. With A_O low, pins 20 to 27 (DB4–11) come out of three-state and present data. With A_O high, pins 16–19 (DB0–3) come out of three-state with data and pins 20–23 present active trailing zeros. In the 8-bit mode pins 16–19 will be hard-wired directly to pins 24–27 for direct two-byte loading onto an 8-bit bus. There are two delay times for the data lines after CE is brought low: t_{HD} is the delay until data is no longer valid; t_{HL} is the delay until the outputs are fully into the high impedance state.

TIMING SPECIFICATIONS – FULL CONTROL MODE

t_{DSC}	300ns max	t_{DD}	400ns max
t_{HEC}	300ns min	t_{HD}	100ns min
t_{SSC}	300ns min	t_{SSR}	350ns min
t_{HSC}	200ns min	t_{SRR}	0 min
t_{SRC}	200ns min	t_{SAR}	200ns min
t_{HRC}	200ns min	t_{HSR}	100ns min
t_{SAC}	0 min	t_{HRR}	0 min
t_{HAC}	300ns min	t_{HAR}	100ns min
t_C	15-32μs (12 bit)	t_{HL}	600ns max
	10-20μs (8 bit)	t_{SAL}	20ns min
t_{SHA}	10-18μs	t_{SA}	0 min

STAND ALONE OPERATION

For simpler control functions, the AD364 can be controlled with just R/$\overline{C}$. In this case, CE is wired high, $\overline{CS}$ low, 12/$\overline{8}$ high, and A_O low. There are two ways of cycling the device with this simple hook-up. If a negative pulse is used to initiate conversion as in Figure 5, the converter will automatically bring the 12 data lines out of three-state at the end of conversion. The data will remain valid on the output lines until another pulse is applied.

If the conversion is initiated by a high pulse as shown in Figure 6, the data lines are held in three-state at the end of conversion until R/$\overline{C}$ is brought high. The next conversion cycle is initiated when R/$\overline{C}$ goes low, the data from the previous cycle will remain valid for the time t_{HDR}. An alternative to the above is to toggle R/$\overline{C}$ as needed to initiate a new cycle on read data. Data will appear when R/$\overline{C}$ is brought high, a new cycle is initiated when R/$\overline{C}$ goes low.

TIMING SPECIFICATIONS – STAND ALONE MODE

t_{HRL}	400ns min	
t_{DS}	500ns max	
t_{HDR}	300ns max	
t_{HS}	-100ns min	+200ns max
t_{HRH}	150ns min	
t_{DDR}	350ns max	

t_C (12 bit convert) 15-35μs
t_C (8 bit convert) 10-20μs

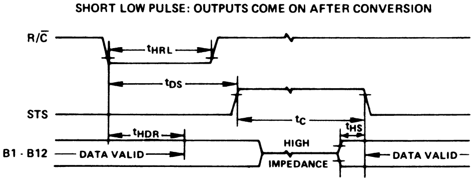


Figure 5.

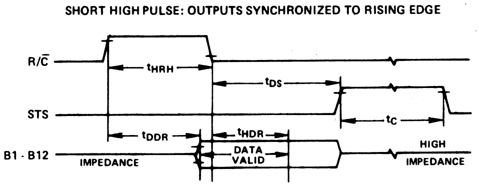


Figure 6.

AIS OPERATION

Single-Ended/Differential Mode Control

The AD364 features an internal analog switch that configures the Analog Input Section in either a 16-channel single-ended or 8-channel differential mode. This switch is controlled by a TTL logic input applied to pin 1 of the Analog Input Section:

"0": Single-Ended (16 channels)
"1": Differential (8 channels)

When in the differential mode, a differential source may be applied between corresponding "High" and "Low" analog input channels.

It is possible to mix SE and DIFF inputs by using the mode control to command the appropriate mode. Figure 10 illustrates an example of a "mixed" application. In this case, four microseconds must be allowed for the output of the Analog Input Section to settle to within ±0.01% of its final value, but if the mode is switched concurrent with changing the channel address, no significant additional delay is introduced. The effect of this delay may be eliminated by changing modes while a conversion is in progress (with the sample-and-hold in the "hold mode"). When SE and DIFF signals are being processed concurrently, the DIFF signals must be applied between corresponding "High" and "Low" analog input channels. Another application of this feature is the capability of measuring 16 sources individually and/or measuring differences between pairs of those sources.

Input Channel Addressing

Table 1 is the truth table for input channel addressing in both the single-ended and differential modes. The 16 single-ended channels may be addressed by applying the corresponding

ADDRESS				ON CHANNEL (Pin Number)		
					Differential	
AE	A2	A1	A0	Single Ended	"Hi"	"Lo"
0	0	0	0	0 (11)	None	
0	0	0	1	1 (10)	None	
0	0	1	0	2 (9)	None	
0	0	1	1	3 (8)	None	
0	1	0	0	4 (7)	None	
0	1	0	1	5 (6)	None	
0	1	1	0	6 (5)	None	
0	1	1	1	7 (4)	None	
1	0	0	0	8 (27)	0 (11)	0 (27)
1	0	0	1	9 (26)	1 (10)	1 (26)
1	0	1	0	10 (25)	2 (9)	2 (25)
1	0	1	1	11 (24)	3 (8)	3 (24)
1	1	0	0	12 (23)	4 (7)	5 (23)
1	1	0	1	13 (22)	5 (6)	5 (22)
1	1	1	0	14 (19)	6 (5)	6 (19)
1	1	1	1	15 (18)	7 (4)	7 (18)

Table 1. Input Channel Addressing Truth Table

digital number to the four Input Channel Select address bits, AE, A0, A1, A2 (Analog Input Section, pins 28–31). In the differential mode, the eight channels are addressed by applying the appropriate digital code to A0, A1 and A2; AE must be enabled with a Logic "1". Internal logic monitors the status of the SE/DIFF Mode input and addresses the multiplexes singly or in pairs as required.

When the channel address is changed, six microseconds must be allowed for the Analog Input Section to settle to within ±0.01% of its final output (including settling times of all elements in the signal path). The effect of this delay may be eliminated by performing the address change while a conversion is in progress (with the sample-and-hold in the "hold" mode).

Input Channel Address Latch

The AD364 is equipped with a latch for the Input Channel Select address bits. If the Latch Control pin (pin 32 of the Analog Input Section) is at Logic "1", input channel select address information is passed through to the multiplexers. A Logic "0" "freezes" the input channel address present at the inputs at the time of the "1" to "0" transition.

This feature is useful when input channel address information is provided from an address, data or control bus that may be required to service many devices. The ability to latch an address is helpful whenever the user has no control of when address information may change.

Sample-and-Hold Mode Control

The Sample-and-Hold Mode Control input (Analog Input Section, pin 13) is normally connected to the Status output (pin 28) from the ADC section. When a conversion is initiated by applying a Convert Start control sequence, Status goes to Logic "1", putting the sample-and-hold into the "hold" mode. This "freezes" the information to be digitized for the period of conversion. When the conversion is complete, Status returns to Logic "0" and the sample-and-hold returns to the sample mode. Eighteen microseconds must be allowed for the sample-and-hold to acquire ("catch up" to) the analog input to within ±0.01% of the final value before a new Convert Start command is issued.

The purpose of a sample-and-hold is to "stop" fast changing input signals long enough to be converted. In this application, it also allows the user to change channels and/or SE/ DIFF mode while a conversion is in progress thus eliminating the effects of multiplexer, analog switch and differential amplifier settling times. If maximum throughput rate is required for slowly changing signals, the Sample-and-Hold Mode Control may be wired to ground (Logic "0") rather than to ADC Status thus leaving the sample-and-hold in a continuous sample mode.

Hold Capacitor

A 2000pF capacitor is provided with each AD364. One side of this capacitor is wired to the Analog Input Section pin 12, the other to analog ground as close to pin 17 as possible. The capacitor provided with the AD364J, K is Polystyrene while the wider operating temperature range of the AD364S, T demands a Teflon Capacitor (supplied).

Larger capacitors may be substituted to minimize noise, but acquisition time of the sample-and-hold will be extended. If less than 12 bits of accuracy is required, a smaller capacitor may be used. This will shorten the S/H acquisition time. In all cases, the proper capacitor dielectric must be used; i.e., Polystyrene (AD364J, K only) or Teflon (any grade). Other types of capacitors may have higher dielectric absorption (memory) and will cause errors. CAUTION: Polystyrene capacitors will be destroyed if subjected to temperatures above +85°C. No capacitor is required if the sample-and-hold is not used.

Analog Input Voltage Range Format

The AD364 may be configured for any of 2 bipolar or unipolar input voltage ranges as shown in Table 2.

Range	Connect Analog Input To ADC Pin:	Connect Bipolar ADC Pin 12 To:
0 to +10V	13	–
-5V to +5V	13	8
-10V to +10V	14	8

Table 2. Analog Input Voltage Range Pin Connections

Analog Input - Volts (Center of Quantization Interval)			Input Normalized to FSR		Digital Output Code (Binary for Unipolar Ranges; Offset Binary for Bipolar Ranges)
0 to +10V Range	-5V to +5V Range	-10V to +10V Range	Unipolar Ranges	Bipolar Ranges	B1 (MSB) B12 (LSB)
+9.9976	+4.9976	+9.9951	+FSR-1 LSB	+½FSR-1 LSB	1 1 1 1 1 1 1 1 1 1 1 1
+9.9952	+4.9952	+9.9902	+FSR-2 LSB	+½FSR-2 LSB	1 1 1 1 1 1 1 1 1 1 1 0
:	:	:	:	:	:
+5.0024	+0.0024	+0.0049	+½FSR+1 LSB	+1 LSB	1 0 0 0 0 0 0 0 0 0 0 1
+5.0000	+0.0000	+0.0000	+½FSR	ZERO	1 0 0 0 0 0 0 0 0 0 0 0
:	:	:	:	:	:
+0.0024	-4.9976	-9.9951	+1 LSB	-½FSR+1 LSB	0 0 0 0 0 0 0 0 0 0 0 1
+0.0000	-5.0000	-10.0000	ZERO	-½FSR	0 0 0 0 0 0 0 0 0 0 0 0

Table 3. Digital Output Codes vs. Analog Input for Unipolar and Bipolar Ranges

Analog Input Section Offset Adjust Circuit

The offset voltage of the AD364 may be adjusted at either the Analog Input Section or the ADC Section. Normally the adjustment is performed at the ADC but in some special applications, it may be helpful to adjust the offset of the Analog Input Section. An example of such a case would be if the input signals were small (<10mV) relative to Analog Input Section voltage offset and gain was inserted between the Analog Input Section and the ADC. To adjust the offset of the Analog Input Section, the circuit shown in Figure 7 is recommended. Under normal conditions, all calibration is performed at the ADC Section.

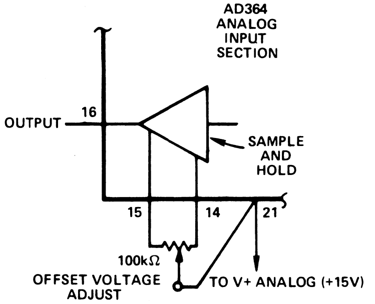


Figure 7. Analog Input Section Offset Voltage Adjustment

RANGE CONNECTIONS FOR THE ADC SECTION

The ADC contains all the active components required to perform a complete 12-bit A/D conversion. Thus, for most situations, all that is necessary is connection of the power supplies (+5, +15, and -15 volts), the analog input, and the conversion initiation command. Analog input connections and calibration are easily accomplished; the unipolar operating mode is shown in Figure 8.

All of the thin film application resistors of the ADC are trimmed for absolute calibration. Therefore, in many applications, no calibration trimming will be required. The absolute accuracy for each grade is given in the specification tables. For example, if no trims are used, the AD364K guarantees 4LSB max zero offset error and ±0.3% (8LSB) max full scale error (typical full scale error is ±2LSB). If the offset trim is not required, pin 12 can be connected directly to pin 9; the two resistors and trimmer for pin 12 are then not needed. If the full scale trim is not needed, a 50Ω ±1% resistor should be connected between pin 8 and pin 10.

The analog input is connected between pin 13 and pin 9 for a 0 to +10V input range, between 14 and pin 9 for an input range of 20V. For the 10 volt span input, the LSB has a nominal value of 2.44mV, for the 20 volt span, 4.88mV. If a 10.24V range is desired (nominal 2.5mV/bit), gain trimmer R2 should be replaced by a 50Ω resistor, and a 200Ω trimmer inserted in series with the analog input to pin 13. For a full scale range of 20.48V (5mV/bit), use a 500Ω trimmer into pin 14. The gain trim described below is now done with these trimmers. The nominal input impedance is 5kΩ into pin 13, and 10kΩ into pin 14.

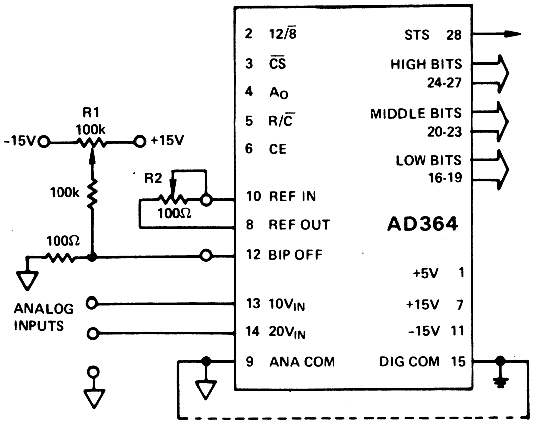


Figure 8. Unipolar Input Connections

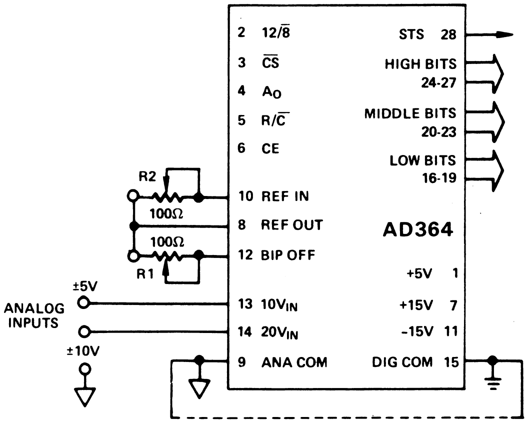


Figure 9. Bipolar Input Connections

Calibration

Calibration of the AD364 consists of adjusting offset and gain. Relative accuracy (linearity) is not affected by these adjustments, so if absolute zero and gain error is not important in a given application, or if system intelligence can correct for such errors, calibration may be unnecessary.

External ZERO ADJ and GAIN ADJ potentiometers, connected as shown in Figures 8 and 9, are used for device calibration. To prevent interaction of these two adjustments, Zero is always adjusted first, then Gain. Zero is adjusted with the analog input near the most negative end of the analog range (0 for unipolar and -FS for bipolar input ranges). Gain is adjusted with the analog input near the most positive end of the analog range.

0 to +10V Range: Set analog input to +1LSB = +0.0024V. Adjust Zero for digital output = 000000000001; Zero is now calibrated. Set analog input to +FSR -2LSB = +9.9952V. Adjust Gain for 111111111110 digital output code; full-scale (Gain) is now calibrated. Half-scale calibration check: set analog input to +5.0000V; digital output code should be 100000000000.

-10V to +10V Range: Set analog input to -9.9951V; adjust Zero for 000000000001 digital output (offset binary) code. Set analog input to +9.9902V; adjust Gain for 111111111110 digital output (offset binary) code. Half-scale calibration check: set analog input to 0.0000V; digital output (offset binary) code should be 100000000000.

Other Ranges: Representative digital coding for 0 to +10V, -5V to +5V, and -10V to +10V ranges is shown in Table 3.

Zero and full-scale calibration can be accomplished to a precision of approximately ±¼LSB using the static adjustment procedure described above. By summing a small sine or triangular-wave voltage with the signal applied to the analog input, the output can be cycled through each of the calibration codes of interest to more accurately determine the center (or end points) of each discrete quantization level. A detailed description of this dynamic calibration technique is presented in "A/D Conversion Notes", D. Sheingold, Analog Devices, Inc., 1977, Part II, Chapter II-4.*

Other Considerations

Grounding: The analog common at pin 9 is the ground reference point for the internal reference and is thus the "high quality" ground for the ADC; it should be connected directly to the analog reference point of the system. In order to achieve all of the high accuracy performance available from the AD364 in an environment of high digital noise content, it is recommended that the analog and digital commons be connected together at the package. The digital common at pin 15 can be connected to the most convenient ground reference point; analog power return is preferred. If digital common contains high frequency noise beyond 200mV this noise may feed through the converter, so that some caution will be required in applying these grounds.

Power Supply Bypassing: The ±15V and +5V power leads should be capacitively bypassed to Analog Ground and Digital Ground respectively for optimum device performance. 1μF tantalum types are recommended; these capacitors should be located close to the system. High frequency power supply decoupling is required for the ADC section only. The AIS has power lead bypassed internally with a 0.039μF ceramic capacitor.

Applications

Transducer Interfacing

The precision +10V reference, buffer amplifier and mode switch can simplify transducer interfacing. Figure 10 illustrates how these features may be used to advantage. The AD590 is a temperature transducer that can be considered an ideal two-terminal current source with an output of one microamp per degree Kelvin (1μA/°K). With an offsetting current of 273μA sourced from the +5.46 volt buffered reference through 20kΩ resistors (R1-R12) each of the 12 AD590 circuits develop -20mV/°C. The outputs are monitored with the AD364 front-end in the single-ended mode (Logic "0" on the Mode Control input).

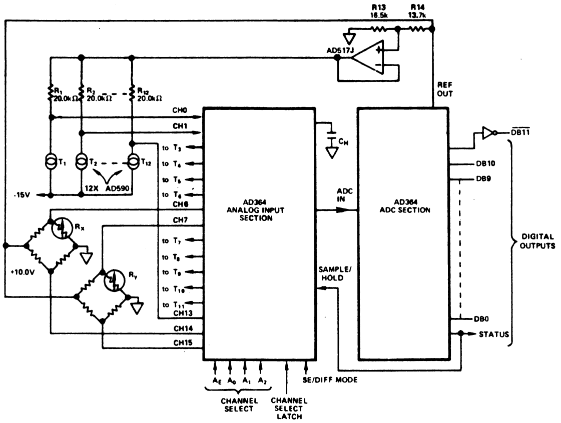


Figure 10. AD364 Transducer Interface Application

The +5.46 volt reference is derived from the ADC +10 volt precision reference and voltage divider R13, R14. Low output impedance for this +5.46 volt reference is provided by the buffer amplifier. (The 3μV/°C offset voltage drift of the buffer amplifier contributes negligible errors.) At 0°C, each temperature transducer circuit delivers a 0 volt output. At 125°C, the output is -2.5V; at -55°C, the output is +1.10V. By using a two's complement ADC output (complementing MSB for a sign bit), the negative voltage versus temperature function is inverted and digital reading proportional to temperature in degrees centigrade is provided. Resolution is 0.061°C per least significant bit.

The precision +10 volt reference is also used to power several bridge circuits that require differential read-out. When addressing these bridge transducers, a Logic "1" at the mode control input will switch the AD364 to the differential mode. In many cases, this feature will eliminate the requirement for a differential amplifier for each bridge transducer.

Microprocessor Interfacing

The ADC section of the AD364 has a versatile set of control functions which will allow interface to a wide variety of microprocessor types as well as stand alone applications.

Table 4 is a summary of the most popular microprocessor types and their interface requirements. Figures 11 & 12 are examples of the simplicity of the microprocessor interface, as it can be seen no additional parts are required to interface to a 6800 μP, only one gate for an 8080.

μP	AD574 CONTROL INPUTS CE	R/$\overline{C}$	$\overline{CS}$	A0
MEMORY MAPPED I/O - 8080 - PROGRAMMED I/O	$\overline{(\overline{MEMW} \bullet \overline{MEMR})}$ $\overline{(\overline{I/OW} \bullet \overline{I/OR})}$	$\overline{(\overline{MEMR})}$ $\overline{(\overline{I/OR})}$	DECODED ADDRESS	A0
6800	ϕ_2	R/$\overline{W}$	DECODED ADDRESS	A0
6502	ϕ_2	R/$\overline{W}$	DECODED ADDRESS	A0
MEMORY MAPPED I/O - Z80 - PROGRAMMED I/O	$\overline{(\overline{RD} \bullet \overline{WR})}$	$\overline{(\overline{RD})}$	DECODED ADDRESS WITH MREQ DECODED ADDRESS WITH IOR	A0
8048	$\overline{(\overline{RD} \bullet \overline{WR})}$	$\overline{(\overline{RD})}$	PORT 2_{0-3}*	PORT 2_{0-3}*

*Port 2, Lines 0-3 Can be Used as a 4 Bit Address Bus. System Address Decoding Requirements Vary from No Hardware to a Fully Latched 12-Bit Address, Depending on System Complexity.

Table 4. Recommended Control Signals for the ADC Section

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*Available from any Analog Devices sales office. Price is $5.95.

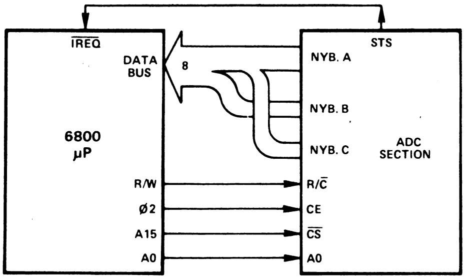


Figure 11. 6800 ⟷ ADC Interface

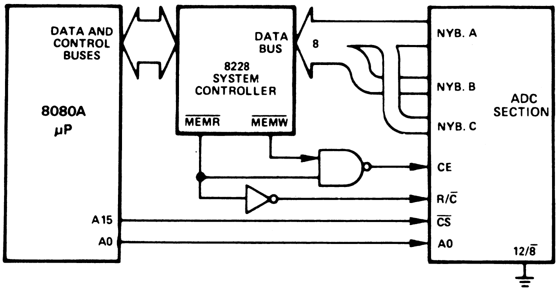


Figure 12. 8080 ⟷ ADC Interface

The single-chip microcomputers now available such as the 8048, 6801 and 3870 include fully decoded I/O ports on the chip, as well as CPU, clock, RAM and ROM. This sidesteps the need for address decoding for I/O devices in many systems. The 8048 contains 64 bytes of RAM, 1k bytes of ROM, and 2 programmable 8-bit I/O ports which can be used either as inputs or outputs. A third 8-bit port, designated BUS, is a bidirectional port which can be used for expanded I/O or memory.

The AD364 interfaces easily to an 8048 single-chip microcomputer to provide a complete data-acquisition system with minimal package count. In this system, 5 of the 8 bits of Port 1 drive the SE/DIFF MODE and channel select address inputs. Since the outputs of Port 1 are already latched, it is not necessary to use the latch built into the AD364. The LATCH input is tied to Logic "1" which causes the latch to be transparent. The set-up byte at Port 1 for the conversion takes the following format:

P_{1-7}							P_{1-0}
MODE	☒	☒	☒	A_E	A_2	A_1	A_0

0: SINGLE-ENDED
1: DIFFERENTIAL

"DON'T CARES"

INPUT CHANNEL ADDRESS

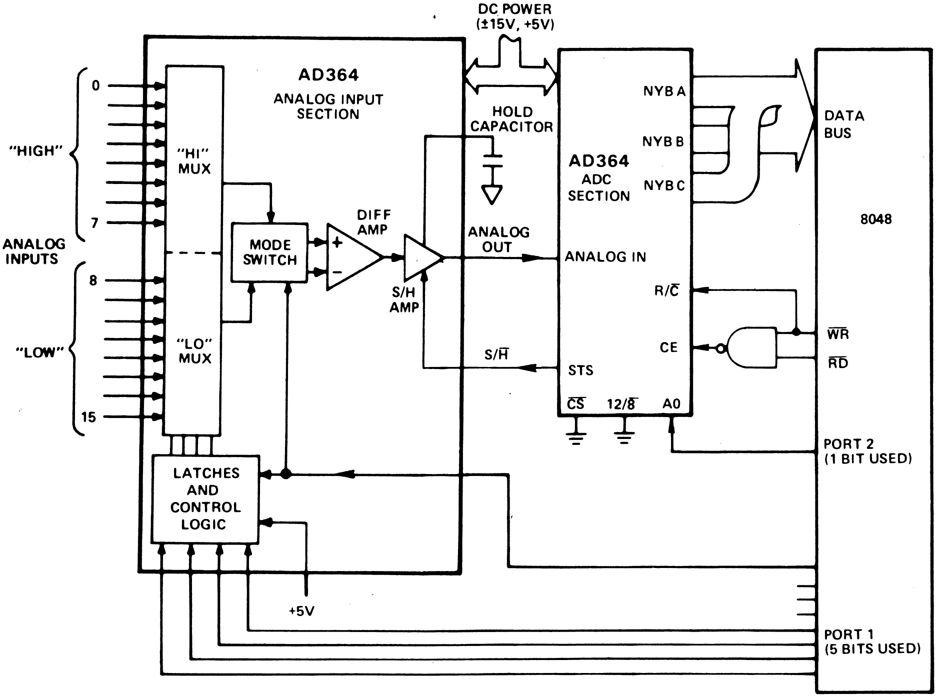
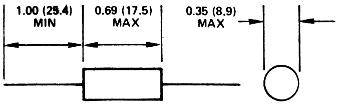


Figure 13. AD364/8048 Interface

OUTLINE DIMENSIONS
PACKAGE SPECIFICATIONS

Dimensions shown in inches and (mm).

HOLD CAPACITOR



*THIS DIMENSION IS FOR POLYSTYRENE CAPACITOR SUPPLIED WITH J AND K GRADES.

MAX BODY LENGTH OF TEFLON CAPACITOR SUPPLIED WITH S AND T GRADES IS 1.00"

AD364 ORDERING GUIDE

			Package Style[1]	
Model	Linearity	Temp. Range	Analog Input Section	Analog to Digital Converter
AD364JD	±0.024%	0 to +70°C	HY32D	D28A
AD364KD	±0.012%	0 to +70°C	HY32D	D28A
AD364SD	±0.024%	-55°C to +125°C	HY32D	D28A
AD364TD	±0.012%	-55°C to +125°C	HY32D	D28A
AD364SD/883B	±0.024%	-55°C to +125°C	HY32D	D28A
AD364TD/883B	±0.012%	-55°C to +125°C	HY32D	D28A

[1] See Section 20 for package outline information.

ANALOG DEVICES

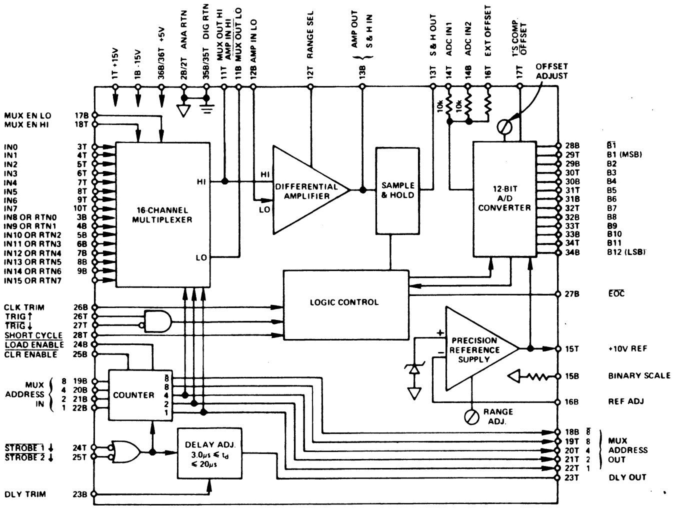
Low-Cost, High Speed Data Acquisition Module

DAS1128

FEATURES

Complete Data Acquisition System
12-Bit Digital Output
16 Single or 8 Differential Analog Inputs
High Throughput Rate
Selectable Analog Input Ranges
Versatile Input/Output/Control Format
Low 3 Watt Power Dissipation
Small 3" x 4.6" x 0.375" Module

DAS1128 FUNCTIONAL BLOCK DIAGRAM



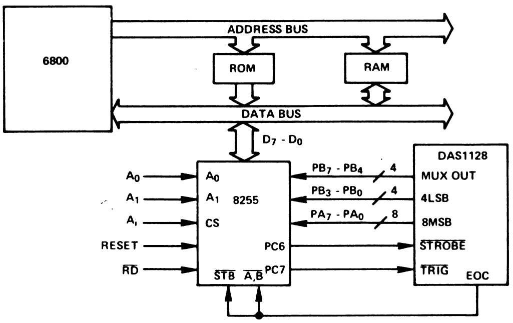
GENERAL DESCRIPTION

The DAS1128 is a complete self-contained miniature high speed data acquisition system. The compact 3" x 4.6" x 0.375" module provides the designer with an easily implemented solution to the data acquisition problem. It contains an analog input signal multiplexer, a sample-and-hold amplifier, a 12-bit A/D converter, and all of the programming, timing and control circuitry needed to perform the complete data acquisition function.

The DAS1128 is a high performance device which can digitize an analog signal to an accuracy of ±½LSB out of 12 bits, relative to full scale. It has ±8ppm/°C gain temperature coefficient, and the maximum throughput rate can be varied from 50,000 conversions/second for a 12 bit conversion from different analog input channels, to 200,000 conversions/second for a successive 4-bit conversion made on a single channel.

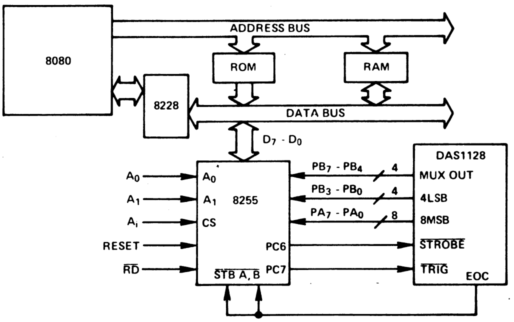
TYPICAL APPLICATIONS

DAS1128 WITH MOTOROLA 6800



NOTE:
1. 8255 USED IN MODE 1 (STROBED I/O)
2. PC6 INDEXES MUX TO DESIRED CHANNEL
3. CS TO A_i (WHERE, A_i IS AN ADDRESS BIT OTHER THAN A_0 OR A_1)
4. PC7 INITIATES CONVERSION
5. EOC STROBES IN DATA AND MUX INFO
6. 8255 SHOWN, HOWEVER 6820 CAN ALSO BE USED

DAS1128 WITH INTEL 8080



NOTE:
1. 8255 USED IN MODE 1 (STROBED I/O)
2. CS TO A_i (WHERE, A_i IS AN ADDRESS BIT OTHER THAN A_0 OR A_1)
3. PC6 INDEXES MUX TO DESIRED CHANNEL
4. PC7 INITIATES CONVERSION
5. EOC STROBES IN DATA AND MUX INFO

This two-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be found in Volume II, page 15–17.

SPECIFICATIONS (typical @ +25°C and ±15V unless otherwise noted)

ANALOG INPUTS

Number of Inputs to Multiplexer	16 Single Ended, 8 True-Differential, 16 Pseudo-Differential
Input Voltage (Full Scale Range)	-10V to +10V, 0V to +10V, -5V to +5V, 0V to +5V, -10.24V to +10.24V, 0V to +10.24V, -5.12V to +5.12V, or 0V to +5.12V.
Maximum Input Voltage	±15V
Input Current (per channel)	5nA max
Input Impedance	$>10^{10}$ ohms
Input Capacitance	10pF for "OFF" channel 100pF for "ON" channel
Input Fault Current (power off or MUX failure)	Internally limited to 20mA
Direct ADC Input Impedance	10kΩ for each input line

ACCURACY[1]

Resolution	12 Bits
Error Relative to F.S.	±½LSB
Quantization Error	±½LSB
Differential Nonlinearity Error	
@ 33kHz throughput rate	±½LSB, 1LSB max
@ 50kHz throughput rate	±1LSB
Noise Error	±¼LSB
-FS to +FS Error Between Successive Channel Transitions	±1LSB

TEMP. COEFFICIENTS

Gain	8ppm/°C, 20ppm/°C max
Offset	5ppm/°C, 15ppm/°C max
Differential Nonlinearity	2.5ppm/°C, 6ppm/°C max

SIGNAL DYNAMICS

Throughput Rate (12 Bits)	50kHz (max) (includes 5μs for MUX and SHA settling time plus 15μs for ADC)
MUX Crosstalk ("OFF" channels to "ON" channel)	>80dB down @ 1kHz
Differential Amplifier CMRR	70dB to 1kHz
SHA Acquisition Time to 0.01%	4.5μs max
SHA Aperture Uncertainty	10ns
SHA Feedthrough	70dB down @ 1kHz

DIGITAL INPUT SIGNALS

Compatibility	Standard DTL/TTL logic levels, 1 unit load/line
MUX Address Inputs (8, 4, 2, 1; Pins 19B through 22B)	Positive true natural binary coding selects channel for random addressing mode. Must be stable for 100ns after $\overline{\text{STROBE}}$.
MUX ENABLE HI (Pin 18T)	High (Logic "1") input enables MUX "HI" output (for inputs 0 through 7)
MUX ENABLE LO (Pin 17B)	High (Logic "1") input enables MUX "LO" output (for inputs 8 through 15)
$\overline{\text{STROBE}}$ (Pin 24T or 25T)	Negative going transition (Logic "1" to Logic "0") updates MUX address register. $\overline{\text{STROBE}}$ 1 must be a Logic "1" to enable $\overline{\text{STROBE}}$ 2. $\overline{\text{STROBE}}$ 2 must be at Logic "1" to enable $\overline{\text{STROBE}}$ 1.
$\overline{\text{LOAD ENABLE}}$ (Pin 24B)	High (Logic "1") input allows next $\overline{\text{STROBE}}$ command to sequentially advance MUX address register. Low (Logic "0") input allows next $\overline{\text{STROBE}}$ command to update MUX address register according to external address inputs.
$\overline{\text{CLEAR ENABLE}}$ (Pin 25B)	Low (Logic "0") input allows next $\overline{\text{STROBE}}$ command to reset MUX address to channel "0" overriding $\overline{\text{LOAD ENABLE}}$.
TRIGGER (Pin 26T)	Positive going transition (Logic "0" to Logic "1") initiates A/D conversion (even during conversion); $\overline{\text{TRIGGER}}$ (Pin 27T) must be at Logic "0" to allow TRIGGER function.
$\overline{\text{TRIGGER}}$ (Pin 27T)	Negative going transition (Logic "1" to Logic "0") initiates A/D conversion; Pin 26T (TRIGGER) must be at Logic "1" to allow $\overline{\text{TRIGGER}}$ function.

DIGITAL OUTPUT SIGNALS

Compatibility	Standard DTL/TTL logic levels; 5 unit loads/line.
Parallel Outputs	$\overline{\text{B1}}$, B1 through B12
Coding	Natural binary, two's complement, offset binary, or one's complement. Pin selectable.
MUX Address Outputs ($\overline{8}$, 8, 4, 2, 1; pins 18B, 19T through 22T)	Positive true natural binary coding indicates channel selected.
DELAY OUT (Pin 23T)	Negative going transition (Logic "1" to Logic "0") occurring normally 5μs (adjustable from 3.0μs to 20μs) after $\overline{\text{STROBE}}$ command initiates A/D conversion automatically when connected to the $\overline{\text{TRIGGER}}$.
$\overline{\text{EOC}}$ (Pin 27B)	High (Logic "1") output during A/D conversion.

ADJUSTMENTS & TRIMS

Offset Adjust	
Internal Adjustment (Externally Accessible)	±10LSBs (min)
Remote External Adjustment (Pin 16T)	±10LSBs (min)
Range Adjust	
Internal Adjustment (Externally Accessible)	±10LSBs (min)
Remote External Adjustment (Pin 16B)	±10LSBs (min)
Clock Trim (Pin 26B)	
Factory Setting (Pin 26B "OPEN")	1.25μs/Bit
External Adjustment Range	1.25μs/Bit to 2.08μs/Bit
Delay Trim (Pin 23B)	
Factory Setting (Pin 23B "OPEN")	3.0μs
External Adjustment Range	3.0μs to 20μs

CONTROLS

SHORT CYCLE (Pin 28T)	Connect to ground for full 12 bit resolution. Connect to B_n output for resolution to B_{n-1} bits.
Channel Selection Mode (MUX Address Loading Mode)	Random, sequential continuous, and sequential triggered. Pin selectable.
A-D Conversion/Channel-Select Sequences	Normal (input channel remains selected during its A/D conversion) and overlap (next channel selected during A/D conversion). Pin selectable.
Range Select (Pin 12T)	Differential Amplifier gain control: connect to ANA RTN (Pin 2T) for X1 gain; connect to AMP OUT (Pin 13B) for X2 gain. This control is used in FSR selection procedure.
BINARY SCALE (Pin 15B)	Connect to REF ADJ (Pin 16B) to set reference to 10.24V. This control is used in FSR selection procedure.
OUTPUT CODING (Pin 17T)	Ground for 1's complement output code; connect to -15V dc for other available codes.

POWER REQUIREMENTS

+15V ±3%	40mA, 50mA max
-15V ±3%	70mA, 100mA max
+5V ±5%	250mA, 500mA max
Power Supply Sensitivity[2]:	
Gain	±2.0mV/V
Offset	±4.0mV/V
Ref	±0.5mV/V

ENVIRONMENT & PHYSICAL

Operating Temperature	0 to +70°C
Storage Temperature	-25°C to +85°C
Relative Humidity	Up to 95% noncondensing
Electrical Shielding	RFI & EMI 6 sides (except connector area)
Packaging	Insulated steel cased module 3.00" x 4.60" x 0.375"

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[1] Warmup time to rated accuracy is 5 minutes.

[2] Specification applies only when tracking +15V and -15V supplies are used, and for slowly occuring variations in power supply voltages.

Specifications subject to change without notice.

ANALOG DEVICES

14-Bit & 15-Bit Sampling Analog To Digital Converter

DAS1152/DAS1153

FEATURES

Complete with High Accuracy Sample/Hold and A/D Converter
Differential Nonlinearity: ±0.002% FSR max (DAS1153)
Nonlinearity: DAS1152: ±0.005% FSR max
DAS1153: ±0.003% FSR max
Low Differential Nonlinearity T.C.: ±2ppm/°C max
High Throughput Rate: 25kHz max (DAS1152)
High Feedthrough Rejection: −100dB
Byte-Selectable Tri-State Buffered Outputs
Internal Gain & Offset Potentiometers
Improved Second Source to A/D/A/M 824 and A/D/A/M 825 Modules
Low Cost

APPLICATIONS

Process Control Data Acquisition
Automated Test Equipment
Seismic Data Acquisition
Nuclear Instrumentation
Medical Instrumentation
Robotics

GENERAL DESCRIPTION

The DAS1152/DAS1153 are 14-/15-bit sampling analog-to-digital converters having a maximum throughput rate of 25kHz/20kHz. They provide high accuracy, high stability, and functional completeness all in a 2″ × 4″ × 0.44″ metal case.

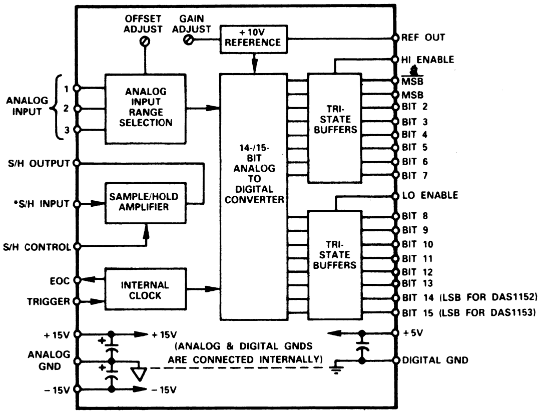
Guaranteed high accuracy system performance such as nonlinearity of ±0.005% FSR (DAS1152)/±0.003% FSR (DAS1153) and differential nonlinearity of ±0.003% FSR (DAS1152)/±0.002% FSR (DAS1153) are provided. Guaranteed stability such as differential nonlinearity T.C. of ±2ppm/°C (DAS1153) maximum, zero T.C. of ±80μV/°C maximum, gain T. C. of ±8ppm/°C maximum and power supply sensitivity of ±0.001% FSR/% V_S are also provided by the DAS1152/DAS1153.

The DAS1152/DAS1153 make extensive use of both integrated circuit and thin film components to obtain their excellent performance, small size, and low cost. The devices contain a precision sample/hold amplifier, high accuracy 14-/15-bit analog-to-digital converter, tri-state output buffers, internal gain and offset trim potentiometers, and power supply bypass capacitors (as shown in Figure 1).

Four analog input voltage ranges are selectable via user pin programming: 0 to +5V, 0 to +10V, ±5V, and ±10V. Unipolar coding is provided in true binary format with bipolar coding displayed in offset binary and two's complement. Tri-state buffers provide easy interface to bus structured applications.

This two-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be found in Volume II, page 15–25.

DAS1152/DAS1153
FUNCTIONAL BLOCK DIAGRAM



*S/H INPUT IS THE ANALOG SIGNAL INPUT IF THE INTERNAL SAMPLE/HOLD AMPLIFIER IS USED.

OPERATION

The DAS1152/DAS1153 are functionally complete data acquisition subsystems being fully characterized as such. All the necessary data acquisition and microprocessor interface elements are provided internal to these devices. Accuracy and performance criteria are tested and specified for the entire system. Thus, design time and associated high accuracy problems are minimized because layout and component optimization have already been performed.

For operation, the only connections necessary to the DAS1152/DAS1153 are the ±15V and +5V power supplies, analog input signal, trigger pulse, and the HI-ENABLE/LO-ENABLE tri-state controls. Analog input and digital output programming are user selectable via external jumper connections.

SPECIFICATIONS (typical @ + 25°C unless otherwise specified)

MODEL	DAS1152	DAS1153
RESOLUTION	14 Bits	15 Bits
DYNAMIC PERFORMANCE		
Throughput Rate	25kHz max	20kHz max
Conversion Time	35μs max	44μs max
S/H Acquisition Time	4μs max	5μs max
S/H Aperture Delay	50ns	*
S/H Aperture Uncertainty	1ns	*
Feedthrough Rejection[1]	− 100dB	*
Droop Rate	0.05μV/μs (0.1μV/μs max)	*
Dielectric Absorption Error	± 0.005% of Input Voltage Change	*
ACCURACY		
Integral Nonlinearity[2]	± 0.005% FSR[3] max	± 0.003% FSR[3] max
Differential Nonlinearity	± 0.003% FSR[3] max	± 0.002% FSR[3] max
No Missing Codes	(+ 10°C to + 40°C)	*
± 3σ Noise (S/H plus A/D)	75μV rms	*
± 3σ Noise (A/D)	50μV rms	*
STABILITY		
Differential Nonlinearity T.C.	± 2ppm/°C max	*
Gain T.C.	± 8ppm/°C max	*
Zero T.C.	± 30μV/°C typ, ± 80μV/°C max	*
Power Supply Sensitivity	± 0.001% FSR[3]/% V_s	*
ANALOG INPUT		
Voltage Range		
Bipolar	± 5V, ± 10V	*
Unipolar	0 to + 5V, 0 to + 10V	*
ADC Input Impedance 0 to + 5V	2.5kΩ	*
0 to + 10V, ± 5V	5kΩ	*
± 10V	10.0kΩ	*
S/H Input Impedance	100MΩ‖5pF	*
DIGITAL INPUTS		
Convert Command[4]	1TTL Load, Positive Pulse	*
	Negative Edge Triggered	*
S/H Control	HOLD = Logic 0	*
	SAMPLE = Logic 1	*
Low Enable, High Enable	ENABLE = Logic 0	*
DIGITAL OUTPUTS		
Parallel Data Outputs		
Unipolar	Binary	*
Bipolar	Offset Binary, 2's Complement	*
Output Drive	2TTL Loads	*
Status	Logic "1" During Conversion	*
Output Drive	2TTL Loads	*
INTERNAL REFERENCE VOLTAGE	+ 10V, ± 0.3%	*
External Load Current (Rated Performance)	2mA max	*
Temperature Stability	± 5ppm/°C max	*
POWER REQUIREMENTS		
Rated Voltages	± 15V (± 3%), + 5V (± 5%)	*
Operating Voltages[5]	± 12V to + 17V, + 4.75V to + 5.25V	*
Supply Current Drain ± 15V	± 37mA	*
+ 5V	80mA	*
TEMPERATURE RANGE		
Specified	0 to + 70°C	*
Operating	0 to + 70°C	*
Storage	− 25°C to + 85°C	*
Relative Humidity	Meets MIL-STD-202E, Method 103B	*
Shielding	Electrostatic (RFI) 6 Sides,	*
	Electromagnetic (EMI) 5 Sides	*
SIZE	2" × 4" × 0.44" Metal Package	*

NOTES

*Specifications same as DAS1152

[1] Measured in hold mode, input 20V pk-pk @ 10kHz.

[2] Worst-case summation of S/H and A/D nonlinearity errors.

[3] FSR means Full Scale Range.

[4] When connecting the Convert Command and the S/H control terminals together, the pulse width must be long enough for the S/H amplifier to acquire the input signal to the required accuracy 4μs (max, DAS1152)/5μs (max, DAS1153). If the A/D converter is only used, the Convert Command pulse width should be 100ns min.

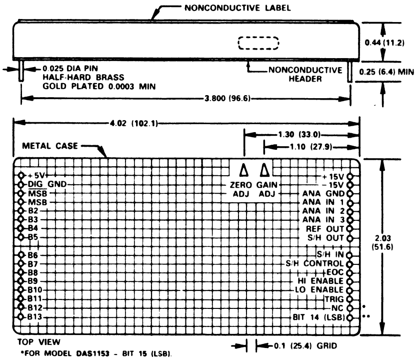
[5] If only the ADC portion is used, the operating power supply voltage can be maintained at ± 12V to ± 17V. But if the S/H section is required, the operating voltage must be maintained at ± 15V (± 3%) or the S/H input voltage must be limited to − 7V to + 10V for a ± 12V supply voltage.

[6] Recommended Power Supply: Analog Devices Model 923.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



TOP VIEW

*FOR MODEL DAS1153 – BIT 15 (LSB).

**FOR MODEL DAS1152 – BIT 14 (LSB).

CASE IS NOT HERMETICALLY SEALED

ANALOG
DEVICES

14-Bit & 15-Bit Low Level Data Acquisition Systems

DAS1155/DAS1156

FEATURES

Functionally Complete:
- **Includes Instrumentation Amplifier, Sample/Hold Amplifier, and Analog to Digital Converter**

Differential Nonlinearity: ±0.002% FSR max (DAS1156)
Guaranteed Nonlinearity: ±0.005% FSR (DAS1155)
±0.003% FSR (DAS1156)
High Common Mode Rejection: −80dB (up to 500Hz)
High Feedthrough Rejection: −96dB
Resistor Programmable Gain: 1V/V to 1000V/V
Byte Selectable Tri-State Buffer Outputs
Internal Gain and Offset Potentiometers

APPLICATIONS

Low Level High Accuracy Data Acquisition Systems
Process Control
Nuclear Instrumentation
Automated Test Equipment
Medical Instrumentation

GENERAL DESCRIPTION

The DAS1155/DAS1156 are 14-/15-bit low level data acquisition systems having a maximum throughput rate of 25kHz/20kHz. These data acquisition systems provide high accuracy, high stability, and functional completeness all in a 2″ × 4″ × 0.44″ metal case.

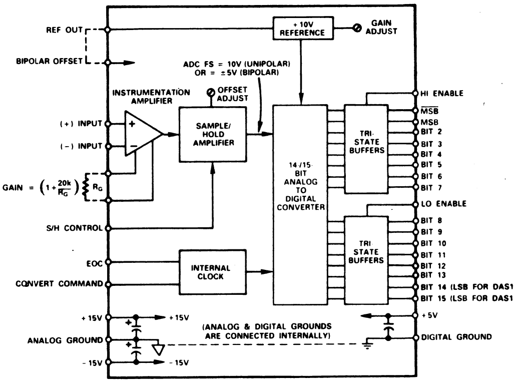
Guaranteed high accuracy system performance such as nonlinearity of ±0.005% FSR (DAS1155)/±0.003% FSR (DAS1156) and differential nonlinearity of ±0.003% FSR (DAS1155)/±0.002% FSR (DAS1156) are provided. Guaranteed stability such as differential nonlinearity T.C. of ±2ppm/°C maximum, offset T.C. of ±(1 + 50/G) μV/° (RTI) and gain T.C. (RTI) of ±16ppm/°C are also provided by the DAS1155/DAS1156.

Each DAS1155/DAS1156 makes extensive use of both integrated circuit and thin-film components to obtain its excellent performance and small size. Incorporated in these devices are a gain programmable instrumentation amplifier, precision sample/hold amplifier, high accuracy 14-/15-bit analog to digital converter, tri-state output buffers, gain and offset trim potentiometers, and power supply bypass capacitors (as shown in Figure 1).

Unipolar coding is provided for true binary format with bipolar coding displayed in offset binary or two's complement. Tri-state buffers are available for easy interface to bus structured applications.

This two-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be found in Volume II, page 15-29.

DAS1155/DAS1156
FUNCTIONAL BLOCK DIAGRAM



OPERATION

The DAS1155/DAS1156 are designed, built, and tested to meet system data acquisition requirements. These units can significantly reduce design and debug time by providing, in one package, all of the circuitry necessary for low level data acquisition and microprocessor bus interface.

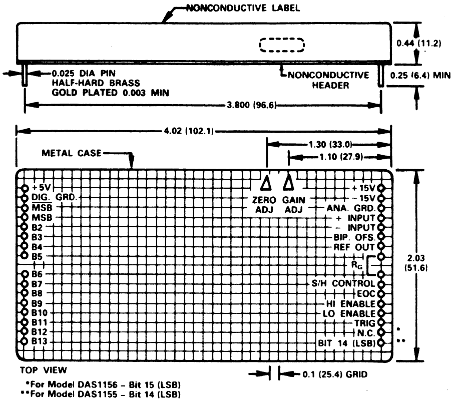
For operation, the only connections necessary to the DAS1155/DAS1156 are the ±15V and +5V power supplies, analog input signal, trigger pulse, and the HI-ENABLE/LO-ENABLE tri-state controls. Digital output programming is user selectable via external jumper connections.

SPECIFICATIONS (typical @ +25°C and rated supplies unless otherwise noted)

MODEL	DAS1155	DAS1156
RESOLUTION	14 Bits	15 Bits
DYNAMIC CHARACTERISTICS		
ADC Conversion Time	35µs max	44µs max
IA Settling Time, (10V Output Step)		
to 0.003% FSR @ G = 1	15µs max	*
to 0.003% FSR @ G = 10	15µs max	*
to 0.01% FSR @ G = 1000	50µs max	*
Throughput Rate @ G = 1, 10	25kHz max	20kHz max
SAMPLE HOLD		
Acquisition Time	4µs max	5µs max
Aperature Delay Time	50ns	*
Aperture Uncertainty Time	1ns	*
Feedthrough Rejection [1]	−96dB	*
Droop Rate	0.05µV/µs	*
ACCURACY		
Differential Nonlinearity (FSR)[2]	±0.003% max	±0.002% max
Integral Nonlinearity (FSR)[3]	±0.005% max	±0.003% max
No Missing Codes	Guaranteed	*
Offset Error	Adjustable to Zero	*
Gain Error	Adjustable to Zero	*
TEMPERATURE COEFFICIENTS		
Offset (RTI)	$\pm\left(1 + \frac{50}{G}\right)\mu V/^\circ C$	*
Gain (RTI)	±16ppm/°C	*
Differential Nonlinearity	±2ppm/°C max	*
ANALOG INPUTS		
Voltage Input Range $\left(\frac{\text{ADC FSR}}{\text{Gain}}\right)$	+10mV to +10V (Unipolar) ±5mV to ±5V (Bipolar)	* *
Instrumentation Amplifier		
Gain	Resistor Programmable	*
Gain Range	1 to 1000	*
Gain Equation	$G = 1 + \left(\frac{20k\Omega}{R_G}\right)$	*
Input Impedance	$10^8\Omega$	*
Bias Current	50nA	*
Offset Current	2nA	*
CMR (up to 500Hz)	−80dB	*
CMV	±10V	*
DIGITAL INPUTS		
ADC Convert Command[4]	1TTL Load, Positive Pulse Negative Edge Triggered	
SHA Control	HOLD = Logic 0 SAMPLE = Logic 1	
Low Enable, High Enable	ENABLE = Logic 0	
DIGITAL OUTPUTS		
Parallel Data Outputs	Tri-State	
Unipolar	Binary	
Bipolar	Offset Binary, 2's Complement	
Output Drive	2TTL Loads	
Status	Logic "1" During Conversion	
Output Drive	2TTL Loads	
INTERNAL REFERENCE VOLTAGE	+10V, ±0.3%	
External Load Current (Rated Performance)	2mA (max)	
Temperature Stability	±8.5ppm/°C (max)	
POWER REQUIREMENTS		
Rated Voltages	±15V ±5%, +5V ±5%	
Operating Voltages[5]	±12V to ±17V, +4.75V to +5.25V	
Supply Current Drain ±15V	±45mA	
+5V	80mA	
TEMPERATURE RANGE		
Specified	0 to +70°C	
Storage	−25°C to +85°C	
Relative Humidity	(Meets MIL-STD-202E, Method 103B)	
SHIELDING	Electrostatic (RFI) 6 sides, Electromagnet (EMI) 5 sides	
SIZE	2" × 4" × 0.44" metal package	

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



INTERCONNECTION AND SHIELDING TECHNIQUES

To preserve the high CMR characteristics of the DAS1155/DAS1156, care must be taken to minimize noise wherever possible. For best performance use twisted shielded cable, for the sensitive input signal, to reduce inductive and capacitive pickup. The cable should be connected as close as possible to the input common mode signal source. Place the gain setting resistor as close as possible to its respective terminal connections to avoid pickup.

NOTES

[1] Measured in hold mode, input 20V pk-pk @ 10kHz.

[2] FSR means Full Scale Range.

[3] Worst-case summation of IA, S/H and A/D nonlinearity errors.

[4] When connecting the Convert Command the S/H control terminals together, the pulse width must be long enough for the S/H amplifier to acquire the input signal to the required accuracy 4µs (min, DAS1155) 5µs (min, DAS1156).

[5] If a ±12V operating power supply is used, the analog input must be limited to ±7V.

[6] Recommended Power Supply: Analog Devices Model 923.

*Same specifications as for DAS1155.

Specifications subject to change without notice.

CMOS Switches & Multiplexers

Contents

	Page
Selection Guide	16–3
General Information and Definitions of Specifications	16–4
AD7501 8-Channel Multiplexer, High Enables	16–5
AD7502 4-Channel Differential Multiplexer	16–5
AD7503 8-Channel Multiplexer, Low Enables	16–5
AD7506 16-Channel Multiplexer	16–9
AD7507 8-Channel Differential Multiplexer	16–9
AD7510DI Dielectrically Isolated Quad SPST; Address High Closes Switch	16–13
AD7511DI Dielectrically Isolated Quad SPST; Address Low Closes Switch	16–13
AD7512DI Dielectrically Isolated Quad SPDT	16–13
•AD7590DI Dielectrically Isolated Quad SPST; Data Latches	16–21
•AD7591DI Dielectrically Isolated Quad SPST; Data Latches	16–21
•AD7592DI Dielectrically Isolated Dual SPDT; Data Latches	16–21
ADG200 Dielectrically Isolated Dual SPST, Replaces DG200	16–29
ADG201 Dielectrically Isolated Quad SPST, Replaces DG201	16–33

•New product since the *1980 Data-Acquisition Components and Subsystems Catalog*

Selection Guide
CMOS Switches & Multiplexers

The devices catalogued in this section are grouped into two classes: Switches and Multiplexers. Descriptions, specifications, and application information can be found in the data sheets; definitions of the terminology can be found in the following pages.

CMOS IC SWITCHES

Type	Characteristics	Vol I Page
AD7510DI	Dielectrically isolated Quad SPST; Address High closes switch	16–13
AD7511DI	Dielectrically isolated Quad SPST; Address Low closes switch	16–13
ADG201	Dielectrically isolated Quad SPST, replace DG201	16–33
ADG200	Dielectrically isolated Dual SPST, replace DG200	16–29
AD7512DI	Dielectrically isolated Quad SPDT	16–13
•AD7590DI	Dielectrically Isolated Quad SPST; Data Latches	16–21
•AD7591DI	Dielectrically Isolated Quad SPST; Data Latches	16–21
•AD7592DI	Dielectrically Isolated Dual SPST; Data Latches	16–21

CMOS IC MULTIPLEXERS

Type	Characteristics	Vol I Page
AD7501	8-channel multiplexer, High enables	16–5
AD7503	8-channel multiplexer, Low enables	16–5
AD7502	4-channel differential multiplexer	16–5
AD7506	16-channel multiplexer	16–9
AD7507	8-channel differential multiplexer	16–9

•New product since the *1980 Data-Acquisition Components and Subsystems Catalog.*

Orientation
CMOS Switches & Multiplexers

Analog Devices offers a complete line of monolithic CMOS analog multiplexers and switches, which utilize a high-breakdown CMOS process, in conjunction with a double-layer interconnect for high density. Both 8- and 16-channel multiplexers are available, in one-line and two-line (4- and 8-channel differential) versions. The switches are dielectrically isolated duals and quads, available in a variety of contact forms. Both direct and inverted logic options are available for the most-popular types. The popular AD7510/11/12DI (quad SPST/dual SPDT), which utilize dielectric isolation, are latchup-proof and can withstand overrange to ±25V beyond the supplies.

CMOS switches have extremely low quiescent power dissipation, require little drive or supply current while switching, and are low in cost. Their R_{ON} is low and is, to a first-order, independent of applied voltage; in the off condition, leakage is quite small, both across the gate and to the drive and supply circuits. Most types respond to TTL/DTL, as well as CMOS, logic.

Definitions for terminal nomenclature used in the data sheets are given below, and a summary of device functions appears on the preceding page. General information on the nature of CMOS, its advantages, its applications, and its protection, is to be found in the *Guide to CMOS Switches and Multiplexers*, available from Analog Devices upon request.

MULTIPLEXER TERMINOLOGY

R_{ON}:	Ohmic resistance between the output and an addressed input.
R_{ON} vs. Temperature:	R_{ON} drift over the temperature range.
ΔR_{ON} between Switches:	Difference between the R_{ON}'s of any two switches.
R_{ON} vs. Temperature between Switches:	Difference between the R_{ON} drifts of any two switches.
I_S:	Current at any switch input, S1 through S_N. This is a leakage current when the switch is open.
I_{OUT}:	Current at the output. This is a leakage current when all switches are open.
$I_{OUT} - I_S$:	Difference between the current going into terminal "S" and the current going out of terminal "out" when terminal "S" is addressed.
V_{INL}:	Digital threshold voltage for the low state.
V_{INH}:	Digital threshold voltage for the high state.
C_S:	Capacitance between any open terminal "S" and ground.
C_{OUT}:	Capacitance between the output terminal and ground with all switches open.
$C_{S - OUT}$:	Capacitance between any open terminal "S" and the output terminal.
C_{SS}:	Capacitance between any two "S" terminals.
$t_{transition}$:	Delay time when switching from one address state to another.
t_{open}:	"OFF" time of both switches when switching from one address state to another.
t_{on} (En):	Delay time between the 50% points of the enable input and the switch "ON" condition.
t_{off} (En):	Delay time between the 50% points of the enable input and the switch "OFF" condition.
V_{DD}:	Most positive voltage supply.
V_{SS}:	Most negative voltage supply.
I_{DD}:	Positive supply current.
I_{SS}:	Negative supply current.

SWITCH TERMINOLOGY

R_{DS}:	Ohmic resistance between terminals D and S.
I_D (I_S):	Current at terminals D or S. This is a leakage current when the switch is OFF.
I_{DS}:	Current flowing through the closed switch.
$I_D - I_S$:	Leakage current that flows from the closed switch into the body. (This leakage will show up as the difference between the current I_D going into the switch and the outgoing current I_S.)
V_D (V_S):	Analog voltage on terminal D (S).
C_S (C_D):	Capacitance between terminal S (D) and ground. (This capacitance is specified for the switch open and closed.)
C_{DS}:	Capacitance between terminals D and S. (This will determine the switch isolation over frequency.)
C_{DD} (C_{SS}):	Capacitance between terminals D (S) of any 2 switches. (This will determine the cross coupling between switches vs. frequency.)
t_{ON}:	Delay time between the 50% points of the digital input and switch "ON" condition.
t_{OFF}:	Delay time between the 50% points of the digital input and switch "OFF" condition.
V_{INL}:	Threshold voltage for the low state.
V_{INH}:	Threshold voltage for the high state.
I_{INL} (I_{INH}):	Input current of the digital input.
C_{IN}:	Input capacitance to ground of the digital input.
V_{DD}:	Most positive voltage supply.
V_{SS}:	Most negative voltage supply.
I_{DD}:	Positive supply current.
I_{SS}:	Negative supply current.

ANALOG DEVICES

CMOS
4/8 Channel Analog Multiplexers
AD7501, AD7502, AD7503

FEATURES

DTL/TTL/CMOS Direct Interface
Power Dissipation: 30μW
R_{ON}: 170Ω
Output "Enable" Control
AD7503 Replaces HI-1818

GENERAL DESCRIPTION

The AD7501 and AD7503 are monolithic CMOS, 8-channel analog multiplexers which switches one of 8 inputs to a common output depending on the state of three binary address lines and an "enable" input. The AD7503 is identical to the AD7501 except its "enable" logic is inverted. All digital inputs are TTL/DTL and CMOS logic compatible.

The AD7502 is a monolithic CMOS dual 4-channel analog multiplexer. Depending on the state of 2 binary address inputs and an "enable", it switches two output buses to two of 8 inputs.

All 3 devices are excellent examples of a high breakdown CMOS process combined with a double layer interconnect for high density. Silicon nitride passivation ensures long term stability and reliability.

PACKAGE IDENTIFICATION[1]

Suffix D: Ceramic DIP – (D16B)
Suffix N: Plastic DIP – (N16B)

[1] See Section 20 for package outline information.

ABSOLUTE MAXIMUM RATINGS

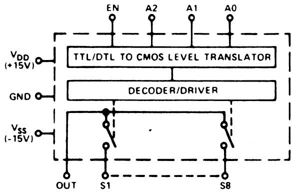
(T_A = +25°C unless otherwise noted)

V_{DD} – GND	+17V
V_{SS} – GND	-17V
V Between Any Switch Terminals	25V
Switch Current (I_S, Continuous)	35mA
Switch Current (I_S, Surge)	
1ms duration, 10% duty cycle	50mA
Digital Input Voltage Range	V_{DD} to GND
Power Dissipation (package)	
16 pin Ceramic DIP	
Up to +75°C	450mW
Derates above +75°C by	6mW/°C
16 pin Plastic DIP	
Up to +70°C	670mW
Derates above +70°C by	8.3mW/°C
Operating Temperature	
Plastic (JN, KN versions)	0 to +70°C
Ceramic (JD, KD versions)	-25°C to +85°C
Ceramic (SD versions)	-55°C to +125°C
Storage Temperature	-65°C to +150°C

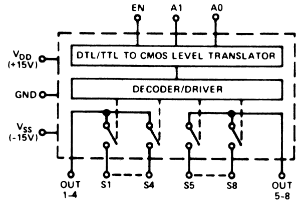
CAUTION:

1. Do not apply voltages higher than V_{DD} and V_{SS} to any other terminal, especially when V_{SS} = V_{DD} = 0V all other pins should be at 0V.
2. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

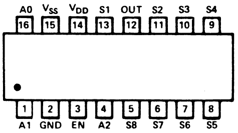
AD7501, AD7503 FUNCTIONAL BLOCK DIAGRAM



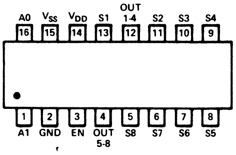
AD7502 FUNCTIONAL BLOCK DIAGRAM



AD7501, AD7503
PIN CONFIGURATION



AD7502
PIN CONFIGURATION



(NOT TO SCALE)

16-PIN DIP
TOP VIEW

SPECIFICATIONS (V_{DD} = +15V, V_{SS} = −15V unless otherwise noted)

PARAMETER	VERSION[1]	SWITCH CONDITION	@25°C AD7501, AD7503	@25°C AD7502	OVER SPECIFIED TEMP. RANGE AD7501, AD7503	OVER SPECIFIED TEMP. RANGE AD7502	TEST CONDITIONS
ANALOG SWITCH							
R_{ON}	All	ON	170Ω typ, 300Ω max	*			−10V ≤ V_S ≤ +10V
R_{ON} vs. V_S	All	ON	20% typ	*			I_S = 1.0mA
R_{ON} vs. Temperature	All	ON	0.5%/°C typ	*			V_S = 0V, I_S = 1.0mA
ΔR_{ON} Between Switches	All	ON	4% typ	*			
R_{ON} vs. Temperature Between Switches	All	ON	±0.01%/°C	*			
I_S	J, K	OFF	0.2nA typ, 2nA max	*	50nA max	*	V_S = −10V, V_{OUT} = +10V and V_S = +10V, V_{OUT} = −10V
	S	OFF	0.5nA max	*	50nA max	*	
I_{OUT}	J, K	OFF	1nA typ, 10nA max	0.6nA typ, 5nA max	250nA max	125nA max	V_S = −10V, V_{OUT} = +10V and V_S = +10V, V_{OUT} = −10V
	S	OFF	5nA max	3nA max	250nA max	125nA max	AD7501/02: Enable LOW AD7503: Enable HIGH
$\lvert I_{OUT} - I_S \rvert$	J, K	ON	12nA max	7nA max	300nA max	175nA max	V_S = 0
	S	ON	5.5nA max	3.5nA max	300nA max	175nA max	
DIGITAL CONTROL							
V_{INL}	All				0.8V max	*	
V_{INH}	J				3.0V min	*	Note 2
	K, S				2.4V min	*	
I_{INL} or I_{INH}	All		10nA typ	*			
C_{IN}	All		3pF typ	*			
DYNAMIC CHARACTERISTICS							
t_{ON}	All		0.8μs typ	*			V_{IN} = 0 to +5.0V (See Test Circuit 2)
t_{OFF}	All		0.8μs typ	*			
C_S	All	OFF	5pF typ	*			
C_{OUT}	All	OFF	30pF typ	15pF typ			
$C_{S\text{-}OUT}$	All	OFF	0.5pF typ	*			
C_{SS} Between Any Two Switches	All	OFF	0.5pF typ	*			
POWER SUPPLY							
I_{DD}	All		500μA max	*	500μA max	*	All Digital Inputs Low
I_{SS}	All		500μA max	*	500μA max	*	
I_{DD}	All		800μA max	*	800μA max	*	All Digital Inputs High
I_{SS}	All		800μA max	*	800μA max	*	

NOTES

*Same specifications as AD7501 and AD7503.

[1] JN, KN versions specified for 0 to +70°C; JD, KD versions for −25°C to +85°C; and SD versions for −55°C to +125°C.

[2] A pullup resistor, typically 1-2kΩ is required to make the AD7501J, AD7502J compatible with TTL/DTL levels. The maximum value is determined by the output leakage current of the driver gate when in the high state.

Specifications subject to change without notice.

TRUTH TABLES

AD7501

A_2	A_1	A_0	E_N	"ON"
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8
X	X	X	0	None

AD7502

A_1	A_0	E_N	"ON"
0	0	1	1 & 5
0	1	1	2 & 6
1	0	1	3 & 7
1	1	1	4 & 8
X	X	0	None

AD7503

A_2	A_1	A_0	E_N	"ON"
0	0	0	0	1
0	0	1	0	2
0	1	0	0	3
0	1	1	0	4
1	0	0	0	5
1	0	1	0	6
1	1	0	0	7
1	1	1	0	8
X	X	X	1	None

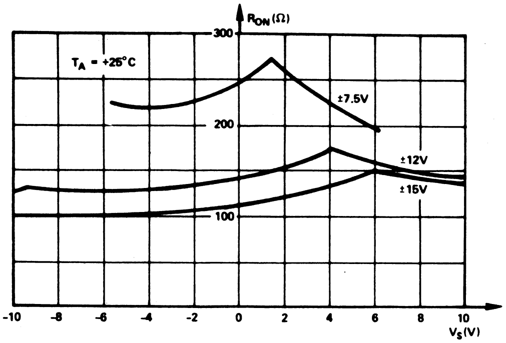
ORDERING INFORMATION

Plastic (Suffix N)	Ceramic (Suffix D)	Operating Temperature Range
AD7501JN AD7501KN AD7503JN AD7503KN		0 to +70°C
	AD7501JD AD7501KD AD7503JD AD7503KD	−25°C to +85°C
	AD7501SD AD7503SD	−55°C to +125°C
AD7502JN AD7502KN		0 to +70°C
	AD7502JD AD7502KD	−25°C to +85°C
	AD7502SD	−55°C to +125°C

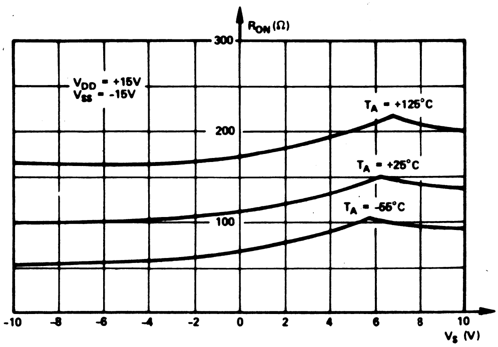
Note: Ceramic versions are available 100% screened to MIL-STD-883, method 5004 for a class B device. To order, add "/883B" to model number.

Typical Performance Characteristics

1. R_{ON} As A Function Of Switch Voltage (V_S)

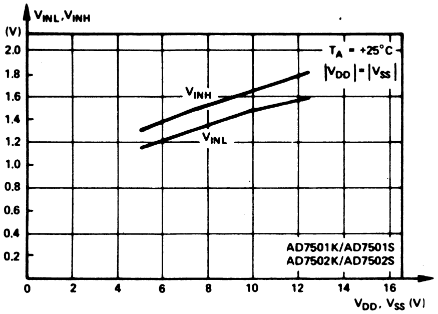


At Different Power Supplies

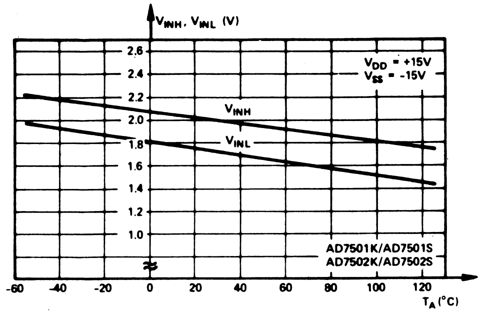


At Different Temperatures

2. Digital Threshold Voltage (V_{INH}, V_{INL})

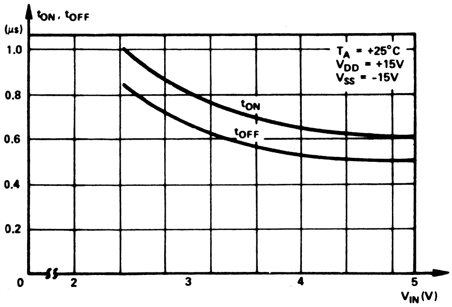


vs. Power Supply



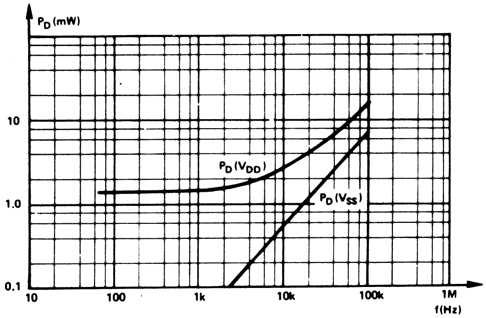
vs. Temperature

3. T_{ON}, T_{OFF}



vs. Digital Input Voltage

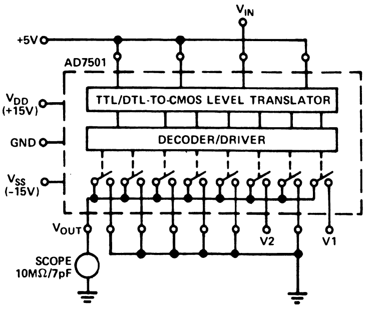
4. Power Dissipation



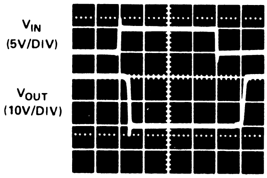
vs. Logic Frequency (50% Duty Cycle)

TYPICAL SWITCHING CHARACTERISTICS

TEST CIRCUIT 1

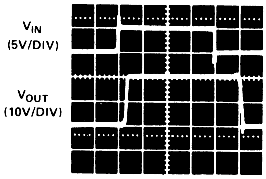


1μs/DIV



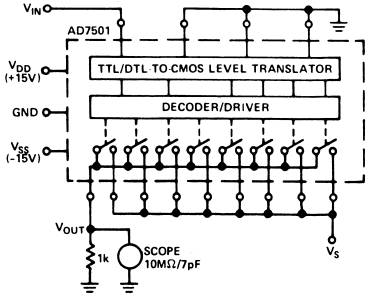
V_1 = -10V, V_2 = +10V

1μs/DIV

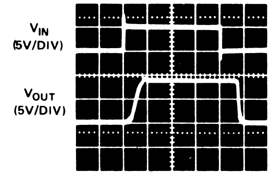


V_1 = +10V, V_2 = -10V

TEST CIRCUIT 2

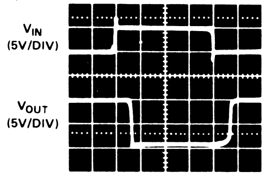


1μs/DIV



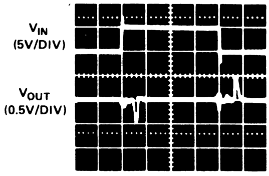
V_S = +10V

1μs/DIV



V_S = -10V

1μs/DIV



V_S = OPEN

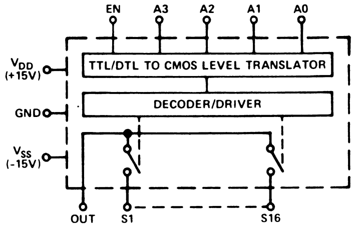
ANALOG DEVICES

CMOS 8- and 16-Channel Analog Multiplexers

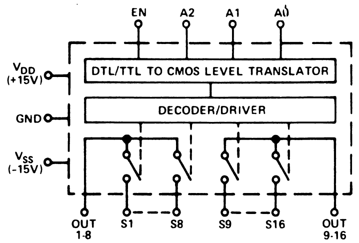
AD7506, AD7507

FEATURES
R_{ON}: 300Ω
Power Dissipation: 1.5mW
TTL/DTL/CMOS Direct Interface
Break-Before-Make Switching
Replaces DG506/DG507

AD7506 FUNCTIONAL BLOCK DIAGRAM



AD7507 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7506 is a monolithic CMOS 16-channel analog multiplexer packaged in a 28-pin DIP. It switches a common output to one of 16 inputs, depending on the state of four address lines and an "enable". The AD7507 is identical to the AD7506 except it has two outputs switched to two of 16 inputs depending on three binary address states and an "enable".

ABSOLUTE MAXIMUM RATINGS

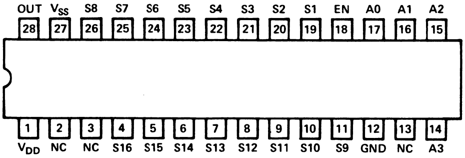
(T_A = +25°C unless otherwise noted)

V_{DD} – GND	+17V
V_{SS} – GND	–17V
V Between Any Switch Terminals	25V
Digital Input Voltage Range	V_{DD} to GND
Switch Current (I_S, Continuous)	20mA
Switch Current (I_S, Surge)	
1ms duration, 10% duty cycle	35mA
Power Dissipation (Package)	
28 pin Ceramic DIP	
Up to +50°C	1000mW
Derates above +50°C by	10mW/°C
28 pin Plastic DIP	
Up to +50°C	1200mW
Derates above +50°C by	12mW/°C
Operating Temperature	
Plastic (J, K versions)	0 to +70°C
Ceramic (J, K versions)	–25°C to +85°C
Ceramic (S, T versions)	–55°C to +125°C
Storage Temperature	–65°C to +150°C

CAUTION:

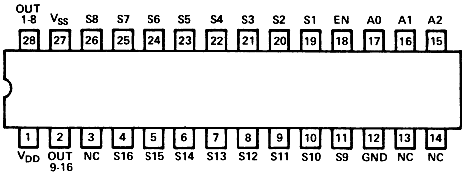
1. Do not apply voltages higher than V_{DD} and V_{SS} to any other terminal, especially when V_{SS} = V_{DD} = 0V all other pins should be at 0V.
2. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

AD7506 PIN CONFIGURATION TOP VIEW



(NOT TO SCALE)

AD7507 PIN CONFIGURATION TOP VIEW



(NOT TO SCALE)

SPECIFICATIONS (V_{DD} = +15V, V_{SS} = -15V unless otherwise noted)

PARAMETER		VERSION[1]	SWITCH CONDITION	@ +25°C	OVER SPECIFIED TEMP. RANGE	TEST CONDITIONS
ANALOG SWITCH						
R_{ON}		J, K	ON	300Ω typ, 450Ω max	550Ω max	V_S = -10V to +10V, I_S = 1mA
		S, T	ON	400Ω max	500Ω max	
R_{ON} vs. V_S		All	ON	15% typ		
R_{ON} vs. Temperature		All	ON	0.5%/°C typ		V_S = 0V, I_S = 1mA
ΔR_{ON} Between Switches		All	ON	4% typ		
R_{ON} vs. Temperature Between Switches		All	ON	0.05%/°C typ		
I_S (OFF)		J, K	OFF	0.05nA typ, 5nA max	50nA max	V_S = -10V, V_{OUT} = +10V and V_S = +10V, V_{OUT} = -10V "Enable" Low
		S, T	OFF	0.05nA typ, 1nA max	50nA max	
I_{OUT} (OFF)	AD7506	J, K	OFF	0.3nA typ, 20nA max	500nA max	
		S, T	OFF	0.3nA typ, 10nA max	500nA max	
	AD7507	J, K	OFF	0.3nA typ, 10nA max	250nA max	
		S, T	OFF	0.3nA typ, 5nA max	250nA max	
$I_{OUT} - I_S$ (Any Switch ON)	AD7506	J, K	ON	0.3nA typ, 20nA max	500nA max	V_S = 0
		S, T	ON	0.3nA typ, 10nA max	500nA max	
	AD7507	J, K	ON	0.3nA typ, 10nA max	250nA max	
		S, T	ON	0.3nA typ, 5nA max	250nA max	
DIGITAL CONTROL						
V_{INL}					0.8V max	Note 2
		J, S			3.0V min	
V_{INH}		K, T			2.4V min	
I_{INL} or I_{INH}		All		10μA max	30μA max	
C_{IN}		All		3pF typ		
DYNAMIC CHARACTERISTICS[3]						
$t_{TRANSITION}$		J, S		700ns typ		V_{IN}: 0 to 3.0V
		K, T		700ns typ, 1000ns max		
t_{OPEN}		All		100ns typ		
t_{ON} (En)		J, S		0.8μs typ		V_{EN}: 0 to 3.0V
		K, T		1.5μs max		
t_{OFF} (En)		J, S		0.8μs typ		
		K, T		1μs max		
"OFF" Isolation		All		70dB typ		V_{EN} = 0, R_L = 200Ω, C_L = 3.0pF, V_S = 3.0V rms, f = 50kHz
C_S		All	OFF	5pF typ		
C_{OUT}	AD7506	All	OFF	40pF typ		
	AD7507	All	OFF	20pF typ		
C_{S-OUT}		All	OFF	0.5pF typ		
C_{SS} Between Any Two Switches		All	OFF	0.5pF typ		
POWER SUPPLY						
I_{DD}		J, K	OFF	0.05mA typ, 1mA max		All Digital Inputs Low
		S, T	OFF	0.05mA typ, 1mA max	2mA max	
I_{SS}		J, K	OFF	0.05mA typ, 1mA max		
		S, T	OFF	0.05mA typ, 1mA max	2mA max	
I_{DD}		J, K	ON	0.3mA typ, 1mA max		All Digital Inputs High
		S, T	ON	0.3mA typ, 1mA max	2mA max	
I_{SS}		J, K	ON	0.05mA typ, 1mA max		
		S, T	ON	0.05mA typ, 1mA max	2mA max	

NOTES:

[1] JN, KN versions specified for 0 to +70°C; JD, KD versions for -25°C to +85°C; and SD, TD versions for -55°C to +125°C.

[2] A pullup resistor, typically 1-2kΩ is required to make the J and S versions compatible with TTL/DTL. The maximum value is determined by the output leakage current of the driver gate when in the high state.

[3] AC parameters are sample tested to ensure conformance to specifications.

Specifications subject to change without notice.

TRUTH TABLES

AD7506

A_3	A_2	A_1	A_0	E_N	"ON"
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16
X	X	X	X	0	None

AD7507

A_2	A_1	A_0	E_N	"ON"
0	0	0	1	1 & 9
0	0	1	1	2 & 10
0	1	0	1	3 & 11
0	1	1	1	4 & 12
1	0	0	1	5 & 13
1	0	1	1	6 & 14
1	1	0	1	7 & 15
1	1	1	1	8 & 16
X	X	X	0	None

ORDERING INFORMATION

	Operating Temperature Range
AD7506JN AD7506KN AD7507JN AD7507KN	0 to +70°C
AD7506JD AD7506KD AD7507JD AD7507KD	-25°C to +85°C
AD7506SD AD7506TD AD7507SD AD7507TD	-55°C to +125°C

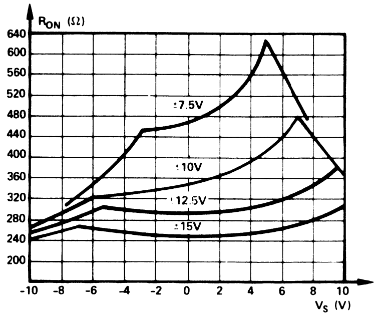
PACKAGE IDENTIFICATION[1]

Suffix D: Ceramic DIP – (D28A)
Suffix N: Plastic DIP – (N28A)

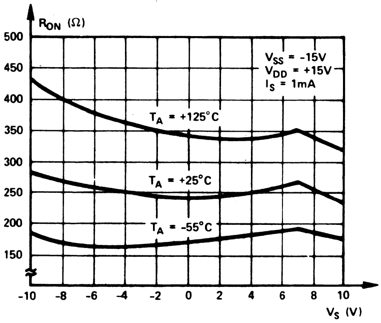
[1] See Section 20 for package outline information.

Typical Performance Characteristics

1. R_{ON} vs. V_S

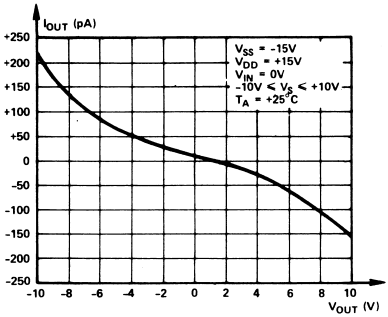


At Different Power Supplies

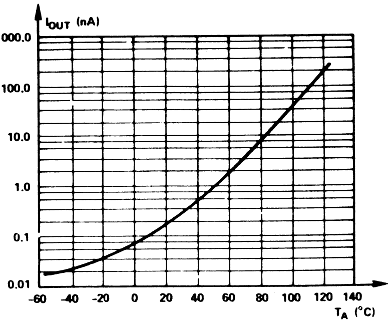


At Different Temperatures

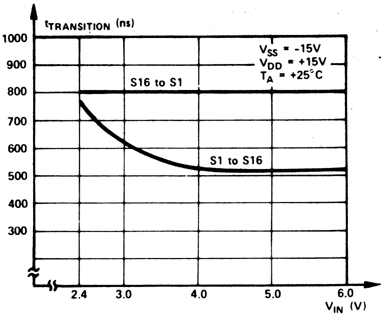
2. I_{OUT} vs. V_{OUT}



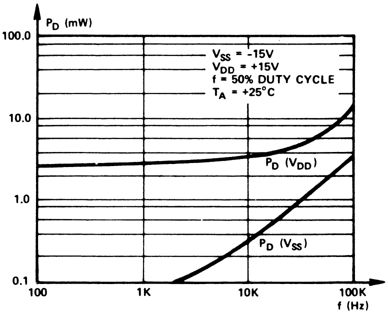
3. I_{OUT} vs. T_A



4. $t_{TRANSITION}$ vs. V_{IN}

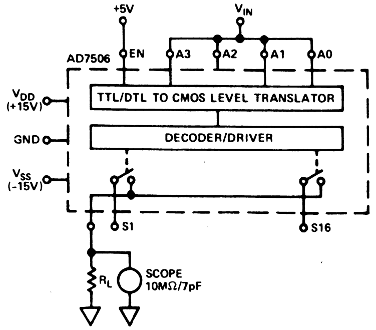


5. P_D vs. Logic Frequency

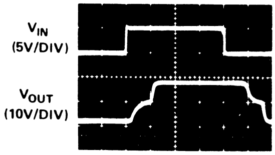


TYPICAL SWITCHING CHARACTERISTICS

TEST CIRCUIT 1

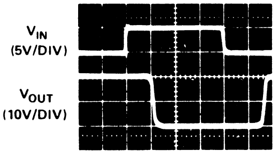


0.5µs/DIV



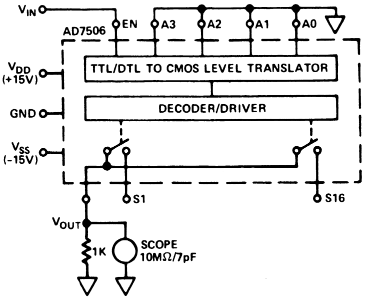
$S_1 = -10V, S_{16} = +10V,$
$S_2 - S_{15} = 0V, R_L = 1K$

0.5µs/DIV

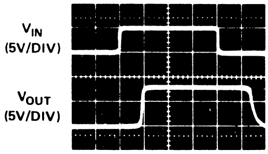


$S_1 = +10V, S_2 = -10V,$
$S_2 - S_{15} = 0V, R_L = \infty$

TEST CIRCUIT 2

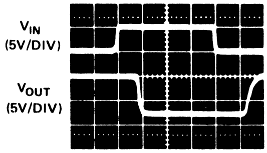


0.5µs/DIV



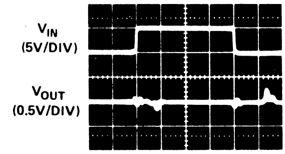
S_1 through $S_{16} = +10V$

0.5µs/DIV



S_1 through $S_{16} = -10V$

0.5µs/DIV



S_1 through $S_{16} = 0V$

ANALOG DEVICES

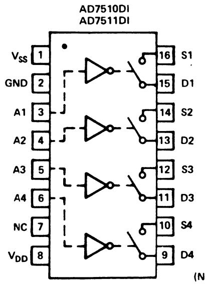
DI CMOS Protected Analog Switches

AD7510DI, AD7511DI, AD7512DI

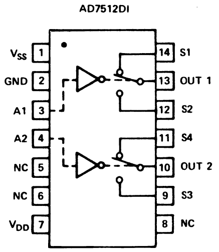
FEATURES

Latch-Proof
Overvoltage-Proof: ±25V
Low R_{ON}: 75Ω
Low Dissipation: 3mW
TTL/CMOS Direct Interface
Silicon-Nitride Passivated
Monolithic Dielectrically-Isolated CMOS

AD7510DI, AD7511DI, AD7512DI FUNCTIONAL BLOCK DIAGRAMS



16-PIN DIP
TOP VIEW



(NOT TO SCALE)

14-PIN DIP
TOP VIEW

GENERAL DESCRIPTION

The AD7510DI, AD7511DI and AD7512DI are a family of latch proof dielectrically isolated CMOS switches featuring overvoltage protection up to ±25V above the power supplies. These benefits are obtained without sacrificing the low "ON" resistance (75Ω) or low leakage current (400pA), the main features of an analog switch.

The AD7510DI and AD7511DI consist of four independent SPST analog switches packaged in a 16-pin DIP. They differ only in that the digital control logic is inverted. The AD7512DI has two independent SPDT switches packaged in a 14-pin DIP.

Very low power dissipation, overvoltage protection and TTL/CMOS direct interfacing are achieved by combining a unique circuit design and a dielectrically isolated CMOS process. Silicon nitride passivation ensures long term stability while monolithic construction provides reliability.

PACKAGE IDENTIFICATION[1]

Suffix D: Ceramic DIP
AD7510DI, AD7511DI – (D16B)
AD7512DI – (D14B)
Suffix N: Plastic DIP
AD7510DI, AD7511DI – (N16B)
AD7512DI – (N14B)

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[1] See Section 20 for package outline information.

ORDERING INFORMATION

Plastic	Ceramic	Operating Temperature Range
AD7510DIJN AD7510DIKN AD7511DIJN AD7511DIKN AD7512DIJN AD7512DIKN		0 to +70°C
	AD7510DIJD AD7510DIKD AD7511DIJD AD7511DIKD AD7512DIJD AD7512DIKD	−25°C to +85°C
	AD7510DISD AD7511DISD AD7511DITD AD7512DISD AD7512DITD	−55°C to +125°C

CONTROL LOGIC

AD7510DI: Switch "ON" for Address "HIGH"

AD7511DI: Switch "ON" for Address "LOW"

AD7512DI: Address "HIGH" makes S1 to Out 1 and S3 to Out 2

SPECIFICATIONS (V_{DD} = +15V, V_{SS} = −15V unless otherwise noted)

COMMERCIAL VERSIONS (J, K)

PARAMETER	MODEL	VERSION	+25°C	0 to +70°C (N) -25°C to +85°C (D)	TEST CONDITIONS
ANALOG SWITCH					
R_{ON}[1]	All	J, K	75Ω typ, 100Ω max	175Ω max	$-10V \leqslant V_D \leqslant +10V$
R_{ON} vs V_D (V_S)	All	J, K	20% typ		I_{DS} = 1.0mA
R_{ON} Drift	All	J, K	+0.5%/°C typ		V_D = 0, I_{DS} = 1.0mA
R_{ON} Match	All	J, K	1% typ		
R_{ON} Drift Match	All	J, K	0.01%/°C typ		
I_D (I_S) OFF[1]	All	J, K	0.5nA typ, 5nA max	500nA max	V_D = -10V, V_S = +10V and V_D = +10V, V_S = -10V
I_D (I_S)ON[1]	All	J, K	10nA max		V_S = V_D = +10V V_S = V_D = -10V
I_{OUT}[1]	AD7512DI	J, K	15nA max	1500nA max	V_{S1} = V_{OUT} = ±10V, V_{S2} = ∓10V and V_{S2} = V_{OUT} = ±10V, V_{S1} = ∓10V
DIGITAL CONTROL					
V_{INL}[1]	All	J, K		0.8V max	
V_{INH}[1]	All	J		3.0V min	
	All	K		2.4V min	
C_{IN}	All	J, K	3pF typ		
I_{INH}[1]	All	J, K	10nA max		V_{IN} = V_{DD}
I_{INL}[1]	All	J, K	10nA max		V_{IN} = 0
DYNAMIC CHARACTERISTICS					
t_{ON}	AD7510DI	J, K	180ns typ		V_{IN} = 0 to +3.0V
	AD7511DI	J, K	350ns typ		
t_{OFF}	AD7510DI	J, K	350ns typ		
	AD7511DI	J, K	180ns typ		
$t_{TRANSITION}$	AD7512DI	J, K	300ns typ		
C_S (C_D)OFF	All	J, K	8pF typ		V_D (V_S) = 0V
C_S (C_D)ON	All	J, K	17pF typ		
C_{DS} (C_{S-OUT})	All	J, K	1pF typ		
C_{DD} (C_{SS})	All	J, K	0.5pF typ		
C_{OUT}	AD7512DI	J, K	17pF typ		
Q_{INJ}	All	J, K	30pC typ		Measured at S or D terminal. C_L = 1000pF, V_{IN} = 0 to 3V, V_D (V_S) = +10V to -10V
POWER SUPPLY					
I_{DD}[1]	All	J, K	800μA max	800μA max	All digital inputs = V_{INH}
I_{SS}[1]	All	J, K	800μA max	800μA max	
I_{DD}[1]	All	J, K	500μA max	500μA max	All digital inputs = V_{INL}
I_{SS}[1]	All	J, K	500μA max	500μA max	
I_{DD}[1]	All	J, K	800μA max		All digital inputs = V_{INH}
I_{SS}[1]	All	J, K	800μA max		
I_{DD}[1]	All	J, K	500μA max		All digital inputs = V_{INL}
I_{SS}[1]	All	J, K	500μA max		

NOTES:

[1] 100% tested.

Specifications subject to change without notice.

MILITARY VERSIONS (S, T)

PARAMETER	MODEL	VERSION	+25°C	-55°C to +125°C	TEST CONDITIONS
ANALOG SWITCH					
R_{ON}[1]	All	S, T	100Ω max	175Ω max	$-10V \leq V_D \leq +10V$ $I_{DS} = 1mA$
I_D $(I_S)_{OFF}$[1]	All	S, T	3nA max	200nA max	$V_D = -10V$, $V_S = +10V$ and $V_D = +10V$, $V_S = -10V$
I_D $(I_S)ON$[1]	All	S, T	10		$V_S = V_D = +10V$ and $V_S = V_D = -10V$
I_{OUT}[1]	AD7512DI	S, T	9nA max	600nA max	$V_{S1} = V_{OUT} = \pm 10V$ $V_{S2} = \mp 10V$ and $V_{S2} = V_{OUT} = \pm 10V$ $V_{S1} = \mp 10V$
DIGITAL CONTROL					
V_{INL}[1]	All	S, T		0.8V max	
V_{INH}[1,2]	AD7510DI	S		2.4V min	
	AD7511DI	T		2.4V min	
	AD7512DI	T		2.4V min	
	AD7511DI	S		3.0V min	
	AD7512DI	S		3.0V min	
I_{INH}[1]	All	S, T	10nA max		$V_{IN} = V_{DD}$
I_{INL}[1]	All	S, T	10nA max		$V_{IN} = 0$
DYNAMIC CHARACTERISTICS					
t_{ON}[3]	AD7510DI	S, T	1.0μs max		V_{IN} = 0 to +3V
	AD7511DI	S, T	1.0μs max		
t_{OFF}[3]	AD7510DI	S, T	1.0μs max		
	AD7511DI	S, T	1.0μs max		
$t_{TRANSITION}$[3]	AD7512DI	S, T	1.0μs max		
POWER SUPPLY					
I_{DD}[1]	All	S, T		800μA max	All digital inputs = V_{INH}
I_{SS}[1]	All	S, T		800μA max	
I_{DD}	All	S, T		500μA max	All digital inputs = V_{INL}
I_{SS}[1]	All	S, T		500μA max	

NOTES:

[1] 100% tested.

[2] A pullup resistor, typically 1-2kΩ is required to make AD7511DISD and AD7512DISD TTL compatible.

[3] Guaranteed, not production tested.

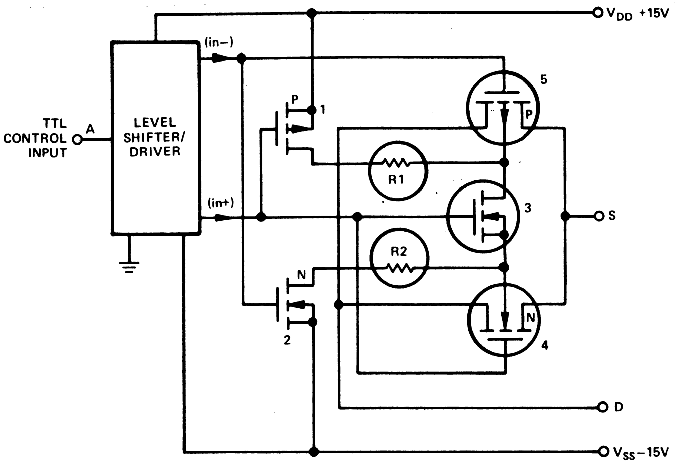
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND	+17V
V_{SS} to GND	−17V
Overvoltage at V_D (V_S)	
(1 second surge)	V_{DD} +25V or V_{SS} −25V
(Continuous)	V_{DD} +20V or V_{SS} −20V
Switch Current (I_{DS}, Continuous)	50mA
Switch Current (I_{DS}, Surge)	
1ms Duration, 10% Duty Cycle	150mA
Digital Input Voltage Range	0V to V_{DD}
Power Dissipation (Package)	
14 & 16 pin Ceramic Dip	
Up to +75°C	450mW
Derates above +75°C by	6mW/°C
14 & 16 pin Plastic Dip	
Up to +70°C	670mW
Derates above +75°C by	8.3mW/°C
Storage Temperature	−65°C to +150°C
Operating Temperature	
Plastic (J, K Versions)	0 to +70°C
Ceramic (J, K Versions)	−25°C to +85°C
Ceramic (S, T Versions)	−55°C to +125°C

CAUTION: The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high electrostatic fields. Keep unused units in conductive foam at all times. Prior to pulling the devices from the conductive foam, ground the foam to deplete any accumulated charge.

CIRCUIT DESCRIPTION



NOTE: CIRCLED DEVICES IN SEPARATE ISOLATED POCKETS.

Figure 1. Typical Output Switch Circuitry of AD7510DI Series

CMOS devices make excellent analog switches; however, problems with overvoltage and latch-up phenomenum necessitated protection circuitry. These protection circuits, however, either caused degradation of important switch parameters such as R_{ON} or leakage, or provided only limited protection in the event of overvoltage.

The AD7510DI series switches utilize a dielectrically-isolated CMOS fabrication process to eliminate the four-layer substrate found in junction-isolated CMOS, thus providing latch-free operation.

A typical switch channel is shown in Figure 1. The output switching element is comprised of device numbers 4 and 5. Operation is as follows: for an "ON" switch, (in+) is V_{DD} and (in–) is V_{SS} from the driver circuits. Device numbers 1 and 2 are "OFF" and number 3 is "ON." Hence, the back-gates of the P- and N-channel output devices (numbers 4 and 5) are tied together and floating. (The circled devices are located in separate dielectrically isolated pockets.) Floating the output switch back-gates with the signal input increases the effective threshold voltage for an applied analog signal, thus providing a flatter R_{ON} versus V_S response.

For an "OFF" switch, device number 3 is "OFF," and the back-gates of devices 4 and 5 are tied through $1k\Omega$ resistors (R1 and R2) to the respective supply voltages through the "ON" devices 1 and 2.

If a voltage is applied to the S or D terminal which exceeds V_{DD} or V_{SS}, the S- or D-to-back-gate diode is forward biased; however, R1 and R2 provide current limiting action.

Consequently, without external current limiting resistance (or increased R_{ON}), the AD7510DI series switches provide:

1. Latch-proof operation
2. Overvoltage protection 25V beyond the V_{SS} and V_{DD} supply voltage

An equivalent circuit of the output switch element in Figure 2 shows that, indeed, the $1k\Omega$ limiting resistors are in series with the back-gates of the P- and N-channel output devices—*not* in series with the signal path between the S and D terminals.

In some applications it is possible to turn on a parasitic NPN (drain to back-gate to source of the N-channel) transistor, causing device destruction under certain conditions. This case will only manifest itself when a negative overvoltage (and not a positive overvoltage) exists with another voltage source on the other side of the switch. Current limitation through external resistors (200Ω) or current limiting devices (output of op amps) will prevent damage to the device.

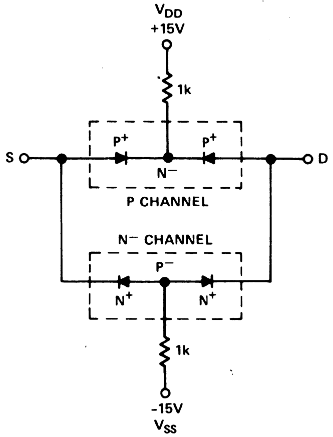
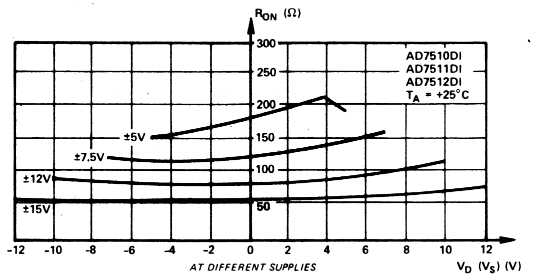
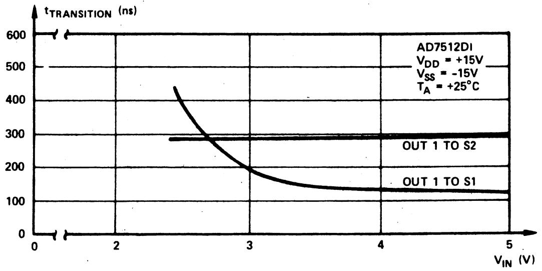


Figure 2. AD7510DI Series Output Switch Diode Equivalent Circuit

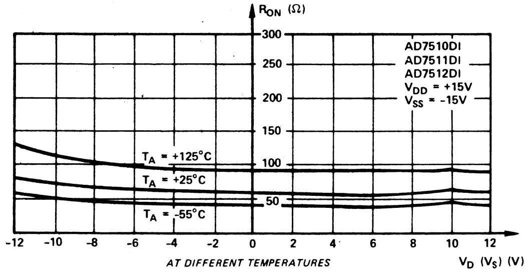
TYPICAL PERFORMANCE CHARACTERISTICS



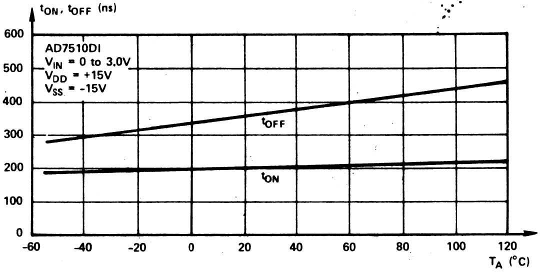
R_{ON} as a Function of V_D (V_S)



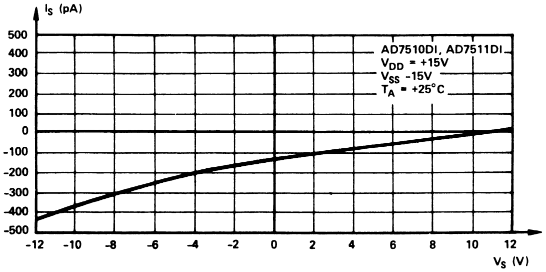
$t_{TRANSITION}$ as a Function of Digital Input Voltage



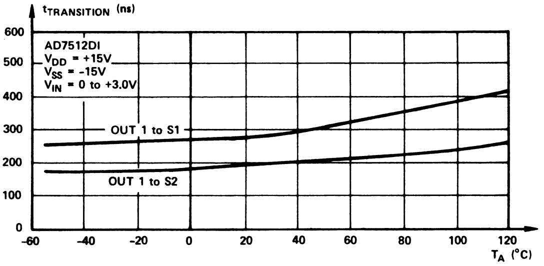
R_{ON} as a Function of V_D (V_S)



t_{ON}, t_{OFF} as a Function of Temperature

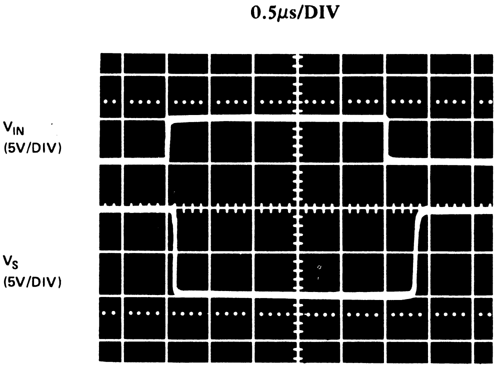


I_S, $(I_D)_{OFF}$ vs V_S

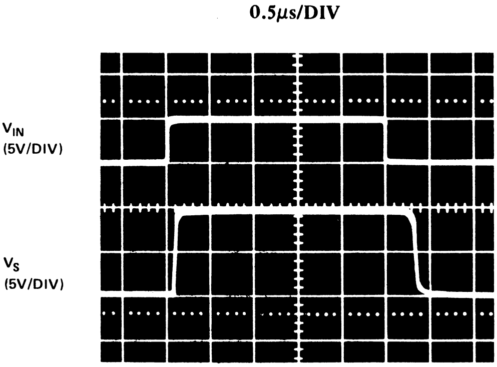


$t_{TRANSITION}$ as a Function of Temperature

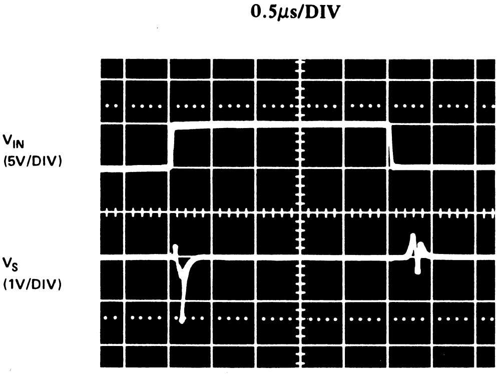
TYPICAL SWITCHING CHARACTERISTICS AD7510DI, AD7511DI



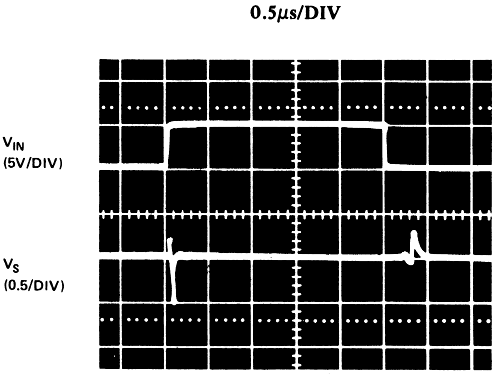
Switching Waveforms for V_D = -10V



Switching Waveforms for V_D = +10V

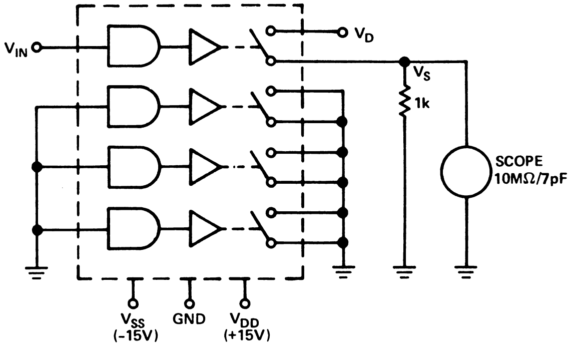


Switching Waveforms for V_D = Open

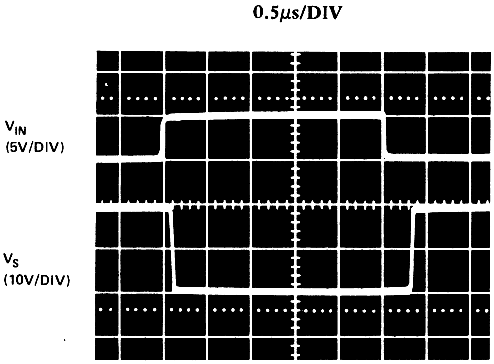


Switching Waveforms for V_D = 0V

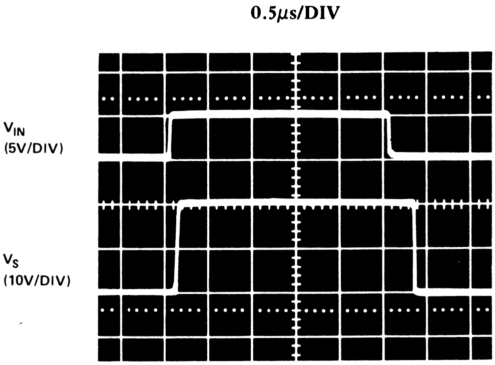
AD7510DI, AD7511DI TEST CIRCUIT



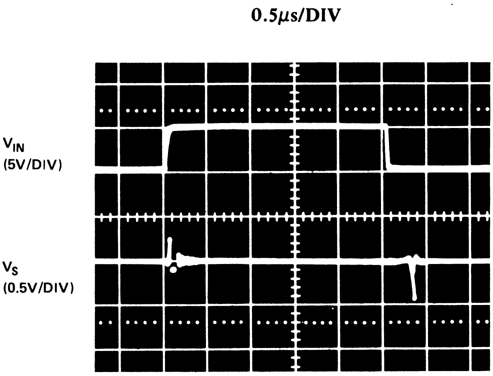
TYPICAL SWITCHING CHARACTERISTICS AD7512DI



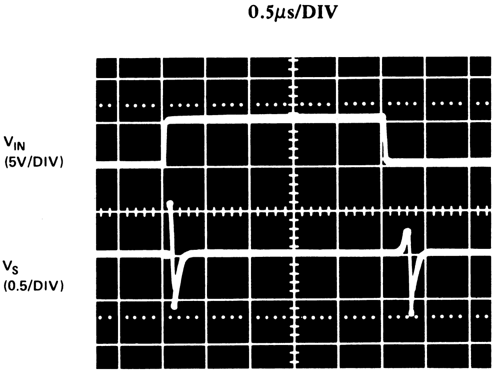
Switching Waveforms for
V_{S1} = -10V, V_{S2} = +10V, R_L = 1k



Switching Waveforms for
V_{S1} = +10V, V_{S2} = -10V, R_L = ∞

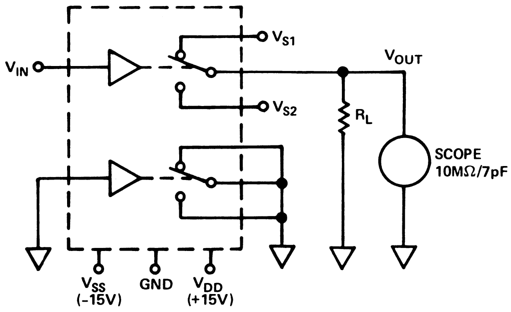


Switching Waveforms for
V_{S1} *and* V_{S2} = 0V, R_L = ∞



Switching Waveforms for
V_{S1} *and* V_{S2} = *Open*, R_L = 1k

AD7512DI TEST CIRCUIT



TERMINOLOGY

R_{ON}:	Ohmic resistance between terminals D and S.
R_{ON} Drift Match:	Difference between the R_{ON} drift of any two switches.
R_{ON} Match:	Difference between the R_{ON} of any two switches.
I_D $(I_S)_{OFF}$:	Current at terminals D or S. This is a leakage current when the switch is "OFF."
I_D $(I_S)_{ON}$:	Leakage current that flows from the closed switch into the body. (This leakage will show up as the difference between the current I_D going into the switch and the outgoing current I_S.)
V_D (V_S):	Analog voltage on terminal D (S).
C_S (CD):	Capacitance between terminal S (D) and ground. (This capacitance is specified for the switch open and closed.)
C_{DS}:	Capacitance between terminals D and S. (This will determine the switch isolation over frequency.)
C_{DD} (C_{SS}):	Capacitance between terminals D (S) of any two switches. (This will determine the cross coupling between switches vs. frequency.)
t_{ON}:	Delay time between the 50% points of the digital input and switch "ON" condition.
t_{OFF}:	Delay time between the 50% points of the digital input and switch "OFF" condition.
$t_{transition}$:	Delay time when switching from one address state to another.
V_{INL}:	Threshold voltage for the low state.
V_{INH}:	Threshold voltage for the high state.
I_{INL} (I_{INH}):	Input current of the digital input.
C_{IN}:	Input capacitance to ground of the digital input.
V_{DD}:	Most positive voltage supply.
V_{SS}:	Most negative voltage supply.
I_{DD}:	Positive supply current.
I_{SS}:	Negative supply current.

ANALOG DEVICES

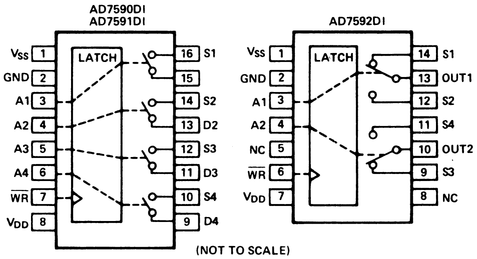
DI CMOS Analog Switches with Data Latches

AD7590DI, AD7591DI, AD7592DI

FEATURES

- **SCR Latch-Proof**
- **Overvoltage-Proof: ±25V**
- **Low R_{ON}: 75Ω**
- **Buffered Switch Logic**
- **μP, TTL, CMOS Compatible**
- **Silicon-Nitride Passivated**
- **Monolithic Dielectrically-Isolated CMOS**
- **Pin Compatible with AD7510DI Series**

AD7590DI, AD7591DI, AD7592DI FUNCTIONAL BLOCK DIAGRAMS



16-PIN DIP
TOP VIEW

14-PIN DIP
TOP VIEW

GENERAL DESCRIPTION

The AD7590DI, AD7591DI and AD7592DI are a family of protected (latch proof) dielectrically isolated CMOS switches featuring overvoltage protection up to ±25V above the power supplies. Microprocessor interfacing is facilitated by the provision of on-chip data latches.

The AD7590DI and AD7591DI consist of four independent SPST analog switches packaged in a 16-pin DIP. They differ only in that the switch control logic is inverted. The AD7592DI has two independent SPDT switches packaged in a 14-pin DIP.

ORDERING INFORMATION

Model Suffix	Operating Temperature Range
KN	0 to +70°C
BD	-25°C to +85°C

Military temperature versions will be available at a later date.

CONTROL LOGIC ($\overline{\text{WR}}$ HELD LOW)

AD7590DI:	Switch "ON" for Address "HIGH"
AD7591DI:	Switch "ON" for Address "LOW"
AD7592DI:	Address "HIGH" makes S1 to Out 1 and S3 to Out 2

PACKAGE IDENTIFICATION[1]

Suffix D: Ceramic DIP Package
AD7590, AD7591 – (D16B)
AD7592 – (D14B)
Suffix N: Plastic DIP Package
AD7590, AD7591 – (N16B)
AD7592 – (N14B)

[1] See Section 20 for package information.

SPECIFICATIONS (V_{DD} = +15V, V_{SS} = −15V unless otherwise noted)

PARAMETER	MODEL	T_A = +25°C	T_A = OPERATING TEMPERATURE RANGE	TEST CONDITIONS/COMMENTS
ANALOG SWITCH				
R_{ON}[1]	All	60Ω typ, 90Ω max	120Ω max	$-10V \leqslant V_D \leqslant +10V$ I_{DS} = 1.0mA
R_{ON} Match[2]	All	1% typ		
R_{ON} Match Drift[2]	All	0.01%/°C typ		V_D = 0, I_{DS} = 1.0mA
I_D (I_S) OFF[1]	All	0.5nA typ, 5nA max	100nA max	V_D = −10V, V_S = +10V and V_D = +10V, V_S = −10V
I_D (I_S) ON[1]	All	0.5nA typ, 5nA max	100nA max	$V_S = V_D$ = +10V and $V_S = V_D$ = −10V
I_{OUT}[1]	AD7592DI	1.0nA typ, 10nA max	200nA max	$V_{S1} = V_{OUT} = \pm 10V$, $V_{S2} = \mp 10V$ and $V_{S2} = V_{OUT} = \pm 10V$, $V_{S1} = \mp 10V$
C_S (C_D) OFF[3]	All	10pF typ		
C_S (C_D) ON[3]	All	30pF typ		
C_{DS} (C_{S-OUT})[3]	All	1pF typ		V_D (V_S) = 0V
C_{DD} (C_{SS})[3]	All	0.5pF typ		
C_{OUT}[3]	AD7592DI	40pF typ		
DIGITAL CONTROL				
V_{INL}[1]	All	0.8V max	0.8V max	
V_{INH}[1]	All	2.4V min	2.4V min	
C_{IN}[3]	All	5pF typ	5pF typ	
I_{INH}[1,4]	All	1μA max	1μA max	V_{IN} = 0 or V_{DD}
I_{INL}[1,4]	All	1μA max	1μA max	
DYNAMIC CHARACTERISTICS				
t_{ON}[2]	AD7590DI	170ns typ, 340ns max	190ns typ, 380ns max	
	AD7591DI	300ns typ, 600ns max	380ns typ, 760ns max	
t_{OFF}[2]	AD7590DI	300ns typ, 600ns max	380ns typ, 760ns max	
	AD7591DI	170ns typ, 340ns max	190ns typ, 380ns max	
$t_{TRANSITION}$[2]	AD7592DI	300ns typ, 600ns max	380ns typ, 760ns max	
Write Pulse-Width (t_{WR})[2]	All	300ns typ, 400ns min	400ns typ, 500ns min	
Address Set Up Time (t_{AS})[2]	All	0ns min	0ns min	See Figure 1
Address Hold Time (t_{AH})[2]	All	150ns typ, 250ns min	250ns typ, 350ns min	
OFF Isolation[3] (Analog Input to Analog Output)	All	Better than −85dB at 1kHz. Feedthrough primarily dependent upon printed circuit board layout.		
Crosstalk[3] (Digital Input to Analog Output)	All	5mV peak, typ		R_L = 1MΩ, C_L = 15pF V_{INH} = 3.0V, V_{INL} = 0V $t_{rise} = t_{fall}$ = 20ns $\overline{WR}$ held HIGH
Q_{INJ} (Charge Injection)[3]	All	40pC typ		Measured at S or D terminal, C_L = 1000pF V_{IN} = 0 to 3.0V, V_D (V_S) = +10V to −10V, $\overline{WR}$ held LOW
POWER SUPPLY				
I_{DD}[1]	All	1mA max	1mA max	All digital inputs
I_{SS}[1]	All	1mA max	1mA max	$V_{IN} = V_{INH}$ or V_{INL}

NOTES

[1] 100% tested.

[2] Guaranteed, not production tested.

[3] Typical values for information only, not subject to test or guarantee.

[4] Inputs are MOS gates typical current less than 10nA.

Specifications subject to change without notice.

Absolute Maximum Ratings

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to GND	+17V
V_{SS} to GND	−17V
Overvoltage at V_D (V_S)	
(1 second surge)	V_{DD} +25V or V_{SS} −25V
(Continuous)	V_{DD} +20V or V_{SS} −20V
Switch Current (I_{DS}, Continuous)	50mA
Switch Current (I_{DS}, Surge)	
1ms Duration, 10% Duty Cycle	150mA
Digital Input Voltage Range	−0.3V to V_{DD} +0.3V

Power Dissipation (Package)	
14- & 16-pin Ceramic Dip	
Up to +75°C	450mW
Derates above +75°C by	6mW/°C
14- & 16-pin Plastic Dip	
Up to +70°C	670mW
Derates above +75°C by	8.3mW/°C
Storage Temperature	−65°C to +150°C
Operating Temperature	
Plastic (KN Versions)	0 to +70°C
Ceramic (BD Versions)	−25°C to +85°C

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION:

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

TIMING AND CONTROL SEQUENCE

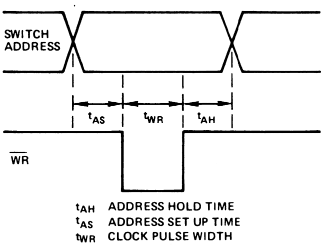
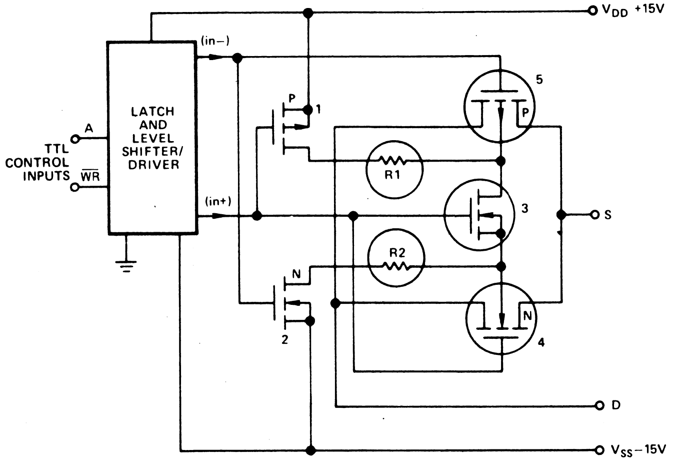

SWITCH ADDRESS
t_{AS}
t_{WR}
t_{AH}
$\overline{WR}$
t_{AH} ADDRESS HOLD TIME
t_{AS} ADDRESS SET UP TIME
t_{WR} CLOCK PULSE WIDTH

Figure 1. Timing and Control Sequence

Figure 1 shows the timing sequence for latching the switch address. The minimum data set up time is zero so that the data may change coincident with the falling edge of $\overline{WR}$. The address is latched on the rising edge of WR and address must be held for T_{AH} minimum to guarantee that it will be latched. While WR is held low the latch is transparent and the switches respond to changes in the input address.

CIRCUIT DESCRIPTION



NOTE: CIRCLED DEVICES IN SEPARATE ISOLATED POCKETS.

Figure 2. Typical Output Switch Circuitry of AD7590DI Series

CMOS devices make excellent analog switches; however, problems with overvoltage and latch-up phenomenum necessitated protection circuitry. These protection circuits, however, either caused degradation of important switch parameters such as R_{ON} or leakage, or provided only limited protection in the event of overvoltage.

The AD7590DI series switches utilize a dielectrically-isolated CMOS fabrication process to eliminate the four-layer substrate found in junction-isolated CMOS, thus providing latch-free operation.

A typical switch channel is shown in Figure 2. The output switching element is comprised of device numbers 4 and 5. Operation is as follows: for an "ON" switch, (in+) is V_{DD} and (in–) is V_{SS} from the driver circuits. Device numbers 1 and 2 are "OFF" and number 3 is "ON." Hence, the back-gates of the P- and N-channel output devices (numbers 4 and 5) are tied together and floating. (The circled devices are located in separate dielectrically isolated pockets.) Floating the output switch back-gates with the signal input increases the effective threshold voltage for an applied analog signal, thus providing a flatter R_{ON} versus V_S response.

For an "OFF" switch, device number 3 is "OFF," and the back-gates of devices 4 and 5 are tied through 1kΩ resistors (R1 and R2) to the respective supply voltages through the "ON" devices 1 and 2.

If a voltage is applied to the S or D terminal which exceeds V_{DD} or V_{SS}, the S- or D-to-back-gate diode is forward biased; however, R1 and R2 provide current limiting action.

Consequently, without external current limiting resistance (or increased R_{ON}), the AD7590DI series switches provide:

1. Latch-proof operation
2. Overvoltage protection 25V beyond the V_{SS} and V_{DD} supply voltage

An equivalent circuit of the output switch element in Figure 3 shows that, indeed the 1kΩ limiting resistors are in series with the back-gates of the P- and N-channel output devices— *not* in series with the signal path between the S and D terminals.

In some applications it is possible to turn on a parasitic NPN (drain to back-gate to source of the N-channel) transistor, causing device destruction under certain conditions. This case will only manifest itself when a negative overvoltage (and not a positive overvoltage) exists with another voltage source on the other side of the switch. Current limitation through external resistors (200Ω) or current limiting devices (output of op amps) will prevent damage to the device.

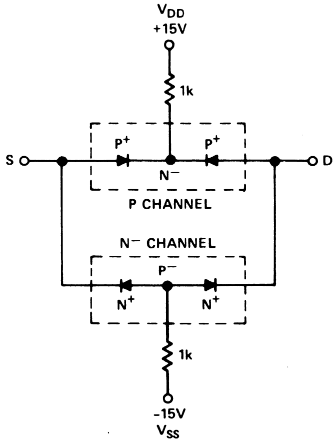
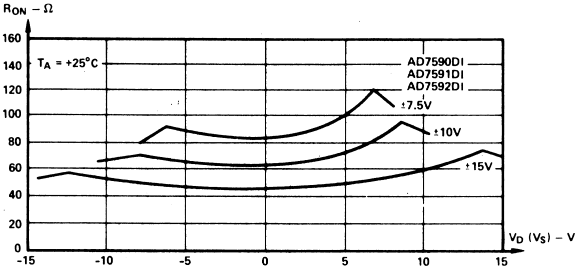
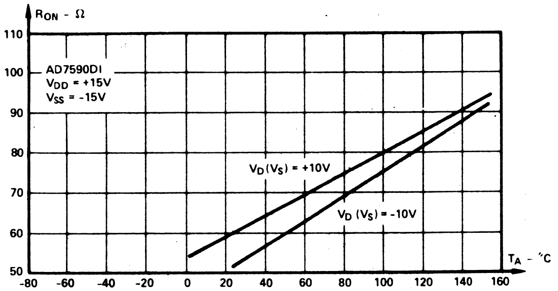


Figure 3. AD7590DI Series Output Switch Diode-Equivalent-Circuit

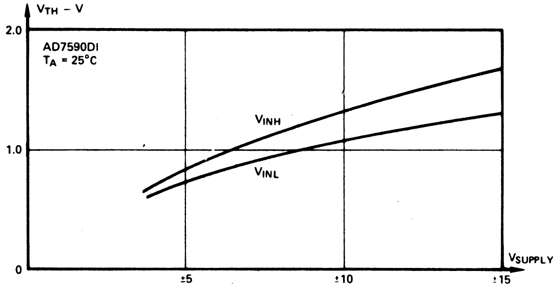
Typical Performance Characteristics



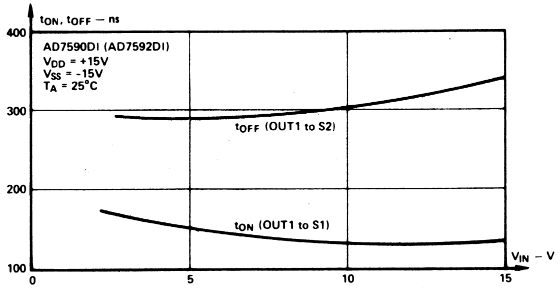
R_{ON} as a Function of V_D (V_S) for Different Supply Voltages



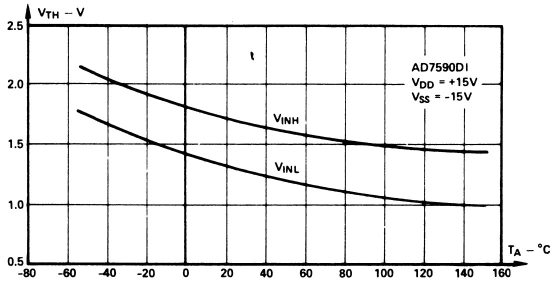
R_{ON} as a Function of Temperature



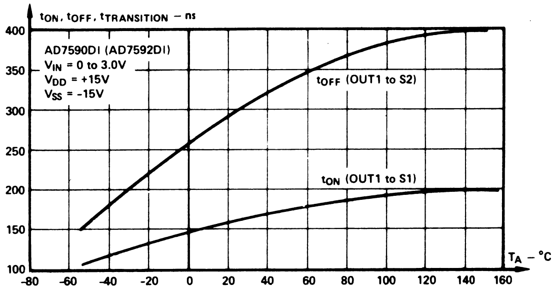
Threshold Voltage as a Function of Supply Voltage



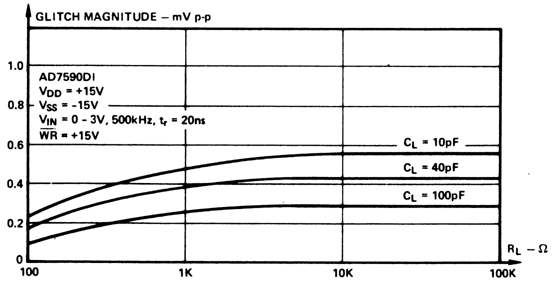
t_{ON}, t_{OFF} ($t_{TRANSITION}$) as a Function of Digital Input Voltage



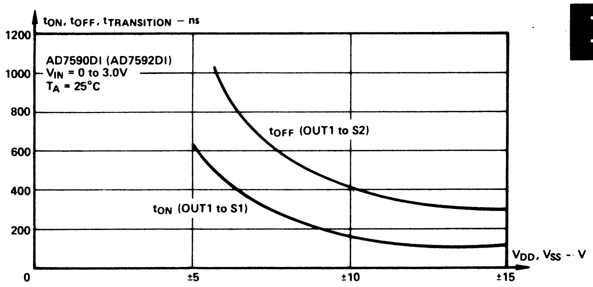
Threshold Voltage as a Function of Temperature



t_{ON}, t_{OFF} ($t_{TRANSITION}$) as a Function of Temperature



Digital Crosstalk as a Function of Load Impedance

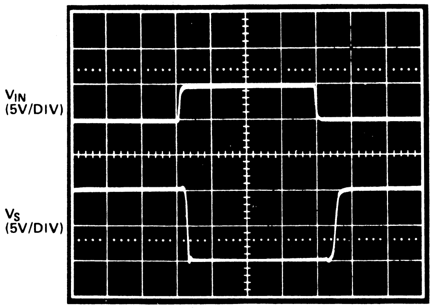


t_{ON}, t_{OFF} ($t_{TRANSITION}$) as a Function of Supply Voltage

TYPICAL SWITCHING CHARACTERISTICS

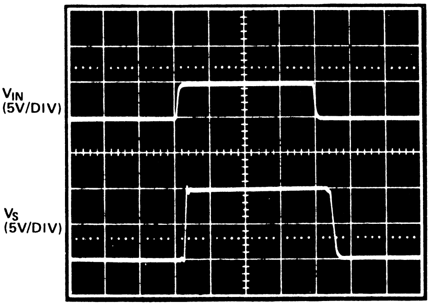
AD7590DI, AD7591DI

0.5µs/DIV



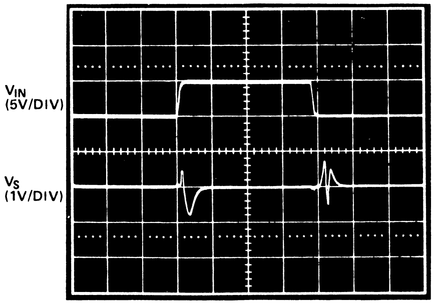
Switching Waveform for V_D = −10V

0.5µs/DIV



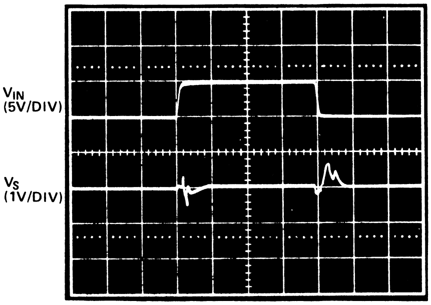
Switching Waveform for V_D = +10V

0.5µs/DIV



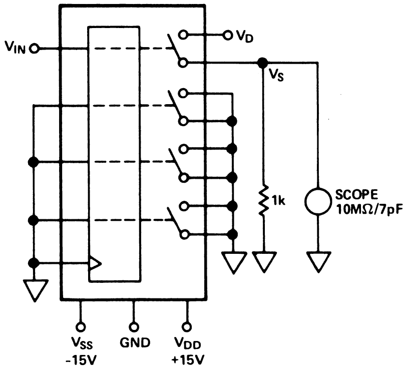
Switching Waveform for V_D = 0

0.5µs/DIV



Switching Waveform for V_D = 0V

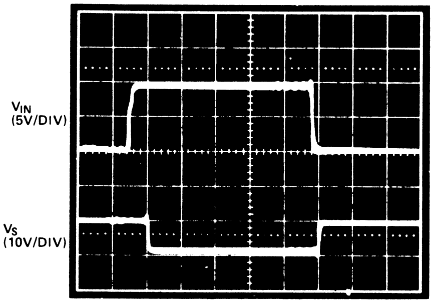
AD7590DI, AD7591DI TEST CIRCUIT



TYPICAL SWITCHING CHARACTERISTICS

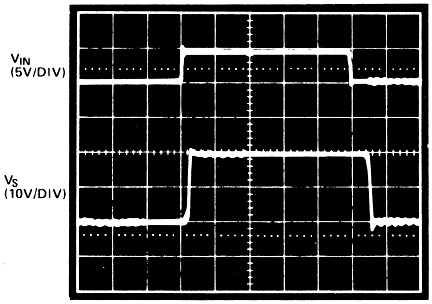
AD7592DI

0.5µs/DIV



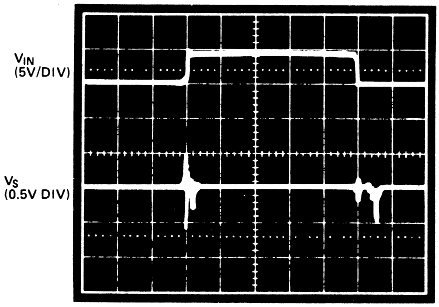
Switching Waveforms for $V_{S1} = -10V$, $V_{S2} = +10V$, $R_L = 1k\Omega$

0.5µs/DIV



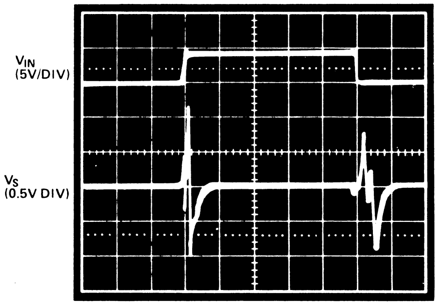
Switching Waveforms for $V_{S1} = +10V$, $V_{S2} = -10V$, $R_L = \infty$

0.5µs/DIV



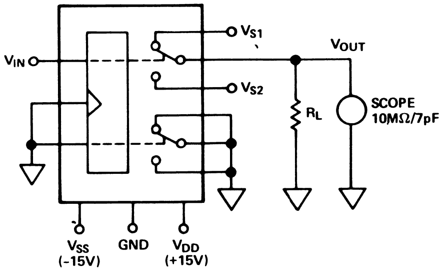
Switching Waveforms for V_{S1} *and* $V_{S2} = 0V$, $R_L = \infty$

0.5µs/DIV



Switching Waveforms for V_{S1} *and* V_{S2} *= Open,* $R_L = 1k\Omega$

AD7592DI TEST CIRCUIT



ANALOG DEVICES

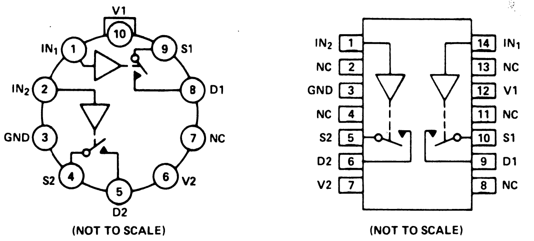
DI CMOS Protected Dual SPST Analog Switch

ADG200

FEATURES

Latch-Proof DI CMOS
Overvoltage-Proof: V_{SUPPLY} ±25V
Superior DG-200 Replacement
Break-Before-Make Switching Action
R_{ON}: 100Ω max over Full Temperature Range
Direct TTL/CMOS Interface

ADG200 FUNCTIONAL BLOCK DIAGRAMS



SWITCH STATES ARE FOR LOGIC "1" INPUT (POSITIVE LOGIC)

TO-100
TOP VIEW

14-PIN DIP
DUAL-IN-LINE PACKAGE
TOP VIEW

GENERAL DESCRIPTION

The ADG200 is a dual single-pole-single-throw analog switch. In the ON condition, the switch conducts current in either direction, maintaining nearly constant ON resistance over the entire analog signal range. In the OFF condition, the switch blocks voltages of peak values equal to the switch V+ and V− supplies. Switch action is break-before-make. The digital inputs interface directly to TTL or CMOS logic over the full operating temperature range.

Fabricated using an advanced monolithic dielectrically-isolated CMOS process, the ADG200 is a superior plug-in replacement for the DG200. The ADG200 provides additional advantages (over the DG200) of: overvoltage protection to ±25V beyond the power supplies, total latch-free operation, much lower power dissipation (30mW max) and faster switching time.

ORDERING INFORMATION

Commercial 0 to +70°C	Industrial -25°C to +85°C		Military -55°C to +125°C	
Plastic (N14B)[1]	Ceramic (D14B)[1]	TO-100	Ceramic (D14B)[1]	TO-100
ADG200CJ	ADG200BP	ADG200BA	ADG200AP	ADG200AA ADG200AA/883

Note: "/883" version is 100% screened to MIL-STD-883, class B as per note 3 on Specifications Table, next page.

[1] See Section 20 for package outline information.

SPECIFICATIONS

CHARACTERISTIC[1]		TYP[1] +25°C	MAX LIMITS AA, AP Suffix[3] -55°C[2]	+25°C	+125°C	MAX LIMITS BA, BP/CJ Suffix -25/0°C[2]	+25°C	+85/70°C[2]	UNITS	TEST CONDITIONS[4] Unless Noted V_1 = +15V V_2 = -15V, GND = 0V	
SWITCH											
$r_{DS(ON)}$	Drain-Source ON Resistance	60	70	70	100	80	80	100	Ω	V_D = 10V	V_{IN} = 0.8V
		40	70	70	100	80	80	100		V_D = -10V	I_S = +1mA
$I_{S(OFF)}$	Source OFF Leakage Current	0.2	500	2	500	500	5	500	nA	V_S = 10V, V_D = -10V	V_{IN} = 2.4V
		-0.2	-500	-2	-500	-500	-5	-500		V_S = -10V, V_D = 10V	
$I_{D(OFF)}$	Drain OFF Leakage Current	0.3	500	2	500	500	5	500		V_D = 10V, V_S = -10V	
		-0.3	-500	-2	-500	-500	-5	-500		V_D = -10V, V_S = 10V	
$I_{D(ON)}$[5]	Channel ON Leakage Current	0.1	500	2	500	500	2	500		$V_D = V_S$ = 10V	V_{IN} = 0.8V
		-0.1	-500	-2	-500	-500	-2	-500		$V_D = V_S$ = -10V	
INPUT											
I_{INH}	Input Current Input Voltage High		-10	-1	-10	-10	-1	-10	μA	V_{IN} = 2.4V	
			10	1	10	10	1	10		V_{IN} = 15V	
$I_{IN(PEAK)}$[6]	Peak Input Current Required for Transition	NOT APPLICABLE[6]									
I_{INL}	Input Current Input Voltage Low		-10	-1	-10	-10	-1	-10	μA	V_{IN} = 0V	
DYNAMIC											
t_{ON}	Turn-ON Time[7]	300		1000[2]			1000[2]		ns	V_{IN} = 3.5V to 0V	R_L = 1kΩ, C_L = 35pF
t_{OFF}	Turn-OFF Time[7]	120		500[2]			500[2]			V_{IN} = 0V to 3.5V	V_S = ±5V
$C_{S(OFF)}$	Source OFF Capacitance	11							pF	V_S = 0V, V_{IN} = 5V	
$C_{D(OFF)}$	Drain OFF Capacitance	11							pF	V_D = 0V, V_{IN} = 5V	f = 140kHz
$C_{D(ON)} + C_{S(ON)}$	Channel ON Capacitance	28							pF	$V_D = V_S$ = 0V V_{IN} = 0V	
OFF Isolation[8]		64							dB	V_{IN} = 5V, R_L = 1kΩ, C_L = 15pF V_S = $7V_{rms}$, f = 500kHz	
SUPPLY											
I_1	Positive Supply Current	0.02	2	1	2	2	1	2	mA	Both Channels ON; V_{IN} = 0V	
I_2	Negative Supply Current	-0.02	-2	-1	-2	-2	-1	-2	mA		
I_1	Positive Supply Current	0.1	2	1	2	2	1	2	mA	Both Channels OFF; V_{IN} = 5V	
I_2	Negative Supply Current	-0.02	-2	-1	-2	-2	-1	-2	mA		

NOTES:

[1] Typical values for information only, not guaranteed or production tested.

[2] Guaranteed, not subject to 100% production test.

[3] ADG200AP is available 100% screened to MIL-STD-883, method 5004, para. 3.1.1 through 3.1.12 for a class B device. Final electrical tests are: $r_{DS(ON)}$, $I_{S(OFF)}$, $I_{D(OFF)}$, I_{INH}, I_{INL}, I_1 and I_2 at +25°C and +125°C (AA/883 version).

[4] Functional operation is possible for supply voltages less than ±15V, but the input logic switching threshold will shift.

[5] I_D(ON) is leakage from driver gate into ON switch.

[6] Digital inputs are MOS gates. Typical leakage (+25°C) is less than 1 nanoamp. This is in contrast to other designs which require typically 150μA to switch.

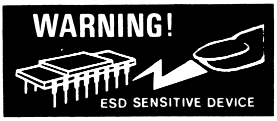
[7] Switch action is guaranteed break-before-make.

[8] OFF isolation (dB) = 20 log V_S/V_D where V_S = input to OFF switch and V_D = output.

Specifications subject to change without notice.

CAUTION:

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



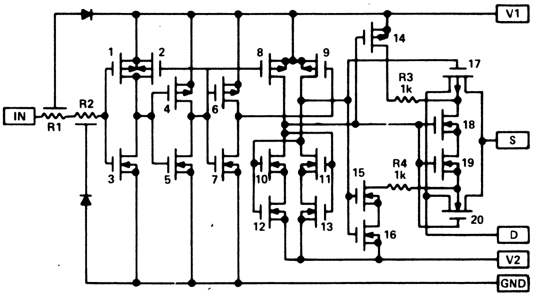
ABSOLUTE MAXIMUM RATINGS

V_{IN}(Digital Input) to Ground . . . . -0.3V, V_1
V_S or V_D to V_1
(1 second surge) . . . . +25V, -40V
(continuous) . . . . +20V, -35V
V_S or V_D to V_2
(1 second surge) . . . . -25V, +40V
(continuous) . . . . -20V, +35V
V_1 to Ground. . . . . -0.3V, +17V
V_2 to Ground. . . . . +0.3V, -17V
Current, Any Terminal Except S or D 30mA
Current, S or D 50mA
Current, S or D Pulsed
(1ms, 10% duty cycle max). 150mA

Operating Temperature
AA, AP Suffix . . . . -55°C to +125°C
BA, BP Suffix. . . . . -25°C to +85°C
CJ Suffix. . . . . 0°C to +70°C
Storage Temperature
CJ Suffix. . . . . -65°C to +125°C
All Others . . . . -65°C to +150°C
Power Dissipation (Package)*
Metal Can**. 450mW
14 Pin Ceramic DIP*** 825mW
14 Pin Plastic DIP****. 470mW

* Devices with all leads welded or soldered to printed circuit board
** Derate 6mW/°C above +75°C
*** Derate 11mW/°C above +75°C
**** Derate 6.5mW/°C above +25°C

CIRCUIT DESCRIPTION



NOTE: LOGIC "0" ON IN TERMINAL CLOSES SWITCH BETWEEN S AND D.

Figure 1. Schematic Diagram (1 of 2 channels)

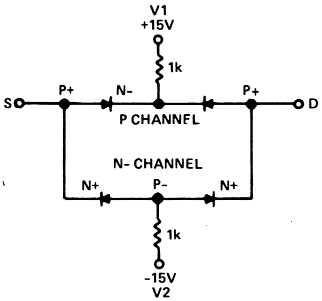


Figure 2. ADG200 Output Switch Diode Equivalent Circuit

CMOS devices make excellent analog switches; however, problems with overvoltage and latch-up phenomenon necessitate protection circuitry. However, these protection circuits either cause degradation of important switch parameters such as R_{ON} or leakage, or provide only limited protection in the event of overvoltage.

The ADG200 switch utilizes a dielectrically-isolated CMOS fabrication process to eliminate the four-layer structure found in junction-isolated CMOS, thus providing latch-free operation.

A typical switch channel is shown in Figure 1. The output switching element consists of device numbers 17 and 20. Operation is as follows: for an "ON" switch, the gate of device 20 is V_1 and the gate of device 17 is V_2 from the driver circuits. Device numbers 14, 15, and 16 are "OFF" and numbers 18 and 19 are "ON". Hence, the back-gates of the P- and N-channel output devices (numbers 17 and 20) are tied together and floating. Floating the output switch back-gates with the signal input provides a flatter R_{ON} versus V_S response.

For an "OFF" switch, device numbers 18 and 19 are "OFF", and the back-gates of devices 17 and 20 are tied through 1kΩ resistors R_3 and R_4 to the respective supply voltages through the "ON" devices 14, 15, and 16.

If a voltage is applied to the S or D terminals which exceeds V_1 or V_2, the S- or D-to-back-gate diode is forward biased; however, R_3 and R_4 provide current limiting action (Fig. 2).

Consequently, without external current limiting resistance (or increased R_{ON}), the ADG200 series switches provide:

1. Latch-proof operation.
2. Overvoltage protection 25V beyond the V_1 or V_2 supply voltage.

An equivalent circuit of the output switch element in Figure 2 shows that, indeed, the 1kΩ limiting resistors are in series with the back-gates of the P- and N-channel output devices – *not* in series with the signal path between the S & D terminals.

In some applications it is possible to turn on a parasitic NPN (drain to back-gate to source of the N-channel) transistor which causes device destruction under certain conditions. This case will only manifest itself when a negative overvoltage (and not a positive overvoltage) exists with another voltage source on the other side of the switch. Current limitation through external resistors (200Ω) or the output of op amps will prevent damage to the device.

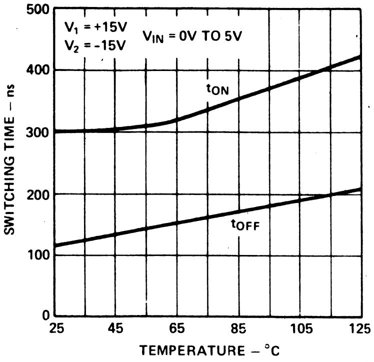


Figure 3. Switching Time vs. Temperature

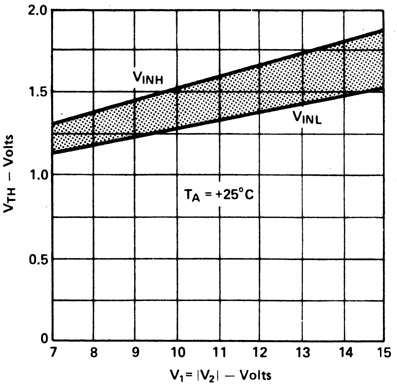


Figure 4. Input Logic Threshold vs. Power Supply Voltage

ANALOG DEVICES

DI CMOS Protected Quad SPST Analog Switch

ADG201

FEATURES

Latch-Proof DI CMOS
Overvoltage Proof to 25V Beyond Supplies
Superior DG201 Replacement
Break-Before-Make Switching Action
Low R$_{ON}$: 80Ω
Low Power Dissipation: 30mW max
Direct TTL or CMOS Interfacing

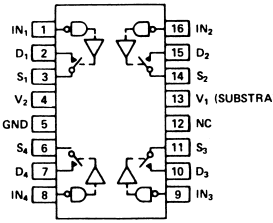
GENERAL DESCRIPTION

The ADG201 is a quad SPST analog switch. In the ON state, the switch conducts current in either direction, maintaining nearly constant ON resistance over its signal handling range. In the OFF state, it blocks voltages equal to the switch V+ and V- supplies. Switch action is break-before-make.

The digital inputs interface directly to TTL or CMOS logic over the full operating temperature range.

Fabricated with an advanced monolithic dielectrically-isolated CMOS process, the ADG201 is a superior plug-in replacement for the DG201. ADG201 advantages over other designs include: lower R$_{ON}$, lower power dissipation, faster switching time, overvoltage protection (25V beyond power supplies), and latch-free operation.

ADG201 FUNCTIONAL BLOCK DIAGRAM



SWITCH IS OPEN FOR LOGIC "1" (POSITIVE TRUE) INPUT

16-PIN DIP
TOP VIEW

ORDERING INFORMATION

Commercial 0 to +70°C	Industrial -25°C to +85°C	Military -55°C to +125°C
Plastic (N16B)[1]	Ceramic (TO-116)[1]	Ceramic (TO-116)[1]
ADG201CJ	ADG201BP	ADG201AP ADG201AP/883[2]

NOTES:
[1] See Section 20 for package outline information.
[2] "/883" version is 100% screened to MIL-STD-883, class B as per note 3 on Specifications Table, next page.

SPECIFICATIONS

CHARACTERISTIC		TYP[1]	MAX LIMITS						UNITS	TEST CONDITIONS[4] Unless Noted V_1 = +15V V_2 = -15V, GND = 0V	
			AP SUFFIX[3]			BP, CJ SUFFIX					
		+25°C	-55°C[2]	+25°C	+125°C	-25/0°C[2]	+25°C	+85/70°C[2]			
SWITCH											
$r_{DS(ON)}$	Drain-Source	60	80	80	125	100	100	125	Ω	V_D = 10V	V_{IN} = 0.8V
	ON Resistance	40	80	80	125	100	100	125		V_D = -10V	I_S = +1mA
$I_{S(OFF)}$	Source OFF	0.2	500	1	500	250	5	250	nA	V_S = 10V, V_D = -10V	V_{IN} = 2.4V
	Leakage Current	0.2	-500	-1	-500	-250	-5	-250		V_S = -10V, V_D = 10V	
$I_{D(OFF)}$	Drain OFF	0.3	500	1	500	250	5	250		V_D = 10V, V_S = -10V	
	Leakage Current	0.3	-500	-1	-500	-250	-5	-250		V_D = -10V, V_S = 10V	
$I_{D(ON)}$[5]	Drain ON	0.1	500	1	500	250	5	250		$V_D = V_S$ = 10V	V_{IN} = 0.8V
	Leakage Current	0.1	-500	-1	-500	-250	-5	-250		$V_D = V_S$ = -10V	
INPUT											
I_{INH}	Input Current		-10	-1	-10	-10	-1	-10	μA	V_{IN} = 2.4V	
	Input Voltage High		10	1	10	10	1	10		V_{IN} = 15V	
$I_{IN(PEAK)}$[6]	Peak Input Current Required for Transition	NOT APPLICABLE[6]									
I_{INL}	Input Current Input Voltage Low		-10	-1	-10	-10	-1	-10	μA	V_{IN} = 0V	
DYNAMIC											
t_{ON}	Turn-ON Time[2,7]	260		1000			1000		ns	V_{IN} = 3.5V to 0V	R_L = 1kΩ, C_L = 35pF
t_{OFF}	Turn-OFF Time[2,7]	130		500			500			V_{IN} = 0V to 3.5V	V_S = ±5V
$C_{S(OFF)}$	Source OFF Capacitance	9							pF	V_S = 0V, V_{IN} = 5V	
$C_{D(OFF)}$	Drain OFF Capacitance	9							pF	V_D = 0V, V_{IN} = 5V	
$C_{D(ON)} + C_{S(ON)}$	Channel ON Capacitance	21							pF	$V_D = V_S$ = 0V V_{IN} = 0V	
OFF Isolation[8]		65							dB	V_{IN} = 5V, R_L = 1kΩ, C_L = 15pF V_S = 7V_{rms}, f = 500kHz	
SUPPLY											
I_1	Positive Supply Current	0.015	2	1	2	2	1	2	mA	One Channel ON, V_{IN} = 0V	
I_2	Negative Supply Current	-0.015	-2	-1	-2	-2	-1	-2	mA		
I_1	Positive Supply Current	0.2	2	1	2	2	1	2	mA	All Channels OFF, V_{IN} = 5V	
I_2	Negative Supply Current	-0.015	-2	-1	-2	-2	-1	-2	mA		

NOTES:

[1] Typical values for information only, not guaranteed or production tested.

[2] Guaranteed, not subject to 100% production test.

[3] ADG201AP is available 100% screened to MIL-STD-883, method 5004, para. 3.1.1 through 3.1.12 for a class B device. Final electrical tests are: $r_{DS(ON)}$, $I_{S(OFF)}$, $I_{D(OFF)}$, $I_{D(ON)}$, I_{INH}, I_{INL}, I_1 and I_2 at +25°C and +125°C (AP/883 version).

[4] Functional operation is possible for supply voltages less than ±15V, but the input switching threshold will shift.

[5] I_D(ON) is leakage from driver gate into ON switch.

[6] Digital inputs are MOS gates. Typical leakage (+25°C) is less than 1 nanoamp. This is in contrast to other designs which require typically 150μA to switch.

[7] Switch action is guaranteed break-before-make.

[8] OFF isolation (dB) = 20 log V_S/V_D where V_S = input to OFF switch and V_D = output.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

V_{IN} (Digital Input) to Ground	-0.3V, V_1
V_S or V_D to V_1	
(1 second surge)	+25V, -40V
(continuous)	+20V, -35V
V_S or V_D to V_2	
(1 second surge)	-25V, +40V
(continuous)	-20V, +35V
V_1 to Ground	-0.3V, +17V
V_2 to Ground	+0.3V, -17V
Current, any terminal except S or D	30mA
Continuous Current, S or D	50mA
Peak Current, S or D	
(pulsed at 1ms, 10% duty cycle max)	150mA

Operating Temperature	
(AP Suffix)	-55°C to +125°C
(BP Suffix)	-25°C to +85°C
(CJ Suffix)	0°C to +70°C
Storage Temperature	
(AP, BP Suffix)	-65°C to +150°C
(CJ Suffix)	-65°C to +125°C
Power Dissipation (Package)*	
16 Pin Ceramic DIP**	900mW
16 Pin Plastic DIP***	470mW

* Device mounted with all leads soldered or welded to PC board
** Derate 12mW/°C above +75°C
*** Derate 6.5mW/°C above +25°C

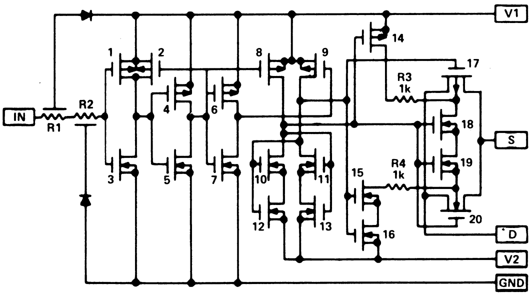
CAUTION:

ESD (Electro-Static-Discharge) sensitive device. The digital inputs are zener protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed for insertion.

WARNING!

ESD SENSITIVE DEVICE

CIRCUIT DESCRIPTION



NOTE: LOGIC "0" ON IN TERMINAL CLOSES SWITCH BETWEEN S AND D.

Figure 1. Schematic Diagram, 1 of 4 Channels

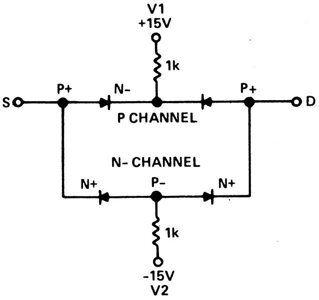


Figure 2. ADG201 Output Switch Diode Equivalent Circuit

CMOS devices make excellent analog switches; however, problems with overvoltage and latch-up phenomenon necessitate protection circuitry. However, these protection circuits either cause degradation of important switch parameters such as R_{ON} or leakage, or provide only limited protection in the event of overvoltage.

The ADG201 switch utilises a dielectrically-isolated CMOS fabrication process to eliminate the four-layer structure found in junction-isolated CMOS, thus providing latch-free operation.

A typical switch channel is shown in Figure 1. the output switching element consists of device numbers 17 and 20. Operation is as follows: for an "ON" switch, the gate of device 20 is V_1 and the gate of device 17 is V_2 from the driver circuits. Device numbers 14, 15 and 16 are "OFF" and numbers 18 and 19 are "ON". Hence, the back-gates of the P- and N-channel output devices (numbers 17 and 20) are tied together and floating. Floating the output switch back-gates with the signal input provides a flatter R_{ON} versus V_S response.

For an "OFF" switch, device numbers 18 and 19 are "OFF", and the back-gates of devices 17 and 20 are tied through 1kΩ resistors R_3 and R_4 to the respective supply voltages through the "ON" devices 14,15 and 16.

If a voltage is applied to the S or D terminals which exceeds V_1 or V_2, the S- or D-to-back-gate diode is forward biased; however, R_3 and R_4 provide current limiting action (Fig. 2).

Consequently, without external current limiting resistance (or increased R_{ON}), the ADG201 series switches provide:

1. Latch-proof operation.
2. Overvoltage protection 25V beyond the V_1 or V_2 supply voltage.

An equivalent circuit of the output switch element in Figure 2 shows that, indeed, the 1kΩ limiting resistors are in series with the back-gates of the P- and N-channel output devices- *not* in series with the signal path between the S & D terminals.

In some applications it is possible to turn on a parasitic NPN (drain to back-gate to source of the N-channel) transistor which causes device destruction under certain conditions. This case will only manifest itself when a negative overvoltage (and not a positive overvoltage) exists with another voltage source on the other side of the switch. Current limitation through external resistors (200Ω) or the output of op amps will prevent damage to the device.

TYPICAL PERFORMANCE CHARACTERISTICS

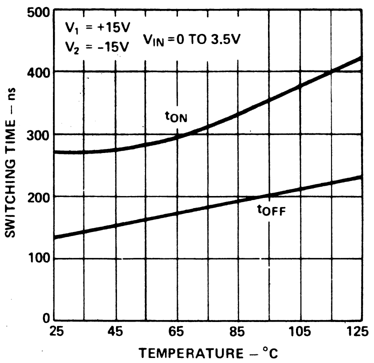


Figure 3. Switching Time vs. Temperature

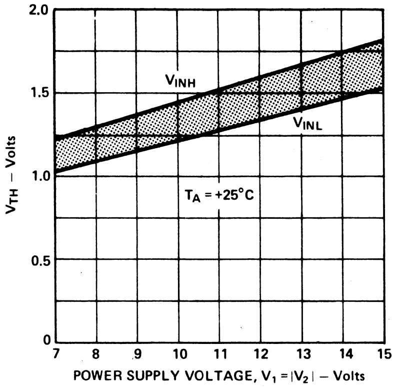


Figure 4. Input Logic Threshold vs. Power Supply Voltage

Monolithic Chips

Contents

Page

BIPOLAR INTEGRATED CIRCUIT CHIPS

General Information 17–3
AD517 Chips Low Cost, Laser Trimmed Precision IC Op Amp 17–5
AD518 Chips Low Cost, High Speed, IC Op Amp 17–7
AD521 Chips Precision Instrumentation Amplifier 17–9
AD532 Chips Trimmed IC Multiplier 17–11
AD534 Chips Trimmed Precision IC Multiplier 17–13
AD536A Chips IC True rms-to-dc Converter 17–15
AD537 Chips Low Cost IC V-to-F Converter 17–17
AD540 Chips High Accuracy Low Cost FET-Input Op Amp 17–19
AD542 Chips Precision Low Cost BIFET Op Amp 17–21
AD544 Chips Precision High Speed BIFET Op Amp 17–23
●AD547 Chips Ultra Low Drift BIFET Operational Amplifier 17–25
AD558 Chips DACPORT^{TM} Low Cost Complete μP-Compatible 8-Bit DAC 17–27
AD561 Chips Low Cost, High Speed 10-Bit D-to-A Converter with Reference 17–29
●AD565A/AD566A Chips Complete High Speed 12-Bit D/A Converter 17–31
●AD567 Chips Microprocessor-Compatible 12-Bit D/A Converter 17–33
AD570/AD571 Chips Low Cost Complete 8- and 10-Bit A-to-D Converter 17–35
●AD573 Chips Fast, Complete 10-Bit A-to-D Converter with Microprocessor Interface 17–37
AD580 Chips Precision 2.5 Volt Reference 17–39
AD581/AD584 Chips Programmable Precision Low-Drift Reference 17–41
AD582 Chips Low Cost Precision Sample-and-Hold 17–43
AD589 Chips Two-Terminal IC 1.2 Volt Reference 17–45
AD590 Chips Two-Terminal IC Temperature Transducer 17–47
AD642 Chips Precision Low Cost Dual BIFET Op Amp 17–49
●AD644 Chips Dual High Speed Implanted FET-Input Op Amp 17–51
AD DAC-08 Chips High Speed 8-Bit D-to-A Converter 17–53
AD OP-07 Chips Ultra-Low Offset Voltage Op Amp 17–55

CMOS INTEGRATED CIRCUIT CHIPS

General Information 17–57
Bonding Diagrams:
AD7501 17–60
AD7502 17–60
AD7503 17–60
AD7506 17–60
AD7507 17–61
AD7510 17–61
AD7511 17–61
AD7512 17–61
AD7520 17–61
AD7521 17–62
AD7522 17–62
AD7523 17–62
AD7524 17–62

Page

AD7533 17–63

AD7541 17–63

AD7542 17–63

AD7543 17–63

AD7550 17–64

AD7574 17–64

●AD7590 17–65

●AD7591 17–65

●AD7592 17–65

●New product since the *1980 Data-Acquisition Components and Subsystems Catalog.*

DACPORT is a trademark of Analog Devices, Inc.

Bipolar Integrated Circuit Chips

General Information

PHYSICAL CHARACTERISTICS

Die Thickness: The standard thickness of Analog Devices Bipolar dice is 20 mils ±2 mils.

Die Dimensions: The dimensions given on the specific device data sheets have a tolerance of ±2 mils.

Backing: The standard backside surface is silicon (not plated). Analog Devices does not recommend gold-backed dice for most applications.

Edges: A diamond saw is used to separate wafers into dice thus providing perpendicular edges half-way through the die.

In contrast to scribed dice, this technique provides a more uniform die shape and size. The perpendicular edges facilitate handling (such as tweezer pick-up) while the uniform shape and size simplifies substrate design and die attach.

Top Surface: The standard top surface of the die is covered by a layer of glassivation. All areas are covered except bonding pads and scribe lines.

Surface Metalization: The metalization on Analog Devices Bipolar dice is aluminum. Minimum thickness is 10,000Å.

Bonding Pads: All bonding pads have a minimum size of 4 mils by 4 mils. The passivation windows are 3.5 mils by 3.5 mils minimum.

PACKAGING

All dice are packaged in plastic waffle packs. The quantity of dice per package depends on die size.

A sheet of anti-static paper and a sheet of anti-static plastic is included in each pack.

Waffle packs are secured and shipped in cardboard shipping containers.

ASSEMBLY INFORMATION

Cleaning: Each die is cleaned prior to packaging in waffle packs. No additional cleaning is recommended.

Dice Inspection: Standard dice are 100% inspected to MIL-STD-883, Method 2010, Class B.

Die Attach: The proper method of die attach is determined by the requirements of the particular application.

If an adhesive die attach technique is required by the constraints of the application, then package moisture content must be monitored. To insure reliability the internal moisture content of the package has to remain below 5000ppm (from 0 to 1000 hrs. minimum).

When eutectic die attach is used, Analog Devices recommends using either a 99.99% gold or a 98% gold, 2% silicon preform.

Recommended eutectic die attach temperature is 410°C ±10°C as measured at the die-substrate interface surface. Time at 410°C shall not exceed 30 seconds.

Lead Bonding: Analog Devices recommends bonding one mil 99.99% gold for gold ball bonding.

Analog Devices recommends ultra-sonic bonding for users requiring aluminum wire. One mil 99% aluminum 1% silicon wire is recommended.

Unless otherwise specified on the device data sheet, there is no required bonding sequence for bipolar chips.

Electrostatic Discharge (ESD): Bipolar integrated circuits are subject to catastrophic damage due to electrostatic charges generated by careless handling.

Furthermore, subtle shifts in transistor characteristics can occur after being subjected to lower amounts of ESD. Precision devices, trimmed to accuracies in the order of ±25 microvolts, can be shifted out of spec due to improper handling.

To preserve the accuracy of precision bipolar integrated circuits, Analog Devices recommends the following:

a. Verify proper grounding of all manufacturing equipment.

b. All workers who handle the chips should be wearing a grounded conductive wrist-strap.

c. All work-in-process, especially any work with incomplete wire-bonding, should be placed on a conductive surface.

d. Dice not in use should be stored in the original waffle pack with anti-static paper.

PACKAGE SEALING RECOMMENDATIONS

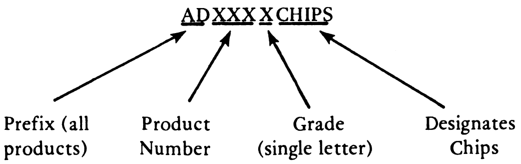
Analog Devices recommends hermetic packaging. The initial precision of trimmed thin-film integrated circuits is retained indefinitely when not subjected to high humidity or corrosive environments.

A maximum sealing temperature of 320°C for a maximum time of 3 minutes is recommended.

The sealing technique must insure that the internal moisture content remain below 5000ppm under all conditions for the life time of the product.

ORDERING INFORMATION

Analog Devices bipolar integrated circuit chips are specified in the same manner as packaged devices, except the package code letter is replaced by the word "CHIPS".



Minimum order quantity is 25 pieces per line item. Analog Devices dice are supplied only in multiples of 25 pieces.

USING DATA SHEETS

Specifications: Electrical tests are performed at wafer probe, before the wafer is separated into individual dice. Maintaining chip performance to specification requires great care in handling and assembly. The specific recommendations in this General Information Section are intended to assist the user in achieving specified performance of Analog Devices chips in assembled circuits. Electrical specifications are given for each product. *NOTE*: Although the specifications generally conform to those of equivalent grades of packaged product, some differences exist.

AC testing at the chip level is also not practical; therefore, ac specifications are also given as typical.

Applications Information: General applications information is not included on the chip data sheets; this information is provided on the data sheet for the packaged version of each product.

Specific application information that applies to the chip version of each product is given on the chip data sheet.

Metalization Photograph: Metalization photographs are provided for each product. Chip dimensions and pad functions are included.

ADDITIONAL PRODUCT AVAILABILITY INFORMATION

Older Products: The data sheets published in this catalog are intended to assist the user in the design of new hybrid circuits using the highest performance, most cost-effective products available from Analog Devices. There are, however, older IC products that may have been designed into circuits in the past but which are no longer the optimum choice for new designs. These products continue to be available as in the past.

If you are using one of these older Analog Devices IC chips and require technical assistance, please contact the factory. Sales-related information may be obtained from the nearest Analog Devices sales office listed on the back cover.

New Products: Analog Devices is continuously introducing new integrated circuit products. Most of these are monolithic and thus may be supplied in chip form. Although it is our policy to obtain first-hand assembly, testing and application experience with new products before introducing the chip version, we encourage potential users to contact the factory for availability information on new IC products not listed in this catalog.

ANALOG DEVICES

Low Cost, Laser Trimmed Precision IC Op Amp

AD517 CHIPS

PRODUCT DESCRIPTION

The Analog Devices AD517 operational amplifier is laser-trimmed for ultra-low offset voltages, thus eliminating the need to trim in most applications. Other features include very low offset voltage drift and high gain. Advanced super-beta techniques provide ultra-low input currents. The AD517 is ideal for precision instrumentation applications. Protected input and output circuitry along with internal compensation for gains of one or greater minimize hybrid component count. AD517 chips are available in two grades specified for operation between 0 and +70°C and one grade specified for operation between -55°C and +125°C.

APPLICATION INFORMATION

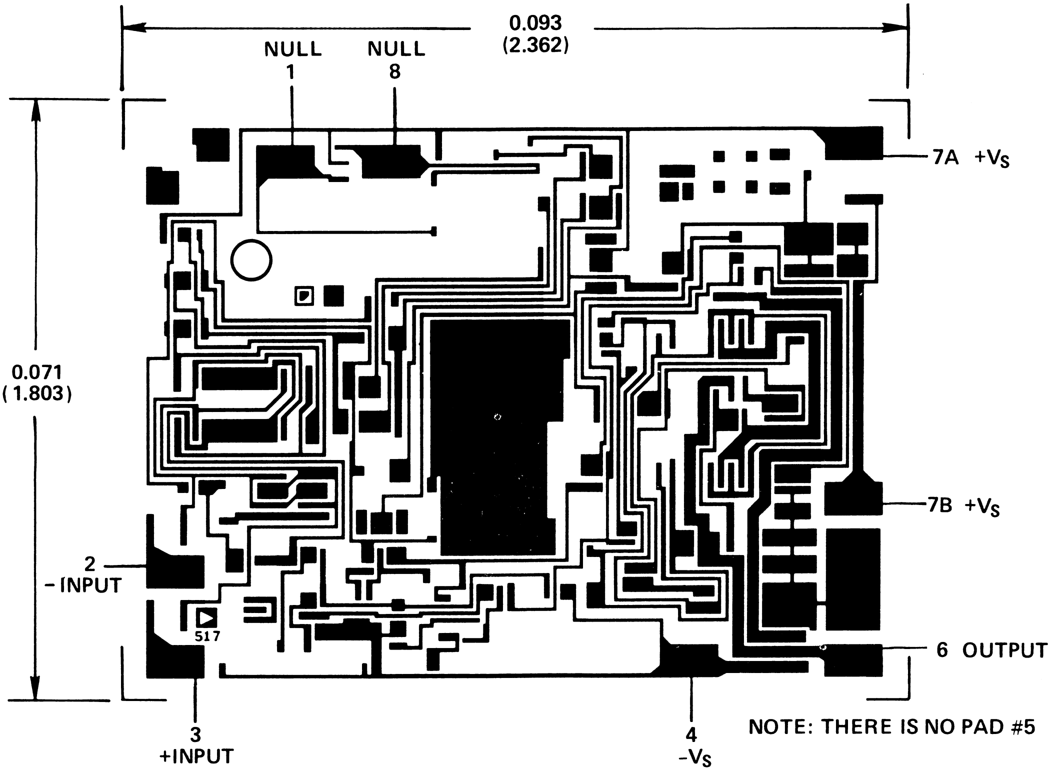
AD517 chips are functionally identical to packaged AD517 devices. For general application information, see the AD517 packaged product catalog data sheet.

The following additional application information applies to AD517 chips:

1. No particular wire-bonding sequence must be followed.
2. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
3. For performance to device specifications, the metal substrate pad or header beneath the AD517 chip must be connected to $-V_S$, device pad number 4.
4. Pads 7A and 7B must *both* be connected to $+V_S$.
5. Do not connect to any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



NOTE: THERE IS NO PAD #5

PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE TO-99 8 PIN METAL PACKAGE.

SPECIFICATIONS[1] (typical @+25°C and ±15V dc unless otherwise noted)

MODEL	AD517J	AD517K	AD517S
OPEN LOOP GAIN			
$V_O = \pm10V$, $R_L \geqslant 2k\Omega$	10^6	*	*
$T_A = +25°C$ to T_{max}	500,000 min	*	250,000
$T_A = T_{min}$ to $+25°C$	500,000	*	250,000
OUTPUT CHARACTERISTICS			
Voltage @ $R_L \geqslant 2k\Omega$, T_{min} to T_{max}	±10V min	*	*
Load Capacitance	1000pF	*	*
Output Current	10mA min	*	*
Short Circuit Current	25mA	*	*
FREQUENCY RESPONSE			
Unity Gain, Small Signal	250kHz	*	*
Full Power Response	1.5kHz	*	*
Slew Rate, Unity Gain	0.10V/μs	*	*
INPUT OFFSET VOLTAGE			
Initial Offset, $R_S \leqslant 10k\Omega$	150μV max	75μV max	**
vs. Temp, $T_A = +25°C$ to T_{max}	3.0μV/°C max	1.8μV/°C max	**
$T_A = T_{min}$ to $+25°C$	3.0μV/°C	1.8μV/°C	**
vs. Supply	25μV/V max	10μV/V max	**
$T_A = +25°C$ to T_{max}	40μV/V max	15μV/V max	20μV/V max
$T_A = T_{min}$ to $+25°C$	40μV/V	15μV/V	20μV/V
INPUT OFFSET CURRENT			
Initial	1nA max	0.75nA max	**
$T_A = +25°C$ to T_{max}	1.5nA max	1.25nA max	2nA max
$T_A = T_{min}$ to $+25°C$	1.5nA	1.25nA	2nA
INPUT BIAS CURRENT			
Initial	5nA max	2nA max	**
$T_A = +25°C$ to T_{max}	8nA max	3.5nA max	10nA max
$T_A = T_{min}$ to $+25°C$	8nA	3.5nA	10nA
vs. Temp, T_{min} to T_{max}	±20pA/°C	±10pA/°C	**
INPUT IMPEDANCE			
Differential	15MΩ‖1.5pF	20MΩ‖1.5pF	**
Common Mode	$2.0 \times 10^{11}\Omega$	*	*
INPUT NOISE			
Voltage, 0.1Hz to 10Hz	2μV p-p	*	*
f = 10Hz	$35nV/\sqrt{Hz}$	*	*
f = 100Hz	$25nV/\sqrt{Hz}$	*	*
f = 1kHz	$20nV/\sqrt{Hz}$	*	*
Current, f = 10Hz	$0.05pA/\sqrt{Hz}$	*	*
f = 100Hz	$0.03pA/\sqrt{Hz}$	*	*
f = 1kHz	$0.03pA/\sqrt{Hz}$	*	*
INPUT VOLTAGE RANGE			
Differential or Common Mode, max safe	$\pm V_S$	*	*
Common Mode Rejection, $V_{IN} = \pm10V$	94dB min	110dB	**
Common Mode Rejection, $T_A = +25°C$ to T_{max}	94dB min	100dB min	**
$T_A = T_{min}$ to $+25°C$	94dB	100dB	**
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	±(5 to 18)V	*	±(5 to 22)V
Current, Quiescent	4mA max	3mA max	**
TEMPERATURE RANGE			
Operating			
Tested ($T_A = +25°C$ to T_{max})	+25°C to +70°C	*	+25°C to +125°C
Guaranteed, Not Tested ($T_A = T_{min}$ to $+25°C$)	0 to +25°C	*	-55°C to +25°C
Storage	-65°C to +150°C	*	*

NOTES

*Specifications same as AD517J.

**Specifications same as AD517K.

[1] Electrical tests are performed at wafer probe, before the wafer is separated into individual dice. Maintaining chip performance to specification requires great care in handling and assembly.

Specifications subject to change without notice.

ANALOG DEVICES

Low Cost, High Speed, IC Op Amp

AD518 CHIPS

PRODUCT DESCRIPTION

The AD518 is a low cost, high speed operational amplifier designed as an improved functional replacement for 118-type devices. It is internally compensated for unity gain, but has the capability of accepting feed-forward compensation for increased slew rate and bandwidth. AD518 chips are available in two grades specified for operation between 0 and +70°C and one grade for operation between -55°C and +125°C.

APPLICATION INFORMATION

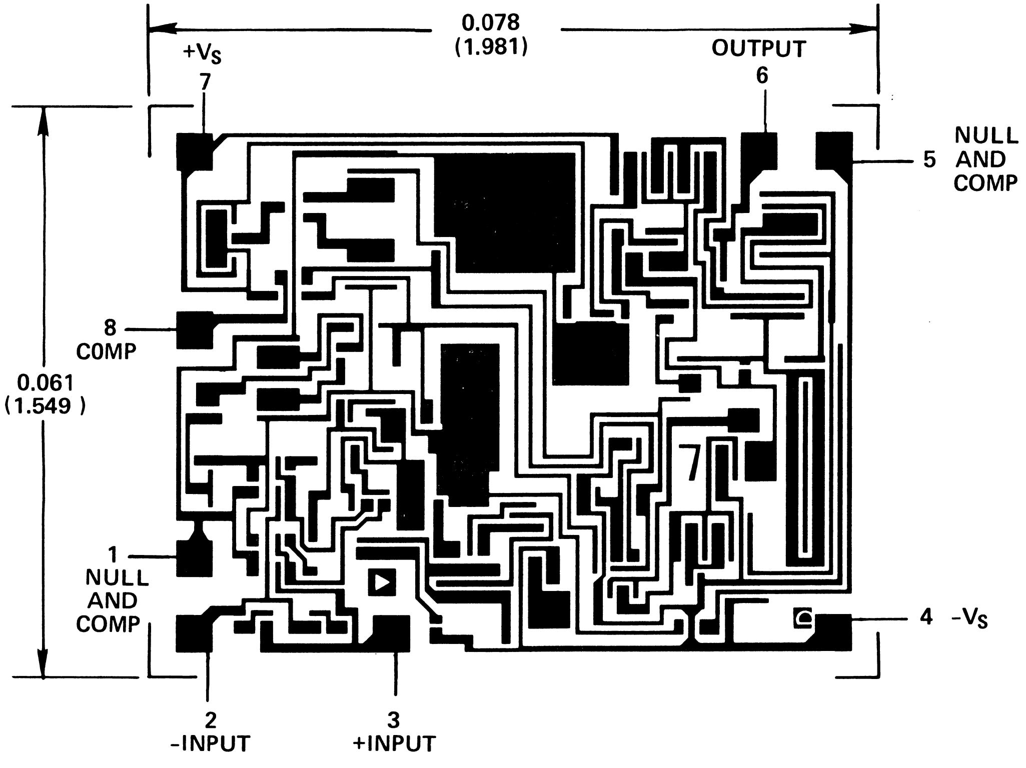
AD518 chips are functionally identical to packaged AD518 devices. For general application information, see the AD518 packaged product catalog data sheet.

The following additional application information applies to AD518 chips:

1. No particular wire-bonding sequence must be followed.
2. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
3. For performance to device specifications, the metal substrate pad or header beneath the AD518 chip must be connected to $-V_S$, device pad number 4.
4. Do not connect to any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE TO-99 8 PIN METAL PACKAGE.

SPECIFICATIONS[1] (typical @ +25°C and V_S = ±15V dc unless otherwise specified)

PARAMETER	AD518J	AD518K	AD518S
OPEN LOOP GAIN			
$R_L \geq 2k\Omega$, $V_O = \pm 10V$	25,000 min (100,000 typ)	50,000 min (100,000 typ)	**
$T_A = +25°C$ to T_{max}	20,000 min	25,000 min	**
$T_A = T_{min}$ to $+25°C$	20,000	25,000	**
OUTPUT CHARACTERISTICS			
Voltage @ $R_L \geq 2k\Omega$, T_A = min to max	±12V min (±13V typ)	*	*
Current @ $V_O = \pm 10V$	±10mA	*	*
Short Circuit Current	25mA	*	*
FREQUENCY RESPONSE			
Unity Gain, Small Signal	12MHz	*	*
Slew Rate, Unity Gain	50V/μs	*	*
Settling Time to 0.1% (Single Capacitor Compensation)	800ns	*	*
Phase Margin, Uncompensated at Unity Gain Crossover Frequency	60°	*	*
INPUT OFFSET VOLTAGE			
Initial, $R_S \leq 10k\Omega$	10mV max (4mV typ)	4mV max (2mV typ)	**
$T_A = +25°C$ to T_{max}	15mV max	6mV max	**
$T_A = T_{min}$ to $+25°C$	15mV	6mV	**
Avg vs. Temp, $T_A = 25°C$ to T_{max}	10μV/°C	15μV/°C max (5μV/°C typ)	20μV/°C max (10μV/°C typ)
$T_A = T_{min}$ to $+25°C$	10μV/°C	5μV/°C	*
Avg vs. Supply, $T_A = +25°C$ to T_{max}	65dB min (80dB typ)	80dB min (90dB typ)	**
$T_A = T_{min}$ to $+25°C$	80dB	90dB	**
INPUT BIAS CURRENT			
Initial	500nA max (120nA typ)	250nA max (120nA typ)	**
$T_A = +25°C$ to T_{max}	750nA max	400nA max	**
$T_A = T_{min}$ to $+25°C$	750nA	400nA	**
INPUT OFFSET CURRENT			
Initial	200nA max (30nA typ)	50nA max (6nA typ)	**
$T_A = +25°C$ to T_{max}	300nA max	100nA max	**
$T_A = T_{min}$ to $+25°C$	300nA	100nA	**
INPUT IMPEDANCE			
Differential	0.5MΩ min (3.0MΩ typ)	*	*
INPUT VOLTAGE RANGE†			
Common Mode, max safe	$\pm V_S$	*	*
Operating, $V_S = \pm 15V$	±11.5V	*	*
Common Mode Rejection Ratio	70dB min (100dB typ)	80dB min (100dB typ)	**
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	±(5 to 20)V	*	*
Current, Quiescent	10mA max (5mA typ)	7mA max (5mA typ)	**
TEMPERATURE RANGE			
Operating			
Tested ($T_A = +25°C$ to T_{max})	+25°C to +70°C	*	+25°C to +125°C
Guaranteed, Not Tested ($T_A = T_{min}$ to $+25°C$)	0 to +25°C	*	-55°C to +25°C
Storage	-65°C to +150°C	*	*

NOTES

†The inputs are shunted with back-to-back diodes; if the differential input may exceed ±1 volt, a resistor should be used to limit the input current to 10mA.

*Specifications same as AD518J.

**Specifications same as AD518K.

Specifications subject to change without notice.

[1] Electrical tests are performed at wafer probe, before the wafer is separated into individual dice. Maintaining chip performance to specification requires great care in handling and assembly.

ANALOG DEVICES

Precision Instrumentation Amplifier

AD521 CHIPS

PRODUCT DESCRIPTION

The AD521 is a second generation, low cost monolithic instrumentation amplifier. As a true IA, it exhibits high input impedance, balanced differential inputs, low bias currents and high CMR. Gain is programmed for values between 0.1 and 1000 by two external resistors. The AD521 is internally compensated and input and output protected. Two AD521 chip grades are specified for operation between 0 and +70°C while one grade is specified over the -55°C to +125°C range.

APPLICATION INFORMATION

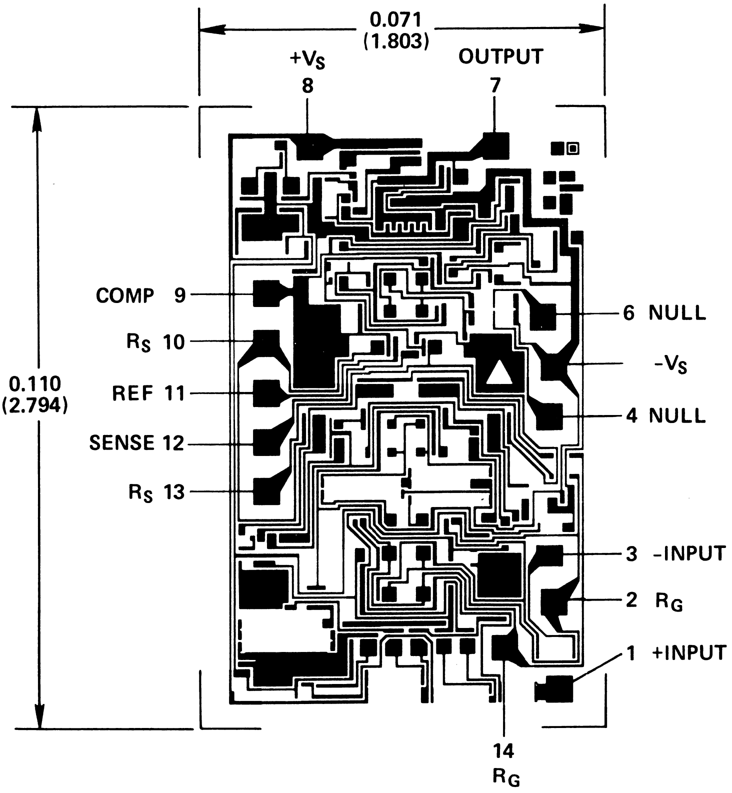
AD521 chips are functionally identical to packaged AD521 devices. For general application information, see the AD521 packaged product catalog data sheet.

The following additional application information applies to AD521 chips:

1. No particular wire-bonding sequence must be followed.
2. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
3. For performance to device specifications, the metal substrate pad or header beneath the AD521 chip must be connected to $-V_S$, device pad number 5.
4. Do not connect to any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE TO-116 14 PIN CERAMIC PACKAGE.

17

SPECIFICATIONS*** (typical @ V_S = ±15V, R_L =2kΩ and T_A = 25°C unless otherwise specified)

MODEL	AD521J	AD521K	AD521S
GAIN			
Range (For Specified Operation, Note 1)	1 to 1000	•	•
Equation	$G = R_S/R_G$ V/V	•	•
Error from Equation	(±0.25−0.004G)%	•	•
Nonlinearity (Note 2)			
$1 \leqslant G \leqslant 1000$	0.2% max	•	•
Gain Temperature Coefficient	±(3 ±0.05G)ppm/°C	•	±(15 ±0.4G)ppm/°C
OUTPUT CHARACTERISTICS			
Rated Output	±10V, ±10mA min	•	•
Output at Maximum Operating Temperature	±10V @ 5mA min	•	•
Impedance	0.1Ω	•	•
DYNAMIC RESPONSE			
Small Signal Bandwidth (±3dB)			
G = 1	>2MHz	•	•
G = 10	300kHz	•	•
G = 100	200kHz	•	•
G = 1000	40kHz	•	•
Small Signal, ±1.0% Flatness			
G = 1	75kHz	•	•
G = 10	26kHz	•	•
G = 100	24kHz	•	•
G = 1000	6kHz	•	•
Full Peak Response (Note 3)	100kHz	•	•
Slew Rate, $1 \leqslant G \leqslant 1000$	10V/μs	•	•
Settling Time (any 10V step to within 10mV of Final Value)			
G = 1	7μs	•	•
G = 10	5μs	•	•
G = 100	10μs	•	•
G = 1000	35μs	•	•
Differential Overload Recovery (±30V Input to within 10mV of Final Value) (Note 4)			
G = 1000	50μs	•	•
Common Mode Step Recovery (30V Input to within 10mV of Final Value) (Note 5)			
G = 1000	10μs	•	•
VOLTAGE OFFSET (may be nulled)			
Input Offset Voltage (V_{OS_1})	3mV max (2mV typ)	1.5mV max (0.5mV typ)	••
vs. Temperature, T_A = +25°C to T_{max}	15μV/°C max (7μV/°C typ)	5μV/°C max (1.5μV/°C typ)	••
$T_A = T_{min}$ to +25°C	7μV/°C	1.5μV/°C	••
vs. Supply	3μV/%	•	
Output Offset Voltage (V_{OS_0})	400mV max (200mV typ)	200mV max (30mV typ)	••
vs. Temperature, T_A = +25°C to T_{max}	400μV/°C max (150μV/°C typ)	150μV/°C max (50μV/°C typ)	••
$T_A = T_{min}$ to +25°C	150μV/°C	50μV/°C	••
vs. Supply (note 6)	$0.005 V_{OS_0}$/%	•	•
INPUT CURRENTS			
Input Bias Current (either input)	80nA max	40nA max	••
vs. Temperature, T_A = +25°C to T_{max}	1nA/°C max	500pA/°C max	••
$T_A = T_{min}$ to +25°C	1nA/°C	500pA/°C	••
vs. Supply	2%/V	•	•
Input Offset Current	20nA max	10nA max	••
vs. Temperature, T_A = +25°C to T_{max}	250pA/°C max	125pA/°C max	••
$T_A = T_{min}$ to +25°C	250pA/°C	125pA/°C	••
INPUT			
Differential Input Impedance (Note 7)	3×10^9Ω‖1.8pF	•	•
Common Mode Input Impedance (Note 8)	6×10^{10}Ω‖3.0pF	•	•
Input Voltage Range for Specified Performance (with respect to ground)	±10V	•	•
Maximum Voltage without Damage to Unit, Power ON or OFF Differential Mode (Note 9)	30V	•	•
Voltage at either input (Note 9)	V_S ±15V	•	•
Common Mode Rejection Ratio, DC to 60Hz with 1kΩ source unbalance			
G = 1	70dB min (74dB typ)	74dB min (80dB typ)	••
G = 10	90dB min (94dB typ)	94dB min (100dB typ)	••
G = 100	100dB min (104dB typ)	104dB min (114dB typ)	••
G = 1000	100dB min (110dB typ)	110dB min (120dB typ)	••
NOISE			
Voltage RTO (p-p) @ 0.1Hz to 10Hz (Note 10)	$\sqrt{(0.5G)^2 + (225)^2}\,\mu V$	•	•
RMS RTO, 10Hz to 10kHz	$\sqrt{(1.2G)^2 + (50)^2}\,\mu V$	•	•
Input Current, rms, 10Hz to 10kHz	15pA (rms)	•	•
REFERENCE TERMINAL			
Bias Current	3μA	•	•
Input Resistance	10MΩ	•	•
Voltage Range	±10V	•	•
Gain to Output	1	•	•
POWER SUPPLY			
Operating Voltage Range	±5 to ±18	•	•
Quiescent Supply Current	5mA max	•	•
TEMPERATURE RANGE			
Operating			
Tested (T_A = +25°C to T_{max})	+25°C to +70°C	•	+25°C to +125°C
Guaranteed, Not Tested ($T_A = T_{min}$ to +25°C)	0 to +25°C	•	−55°C to +25°C
Storage	−65°C to +150°C	•	•

NOTES:

All Numbered Notes Refer to AD521 Packaged Product Catalog Data Sheet in Section 5.

•Specifications same as AD521J.

••Specifications same as AD521K.

•••Electrical tests are performed at wafer probe, before the wafer is separated into individual dice. Maintaining chip performance to specification requires great care in handling and assembly.

Specifications subject to change without notice.

ANALOG DEVICES

Trimmed IC Multiplier

AD532 CHIPS

PRODUCT DESCRIPTION

The AD532 is a complete laser-trimmed analog multiplier/divider that performs to specification without any external trims or additional components. In hybrid applications, AD532 chips can eliminate the need to design and operate complicated trim and test equipment while conserving valuable substrate area. As a multiplier, the AD532 operates as a full four-quadrant device; division is performed in two quadrants. AD532 chips are available in two grades specified for 0 to +70°C operation and one grade for -55°C to +125°C.

APPLICATION INFORMATION

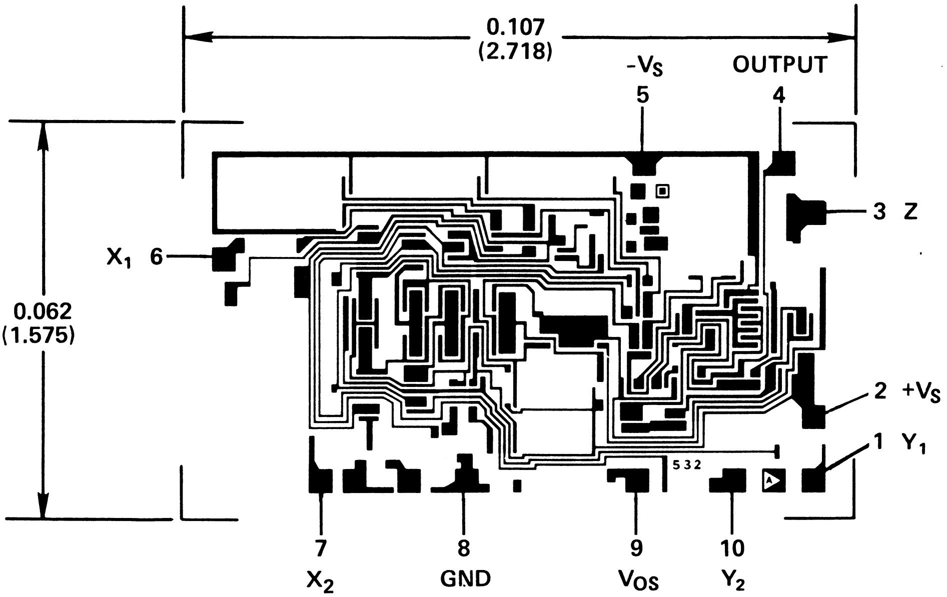
AD532 chips are functionally identical to packaged AD532 devices. For general application information, see the AD532 packaged product catalog data sheet and the Analog Devices "Multiplier Application Guide".

The following additional application information applies to AD532 chips:

1. No particular wire-bonding sequence must be followed.
2. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
3. For performance to device specifications, the metal substrate pad or header beneath the AD532 chip must be connected to $-V_S$, device pad number 5.
4. Do not connect to any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE TO-100 10 PIN METAL PACKAGE.

SPECIFICATIONS[1] (typical @ +25°C with V_S = ±15V dc, V_{OS} grounded, unless otherwise specified)

PARAMETER	CONDITIONS	AD532J	AD532K	AD532S
ABSOLUTE MAX RATINGS				
Supply Voltage		±18V	*	±22V
Internal Power Dissipation		500mW	*	*
Input Voltage[2]				
X, Y, V_{OS}, Z		±V_S	*	*
Output Short Circuit	To Ground	Indefinite	*	*
MULTIPLIER SPECIFICATIONS				
Transfer Function		$(X_1-X_2)(Y_1-Y_2)/10$	*	*
Total Error (% F.S.)	V_X = 0/±10V, V_Y = 0/±10V	±2.0% max [±1.5% typ]	±1.0% max [±0.7% typ]	±1.0% max [±0.5% typ]
	T_A = +25°C to T_{max}	±2.5%	±1.5%	±4.0% max
	T_A = T_{min} to +25°C	±2.5%	±1.5%	±4.0%
vs. Temperature	T_A = +25°C to T_{max}	±0.04%/°C	±0.03%/°C	±0.04%/°C max [±0.01%/°C typ]
	T_A = T_{min} to +25°C	±0.04%/°C	±0.03%/°C	±0.01%/°C
Nonlinearity				
X Input	V_X = 20V(p-p), V_Y = ±10V	±0.8%	±0.5%	**
Y Input	V_Y = 20V(p-p), V_X = ±10V	±0.3%	±0.2%	**
Feedthrough				
X Input	V_X = 20V(p-p), V_Y = 0, f = 50Hz	200mV(p-p) max [50mV(p-p) typ]	100mV(p-p) max [30mV(p-p) typ]	**
Y Input	V_Y = 20V(p-p), V_X = 0, f = 50Hz	150mV(p-p) max [30mV(p-p) typ]	80mV(p-p) max [25mV(p-p) typ]	**
vs. Temperature	T_A = min to max	2.0mV(p-p)/°C	1.0mV(p-p)/°C	**
DIVIDER SPECIFICATIONS				
Transfer Function		$10Z/(X_1-X_2)$	*	*
Total Error[3]	V_X = −10V, V_Z = ±10V	±2%	±1%	**
	V_X = −1V, V_Z = ±10V	±4%	±3%	**
SQUARER SPECIFICATIONS				
Transfer Function		$(X_1-X_2)^2/10$	*	*
Total Error		±0.8%	±0.4%	**
SQUARE ROOTER SPECIFICATIONS				
Transfer Function		$-\sqrt{10Z}$	*	*
Total Error[3]	V_Z = 0/+10V	±1.5%	±1.0%	**
INPUT SPECIFICATIONS				
Input Resistance				
X, Y Inputs		10MΩ	*	*
Z Input		36kΩ	*	*
Input Bias Current				
X, Y Inputs		3μA	4μA max [1.5μA typ]	**
Z Input		±10μA	±15μA max [±5μA typ]	**
X, Y Inputs	T_A = min to max	10μA	8μA	**
Z Input	T_A = min to max	±30μA	±25μA	**
Input Offset Current				
X, Y Inputs		±0.3μA	±0.1μA	**
Input Voltage Diff/CM	T_A = min to max			
X, Y, Z Inputs	For Rated Accuracy	±10V	*	*
CMRR (X or Y Inputs)	X or Y = ±10V	40dB min	50dB min	**
DYNAMIC SPECIFICATIONS				
Small Signal, Unity Gain		1.0MHz	*	*
Full Power Bandwidth		750kHz	*	*
Slew Rate		45V/μs to 2%	*	*
Small Signal Amplitude Error		1% at 75kHz	*	*
Small Signal 1% Vector Error	0.5° phase shift	5kHz	*	*
Settling Time	±10V step	1μs to 2%	*	*
Overload Recovery		2μs to 2%	*	*
OUTPUT AMPLIFIER SPECIFICATIONS				
Output Impedance	Closed Loop	1Ω	*	*
Output Voltage Swing	T_A = min to max $R_L \geqslant 2k\Omega$, $C_L \leqslant 1000pF$	±10V min [±13V typ]	*	*
Output Noise	f = 5Hz to 10kHz	0.6mV(rms)	*	*
	f = 5Hz to 5MHz	3.0mV(rms)	*	*
Output Offset Voltage				
Initial Offset	Trimmable To Zero	±40mV	±30mV max	**
vs. Temperature	T_A = +25°C to T_{max}	0.7mV/°C	*	2.0mV/°C max
	T_A = T_{min} to +25°C	0.7mV/°C	*	*
POWER SUPPLY SPECIFICATIONS				
Supply Voltage	Rated Performance	±15V	*	*
	Operating	±10V to ±18V	*	±10V to ±22V
Supply Current	Quiescent	±6mA max [±4mA typ]	*	*
Power Supply Variation				
Multiplier Accuracy		±0.05%/%	*	*
Output Offset		±2.5mV/%	*	*
Scale Factor		−0.03%/%	*	*
Feedthrough		±0.25mV/%	*	*
TEMPERATURE				
Operating,	tested (T_A = +25°C to T_{max})	+25°C to +70°C	*	+25°C to +125°C
	guaranteed, not tested (T_A = T_{min} to +25°C)	0 to +25°C	*	-55°C to +25°C
Storage		-65°C to +150°C	*	*

NOTES:

[1] Electrical tests are performed at wafer probe, before the wafer is separated into individual dice. Maintaining chip performance to specification requires great care in handling and assembly.

[2] Max input voltage is zero when supplies are turned off.

[3] With recommended external trim (see packaged AD532 data sheet).

*Specifications same as AD532J.

**Specifications same as AD532K.

Specifications subject to change without notice.

ANALOG DEVICES

Trimmed Precision IC Multiplier

AD534 CHIPS

AD535 NOTE:

The AD534 is a functional equivalent to the AD535 divider. Since the AD535 is not available in chip form, AD534 chips are recommended for divider as well as multiplier applications; see the AD535 packaged product data sheet for application recommendations.

PRODUCT DESCRIPTION

The AD534 is a precision laser-trimmed four-quadrant multiplier/two-quadrant divider that requires no external components to achieve accuracies usually found in expensive assemblies. As a hybrid building-block, AD534 chips can guarantee errors as small as ±0.50%. Differential inputs, internal calibrated reference, output amplifier and a versatile configuration are all features of the AD534. AD534 chips are available in two grades specified for operation between 0 and +70°C and one grade specified for -55°C to +125°C.

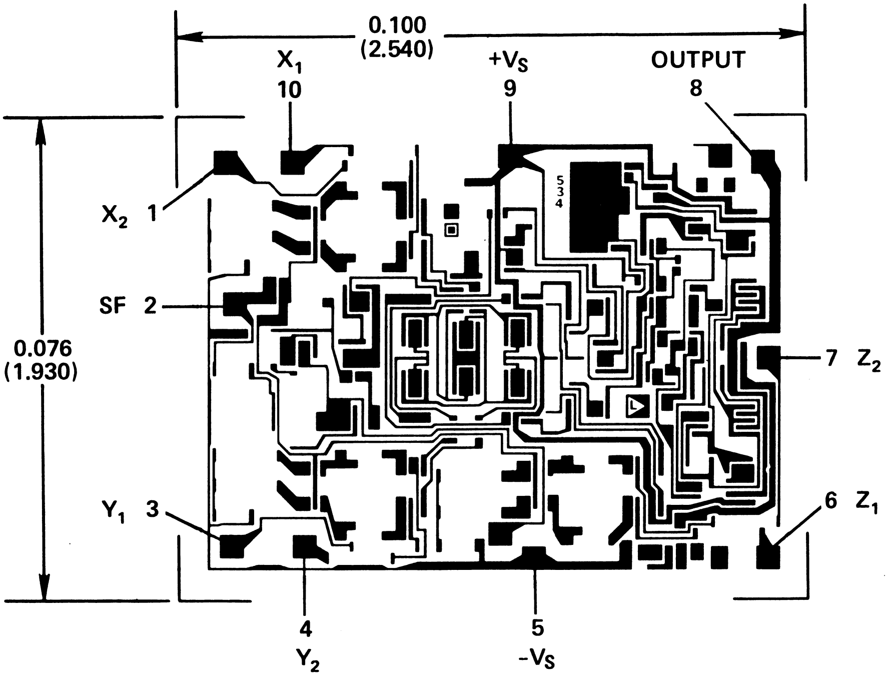
APPLICATION INFORMATION

AD534 chips are functionally identical to packaged AD534 and AD535 devices. For general application information, see the AD534 and AD535 packaged product catalog data sheets and the Analog Devices "Multiplier Application Guide."

The following additional application information applies to AD534 chips:

1. No particular wire-bonding sequence must be followed.
2. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
3. For performance to device specifications, the metal substrate pad or header beneath the AD534 chip must be connected to $-V_S$, device pad number 5.
4. Do not connect to any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.

METALIZATION PHOTOGRAPH
Dimensions shown in inches and (mm).



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE TO-100 10 PIN METAL PACKAGE.

SPECIFICATIONS[1] (typical at +25°C, with ±V_S = 15V, $R_L \geqslant$ 2k, unless otherwise stated)

PARAMETER	CONDITIONS	AD534J	AD534K	AD534S
MULTIPLIER PERFORMANCE				
Transfer Function		$\frac{(X_1 - X_2)(Y_1 - Y_2)}{10} + Z_2$	•	•
Total Error[2]	$-10V \leqslant X, Y \leqslant +10V$	±1.0% max	±0.5%	•
	V_S = ±14V to ±16V T_A = +25°C to T_{max}	±1.5%	±1.0%	±2.0% max
	V_S = ±14V to ±16V T_A = T_{min} to +25°C	±1.5%	±1.0%	±2.0%
vs. Temperature	T_A = +25°C to T_{max}	±0.022%/°C	±0.015%/°C	±0.02%/°C max
	T_A = T_{min} to +25°C	±0.022%/°C	±0.015%/°C	±0.02%/°C
Scale Factor Error	SF = 10.00 nominal[3]	±0.25%	±0.1%	•
Temperature-Coefficient of Scaling-Voltage	T_A = min to max	±0.02%/°C	±0.01%/°C	•
Supply Related Error	±V_S = (15V) ±1V	±0.01%	•	•
Nonlinearity, X	X = 20V pk-pk Y = ±10V	±0.4%	±0.2% (0.3% max)	•
Nonlinearity, Y	Y = 20V pk-pk X = ±10V	±0.01%	±0.01% (±0.1% max)	•
Feedthrough[4], X	Y nulled X = 20V pk-pk 50Hz	±0.3%	±0.15% (0.3% max)	•
Feedthrough[4], Y	X nulled Y = 20V pk-pk 50Hz	±0.01%	±0.01% (±0.1% max)	•
Output Offset	T_A = +25°C to T_{min}	±5mV (±30mV max)	±2mV (±15mV max)	•
Voltage Drift		200µV/°C	100µV/°C	500µV/°C max
	T_A = T_{min} to +25°C	±5mV	±2mV	•
		200µV/°C	100µV/°C	500µV/°C
DYNAMICS				
Small-Signal BW	V_{OUT} = 0.1V rms	1MHz	•	•
1% Amplitude Error	C_{LOAD} = 1000pF	50kHz	•	•
Slew Rate	V_{OUT} 20V pk-pk	20V/µs	•	•
Settling Time to ±1%	ΔV_{OUT} = 20V	2µs	•	•
NOISE				
Noise Spectral-Density	SF = 10	$0.8\mu V/\sqrt{Hz}$	•	•
	SF = 3 (Note 5)	$0.4\mu V/\sqrt{Hz}$	•	•
Wideband Noise	f = 10Hz to 5MHz	1mV rms	•	•
	f = 10Hz to 10kHz	90µV rms	•	•
	f = 10Hz to 10kHz, SF = 3 (Note 5)	60µV rms	•	•
OUTPUT				
Output Voltage Swing	T_A = min to max	±11V min	•	•
Output Impedance	Unity-Gain, f ⩽ 1kHz	0.1Ω	•	•
Amplifier Open-Loop Gain	f = 50Hz	70dB	•	•
Maximum Output Current	R_L = 0, T_A = min to max	30mA	•	•
INPUT AMPLIFIERS (X, Y and Z)[6]				
Signal Voltage Range	Rated Accuracy (Diff. or CMR)	±10V	•	•
	Operating (Diff.)	±12V	•	•
Offset Voltage, X, Y		±5mV (±20mV max)	±2mV (±10mV max)	•
Drift	T_A = T_{min} to T_{max}	100µV/°C	50µV/°C	•
Offset Voltage, Z		±5mV (±30mV max)	±2mV (±15mV max)	•
Drift	T_A = +25°C to T_{max}	200µV/°C	100µV/°C	500µV/°C max
		±5mV	±2mV	•
	T_A = T_{min} to +25°C	200µV/°C	100µV/°C	500µV/°C
CMRR (X, Y, Z)	50Hz, 20V pk-pk	80dB (60dB min)	90dB (70dB min)	•
Bias Current	Diff. Input = 0	0.8µA (2µA max)	•	•
Offset Current	Diff. Input = 0	0.1µA	•	•
Differential Resistance		10MΩ	•	•
DIVIDER PERFORMANCE				
Transfer Function	$X_1 > X_2$	$10\frac{(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1$	•	•
Total Error[2]	X = 10V $-10V \leqslant Z \leqslant +10V$	±0.75%	±0.35%	•
	X = 1V $-1V \leqslant Z \leqslant +1V$	±2.0%	±1.0%	•
	$0.1V \leqslant X \leqslant 10V$ $-10V \leqslant Z \leqslant +10V$	±2.5%	±1.0%	•
SQUARER PERFORMANCE				
Transfer Function		$\frac{(X_1 - X_2)^2}{10} + Z_2$	•	•
Total Error[2]	$-10V \leqslant X \leqslant +10V$	±0.6%	±0.3%	•
SQUARE-ROOTER PERFORMANCE				
Transfer Function	$Z_1 \leqslant Z_2$	$\sqrt{10(Z_2 - Z_1)} + X_2$	•	•
Total Error[1]	$1V \leqslant Z \leqslant 10V$	±1.0%	±0.5%	•
POWER SUPPLY SPECIFICATIONS				
Supply Voltage	Rated Performance	±15V	•	•
	Operating	±8V to ±18V	•	±8V to ±22V
Supply Current	Quiescent	4mA (6mA max)	•	•
TEMPERATURE				
Operating, tested	(T_A = +25°C to T_{max})	+25°C to +70°C	•	+25°C to +125°C
guaranteed, not tested	(T_A = T_{min} to +25°C)	0 to +25°C	•	-55°C to +25°C
Storage		-65°C to +150°C	•	•
ABSOLUTE MAXIMUM RATINGS				
Internal Power Dissipation		500mW	•	•
Supply Voltage		±15V	•	±22V
Output Short-Circuit to Ground		Indefinite	•	•
Input Voltages, $X_1, X_2, Y_1, Y_2, Z_1, Z_2$		±V_S	•	•

NOTES:

•Same as AD534J specs.

[1] Electrical tests are performed at wafer probe, before the wafer is separated into individual dice. Maintaining chip performance to specification requires great care in handling and assembly.

[2] Figures given are percent of full-scale, ±10V (i.e., 0.01% = 1mV).

[3] May be reduced to 3V using external resistor between $-V_S$ and SF.

[4] Irreducible component due to nonlinearity: excludes effect of offsets.

[5] Using external resistor adjusted to give SF = 3.

[6] See Functional Block Diagram, Figure 1 of packaged AD534 data sheet for definition of sections.

[7] With external Z-offset adjustment, Z < ±X.

Specifications subject to change without notice.

ANALOG DEVICES

IC True rms-to-dc Converter

AD536A CHIPS

PRODUCT DESCRIPTION

The AD536A is a complete true rms-to-dc converter. As a single-chip IC, it is ideally suited to hybrid circuits as it requires only one external capacitor for operation. Features include factory calibration by laser trimming, dB output with 60dB range, low power (1mA) single or dual supply operation, wide bandwidth and 1% errors at crest factors of 7. One grade of the AD536A chip is specified for operation between 0 and +70°C, one grade for -55°C to +125°C.

APPLICATION INFORMATION

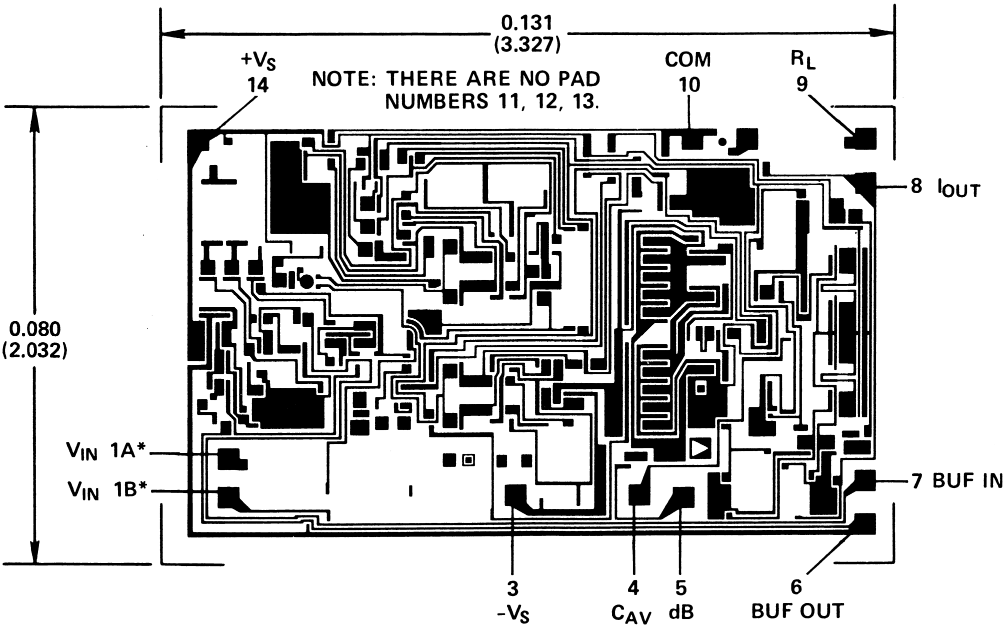
The AD536A chips are functionally identical to packaged AD536A devices. For general application information, see the AD536A packaged product catalog data sheet.

The following additional application information applies to AD536A chips:

1. No particular wire-bonding sequence must be followed.
2. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
3. For performance to device specifications, the metal substrate pad or header beneath the AD536A chip must be connected to $-V_S$, device pad number 3.
4. Pads 1A and 1B must *both* be connected to V_{IN}.
5. Do not connect to any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE TO-116 14 PIN CERAMIC DIP PACKAGE.

NOTE:
*BOTH PADS SHOWN MUST BE CONNECTED TO V_{IN}.

SPECIFICATIONS[1] (typical @ +25°C and ±15V dc unless otherwise noted)

MODEL	AD536AJ	AD536AS
TRANSFER EQUATION	$V_{OUT} = \sqrt{\text{avg.}\ (V_{IN})^3}$	•
CONVERSION ACCURACY		
Total Error, Internal Trim[2] (Fig. 1)†	±5mV ±0.5% of Reading, max	•
vs. Temperature, T_A = +25°C to +70°C	±(0.1mV ±0.01% Reading)/°C, max	±(0.1mV ±0.005% Reading)/°C, max
T_A = +70°C to +125°C	–	±(0.3mV ±0.005% Reading)/°C, max
$T_A = T_{min}$ to +25°C	±(0.1mV ±0.01% Reading)/°C,	±(0.1mV ±0.005% Reading)/°C
vs. Supply Voltage	±(0.1mV ±0.01% Reading)/V	•
dc Reversal Error	±0.05% of Reading	•
Total Error, External Trim[2] (Fig. 2)†	±3mV ±0.3% of Reading	•
ERROR vs CREST FACTOR[3]		
Crest Factor 1 to 2	Specified Accuracy	•
Crest Factor = 3	-0.1% of Reading	•
Crest Factor = 7	-1% of Reading	•
FREQUENCY RESPONSE[4]		
Bandwidth for 1% additional error (0.1dB)		
$10mV < V_{IN} \leq 100mV$	6kHz	•
$100mV < V_{IN} \leq 1V$	40kHz	•
$1V < V_{IN} \leq 7V$	100kHz	•
±3dB Bandwidth		
$10mV < V_{IN} \leq 100mV$	50kHz	•
$100mV < V_{IN} \leq 1V$	300kHz	•
$1V < V_{IN} \leq 7V$	2MHz	•
AVERAGING TIME CONSTANT (Fig. 5)†	25ms/μF C_{AV}	•
INPUT CHARACTERISTICS		
Signal Range, ±15V Supply	±20V Peak	•
Signal Range, +5V Supply (Fig. 17)†	±5V Peak	•
Safe Input, All Supply Voltages	±25V max	•
Input Resistance	16.7kΩ ±25%	•
Input Offset Voltage	±2mV max	•
OUTPUT CHARACTERISTICS		
Offset Voltage	±2mV max	•
vs. Temperature, T_A = +25°C to T_{max}	±0.1mV/°C	±0.2mV/°C, max
$T_A = T_{min}$ to +25°C	±0.1mV/°C	±0.2mV/°C
vs. Supply Voltage	±0.1mV/V	±0.2mV/V max
Voltage Swing, ±15V Supplies	0 to +10V min	•
±5V Supply	0 to +2V min	•
Output Current	(+5mA, -130μA) min	•
Short Circuit Current	+20mA	•
Resistance	0.5Ω max	•
dB OUTPUT (Fig. 13)†		
Error, V_{IN} 7mV to 7V rms, 0dB = 1V rms	±0.5dB	•
Scale Factor	-3mV/dB	•
Scale Factor TC (Uncompensated, see Fig. 13† for Temperature Compensation)	-0.3% Reading/°C (-0.03dB/°C)	•
I_{REF} for 0dB = 1V rms	20μA (5μA min, 80μA max)	•
I_{REF} Range	1μA to 100μA	•
I_{OUT} TERMINAL		
I_{OUT} Scale Factor	40μA/Volt rms	•
I_{OUT} Scale Factor Tolerance	±25%	•
Output Resistance	10^8Ω	•
Voltage Compliance	$-V_S$ to ($+V_S$ -2.5V)	•
BUFFER AMPLIFIER		
Input and Output Voltage Range	$-V_S$ to ($+V_S$ -2.5V)min	•
Input Offset Voltage, R_S = 25k	±4mV max	•
Input Current	100nA typ, 300nA max	•
Input Resistance	10^8Ω	•
Output Current	(5mA, -130μA) min	•
Short Circuit Current	+20mA	•
Small Signal Bandwidth	1MHz	•
Slew Rate[5]	5V/μs	•
POWER SUPPLY		
Voltage, Rated Performance		
Dual Supply	±3.0V to ±18V	•
Single Supply	+5V to +36V	•
Quiescent Current		
Total V_S, 5V to 36V, T_{min} to T_{max}	2mA max (1mA typ)	•
TEMPERATURE RANGE		
Operating		
Tested (T_A = +25°C to T_{max})	+25°C to +70°C	+25°C to +125°C
Guaranteed, Not Tested ($T_A = T_{min}$ to +25°C)	0 to +25°C	-55°C to +25°C
Storage	-55°C to +150°C	•

NOTES:

[1] Electrical tests are performed at wafer probe, before the wafer is separated into individual dice. Maintaining chip performance to specification requires great care in handling and assembly.

[2] Accuracy is specified for 0 to 7V rms, dc or 1kHz sinewave input with the AD536A connected as in Figure 1.

[3] Error vs. crest factor is specified for 1V rms rectangular pulse input, pulse width - 200μs.

[4] Input voltages are expressed in volts rms.

[5] With 2K external pulldown resistor.

†Figure references refer to figures on AD536A packaged product catalog data sheet in Section 7.

•Specifications same as AD536AJ.

Specifications subject to change without notice.

ANALOG DEVICES

Low Cost IC V-to-F Converter

AD537 CHIPS

PRODUCT DESCRIPTION

The AD537 is a V to F converter consisting of an input amplifier, precision oscillator, accurate voltage reference and a high current output stage. Only a single external RC network is required to set up any full scale frequency up to 100kHz and any full scale input voltage up to ±30V. AD537 chips feature a precision reference output, low quiescent current (1.2mA), high linearity and excellent stability. The device operates from single or dual supplies from 4.5 to 36 volts. The AD537 chip is specified for 0 to +70°C operation.

APPLICATION INFORMATION

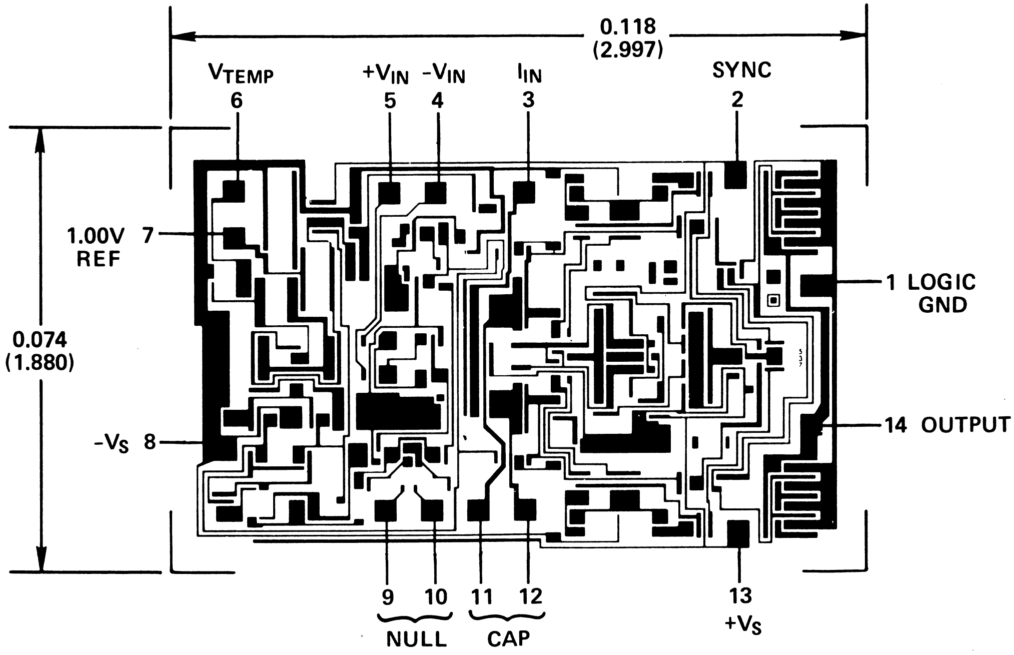
AD537 chips are functionally identical to dual-in-line packaged AD537 devices. For general application information, see the AD537 packaged product catalog data sheet.

The following additional application information applies to AD537 chips:

1. No particular wire-bonding sequence must be followed.
2. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
3. For performance to device specifications, the metal substrate pad or header beneath the AD537 chip must be connected to $-V_S$, device pad number 8.
4. Do not connect to any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE 14 PIN CERAMIC PACKAGE.

SPECIFICATIONS[1] (typical @ +25°C with V_S (total) = 5 to 36V, unless otherwise noted)

MODEL	AD537J
ANALOG INPUT AMPLIFIER	
(Voltage-to-Current Converter)	
Voltage Input Range	
Single Supply	0 to $(+V_S - 4)$ Volts (min)
Dual Supply	$-V_S$ to $(+V_S - 4)$ Volts (min)
Input Bias Current	
(Either Input)	100nA
Input Resistance (Non-Inverting)	250MΩ
Input Offset Voltage	
(Trimmable to Zero)	5mV max
vs. Supply	100μV/V max
vs. Temp, $T_A = T_{min}$ to T_{max}	5μV/°C
Safe Input Voltage[2]	$\pm V_S$
CURRENT-TO-FREQUENCY CONVERTER	
Frequency Range	0 to 150kHz
Nonlinearity[3]	
f_{max} = 10kHz	0.1%
f_{max} = 100kHz	0.15%
Full Scale Calibration Error	
C = 0.0100μF, I_{IN} = 1.000mA	±7% max
vs. Supply, ($f_{max} <$ 100kHz)	±0.1%/V max (0.01% typ)
vs. Temp, $T_A = T_{min}$ to T_{max}	50ppm typ
REFERENCE OUTPUTS	
Voltage Reference	
Absolute Value	1.00 Volt ±5% max
vs. Temp, $T_A = T_{min}$ to T_{max}	50ppm/°C
vs. Supply	±0.03%/V max
Output Resistance[4]	380Ω
Absolute Temperature Reference	
Nominal Output Level	1.00mV/°K
Initial Calibration @ +25°C	298mV ±5mV typ
Slope Error from 1.00mV/°K	±0.02mV/°K
Slope Nonlinearity	±0.1°K
Output Resistance[4]	900Ω
OUTPUT INTERFACE (Open Collector Output)	
(Symmetrical Square Wave)	
Output Sink Current in Logic "0"	
(V_{OUT} = 0.4V max, T_{min} to T_{max})	20mA min
Output Leakage Current in Logic "1"	
(T_{min} to T_{max})	200nA max
Logic Common Level Range	$-V_S$ to $(+V_S - 4)$ Volts
Rise/Fall Times (C_T = 0.01μF)	
I_{IN} = 1mA	0.2μs
I_{IN} = 1μA	1μs
POWER SUPPLY	
Voltage, Rated Performance	
Single Supply	4.5 to 36V
Dual Supply	±5 to ±18V
Quiescent Current	1.2mA
TEMPERATURE RANGE	
Operating	
Tested (T_A = +25°C to T_{max})	+25°C to +70°C
Guaranteed, Not Tested	
($T_A = T_{min}$ to +25°C)	0 to +25°C
Storage	-65°C to +150°C

NOTES:

[1] Electrical tests are performed at wafer probe, before the wafer is separated into individual dice. Maintaining chip performance to specification requires great care in handling and assembly.

[2] Maximum voltage input level is equal to the supply on either input terminal. However, large negative voltage levels can be sensed at the negative terminal if the input is scaled to a nominal 1mA full scale through an appropriate value resistor.

[3] Nonlinearity is specified for a current input level (I_{IN}) to the converter from 0.1 to 1000μA. Converter has 100% overrange capability up to I_{IN} = 2000μA with slightly reduced linearity. Nonlinearity is defined as deviation from a straight line from zero to full scale, expressed as a percentage of full scale.

[4] Loading the 1.0 volt or 1mV/°K outputs can cause a significant change in overall circuit performance, as indicated in the applications section of the packaged AD537 catalog data sheet. To maintain normal operation, these outputs should be operated into the internal buffer or an external amplifier.

Specifications subject to change without notice.

ANALOG DEVICES

High Accuracy Low Cost FET-Input Op Amp

AD540 CHIPS

PRODUCT DESCRIPTION

The AD540 is a low cost, high accuracy FET input operational amplifier. The low maximum bias current of 25pA (K-grade) is specified warmed up. The device is latch-up proof and short circuit protected. It is internally compensated for gains of one or greater. Two grades of AD540 chips are specified for operation over the 0 to +70°C temperature range and one grade is specified for operation between -55°C and +125°C.

APPLICATION INFORMATION

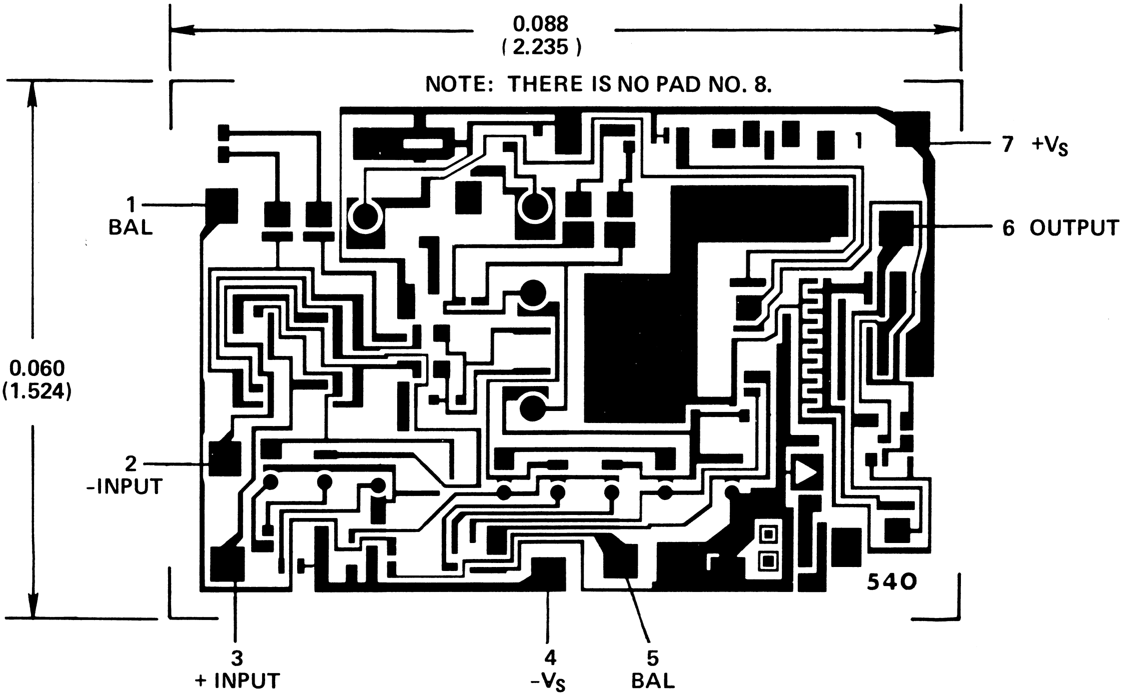
AD540 chips are functionally identical to packaged AD540 devices. For general application information, see the AD540 packaged product catalog data sheet.

The following additional application information applies to AD540 chips:

1. No particular wire-bonding sequence must be followed.
2. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
3. For performance to device specifications, the metal substrate pad or header beneath the AD540 chip must be connected to $-V_S$, device pad number 4.
4. Do not connect to any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE TO-99 8 PIN METAL PACKAGE.

SPECIFICATIONS[1] (typical @ +25°C and V_S = ±15V dc unless otherwise specified)

MODEL	AD540J	AD540K	AD540S
OPEN LOOP GAIN[2]			
V_{OUT} = ±10V, $R_L \geqslant 2k\Omega$	20,000 min	50,000	**
T_A = +25°C to T_{max}	15,000 min	25,000 min	**
T_{min} to +25°C	15,000	25,000	**
OUTPUT CHARACTERISTICS			
Voltage @ R_L = 2kΩ, T_A = min to max	±10V min (±13V typ)	*	*
Voltage @ R_L = 10kΩ, T_A = min to max	±12V min (±14V typ)	*	*
Short Circuit Current	25mA	*	*
FREQUENCY RESPONSE			
Unity Gain, Small Signal	1.0MHz	*	*
Full Power Response	100kHz	*	*
Slew Rate, Unity Gain	6.0V/μs	*	*
INPUT OFFSET VOLTAGE[3]	50mV max	20mV max	**
vs. Temp, T_A = +25°C to T_{max}	75μV/°C max	25μV/°C max	50μV/°C max
T_A = T_{min} to +25°C	75μV/°C	25μV/°C	50μV/°C
vs. Supply, T_A = +25°C to T_{max}	400μV/V max	300μV/V max	**
T_A = T_{max} to +25°C	400μV/V	300μV/V	**
INPUT BIAS CURRENT			
Either Input[4]	50pA max	25pA max	**
INPUT IMPEDANCE			
Differential	$10^{10}\Omega \| 2pF$	*	*
Common Mode	$10^{11}\Omega \| 2pF$	*	*
INPUT VOLTAGE RANGE			
Differential[5]	±20V	*	*
Common Mode	±10V min (±12V typ)	*	*
Common Mode Rejection, V_{in} = ±10V	70dB min	*	*
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	±(5 to 18)V	*	*
Quiescent Current	7mA max (3mA typ)	*	*
TEMPERATURE RANGE			
Operating			
Tested (T_A = +25°C to T_{max})	+25°C to +70°C	*	+25°C to +125°C
Guaranteed, Not Tested (T_A = T_{min} to +25°C)	0 to +25°C	*	−55°C to +25°C
Storage	−65°C to +150°C	*	*

NOTES:

[1] Electrical tests are performed at wafer probe, before the wafer is separated into individual dice. Maintaining chip performance to specification requires great care in handling and assembly.

[2] Open Loop Gain is specified with V_{OS} both nulled and unnulled.

[3] Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[4] Bias Current specifications are guaranteed after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

[5] Defined as voltage between inputs, such that neither exceeds ±10V from ground.

*Specifications same as AD540J

**Specifications same as AD540K.

Specifications subject to change without notice.

ANALOG DEVICES

Precision Low Cost BIFET Op Amp

AD542 CHIPS

PRODUCT DESCRIPTION

The AD542 is a precision FET-input operational amplifier fabricated with the most advanced BIFET and laser-trimming technologies. Bias currents as low as 25pA max, warmed-up, and offset voltages as low as 1.0mV max and offset voltage drifts as low as 10μV/°C max make the AD542 ideal for precision instrumentation applications. This precision is gained without sacrificing the low cost, high-speed features of other BIFET amplifiers. Two grades of AD542 chips are specified for operation between 0 and +70°C and one grade is specified for the -55°C to +125°C temperature range.

APPLICATION INFORMATION

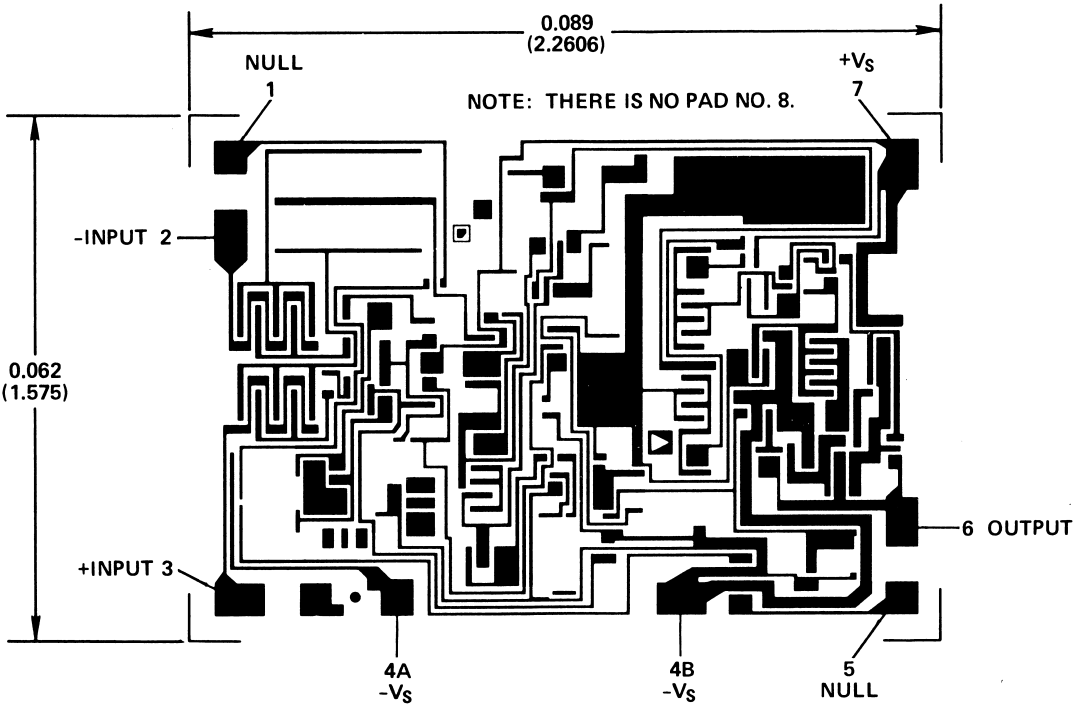
AD542 chips are functionally identical to packaged AD542 devices. For general application information, see the AD542 packaged product catalog data sheet.

The following additional application information applies to AD542 chips:

1. No particular wire-bonding sequence must be followed.
2. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
3. For performance to device specifications, the metal substrate pad or header beneath the AD542 chip must be connected to $-V_S$, device pad numbers 4A and 4B.
4. Pads 4A and 4B must *both* be connected to $-V_S$.
5. Do not connect to any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE TO-99 8 PIN METAL PACKAGE.

SPECIFICATIONS[1] (typical @ +25°C and V_S = ±15V dc unless otherwise specified)

MODEL	AD542J	AD542K	AD542S
OPEN LOOP GAIN[2]			
V_{out} = ±10V, $R_L \geqslant 2k\Omega$	100,000 min	300,000 min	**
T_A = +25°C to T_{max}	100,000 min	300,000 min	**
T_A = T_{min} to +25°C	100,000	300,000	**
OUTPUT CHARACTERISTICS			
Voltage @ $R_L = 2k\Omega$, T_A = T_{min} to T_{max}	±10V min (±12V typ)	*	*
Voltage @ $R_L = 10k\Omega$, T_A = T_{min} to T_{max}	±12V min (±13V typ)	*	*
Short Circuit Current	25mA	*	*
FREQUENCY RESPONSE			
Unity Gain, Small Signal	1.0MHz	*	*
Full Power Response	50kHz	*	*
Slew Rate, Unity Gain	3.0V/μs	*	*
INPUT OFFSET VOLTAGE[3]	2.0mV max	1.0mV max	**
vs. Temp, T_A = +25°C to T_{max}	20μV/°C max	10μV/°C max	15μV/°C max
T_A = T_{min} to +25°C	20μV/°C	10μV/°C	15μV/°C
vs. Supply, T_A = +25°C to T_{max}	200μV/V max	100μV/V max	**
T_A = T_{min} to +25°C	200μV/V	100μV/V	**
INPUT BIAS CURRENT			
Either Input[4]	50pA max	25pA max	**
Input Offset Current	5pA	2pA	**
INPUT IMPEDANCE			
Differential	$10^{10}\Omega \| 2pF$	*	*
Common Mode	$10^{11}\Omega \| 2pF$	*	*
INPUT VOLTAGE RANGE			
Differential[5]	±20V	*	*
Common Mode	±10V min (±12V typ)	*	*
Common Mode Rejection, V_{in} = ±10V	76dB min	80dB min	**
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	±(5 to 18)V	*	*
Quiescent Current	1.5mA max	*	*
VOLTAGE NOISE			
0.1-10Hz	2μV p-p	*	*
10Hz	$70nV/\sqrt{Hz}$	*	*
100Hz	$45nV/\sqrt{Hz}$	*	*
1kHz	$30nV/\sqrt{Hz}$	*	*
10kHz	$25nV/\sqrt{Hz}$	*	*
TEMPERATURE RANGE			
Operating			
Tested (T_A = +25°C to T_{max})	+25°C to +70°C	*	+25°C to +125°C
Guaranteed, Not Tested (T_A = T_{min} to +25°C)	0 to +25°C	*	-55°C to +25°C
Storage	-65°C to +150°C	*	*

NOTES:

[1] Electrical tests are performed at wafer probe, before the wafer is separated into individual dice. Maintaining chip performance to specification requires great care in handling and assembly.

[2] Open Loop Gain is specified with V_{OS} both nulled and unnulled.

[3] Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[4] Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

[5] Defined as voltage between inputs, such that neither exceeds ±10V from ground.

*Specifications same as AD542J.

**Specifications same as AD542K.

Specifications subject to change without notice.

ANALOG DEVICES

Precision High Speed BIFET Op Amp

AD544 CHIPS

PRODUCT DESCRIPTION

The AD544 is a precision, high speed, FET-input operational amplifier fabricated with the most advanced BIFET and laser-trimming technologies. Bias currents as low as 25pA max, warmed-up, offset voltages as low as 1.0mV max and offset voltage drifts as low as 10μV/°C max and fast settling time of 3μs to ±0.01% make the AD544 ideal for use as a precision output amplifier for digital to analog converters. Two grades of AD544 chips are specified for operation between 0 and +70°C and one grade is specified for the -55°C to +125°C temperature range.

APPLICATION INFORMATION

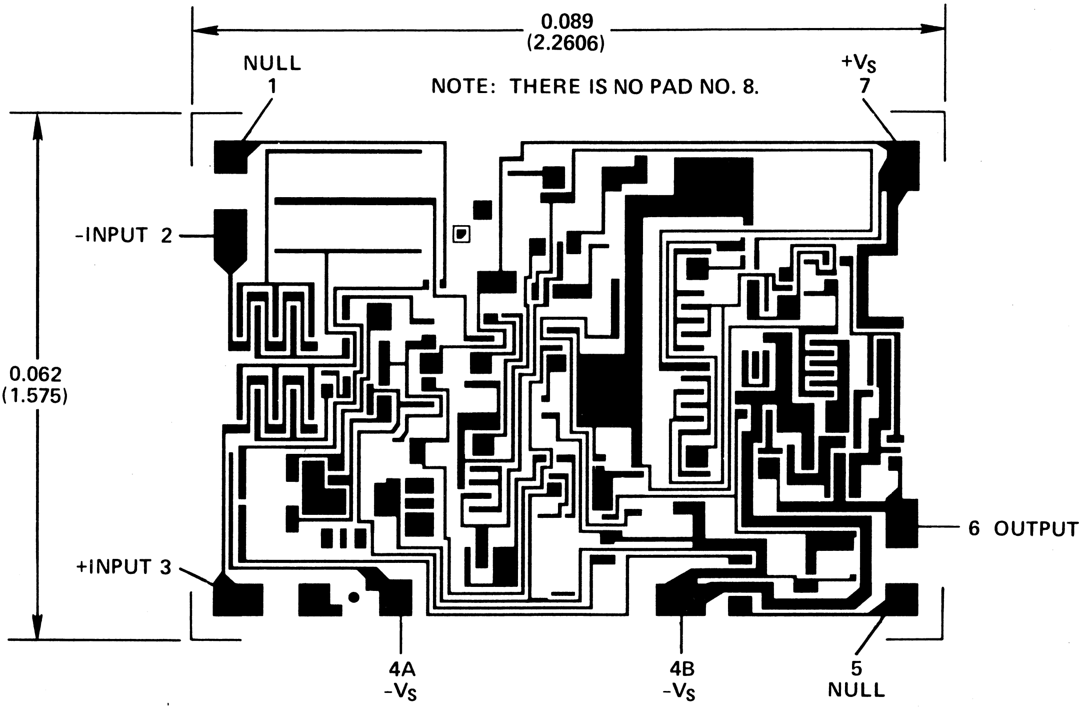
AD544 chips are functionally identical to packaged AD544 devices. For general application information, see the AD544 packaged product catalog data sheet.

The following additional application information applies to AD544 chips:

1. No particular wire-bonding sequence must be followed.
2. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
3. For performance to device specifications, the metal substrate pad or header beneath the AD544 chip must be connected to $-V_S$, device pad numbers 4A and 4B.
4. Pads 4A and 4B must *both* be connected to $-V_S$.
5. Do not connect to any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE TO-99 8 PIN METAL PACKAGE.

SPECIFICATIONS[1] (typical @ +25°C and V_S = ±15V dc unless otherwise specified)

MODEL	AD544J	AD544K	AD544S
OPEN LOOP GAIN[2]			
V_{out} = ±10V, $R_L \geqslant 2k\Omega$	30,000 min	50,000 min	**
T_A = +25°C to T_{max}	20,000 min	40,000 min	**
T_A = T_{min} to +25°C	20,000	40,000	**
OUTPUT CHARACTERISTICS			
Voltage @ $R_L = 2k\Omega$, $T_A = T_{min}$ to T_{max}	±10V min (±12V typ)	*	*
Voltage @ $R_L = 10k\Omega$, $T_A = T_{min}$ to T_{max}	±12V min (±13V typ)	*	*
Short Circuit Current	25mA	*	*
FREQUENCY RESPONSE			
Unity Gain, Small Signal	2.0MHz	*	*
Full Power Response	200kHz	*	*
Slew Rate, Unity Gain	13.0V/μs	*	*
INPUT OFFSET VOLTAGE[3]	2.0mV max	1.0mV max	**
vs. Temp, T_A = +25°C to T_{max}	20μV/°C max	10μV/°C max	15μV/°C max
T_A = T_{min} to +25°C	20μV/°C	10μV/°C	15μV/°C
vs. Supply, T_A = +25°C to T_{max}	200μV/V max	100μV/V max	**
T_A = T_{min} to +25°C	200μV/V	100μV/V	**
INPUT BIAS CURRENT			
Either Input[4]	50pA max	25pA max	**
Input Offset Current	5pA	2pA	**
INPUT IMPEDANCE			
Differential	$10^{10}\Omega\|2pF$	*	*
Common Mode	$10^{11}\Omega\|2pF$	*	*
INPUT VOLTAGE RANGE			
Differential[5]	±20V	*	*
Common Mode	±10V min (±12V typ)	*	*
Common Mode Rejection, V_{in} = ±10V	74dB min	80dB min	**
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	±(5 to 18)V	*	*
Quiescent Current	2.5mA max (1.8mA typ)	*	*
VOLTAGE NOISE			
0.1-10Hz	2μV p-p	*	*
10Hz	$35nV/\sqrt{Hz}$	*	*
100Hz	$22nV/\sqrt{Hz}$	*	*
1kHz	$18nV/\sqrt{Hz}$	*	*
10kHz	$16nV/\sqrt{Hz}$	*	*
TEMPERATURE RANGE			
Operating			
Tested (T_A = +25°C to T_{max})	+25°C to +70°C	*	+25°C to +125°C
Guaranteed, Not Tested (T_A = T_{min} to +25°C)	0 to +25°C	*	-55°C to +25°C
Storage	-65°C to +150°C	*	*

NOTES:

[1] Electrical tests are performed at wafer probe, before the wafer is separated into individual dice. Maintaining chip performance to specification requires great care in handling and assembly.

[2] Open Loop Gain is specified with V_{OS} both nulled and unnulled.

[3] Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[4] Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

[5] Defined as voltage between inputs, such that neither exceeds ±10V from ground.

*Specifications same as AD544J.

**Specifications same as AD544K.

Specifications subject to change without notice.

ANALOG DEVICES

Ultra Low Drift BIFET Operational Amplifier

AD547 CHIPS

PRODUCT DESCRIPTION

The AD547 is a monolithic, FET input operational amplifier combining the very low input bias current advantages of a BIFET op amp with offset and drift performance previously available only in high quality bipolar amplifiers.

The exclusive Analog Devices laser wafer trim process trims both the input offset voltage and offset voltage drift to levels far lower than any competing BIFET amplifier (1mV, 5μV/°C).

In addition to superior low drift performance, the AD547 offers the lowest guaranteed input bias currents of any BIFET amplifier (50pA max warmed-up).

APPLICATION INFORMATION

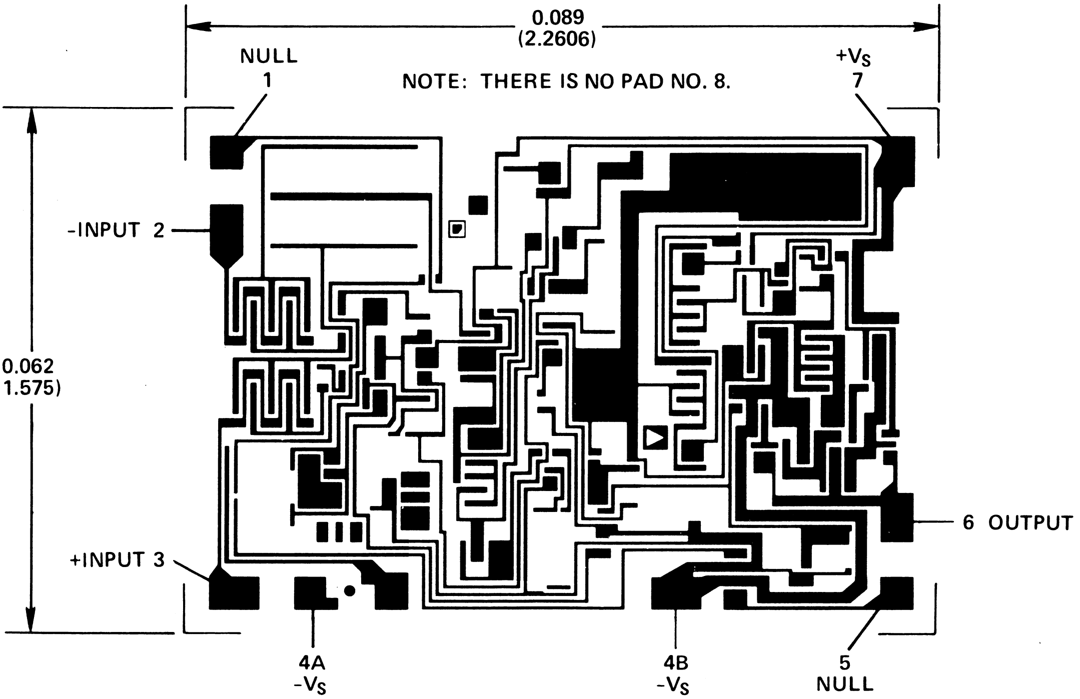
AD547 chips are functionally identical to packaged AD547 devices. For general application information, see the AD547 packaged product catalog data sheet.

The following additional application information applies to AD547 chips:

1. No particular wire-bonding sequence must be followed.
2. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
3. For performance to device specifications, the metal substrate pad or header beneath the AD547 chip must be connected to $-V_S$, device pad numbers 4A and 4B.
4. Pads 4A and 4B must *both* be connected to $-V_S$.
5. Do not connect to any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE TO-99 8 PIN METAL PACKAGE.

SPECIFICATIONS[1] (typical @ +25°C and V_S = ±15V dc unless otherwise specified)

MODEL	AD547J
OPEN LOOP GAIN[2]	
$V_{OUT} = \pm10V$, $R_L \geqslant 2k\Omega$	100,000 min
$T_A = +25°C$ to T_{max}	100,000 min
$T_A = T_{min}$ to +25°C	100,000
OUTPUT CHARACTERISTICS	
Voltage @ $R_L = 2k\Omega$, T_A = min to max	±10V min (±12V typ)
Voltage @ $R_L = 10k\Omega$, T_A = min to max	±12V min (±13V typ)
Short Circuit Current	25mA
FREQUENCY RESPONSE	
Unity Gain, Small Signal	1.0MHz
Full Power Response	50kHz
Slew Rate, Unity Gain	3.0V/μs
INPUT OFFSET VOLTAGE[3]	1.0mV max
vs. Temperature, $T_A = +25°C$ to T_{max}	5μV/°C max
$T_A = T_{min}$ to +25°C	5μV/°C
vs. Supply, $T_A = +25°C$ to T_{max}	200μV/V max
$T_A = T_{min}$ to +25°C	200μV/V
INPUT BIAS CURRENT	
Either Input[4]	10pA (50pA max)
Input Offset Current	5pA
INPUT IMPEDANCE	
Differential	$10^{12}\Omega \parallel 6pF$
Common Mode	$10^{12}\Omega \parallel 6pF$
INPUT VOLTAGE RANGE	
Differential[5]	±20V
Common Mode	±10V min (±12V typ)
Common Mode Rejection, $V_{in} = \pm10V$	76dB min
POWER SUPPLY	
Rated Performance	±15V
Operating	±(5 to 18)V
Quiescent Current	1.5mA max (1.1mA typ)
VOLTAGE NOISE	
0.1-10Hz	2μV p-p typ
10Hz	$70nV/\sqrt{Hz}$
100Hz	$45nV/\sqrt{Hz}$
1kHz	$30nV/\sqrt{Hz}$
10kHz	$25nV/\sqrt{Hz}$
TEMPERATURE RANGE	
Tested ($T_A = +25°C$ to T_{max})	+25°C to +70°C
Guaranteed, Not Tested ($T_A = T_{min}$ to +25°C)	0 to +25°C
Storage	-65°C to +150°C

NOTES:

[1] Electrical tests are performed at wafer probe, before the wafer is separated into individual dice. Maintaining chip performance to specification requires great care in handling and assembly.

[2] Open Loop Gain is specified with V_{OS} both nulled and unnulled.

[3] Input Offset Voltage specifications are guaranteed after 5 minutes of operation at $T_A = +25°C$.

[4] Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at $T_A = +25°C$. For higher temperatures, the current doubles every 10°C.

[5] Defined as the maximum safe voltage between inputs, such that neither exceeds ±10V from around.

Specifications subject to change without notice.

ANALOG DEVICES

DACPORT™ Low Cost Complete μP-Compatible 8-Bit DAC

AD558 CHIPS

PRODUCT DESCRIPTION

The AD558 DACPORT is a complete voltage-output 8-bit digital-to-analog converter, including output amplifier, full microprocessor interface and precision voltage reference on a single monolithic chip. No external components or trims are required to interface, with full accuracy, an 8-bit data bus to an analog system.

The performance and versatility of the DACPORT is a result of several recently-developed monolithic bipolar technologies. The complete microprocessor interface and control logic is implemented with integrated injection logic (I^2L), an extremely dense and low-power logic structure that is process-compatible with linear bipolar fabrication. The internal precision voltage reference is the patented low-voltage band-gap circuit which permits full-accuracy performance on a single +5V to +15V power supply. Thin-film silicon-chromium resistors provide the stability required for guaranteed monotonic operation over the entire operating temperature range, while recent advances in laser-wafer-trimming of these thin-film resistors permit absolute calibration at the factory to within ±1LSB; thus no user-trims for gain or offset are required. A new circuit design provides voltage settling to ±1/2LSB for a full-scale step in 800ns.

The AD558J is specified for use over the 0 to +70°C temperature range and the AD558T is specified for the −55°C to +125°C range.

APPLICATION INFORMATION

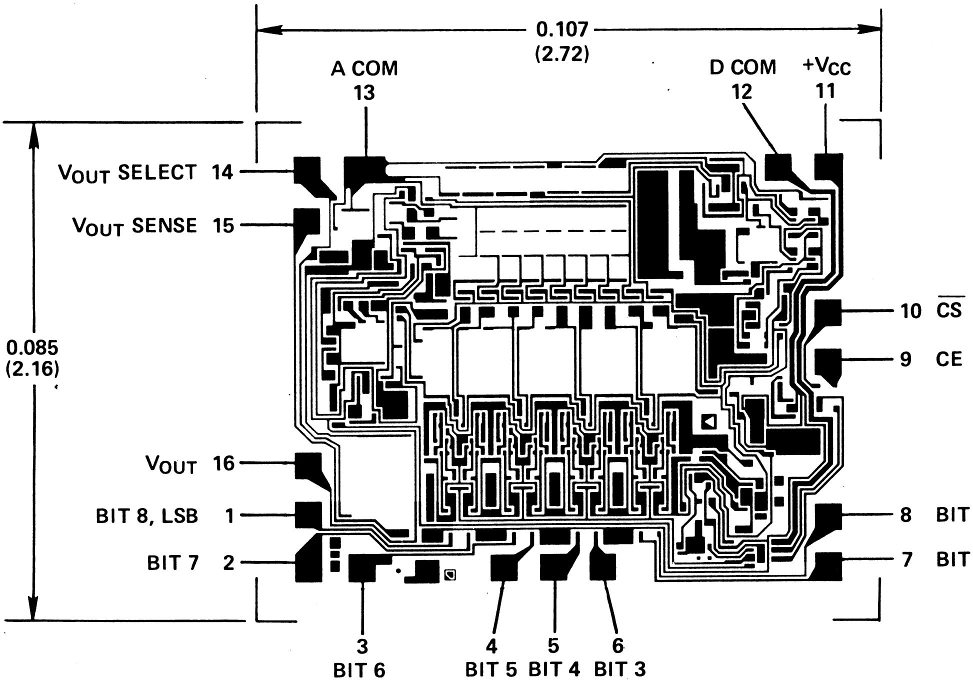
AD558 chips are functionally identical to packaged AD558 devices. For general application information, see the AD558 packaged product catalog data sheet.

The following additional application information applies to AD558 chips:

1. No particular wire-bonding sequence must be followed.
2. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
3. For performance to device specifications, the metal substrate pad or header beneath the AD558 chip must be connected to analog ground, device pad number 13.
4. Do not connect to any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



DACPORT is a trademark of Analog Devices, Inc.

SPECIFICATIONS[1] (typical @ +25° C, V_{CC} = +5V to +15V unless otherwise specified)

MODEL	AD558J	AD558T
RESOLUTION	8 Bits	*
RELATIVE ACCURACY[2]		
$T_A = T_{min}$ to T_{max}	±1/2LSB max	±3/8LSB max
OUTPUT		
Ranges	0V to +2.56V	*
	0V to +10V[3]	*
Current, Source	+5mA	+5mA min
Sink	Internal Passive Pull-Down to Ground[4]	*
OUTPUT SETTLING TIME[5]		
0 to 2.56 volt range	0.8μs	*
0 to 10 volt range[3]	2.0μs	*
FULL SCALE ACCURACY		
@ 25°C	±1.5LSB (±0.6%) max	*
T_A = +25°C to T_{max}	±2.5LSB (±1.0%) max	*
$T_A = T_{min}$ to +25°C	±2.5LSB (±1.0%)	*
ZERO ERROR		
@ 25°C	±1LSB max	*
T_A = +25°C to T_{max}	±2LSB max	*
$T_A = T_{min}$ to +25°C	±2LSB	*
MONOTONICITY[6]	Guaranteed, T_A = +25°C to T_{max}	*
	Typical, $T_A = T_{min}$ to +25°C	*
DIGITAL INPUTS		
T_{min} to T_{max}		
Input Current	±100μA max	*
Data Inputs, Voltage		
Bit On – Logic "1"	2.0V min	*
Bit Off – Logic "0"	0.8V max	*
Control Inputs, Voltage		
On – Logic "1"	2.0V min	*
Off – Logic "0"	0.8V max	*
Input Capacitance	4pF	*
TIMING		
T_{min} to T_{max}		
t_W (Strobe Pulse Width)	100ns min	*
t_{DH} (Data Hold Time)	10ns max	*
t_{DS} (Data Set-Up Time)	100ns min	*
POWER SUPPLY		
Operating Voltage Range (V_{CC})		
2.56 Volt Range	+4.5V to +16.5V	*
10 Volt Range	+11.4V to +16.5V	*
Current (I_{CC})	15mA typ, 25mA max	*
Rejection Ratio	0.03%/% max	*
POWER DISSIPATION, V_{CC} = 5V	75mW (125mW max)	*
V_{CC} = 15V	225mW (375mW max)	*
TEMPERATURE RANGE		
Operating		
Tested (T_A = +25°C to T_{max})	+25°C to +70°C	+25°C to +125°C
Guaranteed, Not Tested ($T_A = T_{min}$ to +25°C)	0 to +25°C	-55°C to +25°C
Storage	-65°C to +150°C	*

NOTES

[1] Electrical tests are performed at wafer probe, before the wafer is separated into individual dice. Maintaining chip performance to specification requires great care in handling and assembly.

[2] Relative Accuracy is defined as the deviation of the code transition points from the ideal transfer point on a straight line from the zero to the full scale of the device.

[3] Operation of the 0 to 10 volt output range requires a minimum supply voltage of +11.4 volts.

[4] Passive pull-down resistance is 2kΩ for 2.56 volt range, 10kΩ for 10 volt range.

[5] Settling time is specified for a positive-going full-scale step to ±1/2LSB. Negative-going steps to zero are slower, but can be improved with an external pull-down.

[6] A monotonic converter has a maximum differential linearity error of ±1LSB.

*Specifications same as AD558J.

Specifications subject to change without notice.

ANALOG DEVICES

Low Cost, High Speed 10-Bit D-to-A Converter with Reference

AD561 CHIPS

PRODUCT DESCRIPTION

The AD561 is a low-cost, high-speed complete current output D to A converter. An on-chip buried zener reference, laser-wafer-trimmed resistors, high-speed switches and control amplifier make the AD561 chip ideal for adjustment-free 10-bit hybrid applications. Monotonicity to 10 bits (guaranteed +25°C to T_{max}) along with a 250ns settling time are among the performance features of the AD561. One grade of the AD561 chip is specified for 0 to +70°C operation and one is specified for -55°C to +125°C.

APPLICATION INFORMATION

The AD561 chip has several features not accessible to users of packaged AD561 devices.

1. On AD561 chips, the internal reference is not permanently connected. This allows the use of an external reference and also makes the internal reference available for external use.
2. The control amplifier summing point is accessible on the AD561 chip. Thus the user may connect an external reference voltage-to-current conversion resistor that may be specified to match an external feedback (range-setting) resistor. This enables the user to set his own output range without degrading the gain temperature coefficient.
3. An additional output span resistor is accessible. This permits the user to connect the AD561 chip for ±5, ±10 or ±20 volt spans.

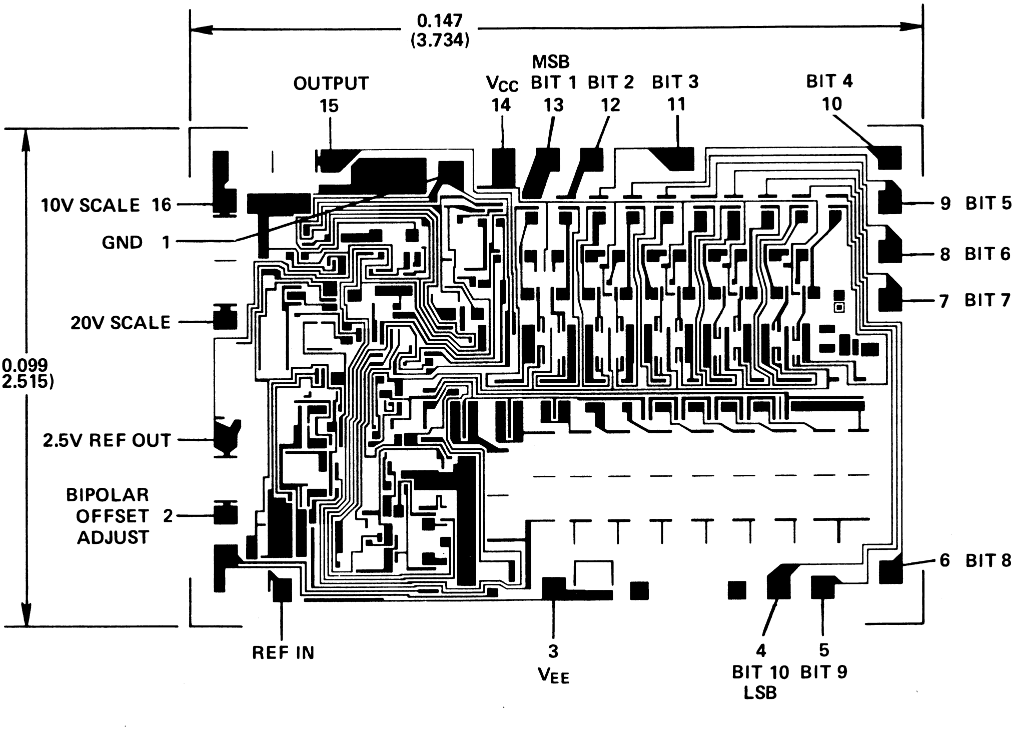
All other general application information on the AD561 packaged product catalog data sheet applies to AD561 chips.

The following additional application information applies to AD561 chips:

1. No particular wire-bonding sequence must be followed.
2. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
3. For performance to device specifications, the metal substrate pad or header beneath the AD561 chip must be connected to $-V_S$, device pad number 5.
4. Do not connect to any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



SPECIFICATIONS[1] (T_A = +25°C, V_{CC} = +5V, V_{EE} = -15V, unless otherwise specified)

	AD561J			AD561T			
MODEL	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
RESOLUTION		10 Bits			10 Bits		
ACCURACY (Error Relative		±1/4	±1/2		±1/8	±1/4	LSB
to Full Scale)		(0.025)	(0.05)		(0.012)	(0.025)	% of F.S.
DIFFERENTIAL NONLINEARITY		±1/2			±1/2		LSB
DATA INPUTS							
TTL, V_{CC} = +5V							
Bit ON Logic "1"	+2.0			+2.0			V
Bit OFF Logic "0"			+0.8			+0.8	V
CMOS, 10V ⩽ V_{CC} ⩽ 16.5V							
(See Figure 1)							
Bit ON Logic "1"	70% V_{CC}			70% V_{CC}			V
Bit OFF Logic "0"			30% V_{CC}			30% V_{CC}	V
Logic Current (Each Bit) (T_{min} to T_{max})							
Bit ON Logic "1"		+5	+100		+20	+100	nA
Bit OFF Logic "0"		-5	-25		-25	-100	μA
OUTPUT							
Current							
Unipolar	1.5	2.0	2.4	1.5	2.0	2.4	mA
Bipolar	±0.75	±1.0	±1.2	±0.75	±1.0	±1.2	mA
Resistance (Exclusive of Application Resistors)		40M			40M		Ω
Unipolar Zero (All Bits OFF)		0.01	0.05		0.01	0.05	% of F.S.
Capacitance		25			25		pF
Compliance Voltage	-2	-3	+10	-2	-3	+10	V
SETTLING TIME TO 1/2LSB							
All Bits ON-to-OFF or OFF-to-ON		250			250		ns
POWER REQUIREMENTS							
V_{CC}, +4.5V dc to +16.5V dc		8	10		6	10	mA
V_{EE}, -10.8V dc to -16.5V dc		12	16		11	16	mA
POWER SUPPLY GAIN SENSITIVITY							
V_{CC}, +4.5V dc to +16.5V dc		2	10		2	10	ppm of F.S./%
V_{EE}, -10.8V dc to -16.5V dc		4	25		4	25	ppm of F.S./%
TEMPERATURE RANGE							
Operating							
Tested (T_A = +25°C to T_{max})		+25 to +70			+25 to +125		°C
Guaranteed, Not Tested (T_A = T_{min} to +25°C)		0 to +25			-55 to +25		°C
Storage		-65 to +150			-65 to +150		°C
TEMPERATURE COEFFICIENTS							
With Internal Reference							
Unipolar Zero, T_A = +25°C to T_{max}		1	10		1	5	ppm of F.S./°C
T_A = T_{min} to +25°C		1			1		ppm of F.S./°C
Bipolar Zero, T_A = +25°C to T_{max}		2	25		2	10	ppm of F.S./°C
T_A = T_{min} to +25°C		2			2		ppm of F.S./°C
Full Scale, T_A = +25°C to T_{max}		15	80		15	30	ppm of F.S./°C
T_A = T_{min} to +25°C		15			15		ppm of F.S./°C
Differential T_A = +25°C to T_{max}		2.5			2.5		ppm of F.S./°C
Nonlinearity, T_A = T_{min} to +25°C		2.5			2.5		ppm of F.S./°C
MONOTONICITY		Guaranteed, T_A = +25°C to T_{max} Typical, T_A = T_{min} to +25°C			Guaranteed, T_A = +25°C to T_{max} Typical, T_A = T_{min} to +25°C		
PROGRAMMABLE OUTPUT		0 to +5, 0 to +10, 0 to +20			0 to 15, 0 to +10, 0 to +20		V
RANGES		-2.5 to +2.5, -5 to +5, -10 to +10			-2.5 to +2.5, -5 to +5, -10 to +10		V
CALIBRATION ACCURACY							
Full Scale Error with Fixed 25Ω Resistor		±0.1			±0.1		% of F.S.
Bipolar Zero Error with Fixed 10Ω Resistor		±0.1			±0.1		% of F.S.
CALIBRATION ADJUSTMENT RANGE							
Full Scale (With 50Ω Trimmer)		±0.5			±0.5		% of F.S.
Bipolar Zero (With 50Ω Trimmer)		±0.5			±0.5		% of F.S.
REFERENCE							
Output Voltage, I_L = 0 to 1mA†	2.490	2.500	2.510	2.490	2.500	2.505	V
Maximum Current Out †		5.0			5.0		mA
Temperature Coefficient							
T_A = +25°C to T_{max}		10	80		10	60	ppm of F.S./°C
T_A = T_{min} to +25°C		10			10		ppm of F.S./°C

NOTES:

[1] Electrical tests are performed at wafer probe, before the wafer is separated into individual dice. Maintaining chip performance to specification requires great care in handling and assembly.

†Referent current out is in addition to reference current required by D-to-A REF IN and BIPOLAR OFFSET.

Specifications subject to change without notice.

ANALOG DEVICES

Complete High Speed 12-Bit D/A Converter

AD565A/AD566A CHIPS

PRODUCT DESCRIPTION

The AD565A/AD566A is a 12-bit digital-to-analog converter that incorporates 12 precision, high speed bipolar current steering switches, control amplifier, laser-trimmed thin film resistor network, and buried zener voltage reference to produce a very fast, high accuracy analog output current. The 10–90% full scale transition time is less than 35ns. The AD565AJ/AD566AJ is specified for use over the 0 to +70°C temperature range and the AD565AS/AD566AS is specified for the -55°C to +125°C range.

APPLICATION INFORMATION

The AD565A/AD566A chip has several features not accessible to users of either the AD565A or AD566A packaged devices.

1. The AD565A chip can be wired to perform as either a AD565A or as a AD566A at the discretion of the user.
2. The control amplifier summing point is accessible on AD565A/AD566A chips. Thus the user may connect an external reference voltage-to-current conversion resistor that may be specified to match an external feedback (range-setting) resistor. This enables the user to set his own output range without degrading the gain temperature coefficient.

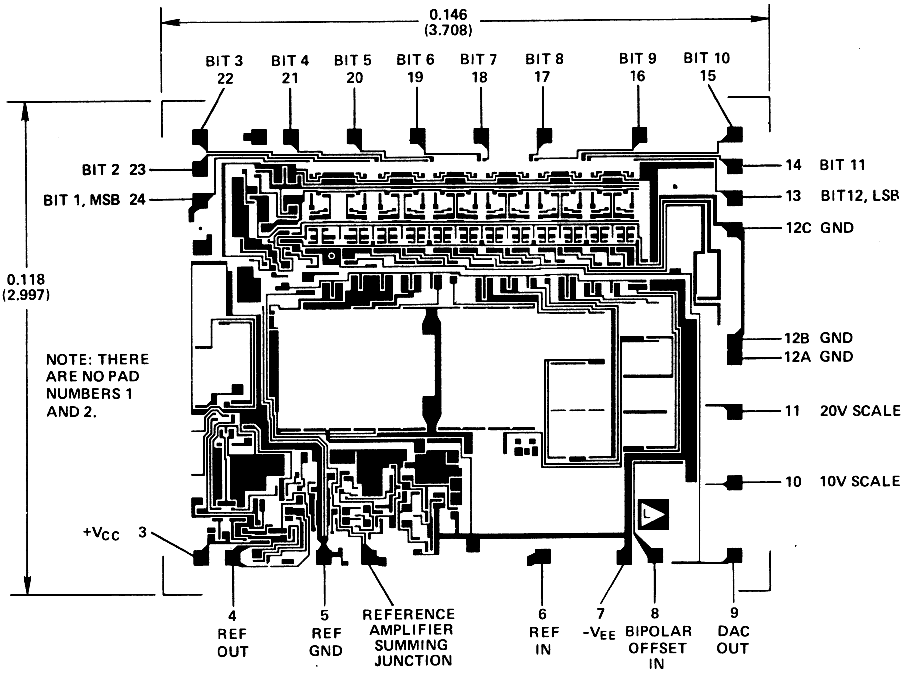
All other general application information on the AD565A or AD566A packaged product catalog data sheets applies to AD565A/AD566A chips.

The following additional application information applies to AD565A/AD566A chips:

1. No particular wire-bonding sequence must be followed.
2. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
3. For performance to device specifications, the metal substrate pad or header beneath the AD565A/AD566A chip must be connected to $-V_{EE}$, device pad number 7.
4. Do not connect to any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.
5. Pads 12A, 12B, 12C must all be connected to ground.
6. To reduce settling time, minimize the effects of stray capacitance on the reference amplifier summing junction. Do not connect to this pad unless necessary. If needed, keep the lid as far from the pad as possible. Ground the lid or tie to a reference point if the summing junction is used.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



PAD NUMBERS SHOWN CORRESPOND TO AD565A PIN NUMBERS.

SPECIFICATIONS[1] (T_A = +25°C, V_{EE} = -15V, unless otherwise specified)

MODEL	AD565AJ/AD566AJ			AD565AS/AD566AS			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
DATA INPUTS[2] (Pads 13 to 24)							
TTL or 5 Volt CMOS							
Input Voltage							
Bit ON Logic "1"	+2.0		+5.5	+2.0		+5.5	V
Bit OFF Logic "0"	0		+0.8	0		+0.8	V
Logic Current (each bit)							
Bit ON Logic "1"		+120	+300		+120	+300	μA
Bit OFF Logic "0"		+35	+100		+35	+100	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current							
Unipolar (all bits on)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar (all bits on or off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (exclusive of span resistors)	6k	8k	10k	6k	8k	10k	Ω
Offset							
Unipolar		0.01	0.05		0.01	0.05	% of F.S.
Bipolar		0.05	0.15		0.05	0.1	% of F.S.
Capacitance		25			25		pF
Compliance Voltage	-1.5		+10	-1.5		+10	V
ACCURACY (error relative to full scale) T_A = +25°C		±1/4	±1/2		±1/8	±1/4	LSB
		(0.006)	(0.012)		(0.003)	(0.006)	% of F.S.
T_A = +25°C to T_{max}		±1/2	±3/4		±1/2	±3/4	LSB
T_A = T_{min} to +25°C		±1/2			±1/2		LSB
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±3/4		±1/4	±1/2	LSB
+25°C to T_{max}		Monotonicity Guaranteed			Monotonicity Guaranteed		
T_{min} to +25°C		Monotonicity Typical			Monotonicity Typical		
TEMPERATURE RANGE							
Operating		0	+70	-55		+125	°C
Storage		-65	+150	-65		+150	°C
TEMPERATURE COEFFICIENTS							
Unipolar Zero							
T_A = +25°C to T_{max}		1	2		1	2	ppm/°C
T_A = T_{min} to +25°C		1			1		ppm/°C
Bipolar Zero							
T_A = +25°C to T_{max}		5	10		5	10	ppm/°C
T_A = T_{min} to +25°C		5			5		ppm/°C
Gain (Full Scale)							
T_A = +25°C to T_{max}		15/7	50/10		10/2	20/3	ppm/°C
T_A = T_{min} to +25°C		15/7			10/2		ppm/°C
Differential Nonlinearity							
T_A = +25°C to T_{max}		2			2		ppm/°C
T_A = T_{min} to +25°C		2			2		ppm/°C
SETTLING TIME TO 1/2LSB							
All Bit ON-to-OFF or OFF-to-ON		150/250	250/350		150/250	250/350	ns
FULL SCALE TRANSITION							
10% to 90% Delay plus Rise Time		15	30		15	30	ns
90% to 10% Delay plus Fall Time		30	50		30	50	ns
POWER REQUIREMENTS							
V_{CC}, +11.4 to +16.5V dc[3]		3	5		3	5	mA
V_{EE}, -11.4 to -16.5V dc		-12	-18		-12	-18	mA
POWER SUPPLY GAIN SENSITIVITY[4]							
V_{CC}, +11.4 to +16.5V dc[3]		3	10		3	10	ppm of F.S./%
V_{EE}, -11.4 to -16.5V dc		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT RANGE		0 to +5			0 to +5		V
		-2.5 to +2.5			-2.5 to +2.5		V
		0 to +10			0 to +10		V
		-5 to +5			-5 to +5		V
		-10 to +10			-10 to +10		V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor for R2		±0.1	±0.25		±0.1	±0.25	% of F.S.
Bipolar Zero Error with Fixed 50Ω Resistor for R1		±0.05	±0.15		±0.05	±0.1	% of F.S.
Gain Adjustment Range	±0.25			±0.25			% of F.S.
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S.
REFERENCE INPUT							
Input Impedance	15k	20k	25k	15k	20k	25k	Ω
REFERENCE OUTPUT[3]							
Voltage	9.90	10.00	10.10	9.90	10.00	10.10	V
Current (available for external loads)[5]	1.5	2.5		1.5	2.5		mA
POWER DISSIPATION		225/180	345/300		225/180	345/300	mW
MULTIPLYING MODE PERFORMANCE[6]							
Quadrants		Two (2): Bipolar Operation at Digital Input Only					
Reference Voltage		+1V to +10V, Unipolar					
Accuracy		10 Bits (±0.05% of Reduced F.S.) for 1V dc Reference Voltage					
Reference Feedthrough (unipolar mode, all bits OFF, and 1 to +10V [p-p], sinewave frequency for 1/2LSB [p-p] feedthrough)		40kHz typ					
Output Slew Rate 10%-90%		5mA/μs					
90%-10%		1mA/μs					
Output Settling Time (all bits on and a 0–10V step change in reference voltage)		1.5μs to 0.01% F.S.					
CONTROL AMPLIFIER[6]							
Full Power Bandwidth		300kHz					
Small-Signal Closed-Loop Bandwidth		1.8MHz					

NOTES:

[1] Electrical tests are performed at wafer probe, before the wafer is separated into individual dice. Maintaining chip performance to specification requires great care in handling and assembly.

[2] The digital input levels are guaranteed but not tested over the temperature range.

[3] This specification applies for the AD565A/AD566A chip configured as a AD565A.

[4] The power supply gain sensitivity is tested in reference to a V_{EE} of -15V dc.

[5] For operation at elevated temperatures the reference cannot supply current for external loads. It, therefore, should be buffered if additional loads are to be supplied.

[6] This specification applies for the AD565A/AD566A chip configured as a AD566A.

Specifications subject to change without notice.

ANALOG DEVICES

Microprocessor-Compatible 12-Bit D/A Converter

AD567 CHIPS

PRODUCT DESCRIPTION

The AD567 is a complete high speed 12-bit digital-to-analog converter including a high stability buried zener voltage reference and double-buffered input latch on a single chip. The converter uses 12 precision high speed bipolar current steering switches and a laser trimmed thin film resistor network to provide fast settling time and high accuracy.

Microprocessor compatibility is achieved by the on-chip double-buffered latch. The design of the input latch allows direct interface to 4-, 8-, 12-, or 16-bit buses. The 12 bits of data from the first rank of latches can then be transferred to the second rank, avoiding generation of spurious analog output values. The latch responds to strobe pulses as short as 100ns, allowing use with the fastest available microprocessors.

The AD567J is specified for use over the 0 to +70°C temperature range and the AD567S is specified for the -55°C to +125°C range.

APPLICATION INFORMATION

1. On AD567 chips, the internal reference is not permanently connected. This allows the use of an external reference and also makes the internal reference available for external use.
2. An additional output span resistor is accessible. This permits the user to connect the AD567 chip for 10 or 20 volt spans.

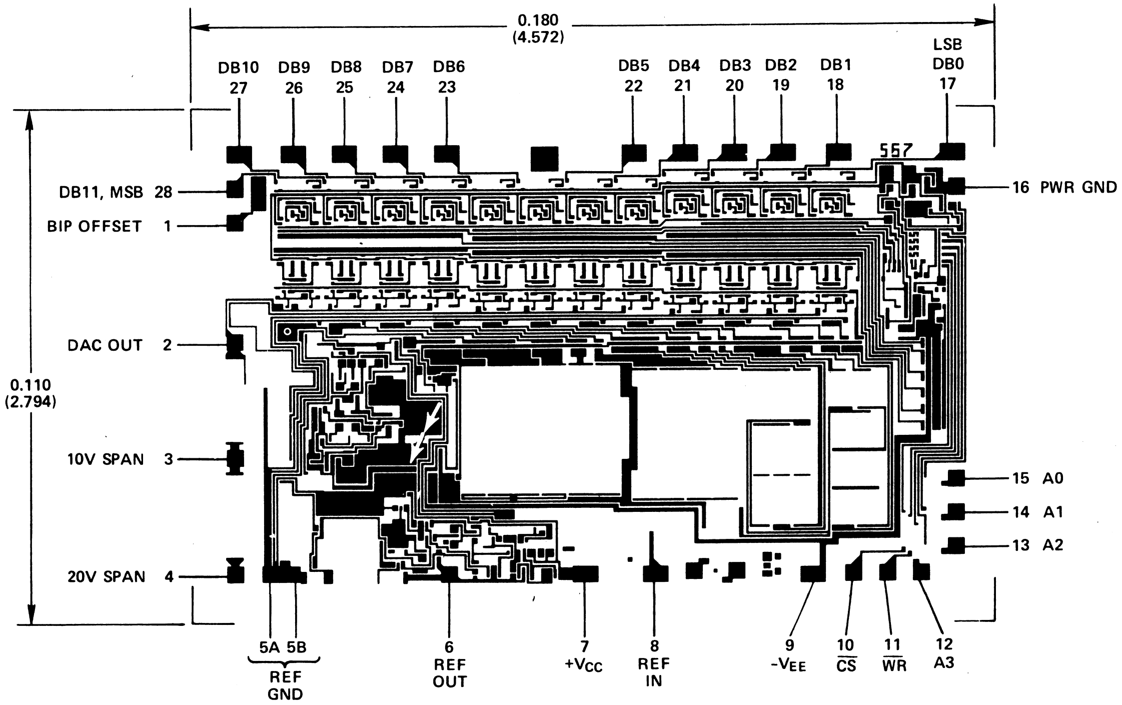
All other general application information on the AD567 packaged product catalog data sheet applies to AD567 chips.

The following additional application information applies to AD567 chips:

1. No particular wire-bonding sequence must be followed.
2. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
3. For performance to device specifications, the metal substrate pad or header beneath the AD567 chip must be connected to $-V_{EE}$, device pad number 9.
4. Do not connect to any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.
5. Pads 5A and 5B must both be connected to reference ground.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



SPECIFICATIONS[1] (T_A = +25°C, V_{CC} = +12V or +15V, V_{EE} = -12V or -15V, unless otherwise specified)

MODEL	AD567J MIN	AD567J TYP	AD567J MAX	AD567S MIN	AD567S TYP	AD567S MAX	UNITS
DATA INPUTS[2] (Pins 10–15 and 17–28)							
TTL or 5 Volt CMOS							
Input Voltage							
Bit ON Logic "1"	+2.0		+5.5	+2.0		+5.5	V
Bit OFF Logic "0"			+0.8			+0.8	V
Logic Current (each bit)							
Bit ON Logic "1"		+120	+300		+120	+300	μA
Bit OFF Logic "0"		+35	+100		+35	+100	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current							
Unipolar (all bits on)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar (all bits on or off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (exclusive of span resistors)	6k	8k	10k	6k	8k	10k	Ω
Offset							
Unipolar		0.01	0.05		0.01	0.05	% of F.S.
Bipolar		0.05	0.15		0.05	0.15	% of F.S.
Capacitance		25			25		pF
Compliance Voltage							
T_{min} to T_{max}	-1.5		+10	-1.5		+10	V
ACCURACY (error relative to full scale) +25°C		±1/4	±1/2		±1/4	±1/2	LSB
		(0.006)	(0.012)		(0.006)	(0.012)	% of F.S.
T_A = +25°C to T_{max}		±1/2	±3/4		±1/2	±3/4	LSB
T_A = T_{min} to +25°C		±1/2			±1/2		LSB
DIFFERENTIAL NONLINEARITY							
T_A = +25°C		±1/2	±3/4		±1/2	±3/4	LSB
T_A = +25°C to T_{max}		Monotonicity Guaranteed			Monotonicity Guaranteed		
T_A = T_{min} to +25°C		Monotonicity Typical			Monotonicity Typical		
TEMPERATURE COEFFICIENTS							
With Internal Reference							
Unipolar Zero							
T_A = +25°C to T_{max}		1	2		1	2	ppm/°C
T_A = T_{min} to +25°C		1			1		ppm/°C
Bipolar Zero							
T_A = +25°C to T_{max}		5	10		5	10	ppm/°C
T_A = T_{min} to +25°C		5			5		ppm/°C
Gain (Full Scale)							
T_A = +25°C to T_{max}		15	50		15	30	ppm/°C
T_A = T_{min} to +25°C		15			15		ppm/°C
Differential Nonlinearity							
T_A = +25°C to T_{max}		2			2		ppm/°C
T_A = T_{min} to +25°C		2			2		ppm/°C
TEMPERATURE RANGE							
Operating	0		+70	-55		+125	°C
Storage	-65		+150	-65		+150	°C
POWER REQUIREMENTS							
V_{CC}, +11.4 to +16.5V dc		3	5		3	5	mA
V_{EE}, -11.4 to -16.5V dc		-17	-25		-17	-25	mA
POWER SUPPLY GAIN SENSITIVITY[3]							
V_{CC} = +11.4 to +16.5V dc		3	10		3	10	ppm of F.S./%
V_{EE} = -11.4 to -16.5V dc		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT RANGE		0 to +5			0 to +5		V
		-2.5 to +2.5			-2.5 to +2.5		V
		0 to +10			0 to +10		V
		-5 to +5			-5 to +5		V
		-10 to +10			-10 to +10		V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor for R2		±0.1	±0.25		±0.1	±0.25	% of F.S.
Bipolar Zero Error with Fixed 50Ω Resistor for R1		±0.05	±0.15		±0.05	±0.15	% of F.S.
Gain Adjustment Range	±0.25			±0.25			% of F.S.
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S.
REFERENCE INPUT							
Input Impedance	15k	20k	25k	15k	20k	25k	Ω
REFERENCE OUTPUT							
Voltage	9.90	10.00	10.10	9.90	10.00	10.10	V
Current (available for external loads)	0.1	1.0		0.1	1.0		mA
POWER DISSIPATION		300	495		300	495	mW

NOTES:

[1] Electrical tests are performed at wafer probe, before the wafer is separated into individual dice. Maintaining chip performance to specification requires great care in handling and assembly.

[2] The digital input specifications are guaranteed but not tested over the operating temperature range.

[3] The power supply gain sensitivity is tested in reference to a V_{CC}, V_{EE} of ±15V dc ±10%.

Specification subject to change without notice.

ANALOG DEVICES

Low Cost, Complete 8- and 10-Bit A-to-D Converters

AD570/AD571 CHIPS

PRODUCT DESCRIPTION

The AD570 is a low-cost 8-bit successive approximation A-to-D converter consisting of a DAC, reference, clock, comparator, successive approximation register and output buffers on a single chip. The AD571 is the 10-bit version of the same chip. Since no additional components or trimming is required to perform a full-accuracy 8-bit conversion in 25μs, AD570/AD571 chips are ideal for hybrid applications. AD570J/AD571J chips are specified for operation between 0 and +70°C, AD570S/AD571S chips for −55°C to +125°C.

APPLICATION INFORMATION

AD570 and AD571 chips have one bonding pad accessible to the user that is not pinned out on packaged AD570 and AD571 devices. That pad provides two additional input ranges thus:

1. If pad 13A or 13B is used alone as the analog input, the input voltage span is 20 volts (for 0V to +20V, or −10V to +10V ranges).
2. If pads 13A and 13B are tied together and used as the analog input, the input voltage span is 10 volts (for 0V to +10V or −5V to +5V ranges) as in packaged AD570/AD571 devices.

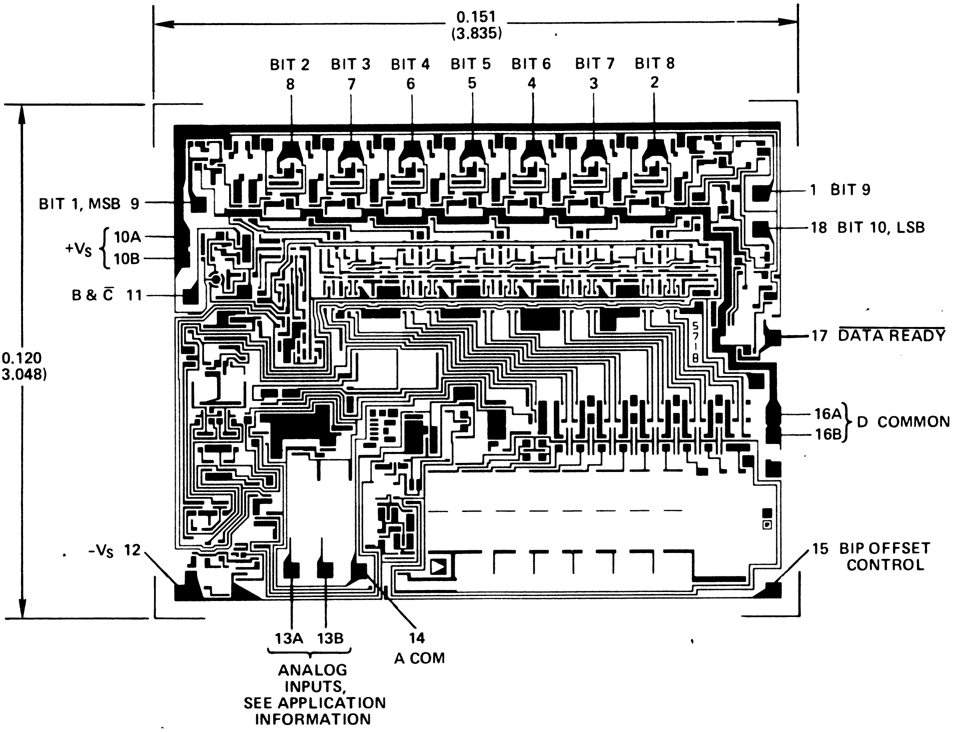
Otherwise, AD570 and AD571 chips are functionally identical to packaged AD570 and AD571 devices. For general application information, see the AD570 or AD571 packaged product catalog data sheets.

The following additional application information applies to AD570 and AD571 chips:

1. No particular wire-bonding sequence must be followed.
2. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
3. For performance to device specifications, the metal substrate pad or header beneath the AD570 and AD571 chip must be connected to $-V_S$, device pad number 12.
4. Pads 10A and 10B must both be connected to $+V_S$. Pads 16A and 16B must both be connected to Digital Common.
5. Do not connect to any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE 18-PIN CERAMIC PACKAGE.

SPECIFICATIONS[1]

(typical @ +25°C with V+ = +5V, V- = -15V, all voltages measured with respect to digital common, unless otherwise indicated)

MODEL	AD570J	AD571J	AD570S	AD571S
RESOLUTION	8 Bits	10 Bits	•	••
RELATIVE ACCURACY @ 25°C[2]	±1/2LSB max	±1LSB max	•	••
T_A = +25°C to T_{max}	±1/2LSB max	±1LSB max	•	••
T_A = T_{min} to +25°C	±1/2LSB	±1LSB	•	••
FULL SCALE CALIBRATION[3] (With 15Ω Resistor In Series With Analog Input	±2LSB (typ)	±2LSB (typ)	•	••
UNIPOLAR OFFSET (max)	±1/2LSB	±1LSB	•	••
BIPOLAR OFFSET (max)	±1/2LSB	±1LSB	•	••
DIFFERENTIAL NONLINEARITY (Resolution for Which no Missing Codes are Guaranteed)				
T_A = +25°C	8 Bits	10 Bits	•	••
T_A = +25°C to T_{max}	8 Bits	9 Bits	•	10 Bits
T_A = T_{min} to +25°C	8 Bits	9 Bits, typ	•	10 Bits, typ
TEMPERATURE RANGE				
Operating				
Tested (T_A = +25°C to T_{max})	+25°C to +70°C	+25°C to +70°C	+25°C to +125°C	+25°C to +125°C
Guaranteed, Not Tested (T_A = T_{min} to +25°C)	0 to +25°C	0 to +25°C	-55°C to +25°C	-55°C to +25°C
TEMPERATURE COEFFICIENTS				
Guaranteed max Change				
T_A = +25°C to T_{max}				
Unipolar Offset	±1LSB (88ppm/°C)	±2LSB (44ppm/°C)	±1LSB (44ppm/°C)	±2LSB (20ppm/°C)
Bipolar Offset	±1LSB (88ppm/°C)	±2LSB (44ppm/°C)	±1LSB (40ppm/°C)	±2LSB (20ppm/°C)
Full Scale Calibration[4] (With 15Ω Fixed Resistor or 50Ω Trimmer)	±2LSB (176ppm/°C)	±4LSB (88ppm/°C)	±2LSB (80ppm/°C)	±5LSB (50ppm/°C)
Typical Change				
T_A = T_{min} to +25°C				
Unipolar Offset	±1LSB	±2LSB	•	±2LSB
Bipolar Offset	±1LSB	±2LSB	•	±2LSB
Full Scale Calibration[4] (With 15Ω Fixed Resistor or 50Ω Trimmer)	±2LSB	±4LSB	•	±5LSB
POWER SUPPLY REJECTION				
Max Change In Full Scale Calibration				
TTL Positive Supply +4.5V≤V+≤+5.5V	±2LSB max	±2LSB max	•	••
Negative Supply -16.5V≤V+≤-13.5V	±2LSB max	±2LSB	•	••
ANALOG INPUT RESISTANCE				
10 Volt Span	3kΩ min	3kΩ min	•	••
	5kΩ min	5kΩ typ	•	••
	7kΩ min	7kΩ max	•	••
20 Volt Span	6kΩ min	6kΩ min	•	••
	10kΩ typ	10kΩ typ	•	••
	14kΩ max	14kΩ max	•	••
ANALOG INPUT RANGES (Analog Input to Analog Common)				
Unipolar	0 to +10V, 0 to +20V	0 to +10V, 0 to +20V	•	••
Bipolar	-5V to +5V, -10V to +10V	-5V to +5V, -10V to +10V	•	••
OUTPUT CODING				
Unipolar	Positive True Binary	Positive True Binary	•	••
Bipolar	Positive True Offset Binary	Positive True Offset Binary	•	••
LOGIC OUTPUT[6]				
Bit Outputs and Data Ready				
Output Sink Current	3.2mA min	3.2mA min	•	••
(V_{OUT} = 0.4V max, T_{min} to T_{max})	(2TTL Loads)	(2TTL Loads)	•	••
Output Source Current (Bit Outputs)[5] (V_{OUT} = 2.4V min, T_{min} to T_{max})	0.5mA min	0.5mA min	•	••
Output Leakage When Blanked	±40μA max	±40μA max	•	••
LOGIC INPUT[6]				
Blank and Convert Input				
$0 \leq V_{in} \leq V+$	±40μA max	±40μA max	•	••
Blank – Logic "1"	2.0V min	2.0V min	•	••
Convert – Logic "0"	0.8V max	0.8V max	•	••
CONVERSION TIME	15μs min	15μs min	•	••
	35μs typ	35μs typ	•	••
	40μs max	40μs max	•	••
POWER SUPPLY				
Absolute Maximum				
V+	+7V	+7V	•	••
V-	-16.5V	-16.5V	•	••
Specified Operating – Rated Performance				
V+	+5V	+5V	•	••
V-	-15V	-15V	•	••
Operating Range				
V+	+4.5V to +5.5V	+4.5V to +5.5V	•	••
V-		-12V to -16.5V	•	••
Operating Current				
Blank Mode				
V+ = +5V	2mA typ (10mA max)	2mA typ (10mA max)	•	••
V- = -15V	9mA typ (15mA max)	9mA typ 15mA max)	•	••
Convert Mode				
V+ = +5V	5mA	5mA	•	••
V- = -15V	10mA	10mA	•	••

NOTES:

[1] Electrical tests are performed at wafer probe, before the wafer is separated into individual dice. Maintaining chip performance to specification requires great care in handling and assembly.

[2] Relative accuracy is defined as the deviation of the code transition points from the ideal transfer point on a straight line from the zero to the full scale of the device.

[3] Full scale calibration is guaranteed trimmable to zero with an external 50Ω potentiometer in place of the 15Ω fixed resistor. Full scale is defined as 10 volts minus 1LSB, or 9.990 volts.

[4] Full-scale calibration temperature coefficient includes the effects of unipolar offset drift as well as gain drift.

[5] The data output lines have active pull-ups to source 0.5mA. The DATA READY line is open collector with a nominal 6kΩ internal pull-up resistor.

[6] Logic Input and Output Thresholds and Levels are tested T_A = +25°C to T_{max}, not tested but guaranteed T_A = T_{min} to +25°C.

•Specifications same as AD570J.
••Specifications same as AD571J.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

V+ to Digital Common	0 to +7V
V- to Digital Common	0 to -16.5V
Analog Common to Digital Common	±1V
Analog Input to Analog Common	±15V
Control Inputs	0 to V+
Digital Outputs (Blank Mode)	0 to V+

ANALOG DEVICES

Fast, Complete 10-Bit A-to-D Converter With Microprocessor Interface

AD573 CHIPS

PRODUCT DESCRIPTION

The AD573 is a 10-bit successive approximation A-to-D converter consisting of a DAC, reference, clock, comparator, successive approximation register and 3 state output buffers on a single chip. Since no additional components or trimming is required to perform a full-accuracy 10-bit conversion in 1.5μs, AD573 chips are ideal for precision hybrid applications. AD573 chips are available in one grade specified for 0 to +70°C operation, and another grade for -55°C to +125°C operation.

APPLICATION INFORMATION

AD573 chips have one bonding pad accessible to the user that is not pinned out on packaged AD573 devices. That pad provides two additional input ranges thus:

1. If pad 14A or 14B is used alone as the analog input, the input voltage span is 20 volts (for 0V to +20V or -10V to +10V ranges).
2. If pads 14A and 14B are tied together and used as the analog input, the input voltage span is 10 volts (for 0V to +10V or -5V to +5V ranges) as in packaged AD573 devices.

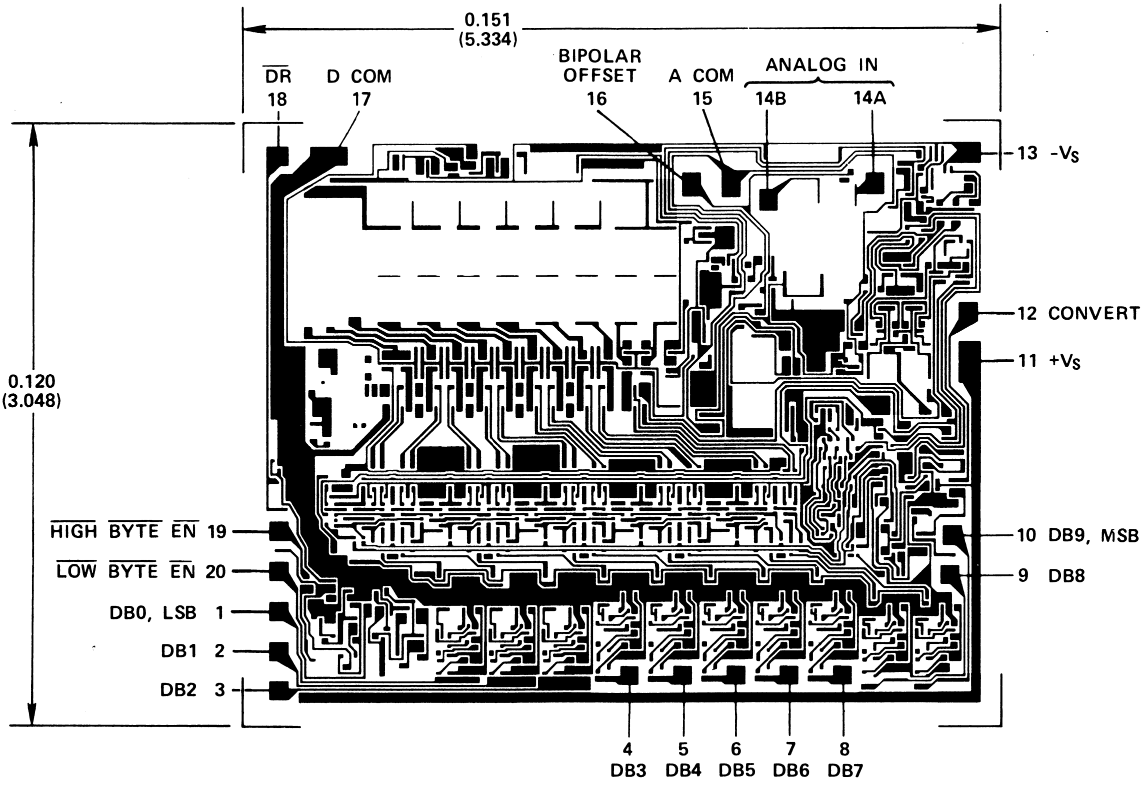
Otherwise, AD573 chips are functionally identical to packaged AD573 devices. For general application information, see the AD573 packaged product catalog data sheet.

The following additional application information applies to AD573 chips:

1. No particular wire-bonding sequence must be followed.
2. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
3. For performance to device specifications, the metal substrate pad or header beneath the AD573 chip must be connected to $-V_S$, device pad number 13.
4. Do not connect to any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).


0.151
(5.334)
$\overline{\text{DR}}$ 18
D COM 17
BIPOLAR OFFSET 16
A COM 15
ANALOG IN
14B
14A
13 $-V_S$
12 CONVERT
11 $+V_S$
10 DB9, MSB
9 DB8
0.120
(3.048)
$\overline{\text{HIGH}}$ $\overline{\text{BYTE}}$ $\overline{\text{EN}}$ 19
$\overline{\text{LOW}}$ $\overline{\text{BYTE}}$ $\overline{\text{EN}}$ 20
DB0, LSB 1
DB1 2
DB2 3
4 DB3
5 DB4
6 DB5
7 DB6
8 DB7

PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE 20-PIN PACKAGE.

SPECIFICATIONS[1]

(typical @ +25° C with V+ = +5V, V- = -15V, all voltages measured with respect to digital common, unless otherwise indicated)

MODEL	AD573J	AD573S
RESOLUTION	10 Bits	•
RELATIVE ACCURACY @ 25°C[2]	±1LSB max	±1LSB max
T_A = +25°C to T_{max}	±1LSB max	±1LSB max
T_A = T_{min} to +25°C	±1LSB	±1LSB
FULL SCALE CALIBRATION[3] (With 15Ω Resistor In Series With Analog Input	±2LSB (typ)	•
UNIPOLAR OFFSET (max)	±1LSB	•
BIPOLAR OFFSET (max)	±1LSB	•
DIFFERENTIAL NONLINEARITY (Resolution for Which no Missing Codes are Guaranteed)		
T_A = +25°C	10 Bits	•
T_A = +25°C to T_{max}	10 Bits	10 Bits
T_A = T_{min} to +25°C	10 Bits, typ	10 Bits, typ
TEMPERATURE RANGE		
Operating		
Tested (T_A = +25°C to T_{max})	+25°C to +70°C	+25°C to +125°C
Guaranteed, Not Tested (T_A = T_{min} to +25°C)	0 to +25°C	-55°C to +25°C
TEMPERATURE COEFFICIENTS		
Guaranteed max Change		
T_A = +25°C to T_{max}		
Unipolar Offset	±2LSB (44ppm/°C)	±2LSB (20ppm/°C)
Bipolar Offset	±2LSB (44ppm/°C)	±2LSB (20ppm/°C)
Full Scale Calibration[4] (With 15Ω Fixed Resistor or 50Ω Trimmer)	±4LSB (88ppm/°C)	±5LSB (50ppm/°C)
Typical Change		
T_A = T_{min} to +25°C		
Unipolar Offset	±2LSB	±2LSB
Bipolar Offset	±2LSB	±2LSB
Full Scale Calibration[4] (With 15Ω Fixed Resistor or 50Ω Trimmer)	±4LSB	±5LSB
POWER SUPPLY REJECTION		
Max Change In Full Scale Calibration		
TTL Positive Supply		
+4.5V≤V+≤+5.5V	±2LSB max	•
Negative Supply		
-15.75V≤V-≤-14.25V	±2LSB max	•
-12.6V≤V-≤-11.4V	±2LSB max	•
ANALOG INPUT RESISTANCE		
10 Volt Span	3kΩ min	•
	5kΩ typ	•
	7kΩ max	•
20 Volt Span	6kΩ min	•
	10kΩ typ	•
	14kΩ max	•
ANALOG INPUT RANGES (Analog Input to Analog Common)		
Unipolar	0 to +10V, 0 to +20V	•
Bipolar	-5V to +5V, -10V to +10V	•
OUTPUT CODING		
Unipolar	Positive True Binary	•
Bipolar	Positive True Offset Binary	•
LOGIC OUTPUT[5]		
Bit Outputs and Data Ready		
Output Sink Current	3.2mA min	•
(V_{OUT} = 0.4V max, T_{min} to T_{max})	(2TTL Loads)	•
Output Source Current (Bit Outputs)[5]		•
(V_{OUT} = 2.4V min, T_{min} to T_{max})	0.5mA min	•
Output Leakage When Blanked	±40μA max	•
LOGIC INPUT (Convert, $\overline{HBE}$, $\overline{LBE}$)		
0≤V_{IN}≤V+	±100μA max	•
Logic "1"	2.0V min	•
Logic "0"	0.8V max	•
CONVERSION TIME	10μs min	•
	15μs typ	•
	20μs max	•
POWER SUPPLY		
Absolute Maximum		
V+	+7V	•
V-	-16.5V	•
Specified Operating – Rated Performance		
V+	+5V	•
V-	-15V	•
Operating Range		
V+	+4.5V to +5.5V	•
V-	-11.4V to -15.75V	•
Operating Current		
V+ = +5V	7mA typ (25mA max)	•
V- = -15V	9mA typ (15mA max)	•

NOTES:

[1] Electrical tests are performed at wafer probe, before the wafer is separated into individual dice. Maintaining chip performance to specification requires great care in handling and assembly.

[2] Relative accuracy is defined as the deviation of the code transition points from the ideal transfer point on a straight line from the zero to the full scale of the device.

[3] Full scale calibration is guaranteed trimmable to zero with an external 50Ω potentiometer in place of the 15Ω fixed resistor. Full scale is defined as 10 volts minus 1LSB, or 9.990 volts.

[4] Full-scale calibration temperature coefficient includes the effects of unipolar offset drift as well as gain drift.

[5] The Data output lines have active pull-ups to source 0.5mA. The $\overline{\text{DATA READY}}$ line is open collector with a nominal 6kΩ internal pull-up resistor.

•Specifications same as AD573J.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

V+ to Digital Common	0 to +7V
V- to Digital Common	0 to -16.5V
Analog Common to Digital Common	±1V
Analog Input to Analog Common	±15V
Control Inputs	0 to V+
Digital Outputs (High Impedance State)	0 to V+

Precision 2.5 Volt Reference

AD580 CHIPS

PRODUCT DESCRIPTION

The AD580 is a three-terminal, low-cost voltage reference that provides a fixed 2.5V output for inputs between 4.5V and 30V. Based on the bandgap principle and implemented with thin film resistors, temperature coefficients as low as 10ppm/°C can be guaranteed. One version of the AD580 chip is specified for 0 to +70°C operation, one grade for −55°C to +125°C.

APPLICATION INFORMATION

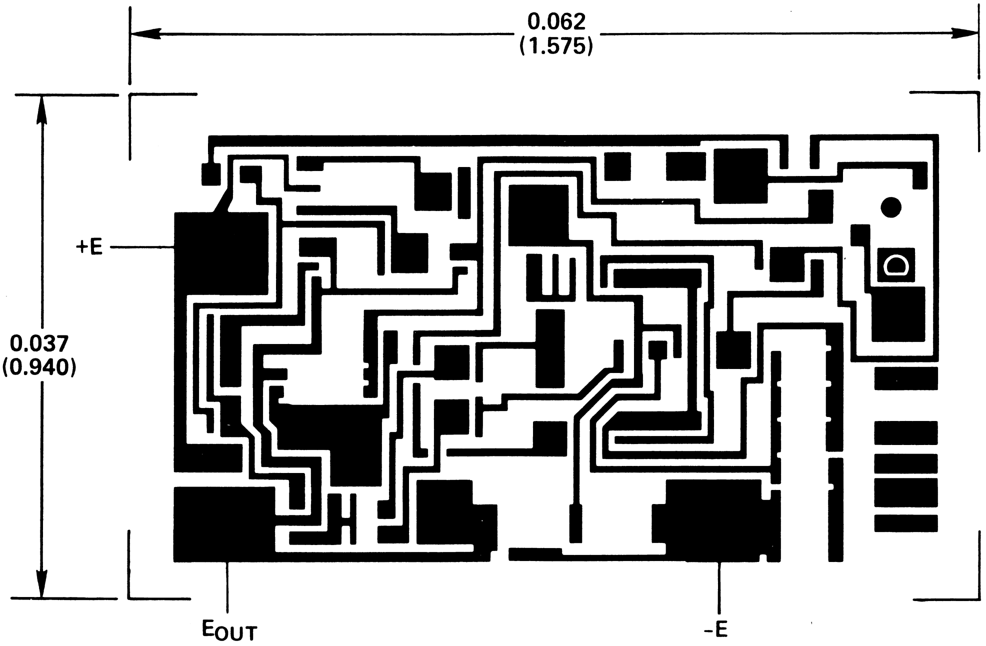
AD580 chips are functionally identical to packaged AD580 devices. For general application information, see the AD580 packaged product catalog data sheet.

The following additional application information applies to AD580 chips:

1. No particular wire-bonding sequence must be followed.
2. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
3. For performance to device specifications, the metal substrate pad or header beneath the AD580 chip must be connected to −E.
4. Do not connect to any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE TO-52, 3 PIN, METAL PACKAGE.

SPECIFICATIONS[1] (typical @ E_{IN} = +15V and 25°C unless otherwise specified)

MODEL	AD580J	AD580S
ABSOLUTE MAX RATINGS		
Input Voltage	40V	*
Operating Junction Temp Range	-55°C to +150°C	*
Storage Temperature Range	-65°C to +175°C	*
Operating Temperature Range		
Tested (T_A = +25°C to T_{max})	+25°C to +70°C	+25°C to +125°C
Guaranteed, Not Tested (T_A = T_{min} to +25°C)	0 to +25°C	-55°C to +25°C
OUTPUT VOLTAGE	2.425V min (2.575V max)	2.490V min 2.510V max
OUTPUT VOLTAGE CHANGE		
T_A = +25°C to T_{max}	15mV max (85ppm/°C)	11mV max (25ppm/°C)
T_A = T_{min} to +25°C	15mV	11mV
LINE REGULATION		
$7V \leqslant V_{IN} \leqslant 30V$	6mV max (0.6mV typ)	2mV max
$4.5V \leqslant V_{IN} \leqslant 7V$	3mV max (0.3mV typ)	1mV max
LOAD REGULATION		
ΔI = 10mA	10mV max	*
QUIESCENT CURRENT	1.5mA max (1.0mA typ)	* *
NOISE (0.1 to 10Hz)	60μV(p-p)	*
STABILITY		
Long Term	250μV	*
Per Month	25μV	*

NOTES:

[1] Electrical tests are performed at wafer probe, before the wafer is separated into individual dice. Maintaining chip performance to specification requires great care in handling and assembly.

*Specification same as AD580J.

Specifications subject to change without notice.

ANALOG DEVICES

Programmable Precision Low-Drift Reference

AD581/AD584 CHIPS

AD581 NOTE: An AD584 is an AD581 with additional specified versatility. When connected in the 10.0 volt configuration, the AD584 is functionally identical to the AD581. In hybrid circuits, AD584 chips may be substituted directly for AD581 chips without any electrical or mechanical design modifications.

AD581 chips will not be offered as a standard product.

PRODUCT DESCRIPTION

The AD584 is a precision voltage reference, "pin" programmable to any of four output voltages: 10.000V, 7.500V, 5.000V and 2.500V. Other voltages, above 10.000V or below 2.500V, can be programmed with an external resistor pair. The initial tolerances and temperature coefficients are laser-trimmed at the factory to provide precise and stable adjustment-free operation. One grade of the AD584 chip is specified for 0 to +70°C operation, one for -55°C to +125°C.

APPLICATION INFORMATION

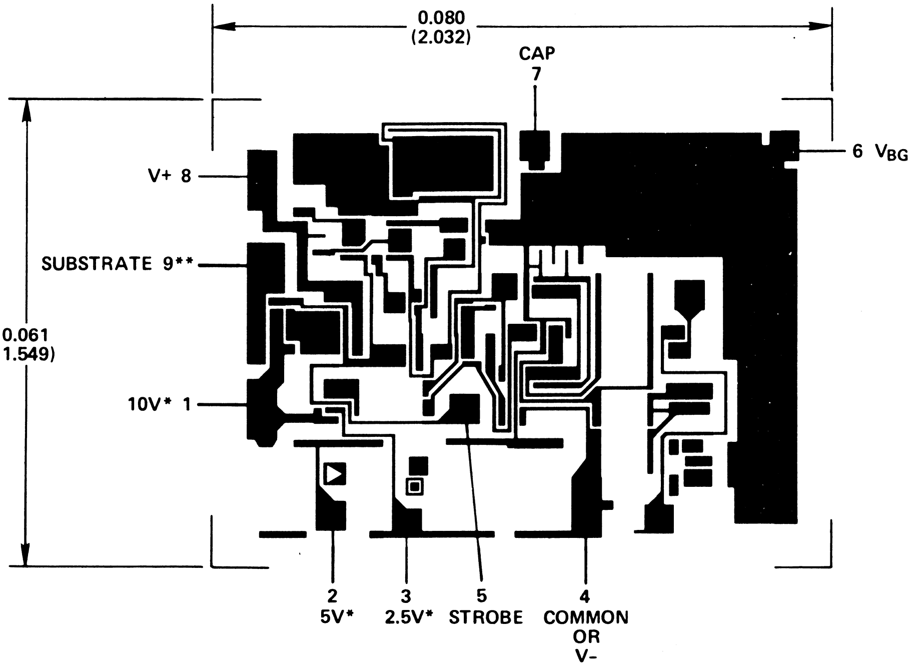
AD584 chips are functionally identical to packaged AD584 devices. For general application information, see the AD584 packaged product catalog data sheet.

The following additional application information applies to AD584 chips:

1. No particular wire-bonding sequence must be followed.
2. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
3. For performance to device specifications, the metal substrate pad or header beneath the AD584 chip must be connected to V- and substrate, pads number 4 and 9.
4. Do not connect to any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE TO-99, 8 PIN METAL PACKAGE.

***CAUTION: INTERCONNECTIONS REQUIRED; SEE PACKAGED AD584 CATALOG DATA SHEET FOR INFORMATION.**
****NOT BROUGHT OUT ON PACKAGED DEVICE.**

SPECIFICATIONS[1] (typical @ V_{IN} = +15V and +25°C unless otherwise noted)

MODEL	AD584J	AD584T
ABSOLUTE MAX RATINGS		
Input Voltage V_{IN} to Ground	40V	*
Operating Junction Temp. Range	-55°C to +150°C	*
Storage Temperature Range	-65°C to +175°C	*
Operating Temperature Range		
Tested (T_A = +25°C to T_{max})	+25°C to +70°C	+25°C to +125°C
Guaranteed, Not Tested		
(T_A = T_{min} to +25°C	0 to +25°C	-55°C to +25°C
OUTPUT VOLTAGE TOLERANCE		
Maximum Error[2] for Nominal		
Outputs of:		
10.000V	±30mV	±10mV
7.500V	±22mV	±8mV
5.000V	±15mV	±6mV
2.500V	±7.5mV	±3.5mV
OUTPUT VOLTAGE CHANGE		
Maximum Deviation from +25°C		
Value, T_A = +25°C to T_{max}[3]		
10.000, 7.500, 5.000V Outputs	30ppm/°C	15ppm/°C
2.500V Output	30ppm/°C	20ppm/°C
Typical Deviation from +25°C		
Value, T_A = T_{min} to +25°C[3]		
10.000, 7.500, 5.000V Outputs	30ppm/°C	15ppm/°C
2.500V Output	30ppm/°C	20ppm/°C
Differential Temperature Coefficients Between Outputs	5ppm/°C typ	3ppm/°C typ
QUIESCENT CURRENT	1.0mA max	*
	750μA typ	*
Temperature Variation	1.5μA/°C typ	*
TURN-ON SETTLING TIME TO 0.1%	200μs	*
NOISE		
(0.1 to 10Hz)	50μV p-p	*
LONG-TERM STABILITY	25ppm/1000 Hrs. (Non-Cumulative)	*
SHORT CIRCUIT CURRENT	30mA	*
LINE REGULATION (No Load)		
15V $\leq V_{IN} \leq$ 30V	0.002%/V	*
(V_{OUT} +2.5V) $\leq V_{IN} \leq$ 15V	0.005%/V	*
LOAD REGULATION		
0 $\leq I_{OUT} \leq$ 5mA, All Outputs	50ppm/mA max	*
	(20ppm/mA typ)	*
OUTPUT CURRENT[4]		
$V_{IN} \geq V_{OUT}$ +2.5V		
Source @ +25°C	10mA min	*
Source T_{min} to T_{max}	5mA min	*
Sink T_{min} to T_{max}	5mA min	200μA min
Sink -55°C to +85°C	—	5mA min

NOTES:

[1] Electrical tests are performed at wafer probe, before the wafer is separated into individual dice. Maintaining chip performance to specification requires great care in handling and assembly.

[2] At Pad 1.

[3] Calculated as average over the specified operating temperature range.

[4] Tested T_A = +25°C to T_{max}. Not tested but guaranteed T_{min} to +25°C.

*Specifications same as AD584J.

Specifications subject to change without notice.

ANALOG DEVICES

Low Cost Precision Sample-and-Hold

AD582 CHIPS

PRODUCT DESCRIPTION

The AD582 is a low-cost precision sample-and-hold amplifier consisting of an operational amplifier, low-leakage analog switch and a JFET integrating amplifier. The only external component required is a holding capacitor. The AD582 may be connected in any popular op amp configuration giving the user control of gain and frequency response. The sample/hold mode control may be operated from any popular logic family. AD582 chips are available in one grade specified for 0 to +70°C operation and one for -55°C to +125°C.

APPLICATION INFORMATION

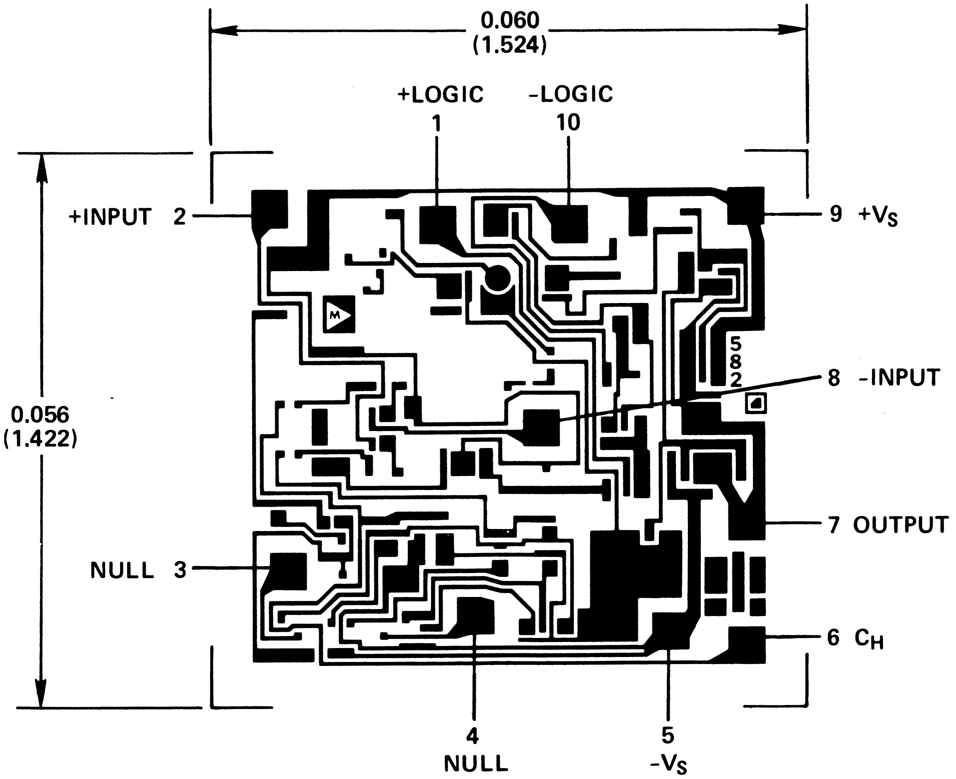
AD582 chips are functionally identical to packaged AD582 devices. For general application information, see the AD582 packaged product catalog data sheet.

The following additional application information applies to AD582 chips:

1. No particular wire-bonding sequence must be followed.
2. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
3. For performance to device specifications, the metal substrate pad or header beneath the AD582 chip must be connected to $-V_S$, device pad number 5.
4. Do not connect to any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE TO-100 10 PIN METAL PACKAGE.

SPECIFICATIONS[1] (typical @ +25°C, V_S = ±15V and C_H = 1000pF, A = +1 unless otherwise specified)

MODEL	AD582K	AD582S
SAMPLE/HOLD CHARACTERISTICS		
Acquisition Time, 10V Step to 0.1%, C_H = 100pF	6µs	*
Acquisition Time, 10V Step to 0.01%, C_H = 1000pF	25µs	*
Aperture Time, 20V p-p Input, Hold 0V	150ns	*
Aperture Jitter, 20V p-p Input, Hold 0V	15ns	*
Settling Time, 20V p-p Input, Hold 0V, to 0.01%	0.5µs	*
Droop Current, Steady State, ±10V_{OUT}	100pA max	*
Droop Current, T_A = +25°C to T_{max}	1nA	150nA max
T_A = T_{min} to +25°C	1nA	100nA
Charge Transfer	5pC max (1.5pC typ)	*
Sample to Hold Offset	0.5mV	*
Feedthrough Capacitance 20V p-p, 10kHz Input	0.05pF	*
TRANSFER CHARACTERISTICS		
Open Loop Gain V_{OUT} = 20V p-p, R_L = 2k	50k (25k min)	*
Common Mode Rejection V_{CM} = 20V p-p, F = 50Hz	70dB (60dB min)	*
Small Signal Gain Bandwidth V_{OUT} = 100mV p-p, C_H = 200pF	1.5MHz	*
Full Power Bandwidth V_{OUT} = 20V p-p, C_H = 200pF	70kHz	*
Slew Rate V_{OUT} = 20V p-p, C_H = 200pF	3V/µs	*
Output Resistance Hold Mode, I_{OUT} = ±5mA	12Ω	*
Linearity V_{OUT} = 20V p-p, R_L = 2k	±0.01%	*
Output Short Circuit Current	±25mA	*
ANALOG INPUT CHARACTERISTICS		
Offset Voltage	2mV (6mV max)	*
Offset Voltage, T_A = +25°C to T_{max}	4mV	5mV (8mV max)
T_A = T_{min} to +25°C	4mV	5mV
Bias Current	3µA max (1.5µA typ)	*
Offset Current	300nA max (75nA typ)	*
Offset Current, T_A = +25°C to T_{max}	100nA	100nA (400nA max)
T_A = T_{min} to +25°C	100nA	100nA
Input Capacitance, f = 1MHz	2pF	*
Input Resistance, Sample or Hold 20V p-p Input, A = +1	30MΩ	*
Absolute Max Diff Input Voltage	30V	*
Absolute Max Input Voltage, Either Input	±V_S	*
DIGITAL INPUT CHARACTERISTICS		
+Logic Input Voltage		
Hold Mode, T_{min} to T_{max}, -Logic @ 0V	+2V min	*
Sample Mode, T_{min} to T_{max}, -Logic @ 0V	+0.8V max	*
+Logic Input Current		
Hold Mode, +Logic @ +5V, -Logic @ 0V	1.5µA	*
Sample Mode, +Logic @ 0V, -Logic @ 0V	1nA	*
-Logic Input Current		
Hold Mode, +Logic @ +5V, -Logic @ 0V	24µA	*
Sample Mode, +Logic @ 0V, -Logic @ 0V	4µA	*
Absolute Max Diff Input Voltage, +L to -L	+15V/-6V	*
Absolute Max Input Voltage, Either Input	±V_S	*
POWER SUPPLY CHARACTERISTICS		
Operating Voltage Range	±9V to ±18V	±9V to ±22V
Supply Current, R_L = ∞	3mA (4.5mA max)	*
Power Supply Rejection, ΔV_S = 5V, Sample Mode	75dB (60dB min)	*
TEMPERATURE RANGE		
Operating		
Tested (T_A = +25°C to T_{max})	+25°C to +70°C	+25°C to +125°C
Guaranteed, Not Tested (T_A = T_{min} to +25°C)	0 to +25°C	-55°C to +25°C
Operating	-25°C to +85°C	-55°C to +125°C
Storage	-65°C to +150°C	*

NOTES:

[1] Electrical tests are performed at wafer probe, before the wafer is separated into individual dice. Maintaining chip performance to specification requires great care in handling and assembly.

*Specifications same as AD582K.

Specifications subject to change without notice.

ANALOG DEVICES

Two-Terminal IC 1.2 Volt Reference

AD589 CHIPS

PRODUCT DESCRIPTION

The AD589 is a two-terminal, low cost, temperature compensated bandgap voltage reference which provides a fixed 1.23V output voltage for input currents between 50μA and 5.0mA.

The high stability of the AD589 is primarily dependent upon the matching and thermal tracking of the on-chip components. Analog Devices' precision bipolar processing and thin-film technology combine to provide excellent performance at low cost.

Additionally, the active circuit produces an output impedance ten times lower than typical low-TC zener diodes. This feature allows operation with no external components required to maintain full accuracy under changing load conditions.

The AD589J is specified for use over the 0 to +70°C temperature range and the AD589T is specified for −55°C to +125°C range.

APPLICATION INFORMATION

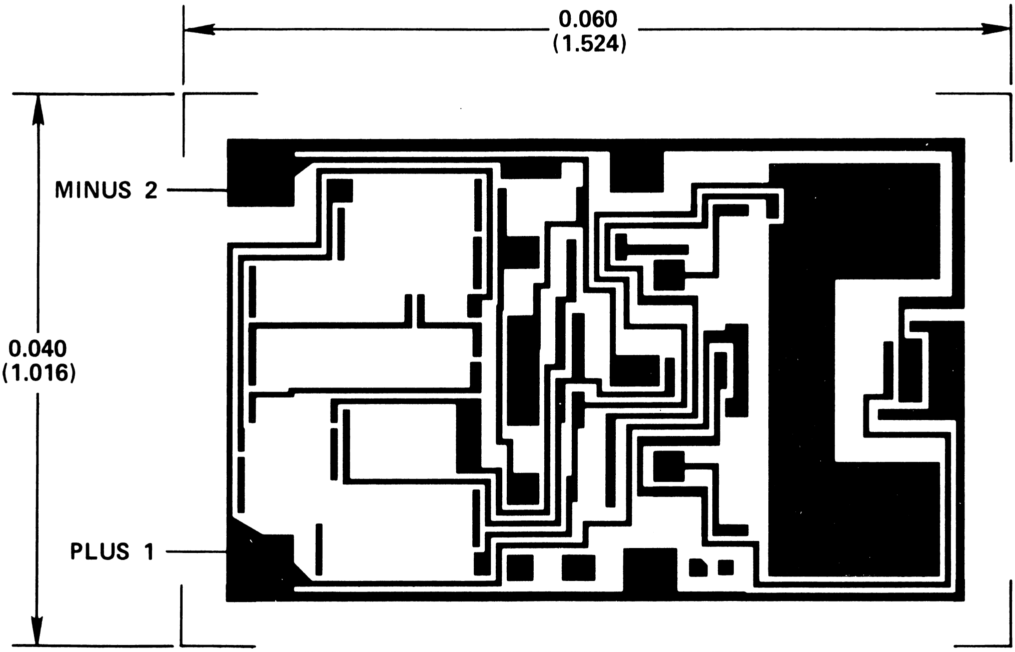
AD589 chips are functionally identical to packaged AD589 devices. For general application information, see the AD589 packaged product catalog data sheet.

The following additional application information applies to AD589 chips:

1. No particular wire-bonding sequence must be followed.
2. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section,
3. For performance to device specifications, the metal substrate pad or header beneath the AD589 chip must be connected to the minus pad.
4. Do not connect to any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



SPECIFICATIONS[1] (typical @ I_{IN} = 500µA and T_A = 25°C unless otherwise noted)

Model	AD589J	AD589T
ABSOLUTE MAXIMUM RATINGS		
Current	10mA	*
Reverse Current	10mA	*
Power Dissipation[2]	125mW	*
Storage Temperature Range	-65°C to +175°C	*
Operating Junction Temperature Range	-55°C to +150°C	*
Lead Temperature (Soldering, 10sec)	300°C	*
Operating Temperature Range	0 to +70°C	-55°C to +125°C
OUTPUT VOLTAGE	1.200V min	*
	1.235V typ	*
	1.250V max	*
OUTPUT VOLTAGE CHANGE vs. CURRENT (50µA - 5mA)	5mV max	*
DYNAMIC OUTPUT IMPEDANCE	0.6Ω	*
	2Ω max	*
RMS NOISE VOLTAGE 10Hz < f < 10kHz	5µV	*
TEMPERATURE COEFFICIENT – ppm/°C	100 max	50 max
TURN-ON SETTLING TIME TO 0.1%	25µs	*
OPERATING CURRENT[3]	50µA min	*
	5mA max	*

NOTES

[1] Electrical tests are performed at wafer probe, before the wafer is separated into individual dice. Maintaining chip performance to specification requires great care in handling and assembly.

[2] Absolute maximum power dissipation is limited by maximum current through the device. Maximum rating at elevated temperatures must be computed assuming $T_J \leq 150°C$, and $\theta_{JA} = 400°C/W$.

[3] Optimum performance is obtained at currents below 500µA. Stray shunt capacitances should be minimized. If strays cannot be avoided, a shunt capacitor of at least 1000pF is recommended.

*Specifications same as AD589J.
Specifications subject to change without notice.

ANALOG DEVICES

Two-Terminal IC Temperature Transducer

AD590 CHIPS

PRODUCT DESCRIPTION

The AD590 is a two-terminal temperature transducer which produces an output current proportional to absolute temperature. For supply voltages between +4V and +30V, the AD590 acts as a high impedance, constant current regulator passing 1μA/°K from -55°C to +150°C. Laser-trimming of on-chip thin-film resistors calibrates the AD590 to provide a 298.2μA output at 298.2°K (+25°C). Low cost, linearity and ease of application make AD590 chips ideal for monitoring temperatures at critical locations in hybrid assemblies.

APPLICATION INFORMATION

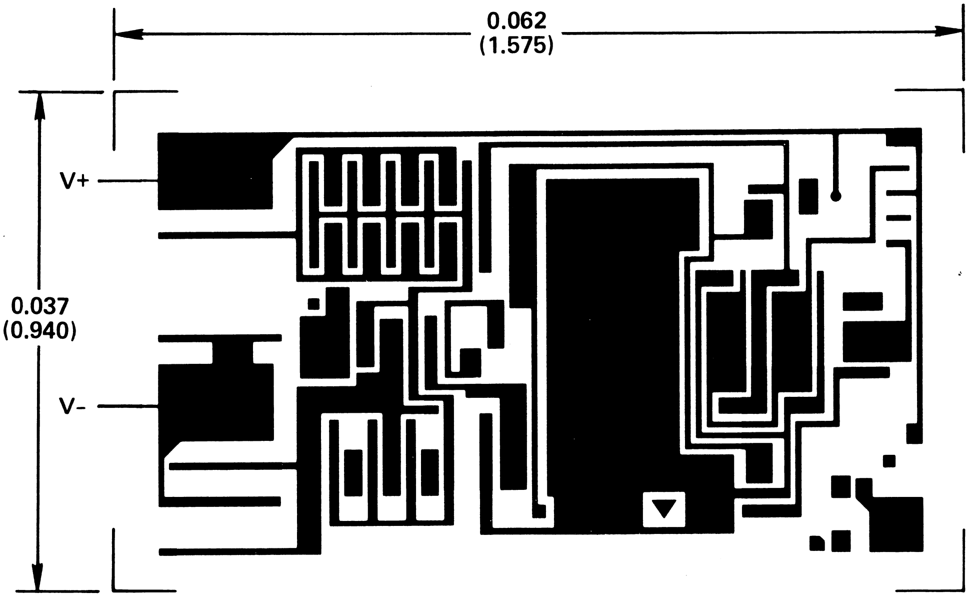
AD590 chips are functionally identical to packaged AD590 devices. For general application information, see the AD590 packaged product catalog data sheet.

The following additional application information applies to AD590 chips:

1. *IMPORTANT!* Unlike other bipolar integrated circuit chips, the AD590 substrate *must* be electrically isolated (floating). The mounting pad or header should be nonconductive, insulated or isolated.
2. No particular wire-bonding sequence must be followed.
3. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
4. Do not connect to any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



SPECIFICATIONS[1] (typical @ +25°C and V_S = 5V unless otherwise noted)

MODEL	AD590J
ABSOLUTE MAXIMUM RATINGS	
Forward Voltage (E+ to E-)	+44V
Reverse Voltage (E+ to E-)	-20V
Rated Performance Temperature Range[2]	-55°C to +150°C
Storage Temperature Range[2]	-65°C to +175°C
POWER SUPPLY	
Operating Voltage Range	+4V to +30V
OUTPUT	
Nominal Current Output @ +25°C (298.2°K)	298.2μA
Nominal Temperature Coefficient	1μA/°C
Calibration Error @ +25°C	±5.0°C max
Absolute Error[3] (over rated performance temperature range)	
Without External Calibration Adjustment	±10.0°C max
With +25°C Calibration Error Set to Zero	±3.0°C max
Nonlinearity	±1.5°C max
Repeatability[4]	±0.1°C max
Long Term Drift[5]	±0.1°C max
Current Noise	$40pA/\sqrt{Hz}$
Power Supply Rejection	
$+4V \leqslant V_S \leqslant +5V$	0.5μA/V
$+5V \leqslant V_S \leqslant +15V$	0.2μA/V
$+15V \leqslant V_S \leqslant +30V$	0.1μA/V
Case Isolation to Either Lead	$10^{10}\Omega$
Effective Shunt Capacitance	100pF
Electrical Turn-On Time[6]	20μs
Reverse Bias Leakage Current[7] (Reverse Voltage = 10V)	10pA

NOTES:

[1] Electrical tests are performed at wafer probe, before the wafer is separated into individual dice. Maintaining chip performance to specification requires great care in handling and assembly.

[2] The AD590 has been used at -100°C and +200°C for short periods of measurement with no physical damage to the device. However, the absolute errors specified apply to only the rated performance temperature range.

[3] See page 9-8 for explanation of error components. Note that ±1°C error is the equivalent of ±1μA error.

[4] Maximum deviation between +25°C readings after temperature cycling between -55°C and +150°C; guaranteed not tested.

[5] Conditions: constant +5V, constant +125°C; guaranteed, not tested.

[6] Does not include self heating effects; see page 9-9 for explanation of these effects.

[7] Leakage current doubles every 10°C.

Specifications subject to change without notice.

ANALOG DEVICES

Precision Low Cost Dual BIFET Op Amp

AD642 CHIPS

PRODUCT DESCRIPTION

The AD642 is a pair of matched high speed monolithic FET-input operational amplifiers fabricated with the most advanced bipolar, JFET and laser trimming technologies. The AD642 offers matched bias currents that are significantly lower than currently available monolithic dual FET input operational amplifiers: 75pA max, matched to 25pA.

The tight matching and temperature tracking between the operational amplifiers is achieved by ion-implanted JFETs and laser-wafer trimming. Ion-implantation permits the fabrication of precision, matched JFETs on a monolithic bipolar chip. This optimizes the process to produce matched bias currents which have lower initial bias currents than other popular FET input op amps. Laser-wafer trimming each amplifier's input offset voltage assures a tight initial match, this combined with superior IC processing guarantees offset voltage tracking over the temperature range.

APPLICATION INFORMATION

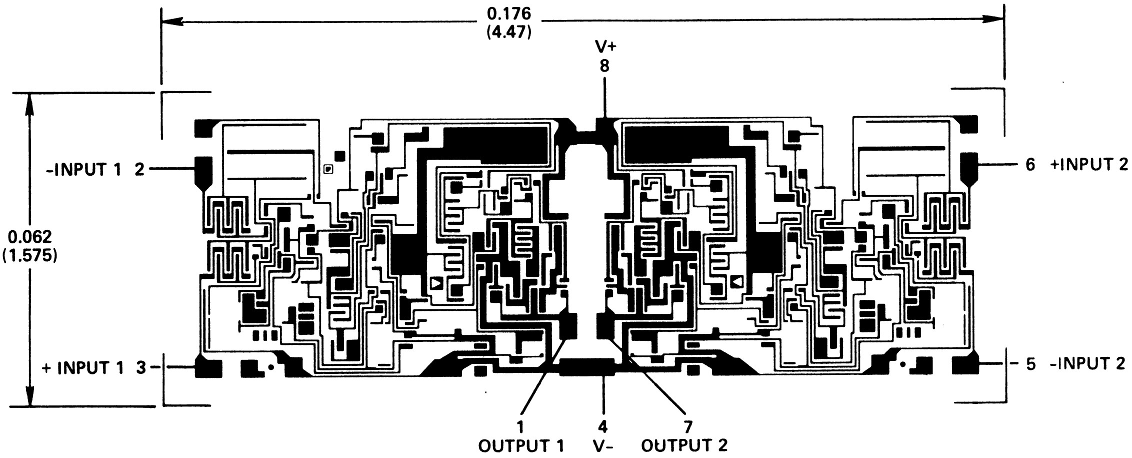
AD642 chips are functionally identical to packaged AD642 devices. For general application information, see the AD642 packaged product catalog data sheet.

The following additional applications information applies to AD642 chips:

1. No particular wire-bonding sequence must be followed.
2. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
3. For performance to device specifications, the metal substrate pad or header beneath the AD642 chip must be connected to $-V_S$, device pad number 4.
4. Do not connect to any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE TO-99 8-PIN METAL PACKAGE.

SPECIFICATIONS[1] (typical @ +25°C and V_S = ±15V dc unless otherwise specified)

MODEL	AD642J
OPEN LOOP GAIN	
V_{OUT} = ±10V, $R_L \geq 2k\Omega$	100,000 min
T_A = +25°C to T_{max}	100,000 min
T_{min} to +25°C	100,000
OUTPUT CHARACTERISTICS	
Voltage @ R_L = 2kΩ, T_A = min to max	(±12V) ±10V min
Voltage @ R_L = 10kΩ, T_A = min to max	(±13V) ±12V min
Short Circuit Current	25mA
FREQUENCY RESPONSE	
Unity Gain, Small Signal	1.0MHz
Full Power Response	50kHz
Slew Rate, Unity Gain	3.0V/μs
INPUT OFFSET VOLTAGE[2]	2.0mV max
vs. Supply, T_A = +25°C to T_{max}	200μV/V max
T_{min} to +25°C	200μV/V
INPUT BIAS CURRENT	
Either Input[3]	10pA, 75pA max
Input Offset Current	5pA
MATCHING CHARACTERISTICS[4]	
Offset Voltage	1.0mV
Offset Voltage T_{min}-T_{max}	3.5mV max
Input Bias Current	35pA max
Crosstalk–1kHz 20V p-p	-124dB
INPUT IMPEDANCE	
Differential	$10^{12}\Omega \| 6pF$
Common Mode	$10^{12}\Omega \| 6pF$
INPUT VOLTAGE RANGE	
Differential[5]	±20V
Common Mode	±12V (±10V min)
Common Mode Rejection, V_{IN} = ±10V	76dB min
POWER SUPPLY	
Rated Performance	±15V
Operating	±(5 to 18)V
Quiescent Current	2.8mA max
VOLTAGE NOISE	
0.1-10Hz	2μV p-p
10Hz	$70nV/\sqrt{Hz}$
100Hz	$45nV/\sqrt{Hz}$
1kHz	$30nV/\sqrt{Hz}$
10kHz	$25nV/\sqrt{Hz}$
TEMPERATURE RANGE	
Operating, Rated Performance	0 to +70°C
Storage	-65°C to +150°C

NOTES

[1] Electrical tests are performed at wafer probe, before the wafer is separated into individual dice. Maintaining chip performance to specification requires great care in handling and assembly.

[2] Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[3] Bias current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

[4] Matching is defined as the difference between parameters of the two amplifiers.

[5] Defined as the maximum safe voltage between inputs, such that neither exceeds ±10V from ground.

Specifications subject to change without notice.

ANALOG DEVICES

Dual High Speed Implanted FET-Input Op Amp

AD644 CHIPS

PRODUCT DESCRIPTION

The AD644 is a pair of matched high speed monolithic FET-input operational amplifiers fabricated with the most advanced bipolar, JFET and laser trimming technologies. The tight matching and temperature tracking between the operational amplifiers is achieved by ion-implanted JFETs and laser-wafer trimming. The AD644 is recommended for applications where both high speed and dc performance are required.

APPLICATION INFORMATION

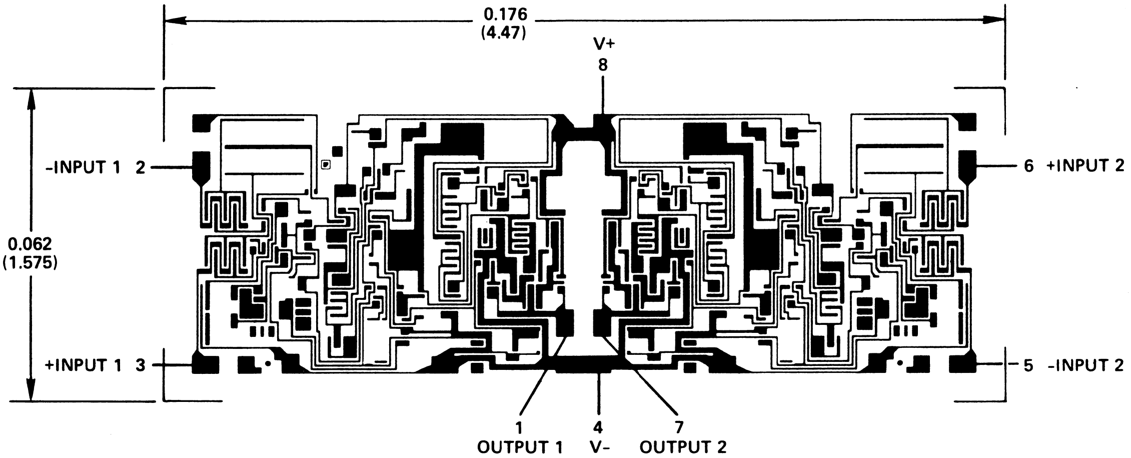
AD644 chips are functionally identical to packaged AD644 devices. For general application information, see the AD644 packaged product catalog data sheet.

The following additional application information applies to AD644 chips:

1. No particular wire-bonding sequence must be followed.
2. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
3. For performance to device specifications, the metal substrate pad or header beneath the AD644 chip must be connected to $-V_S$, device pad number 4.
4. Do not connect to any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE TO-99 8-PIN METAL PACKAGE.

SPECIFICATIONS[1] (typical @ +25°C and $V_S = \pm 15V$ dc unless otherwise specified)

MODEL	AD644J
OPEN LOOP GAIN	
$V_{OUT} = \pm 10V$, $R_L \geqslant 2k\Omega$	30,000 min
$T_A = +25^\circ C$ to T_{max}, $R_L = 2k\Omega$	20,000 min
$T_A = T_{min}$ to $+25^\circ C$, $R_L = 2k\Omega$	20,000
OUTPUT CHARACTERISTICS	
Voltage @ $R_L = 2k\Omega$, T_A = min to max	±12V (±10V min)
Voltage @ $R_L = 10k\Omega$, T_A = min to max	±13V (±12V min)
Short Circuit Current	25mA
FREQUENCY RESPONSE	
Unity Gain, Small Signal	2.0MHz
Full Power Response	200kHz
Slew Rate, Unity Gain	13.0V/μs
Total Harmonic Distortion, f = 1kHz	0.0015%
INPUT OFFSET VOLTAGE[2]	2.0mV max
vs. Supply, $T_A = +25^\circ C$ to T_{max}	200μV/V max
$T_A = T_{min}$ to $+25^\circ C$	200μV/V
INPUT BIAS CURRENT	
Either Input[3]	10pA (75pA max)
Input Offset Current	10pA
MATCHING CHARACTERISTICS[4]	
Input Offset Voltage	1.0mV max
Input Offset Voltage $T_{min} - T_{max}$	3.5mV max
Input Bias Current	35pA max
Crosstalk	-124dB
INPUT IMPEDANCE	
Differential	$10^{12}\Omega \| 6pF$
Common Mode	$10^{12}\Omega \| 3pF$
INPUT VOLTAGE RANGE	
Differential[5]	±20V
Common Mode	±12V (±10V min)
Common Mode Rejection, $V_{IN} = \pm 10V$	76dB min
POWER SUPPLY	
Rated Performance	±15V
Operating	±(5 to 18)V
Quiescent Current	3.5mA (4.5mA max)
VOLTAGE NOISE	
0.1-10Hz	2μV p-p
10Hz	$35nV/\sqrt{Hz}$
100Hz	$22nV/\sqrt{Hz}$
1kHz	$18nV/\sqrt{Hz}$
10kHz	$16nV/\sqrt{Hz}$
TEMPERATURE RANGE	
Operating, Rated Performance	0 to +70°C
Storage	-65°C to +150°C

NOTES

[1] Electrical tests are performed at wafer probe, before the wafer is separated into individual dice. Maintaining chip performance to specification requires great care in handling and assembly.

[2] Input Offset Voltage specifications are guaranteed after 5 minutes of operation at $T_A = +25^\circ C$.

[3] Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at $T_A = +25^\circ C$. For higher temperatures, the current doubles every 10°C.

[4] Matching is defined as the difference between parameters of the two amplifiers.

[5] Defined as voltage between inputs, such that neither exceeds ±10V from ground.

Specifications subject to change without notice.

ANALOG
DEVICES

High Speed
8-Bit D-to-A Converter

AD DAC-08 CHIPS

PRODUCT DESCRIPTION

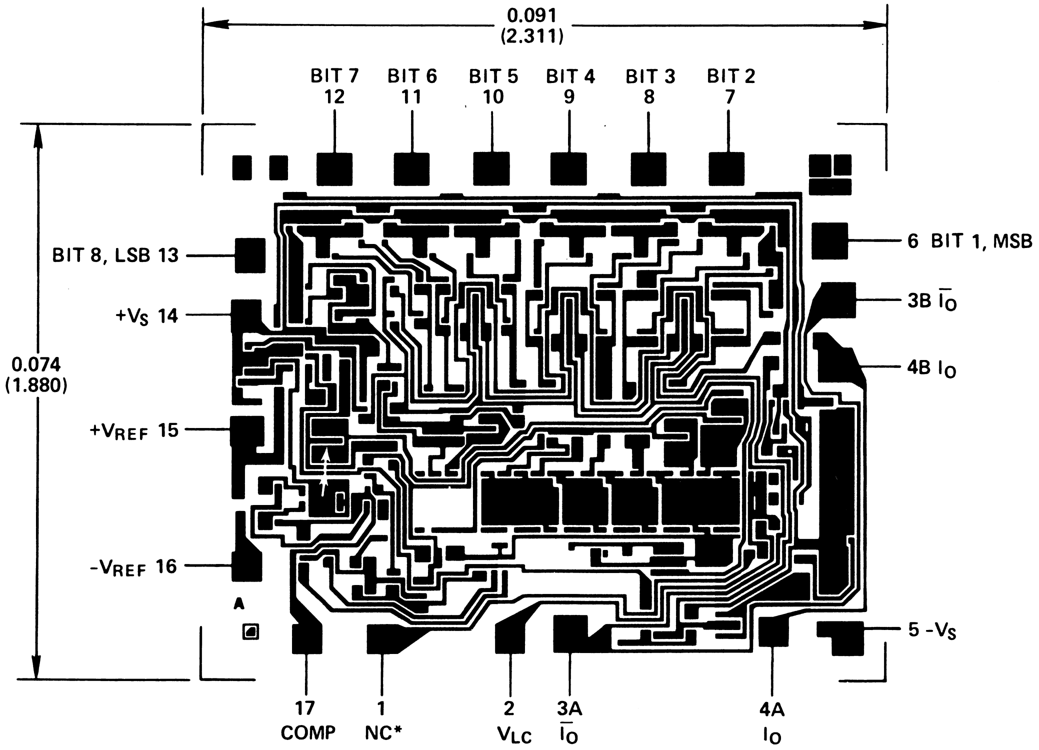
The AD DAC-08 is a high-speed 8-bit two-quadrant multiplying D-to-A converter, consisting of matched bipolar switches, a control amplifier and a precision resistor network. Advanced design and manufacturing techniques result in 85 nanosecond settling time, and compatibility with older industry standard DAC-08 devices. One accuracy grade is specified for 0 to +70°C, one for -55°C to +125°C.

APPLICATION INFORMATION

1. I_O and $\overline{I_O}$ are provided at two alternate locations.
   a.) Do not use both I_O (or both $\overline{I_O}$) locations for different functions. They are merely the same output wired to two different locations.
   b.) If $\overline{I_O}$ (or I_O) is to be unused in both locations, it should be grounded at one of the two locations.
2. No particular wire-bonding sequence must be followed.
3. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
4. For performance to device specifications, the metal substrate pad or header beneath the AD DAC-08 chip must be connected to $-V_S$, device pad number 5.
5. Do not connect to any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph. On AD DAC-08 chips, specifically do not connect to bonding pad area marked number 1 on metalization photograph.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



*NOTE: DO NOT CONNECT TO PAD NUMBER 1.
PAD NUMBERS DO NOT CORRESPOND TO PACKAGED DEVICE PIN NUMBERS.

SPECIFICATIONS[1] (V_S = ±15V and I_{REF} = 2.0mA unless otherwise noted)

CHARACTERISTIC	SYMBOL	CONDITIONS	T_A = 25°C to T_{MAX} MIN	TYP	MAX	T_A = T_{MIN} to +25°C MIN	TYP	MAX	UNITS
NONLINEARITY									
AD DAC-08A					±0.1		±0.1		%FS
AD DAC-08C					±0.39		±0.39		%FS
SETTLING TIME	t_s	Full-Scale Step to 1/2LSB		85			85		ns
PROPAGATION DELAY	t_{PLH}, t_{PHL}	All Bits Switched		35			35		ns
FULL SCALE TEMPCO	TC I_{FS}								
AD DAC-08A				±10	±50		±10		ppm/°C
AD DAC-08C				±10	±80		±10		ppm/°C
OUTPUT VOLTAGE COMPLIANCE	V_{OC}	$\Delta I_{FS} < 1/2$LSB $R_{OUT} > 20M\Omega$	-10		+18	-10		+18	V
FULL SCALE CURRENT	I_{FS4}	V_{REF} = 10.000V $R_{14} = R_{15}$ = 5.000kΩ T_A = 25°C							
AD DAC-08C			1.94	1.99	2.04		1.99		mA
AD DAC-08A			1.984	1.992	2.000		1.992		mA
FULL SCALE SYMMETRY	I_{FSS}	($I_{FS4} - I_{FS2}$)							
AD DAC-08A				±0.5	±4.0		±0.5		µA
AD DAC-08C				±2.0	±16.0		±2.0		µA
ZERO SCALE CURRENT	I_{ZS}								
AD DAC-08A				0.1	1.0		0.1		µA
AD DAC-08C				0.2	4.0		0.2		µA
OUTPUT CURRENT RANGE	I_{FSR}	V- = -5.0V	0	2.0	2.1		2.0		mA
		V- = -7.0 to -18V	0	2.0	4.2		2.0		mA
LOGIC INPUT LEVELS									
Logic "0"	V_{IL}	V_{LC} = 0V			0.8		0.8		V dc
Logic "1"	V_{IH}	V_{LC} = 0V	2.0				2.0		V dc
LOGIC INPUT CURRENTS									
Logic "0"	I_{IL}	$-10V < V_{IN} < +0.8V$		-2.0	-10		-2.0		µA
Logic "1"	I_{IH}	$2.0V < V_{IN} < 18V$		0.002	10		0.002		µA
LOGIC INPUT SWING	V_{IS}	V- = -15V	-10		+18	-10		+18	V
LOGIC THRESHOLD RANGE	V_{IHL}	V_S = ±15V	-10		+13.5	-10		+13.5	V
REFERENCE BIAS CURRENT	I_{REF}		+0.1	-1.0	-3.0		-1.0		µA
REFERENCE INPUT SLEW RATE	dI/dt		4.0	8.0			8.0		mA/µs
POWER SUPPLY SENSITIVITY	$PSSI_{FS+}$	V+ = 4.5V to 18V		±0.003	±0.01		±0.0003		%/%
	$PSSI_{FS-}$	V- = -4.5V to -18V		±0.002	±0.01		±0.002		%/%
		I_{REF} = 1.0mA							
POWER SUPPLY CURRENT	I+	From $+V_S$	0.4	2.3	3.8		2.3		mA
	I-	From $-V_S$	-0.8	-6.4	-7.8		-6.4		mA
POWER DISSIPATION	P_D	±5V, I_{REF} = 1.0mA		33	48		33		mW
		+5V, -15V, I_{REF} = 2.0mA		108	136		108		mW
		±15V, I_{REF} = 2.0mA		135	174		135		mW

NOTES:

[1] AD DAC-08A specifications apply for the -55°C to +125°C range. The AD DAC-08C specifications apply for T_A = 0 to +70°C.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
  AD DAC-08A . . . . -55°C to +125°C
  AD DAC-08C . . . . 0 to +70°C
Storage Temperature . . . . -65°C to +150°C
  Power Dissipation 500mW
    Above 100°C Derate by . . . . 10mW/°C
$-V_S$ Supply to $+V_S$ Supply 36V
Logic Inputs. . . . . $-V_S$ to ($-V_S$ +36V)
V_{LC} . . . . $-V_S$ to $+V_S$
Reference Inputs (V_{14}, V_{15}) . . . . $-V_S$ to $+V_S$
Reference Input Differential
  Voltage (V_{14} to V_{15}). . . . . ±18V
Reference Input Current (I_{14}) 5.0mA

ANALOG DEVICES

Ultra-Low Offset Voltage Op Amp

AD OP-07 CHIPS

PRODUCT DESCRIPTION

The AD OP-07 is an improved version of the industry-standard. OP-07 precision operational amplifier. A guaranteed minimum open-loop voltage gain of 1,200,000 affords increased accuracy in high closed loop gain applications. Input offset voltages of 60μV, bias currents of 1.8nA, internal compensation and device protection eliminate the need for external components and adjustments. An input offset voltage temperature coefficient of 0.4μV/°C and long-term stability of 0.4μV/month eliminate recalibration or loss of initial accuracy. Two grades of AD OP-07 chips are specified for 0 to +70°C operation.

APPLICATION INFORMATION

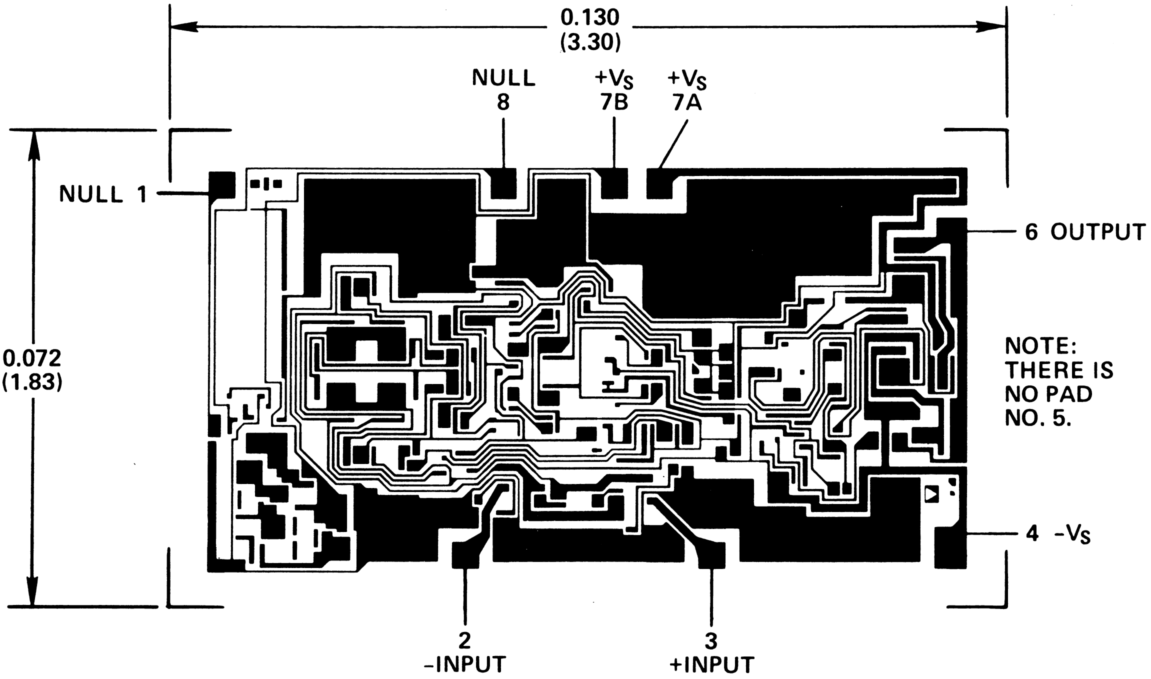
AD OP-07 chips are functionally identical to packaged AD OP-07 devices. For general application information, see the AD OP-07 packaged product catalog data sheet.

The following additional application information applies to AD OP-07 chips:

1. No particular wire-bonding sequence must be followed.
2. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
3. For performance to device specifications, the metal substrate pad or header beneath the AD OP-07 chip must be connected to $-V_S$, device pad number 4.
4. Pads 7A and 7B must *both* be connected to $+V_S$.
5. Do not connect to any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



PAD NUMBER CORRESPOND TO PIN NUMBERS FOR THE TO-99 8-PIN METAL PACKAGES.

SPECIFICATIONS[1] (T_A = +25°C, V_S = ±15V, unless otherwise specified)

Model			AD OP-07C			AD OP-07D			
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
OPEN LOOP GAIN	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm10V$	1,200	4,000		1,200	4,000		V/mV
		$R_L \geq 2k\Omega$, $V_O = \pm10V$							
		$T_A = +25°C$ to T_{max}	1,000	4,000		1,000	4,000		V/mV
		$T_A = T_{min}$ to $+25°C$		1,000			1,000		V/mV
		$R_L \geq 500\Omega$, $V_O = \pm0.5V$, $V_S = \pm3V$	300	1,000		300	1,000		V/mV
OUTPUT CHARACTERISTICS									
Maximum Output Swing	V_{OM}	$R_L \geq 10k\Omega$	±12.0	±13.0		±12.0	±13.0		V
		$R_L \geq 2k\Omega$	±11.5	±12.8		±11.5	±12.8		V
		$R_L \geq 1k\Omega$		±12.0					V
Open Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$		60			60		Ω
FREQUENCY RESPONSE									
Closed Loop Bandwidth	BW	$A_{VCL} = +1.0$		0.6			0.6		MHz
Slew Rate	SR	$R_L \geq 2k$		0.17			0.17		V/µs
INPUT OFFSET VOLTAGE									
Initial	V_{OS}	Note 2		60	150		60	150	µV
		Note 2, $T_A = +25°C$ to T_{max}		85	250		85	250	µV
		$T_A = T_{min}$ to $+25°C$		85			85		µV
Adjustment Range		$R_P = 20k\Omega$		±4			±4		mV
INPUT OFFSET CURRENT									
Initial	I_{OS}			0.8	6.0		0.8	6.0	nA
INPUT BIAS CURRENT									
Initial	I_B			±1.8	±7.0		±2.0	±12	nA
INPUT RESISTANCE									
Differential	R_{IN}		8	33		7	31		MΩ
Common Mode	R_{IN} CM			120			120		GΩ
INPUT VOLTAGE RANGE									
Common Mode	CMVR		±13.0	±14.0		±13.0	±14.0		V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm$CMVR	100	120		94	110		dB
		$V_{CM} = \pm$CMVR, T_{min} to T_{max}	97	120		94	106		dB
POWER SUPPLY									
Current, Quiescent	I_Q	$V_S = \pm15V$		3.5	5.0		3.5	5.0	mA
Power Consumption	P_D	$V_S = \pm15V$		105	150		105	150	mW
		$V_S = \pm3V$		6.0	8.4		6.0	8.4	mW
Rejection Ratio	PSRR	$V_S = \pm3V$ to $\pm18V$	90	104		90	104		dB
OPERATING TEMPERATURE RANGE	T_{min}, T_{max}		0		+70	0		+70	°C

NOTE:

[1] Electrical tests are performed at wafer prove, before the wafer is separated into individual dice. Maintaining chip performance to specification requires great care in handling and assembly.

[2] Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

Specifications subject to change without notice.

CMOS Integrated Circuit Chips

General Information

PHYSICAL CHARACTERISTICS

Die Thickness: The thickness of Analog Devices CMOS dice is 20 mils ±1 mil except dielectrically isolated CMOS, which is 20 mils ±3 mils.

Die Dimensions: The dimensions given on the specific device data sheets have a tolerance of ±3 mils.

Backing: The backside surface of Analog Devices CMOS dice is silicon (not plated). Analog Devices has determined that an unplated backing allows thinner dice, better controlled thickness, better thermal transfer and more reliable die attach. Gold backing is not available for CMOS die.

Edges: A diamond saw is used to separate wafers into dice thus providing perpendicular edges half-way through the die.

In contrast to scribed dice, this technique provides a more uniform die shape and size. The perpendicular edges facilitate handling (such as tweezer pick-up) while the uniform shape and size simplifies substrate design and die attach.

Top Surface: The top surface of the dice is covered by a layer of Phosphorous-doped-Vapox glassivation. All areas are covered except bonding pads and scribe lines.

Surface Metalization: The metalization on Analog Devices CMOS dice is aluminum. Minimum metalization thickness is 10,000Å.

Bonding Pads: All bonding pads have a minimum size of 4 mils by 4 mils. The passivation windows are 3.5 mils minimum.

VISUAL INSPECTION

All Analog Devices CMOS dice are 100% inspected to MIL-STD-883, Method 2010, Condition B. In addition, Quality Assurance performs a sample audit to the same visual criteria to an AQL of 0.65%.

PROCESS FLOW

The process flow chart for Analog Devices CMOS dice is shown on page 17–58. All CMOS dice are 100% probed to +25°C functional and dc parametic limits as per the data sheet limits for the equivalent packaged version. (See page 17–59 for the packaged product equivalent of CMOS dice). Reject die are inked.

Additionally, all CMOS dice are 100% inspected to MIL-STD-883, method 2010, condition B. Quality assurance audits to the same visual criteria to an AQL of 0.65%.

Following visual inspection, a sample of the die lot is assembled in ceramic packages and submitted to opens/shorts testing to cull out any assembled-related failures.

Following open/short testing, the remaining packaged sample is submitted to 100% temperature testing of dc parameters. The limits used are the upper temperature limits of the similar grade packaged product (see page 17–59). The lot is rejected if the temperature test PDA (percent defective allowable) is greater than 15%.

Special electrical sorts or sample plans can sometimes be accommodated at extra cost if volume warrants.

ELECTRICAL TESTS

All chips are 100% tested at wafer sort per published +25°C dc parameters for the equivalent grade packaged product (see page 17–59) before the wafer is separated into individual dice.

Additionally, a packaged sample of each die lot is submitted to hot temperature testing. A maximum PDA of 15% is required for lot acceptance by Q.A.

Maintaining chip performance to specifications requires great care in handling and assembly. The specific recommendations in this general information section are intended to assist the user in achieving specified performance of Analog Devices CMOS chips in assembled circuits.

ELECTRICAL GUARANTEES

Analog Devices CMOS chips are guaranteed to provide an 85% yield to standard packaged product data sheet performance specifications over the operating temperature range indicated on the data sheet for the equivalent packaged grade.

PACKAGING

All dice are packaged in plastic waffle packs. The quantity of dice per package depends on die size.

A sheet of anti-static paper is included in each pack.

The waffle pack is sealed in a plastic vacuum-sealed package. The package is back-filled with nitrogen.

ASSEMBLY INFORMATION

Cleaning: Each die is cleaned prior to packaging in waffle packs. No additional cleaning is recommended.

Die Inspection: All Analog Devices CMOS dice are 100% inspected to MIL-STD-883, Method 2010, Condition B.

No further inspection is required.

Die Attach: The proper method of die attach is determined by the requirements of the particular application.

When eutectic die attach is indicated, Analog Devices recommends using either a 99.99% gold or a 98% gold 2% silicon preform.

When conductive epoxy die attach is indicated, Analog Devices recommends the use of Able Bond 36-2 or equivalent.

Die attach temperature should be as low as possible and should never exceed 400°C as measured at the die-substrate interface surface. Time at 400°C shall not exceed 120 seconds.

Lead Bonding: Analog Devices recommends using thermosonic or thermo-compression bonding for users requiring gold wire. One mil 99.99% gold wire is recommended.

Analog Devices recommends using ultra-sonic bonding for users requiring aluminum wire. One mil 99% aluminum 1% silicon wire is recommended.

To prevent damage from electrostatic discharge, bond the GND pin first. If a device has both an analog and a digital ground, bond DGND first.

Electrostatic Discharge (ESD): CMOS integrated circuits may be catastrophically damaged by ESD if not handled properly.

Furthermore, subtle shifts in transistor characteristics can be caused by a more limited exposure to ESD, causing the performance of a precision device to become degraded.

To prevent damage caused by ESD, Analog Devices recommends the following:

a. Verify proper grounding of all manufacturing equipment.

b. All workers who handle the chips should be wearing a grounded conductive wrist-strap.

c. All work-in-process, especially any work with incomplete wire-bonding, should be placed on a conductive surface.

d. Dice not in use should be stored in the original waffle pack with anti-static paper.

Specific data sheets in this catalog describe the recommended bonding sequence for each CMOS device.

ORDERING INFORMATION

Analog Devices CMOS integrated circuit chips are specified in the same manner as packaged devices, except the package code letter is replaced by the word "CHIPS".

AD XXXX X CHIPS

AD	XXXX	X	CHIPS
Prefix (All IC Products)	Product Number	Grade (Single Letter)	Designates Chips

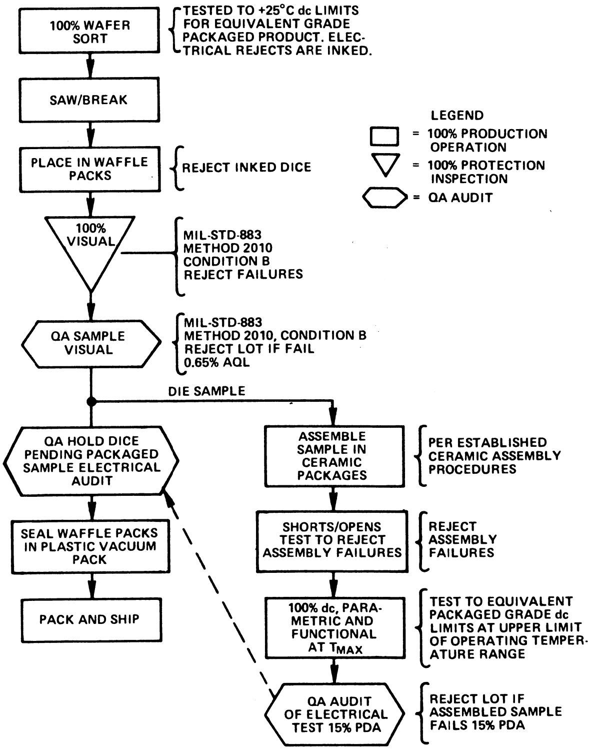
Minimum order quantity for CMOS chips is 50 pieces per line item. Additionally, Analog Devices CMOS dice are supplied in multiples of 25 pieces.

Not all packaged product generics, grades or temperature ranges can be supplied in chip form. See page 17-59 for available CMOS chips.

Bonding Diagrams: Bonding diagrams are provided for each product. Dimensions are given in inches and millimeters. See pages 17-60 through 17-65.

APPLICATIONS INFORMATION

Product descriptions, features and applications information is available for CMOS chips in the packaged product data sheets of this catalog.


100% WAFER SORT
TESTED TO +25°C dc LIMITS FOR EQUIVALENT GRADE PACKAGED PRODUCT. ELECTRICAL REJECTS ARE INKED.
SAW/BREAK
PLACE IN WAFFLE PACKS
REJECT INKED DICE
100% VISUAL
MIL-STD-883 METHOD 2010 CONDITION B REJECT FAILURES
QA SAMPLE VISUAL
MIL-STD-883 METHOD 2010, CONDITION B REJECT LOT IF FAIL 0.65% AQL
DIE SAMPLE
QA HOLD DICE PENDING PACKAGED SAMPLE ELECTRICAL AUDIT
SEAL WAFFLE PACKS IN PLASTIC VACUUM PACK
PACK AND SHIP
ASSEMBLE SAMPLE IN CERAMIC PACKAGES
PER ESTABLISHED CERAMIC ASSEMBLY PROCEDURES
SHORTS/OPENS TEST TO REJECT ASSEMBLY FAILURES
REJECT ASSEMBLY FAILURES
100% dc, PARAMETRIC AND FUNCTIONAL AT T_{MAX}
TEST TO EQUIVALENT PACKAGED GRADE dc LIMITS AT UPPER LIMIT OF OPERATING TEMPERATURE RANGE
QA AUDIT OF ELECTRICAL TEST 15% PDA
REJECT LOT IF ASSEMBLED SAMPLE FAILS 15% PDA
LEGEND
= 100% PRODUCTION OPERATION
= 100% PROTECTION INSPECTION
= QA AUDIT

ANALOG DEVICES CMOS INTEGRATED CIRCUIT CHIP PROCESS FLOW DIAGRAM "COM" PROCESS

CMOS CHIP AVAILABLE

Due to limitations imposed on testing and grading devices in chip form, not all packaged product grades or temperature ranges are available at this time as standard product.

Following is a list of CMOS chip standard product offerings which are presently available. Refer to the packaged-product data sheet shown to determine the chip's dc performance characteristics.

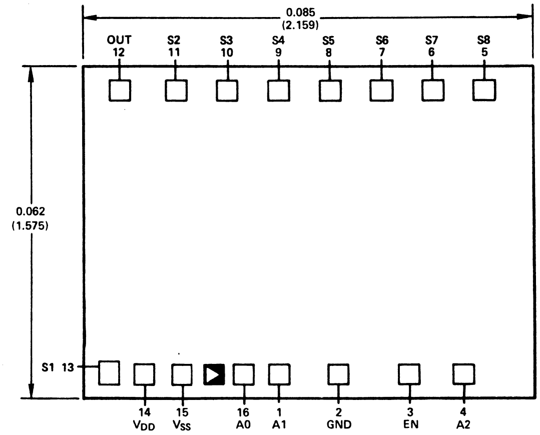
LEADLESS CHIP CARRIERS FOR FULLY TESTED AND GUARANTEED PERFORMANCE

Due to test limitations, it is often difficult (or impossible) to provide the exhaustive testing required to guarantee chips to the equivalent grade packaged-product performance over the MILITARY temperature range.

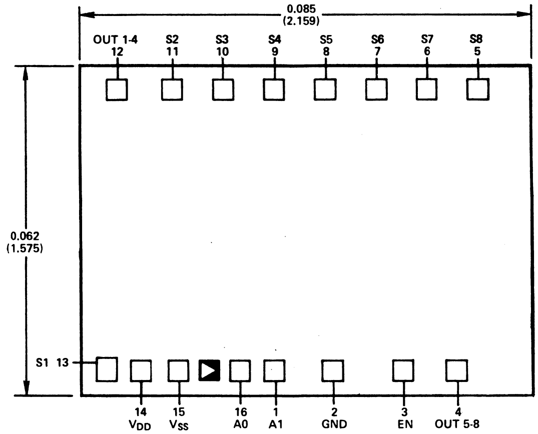
Consequently, Analog Devices offers many CMOS devices packaged in leadless chip carriers. Chip carriers offer the advantage of fully specified, 100% tested, guaranteed performance in a package not much larger than the chip itself. Contact Analog Devices for further information on products available in chip carriers.

Chip Model Number	**Equivalent Packaged Product to Determine dc Performance (Vol. I)**	**Operating Temperature Range for Rated dc Performance**
CMOS MULTIPLEXERS		
AD7501 J CHIP	AD7501JD ; page 16-5	-25°C to +85°C
AD7502 J CHIP	AD7502JD ; page 16-5	-25°C to +85°C
AD7503 J CHIP	AD7503JD ; page 16-5	-25°C to +85°C
AD7506 J CHIP	AD7506JD ; page 16-9	-25°C to +85°C
AD7507 J CHIP	AD7507JD ; page 16-9	-25°C to +85°C
CMOS SWITCHES		
AD7510DI J CHIP	AD7510DIJD ; page 16-13	-25°C to +85°C
AD7511DI J CHIP	AD7511DIJD ; page 16-13	-25°C to +85°C
AD7512DI J CHIP	AD7512DIJD ; page 16-13	-25°C to +85°C
AD7590DI B CHIP	AD7590DIBD ; page 16-21	-25°C to +85°C
AD7591DI B CHIP	AD7591DIBD ; page 16-21	-25°C to +85°C
AD7592DI B CHIP	AD7592DIBD ; page 16-21	-25°C to +85°C
CMOS D/A CONVERTERS		
AD7520 J CHIP	AD7520JD ; page 10-97	-25°C to +85°C
AD7520 K CHIP	AD7520KD ; page 10-97	-25°C to +85°C
AD7520 L CHIP	AD7520LD ; page 10-97	-25°C to +85°C
AD7521 J CHIP	AD7521JD ; page 10-97	-25°C to +85°C
AD7521 K CHIP	AD7521KD ; page 10-97	-25°C to +85°C
AD7521 L CHIP	AD7521LD ; page 10-97	-25°C to +85°C
AD7522 J CHIP	AD7522JD ; page 10-105	-25°C to +85°C
AD7522 L CHIP	AD7522LD ; page 10-105	-25°C to +85°C
AD7523 J CHIP	AD7523JN ; page 10-111	0 to +70°C
AD7524 A CHIP	AD7524AD ; page 10-115	-25°C to +85°C
AD7523 A CHIP	AD7533AD ; page 10-151	-25°C to +85°C
AD7533 B CHIP	AD7533BD ; page 10-151	-25°C to +85°C
AD7541 A CHIP	AD7541AD ; page 10-157	-25°C to +85°C
AD7541 B CHIP	AD7541BD ; page 10-157	-25°C to +85°C
AD7542 A CHIP	AD7542AD ; page 10-165	-25°C to +85°C
AD7542 B CHIP	AD7542BD ; page 10-165	-25°C to +85°C
AD7543 A CHIP	AD7543AD ; page 10-173	-25°C to +85°C
AD7543 B CHIP	AD7543BD ; page 10-173	-25°C to +85°C
CMOS A/D CONVERTERS		
AD7550 B CHIP	AD7550BD ; page 11-81	-25°C to +85°C
AD7574 A CHIP	AD7574AD ; page 11-113	-25°C to +85°C

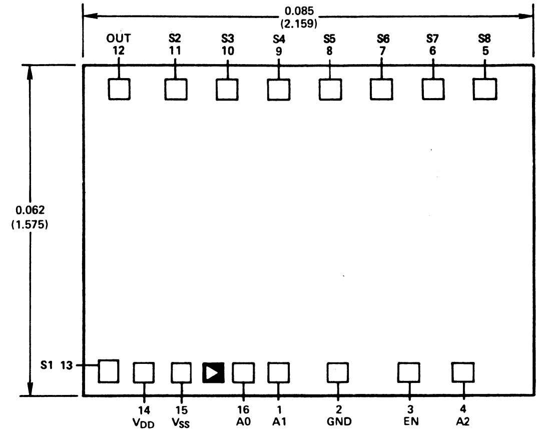
BONDING DIAGRAMS



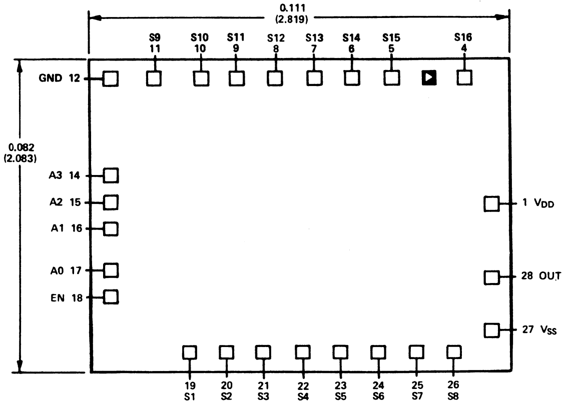
AD7501



AD7502



AD7503

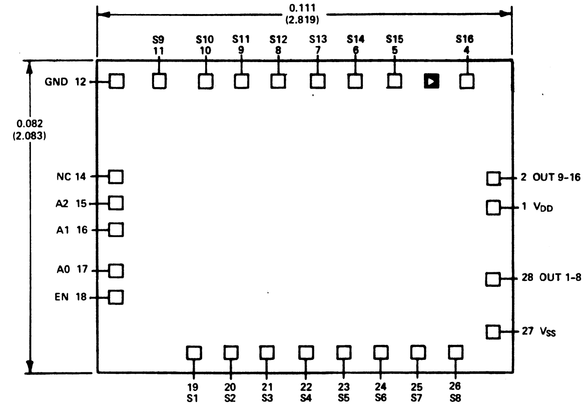


PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE 28 PIN DIP PACKAGE.

AD7506

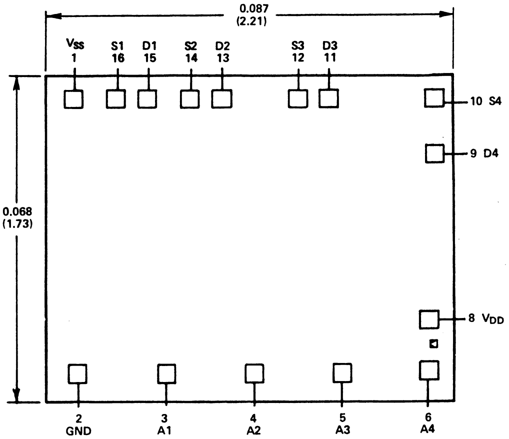
**LINES FROM BONDING PADS IN ALL DIAGRAMS
DO NOT INDICATE BOND WIRES**

BONDING DIAGRAMS



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE 28 PIN DIP PACKAGE.

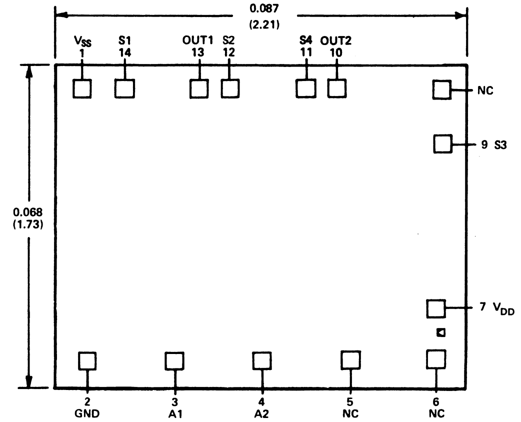
AD7507



NOTE: AD7510DI: SWITCH "ON" FOR ADDRESS "HIGH"
AD7511DI: SWITCH "ON" FOR ADDRESS "LOW"

PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE 16 PIN DIP PACKAGE.

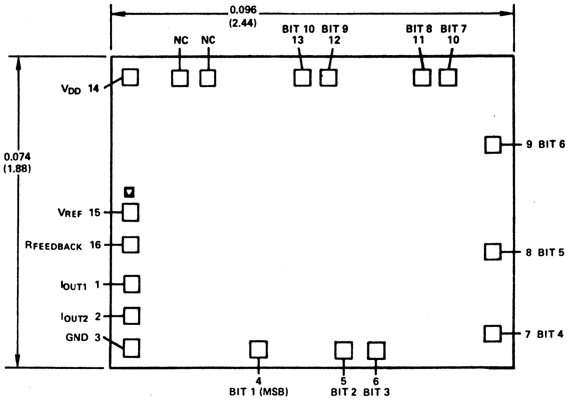
AD7510, 11



NOTE: AD7512DI: ADDRESS "HIGH" MAKES
S1 TO OUT1 AND S3 TO OUT2

PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE 16 PIN DIP PACKAGE.

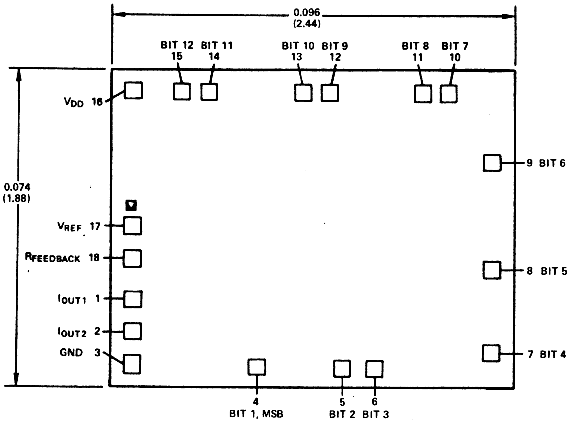
AD7512



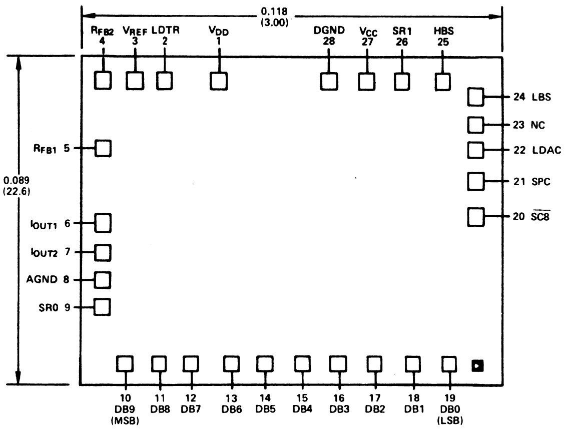
AD7520

**LINES FROM BONDING PADS IN ALL DIAGRAMS
DO NOT INDICATE BOND WIRES**

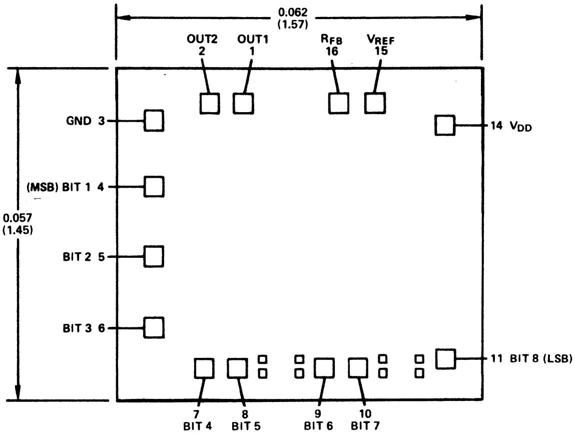
BONDING DIAGRAMS



AD7521

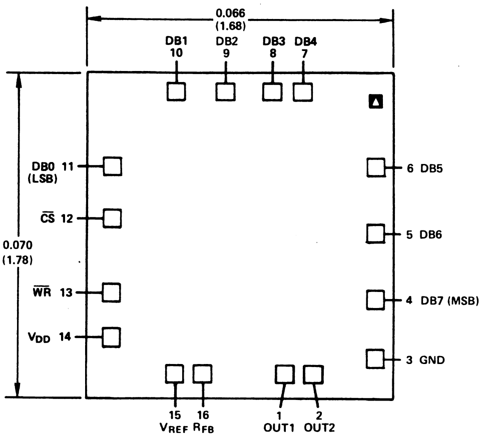


AD7522



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE 16 PIN DIP PACKAGE.

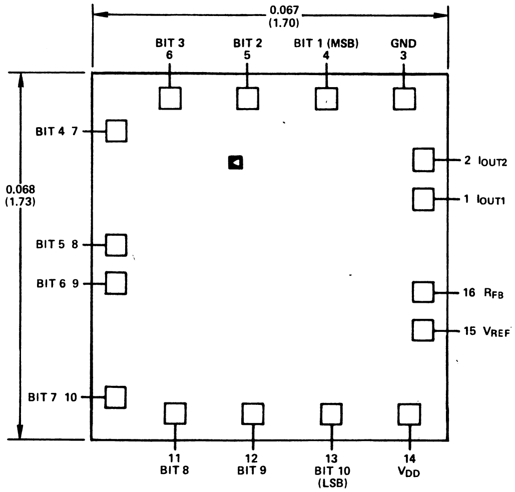
AD7523



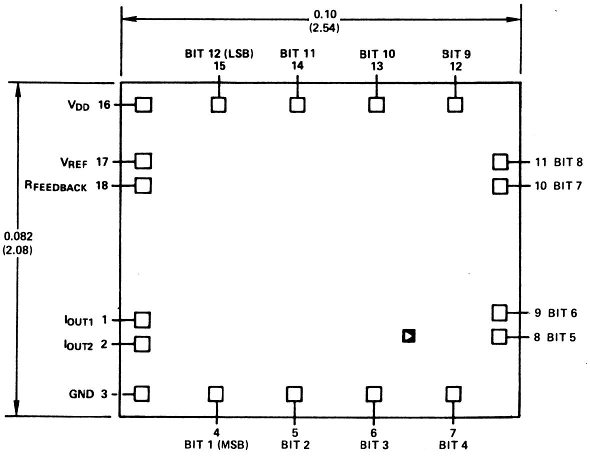
AD7524

LINES FROM BONDING PADS IN ALL DIAGRAMS
DO NOT INDICATE BOND WIRES

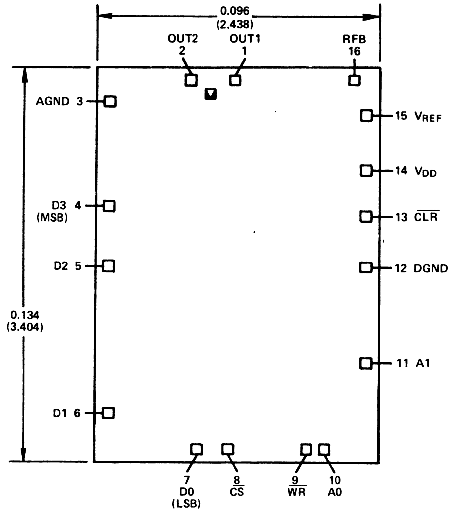
BONDING DIAGRAMS



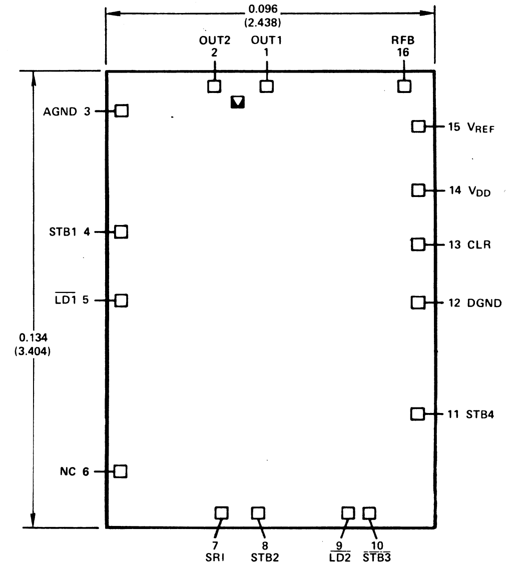
AD7533



AD7541



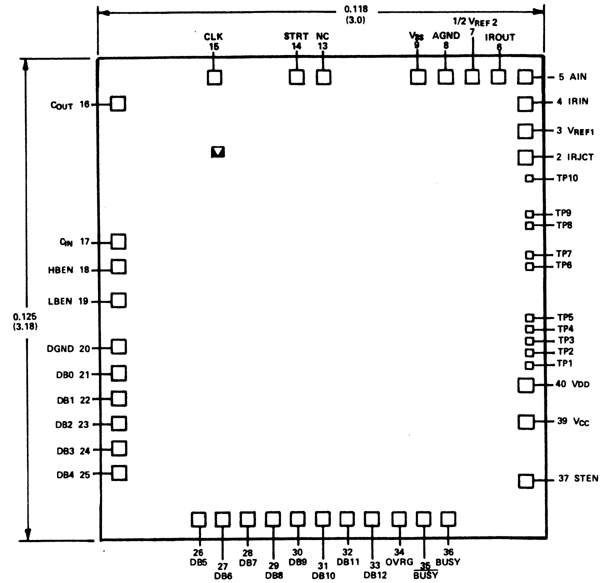
AD7542



AD7543

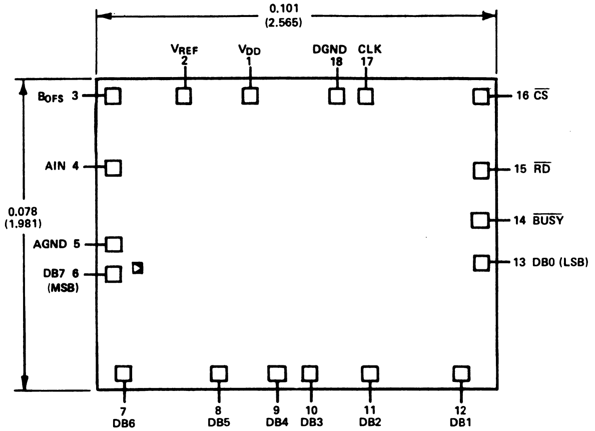
LINES FROM BONDING PADS IN ALL DIAGRAMS
DO NOT INDICATE BOND WIRES

BONDING DIAGRAMS



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE 40 PIN DIP PACKAGE.

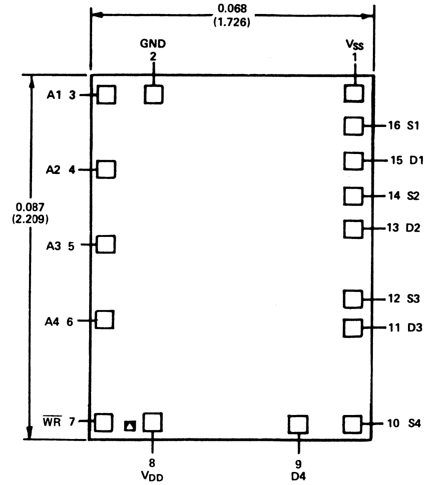
AD7550



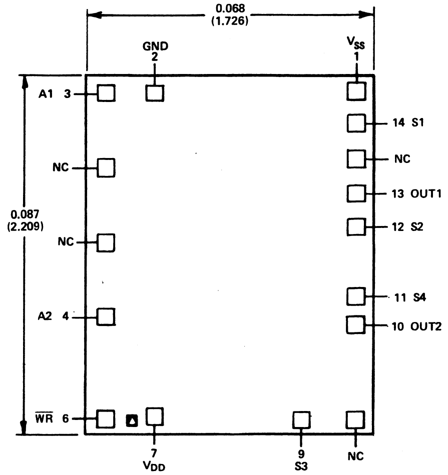
AD7574

**LINES FROM BONDING PADS IN ALL DIAGRAMS
DO NOT INDICATE BOND WIRES**

BONDING DIAGRAMS



AD7590, 91



AD7592

LINES FROM BONDING PADS IN ALL DIAGRAMS DO NOT INDICATE BOND WIRES

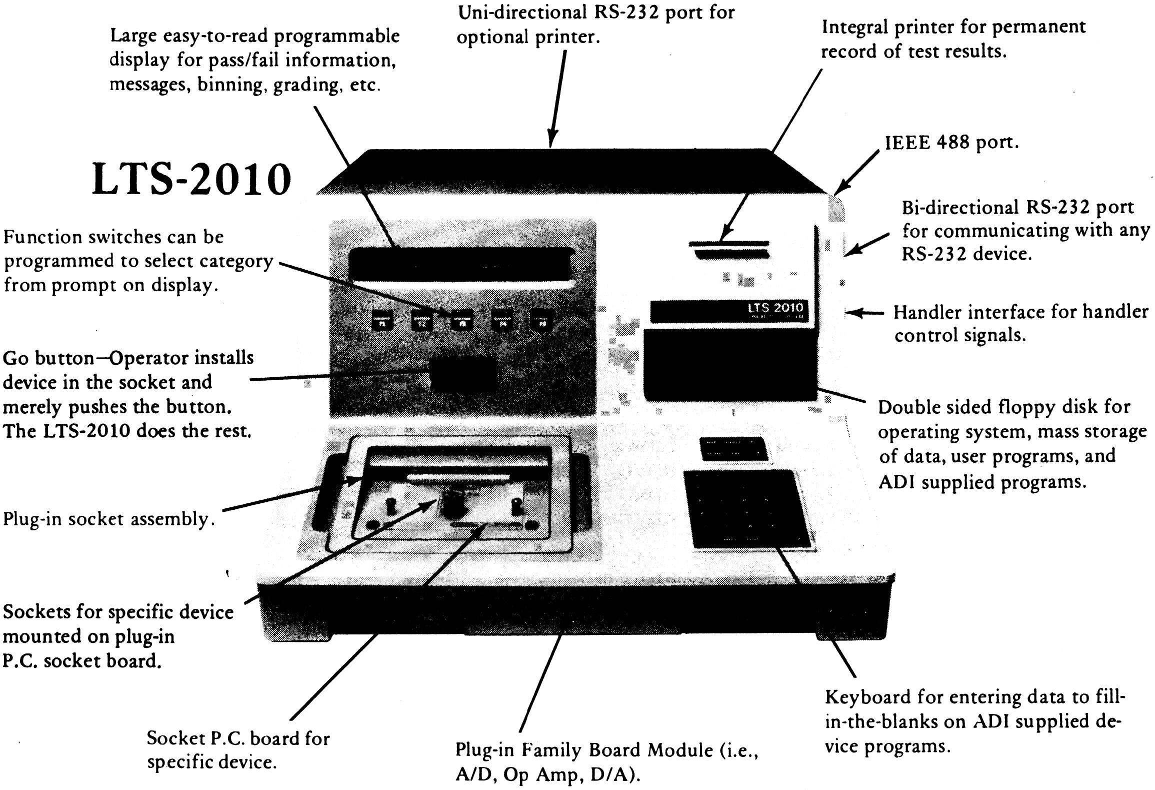
Linear IC Test Systems

Contents

	Page
The LTS System Concept	18-3
LTS-2000	18-3
LTS-2010	18-4
LTS Specifications	18-4

Linear IC Test Systems

TEST OP AMPS, DACs & ADCs WITH 16-BIT ACCURACY


Uni-directional RS-232 port for optional printer.
Large easy-to-read programmable display for pass/fail information, messages, binning, grading, etc.
Integral printer for permanent record of test results.
IEEE 488 port.
LTS-2010
Bi-directional RS-232 port for communicating with any RS-232 device.
Function switches can be programmed to select category from prompt on display.
LTS 2010
Handler interface for handler control signals.
Go button—Operator installs device in the socket and merely pushes the button. The LTS-2010 does the rest.
Double sided floppy disk for operating system, mass storage of data, user programs, and ADI supplied programs.
Plug-in socket assembly.
Sockets for specific device mounted on plug-in P.C. socket board.
Keyboard for entering data to fill-in-the-blanks on ADI supplied device programs.
Socket P.C. board for specific device.
Plug-in Family Board Module (i.e., A/D, Op Amp, D/A).

THE LTS SYSTEM CONCEPT
The LTS systems are easy-to-use, flexible component test systems that allow you to test any component to the manufacturer's own specifications, ADCs, DACs, op amps, regulators, comparators and other linear devices. The system also offers such features as datalogging, statistical analysis, yield analysis and two RS-232 interfaces, IEEE interface and a handler interface.

The computing power of the LTS-systems lies in their 16-bit central processing unit. The microprocessor incorporates a minicomputer instruction set which includes hardware multiply and divide as well as 15 prioritized interrupts for the system keypad, function switches, floppy disk drive, and the IEEE 488 interface.

A real time, 3MHz, four-phase crystal stabilized system clock generates system timing, allowing the implementation of a real time clock. The system memory includes 60K bytes of dynamic RAM, of which 32K bytes are available for program generation by the user.

The LTS-systems not only provide for several data output formats—data log, yield analysis or statistical analysis—they also provide a choice of data display. If desired, the data may be presented via the single line LED display, the integral 20-column thermal printer, through either of the RS-232 ports or the IEEE port. (All data outputs are standard features on both the LTS-2000 and the LTS-2010.)

LTS-2000
The LTS-2000 is far more than a simple tester; it is an optimal low cost solution for incoming inspection. It can be used for basic GO/NO-GO testing, for component selection, for qualification testing, or as a diagnostic tool for component evaluation.

The LTS-2000 can be set up in minutes by using either a program from the device library, or the complete test menu of "Fill-in-the-Blanks" software. Prompts for each step of the "Fill-in-the-Blanks" test programs are conveniently displayed directly over the associated function switches. Standard test programs can be easily altered to suit your needs. Select your test, and arrange them in the order you prefer. The full edit capability enables you to change test parameters quickly and simply.

LTS-2010

The LTS-2010 is the first benchtop tester that's programmable in BASIC, as well as "Fill-in-the-Blanks" programming, and its 16-bit CPU and 64K bytes of memory offer a new level of programmable sophistication.

Far more than just a comprehensive production tester, it can handle complex engineering analysis, and even incoming inspection. It is the first system that can provide all the capabilities of today's large, centralized test systems at a cost that is approximately one-third the "big system" price.

The LTS-2010 not only provides the flexibility of distributed or decentralized testing, it allows for cost-effective multiple system purchases. And it increases overall test reliability, since the threat of a single big system failure is eliminated in a distributed testing environment.

LTS SPECIFICATIONS

MEASUREMENT ACCURACY

High Accuracy	±(0.0015% of Reading +0.025% of Range +100μV)
Direct	±(0.025% of Reading +0.025% of Range +100μV)
Null and Difference	±(0.025% of Reading +0.025% of [Diff Range + Null Range] +100μV)
Input Voltage Range	±10V (64 Different Ranges)

REFERENCE DAC

Range	Resolution	Software Corrected Accuracy
0 to 10V	2.5mV	RDVO ± 150μV
-5V to 5V	2.5mV	RDVO ± 150μV
-10V to 10V	5mV	RDVO ± 300μV

SYSTEM REFERENCE

Short Term	10V Adjustable in hardware or software
Long Term	10V ±50ppm/1000 hrs, noncumulative

SOURCES

Source	Voltage Range	Resolution	Software Corrected Accuracy
SA	0 to 20V	±0.1V	SAVO ± 0.05V
SB	0 to 20V	±0.1V	SBVO ± 0.05V
SC	0 to -20V	±0.1V	SCVO ± 0.05V
SD	0 to -20V	±0.1V	SDVO ± 0.05V
TH	0 to 10V	±0.05V	THVO ± 0.025V
SR	-10V to 10V	±0.001V	SRVO ± 0.0005V

Source	Current Range	Accuracy of Measurement
SA	-10mA to 150mA	±(2.5% of Reading + 10μA/V + 15μA)
SB	-10mA to 150mA	±(2.5% of Reading + 10μA/V + 15μA)
SC	10mA to -150mA	±(2.5% of Reading + 10μA/V + 15μA)
SD	10mA to -150mA	±(2.5% of Reading + 10μA/V + 15μA)
TH	-10mA to +10mA	±(0.5% of Reading + 10μA)
SR	-10mA to +10mA	±(0.5% of Reading + 10μA)

OPERATING TEMPERATURE

At Rated Accuracy after 1 hr warm-up
0 to 40°C
32°F to 104°F

OPERATING VOLTAGE

105V ac to 125V ac @ 50Hz to 60Hz
210V ac to 250V ac @ 50Hz to 60Hz

Quality Assurance Program

MIL-STD-883 Class B

Contents

	Page
Introduction	19-3
MIL-STD-883, Method 5004, Class B Product Flow-Semiconductor Products	19-4
MIL-STD-883, Method 5008 Product Flow-Hybrid Products	19-7
Bipolar Integrated Circuits Processed to MIL-STD-883, Method 5004, Class B	19-10
CMOS Integrated Circuits Processed to MIL-STD-883, Method 5004, Class B	19-11
Hybrid Circuits, Manufactured at the Microelectronics Division, Processed to MIL-STD-883, Method 5008	19-12
Hybrid Circuits, Manufactured at the Computer Labs Division, Processed to MIL-STD-883, Method 5008	19-12

INTRODUCTION

This section establishes the requirements for screening integrated circuits at Analog Devices in accordance with MIL-STD-883, Class B. Our monolithic and hybrid ICs are subjected to the accelerated stress tests or Methods 5004 and 5008 respectively.

The following specifications and test methods of the issue in effect provides the general requirements and test procedures for the manufacture, test and environmental standards of our 883B program.

MIL-M-38510: General Specification of Microcircuits.

MIL-STD-883: Test Methods and Procedures for Microelectronics.

Table 1 and Table 2 outline the screening tests for Analog Devices' MIL Program. The purpose of these tests is to assure the quality and reliability of the product to a particular process level commensurate with the product's intended application.

Table 1 outlines the test sequence used in the reliability screening of our monolithic ICs.

TABLE 1

Test	Method
1) Internal Visual (Pre-Cap)	Method 2010, Test Condition B
2) Stabilization Bake	Method 1008, 24 hrs. @ + 150°C, or equivalent
3) Temperature Cycling	Method 1010, Test Condition C, 10 Cycles, − 65°C to + 150°C
4) Constant Acceleration	Method 2001, Test Condition E, Y1 plane, 30,000G
5) Seal Test: Fine Leak	Method 1014, Test Condition A or B
Gross Leak	Method 1014, Test Condition C
6) Burn-In Test	Method 1015, per applicable device specification 160 hrs. @ + 125°C min
7) Final Electrial Tests	Per applicable device specification
8) External Visual	Method 2009

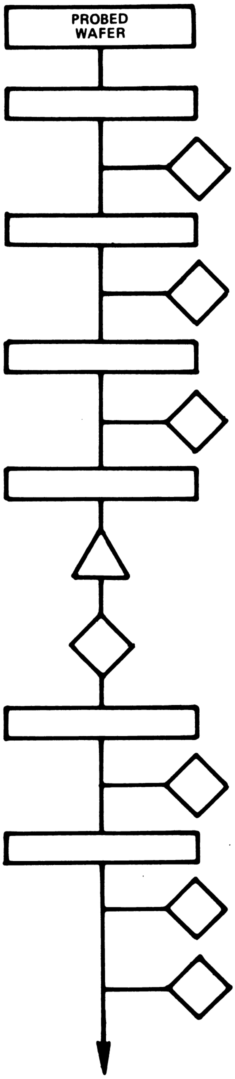
Table 2 outlines the test sequence used in the reliability screening of our hybrid ICs to Method 5008.

TABLE 2

Process	Method
1) 100% Pre-Cap Visual Inspection	Method 2017
2) Stabilization Bake	Method 1008, 24hrs. @ + 150°C, Condition C
3) Temperature Cyle	Method 1010, Test Condition C, 10 Cycles, − 65°C to + 150°C
4) Constant Acceleration	Method 2001, Y1 plane, per applicable device specification
5) Visual Inspection	Visible Damage
6) Seal Test: Fine Leak	Method 1014, Test Condition A or B
Gross Leak	Method 1014, Condition C
7) Operating Burn-In	Method 1015, per applicable device specification, 160 hrs @ + 125°C
8) Final Electrical Test	Per applicable device specification
9) External Visual Inspection	Method 2009

MIL-STD-883, METHOD 5004, CLASS B
PRODUCT FLOW SEMICONDUCTOR PRODUCTS

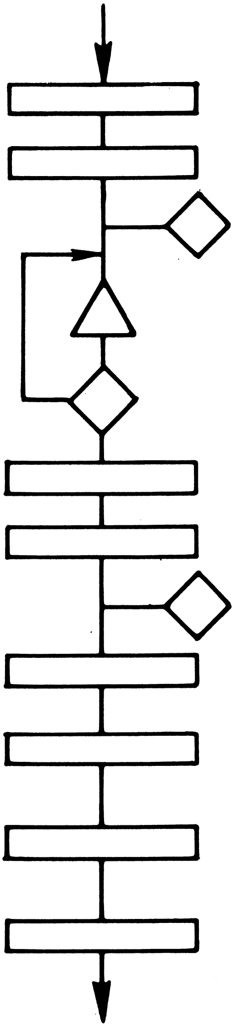
Process Flow



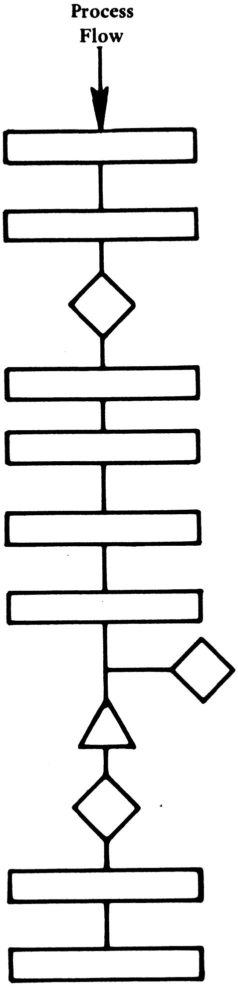
Operation Description	Bipolar Integrated Circuits	CMOS Integrated Circuits
Wafer Trim (Applicable Products)	X	X
Monitor Wafer Trim	X	X
Wafer Probe	X	X
Monitor Wafer Probe	X	X
Saw/Scribe and Break	X	X
Monitor Saw/Scribe	X	X
Dice Sort	X	X
Dice Visual Inspection	X	X
Dice Lot Acceptance, MIL-STD-883, Method 2010, Condition B	X	X
Die Mount	X	X
Monitor Die Mount	X	X
Wire Bond	X	X
Monitor Wire Bond (Visual)	X	X
Monitor Wire Bond (Mechanical)	X	X

Legend: ▭ Manufacturing Operation △ Manufacturing Inspection ◇ Quality Control Inspection

Process Flow



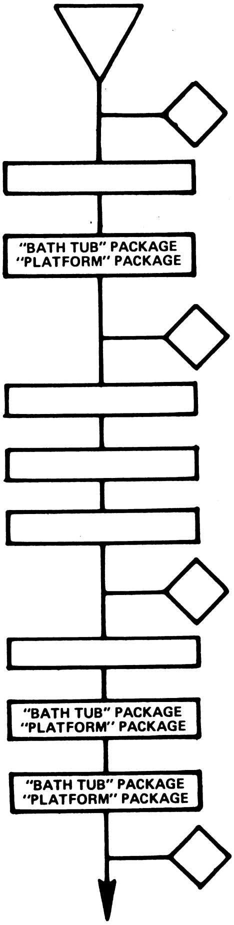
Operation Description	Bipolar Integrated Circuits	CMOS Integrated Circuits
Pre-Trim Bake (Package Trimmed Products)	X	N/A
Trim (Package Trimmed Products)	X	N/A
Monitor Laser Trim	X	N/A
Visual Inspection	X	X
Q.C. Precap Visual 1% AQL, MIL-STD-883, Method 2010, Test Condition B	X	X
Stabilization Bake	X	N/A
Cap/Seal	X	X
Monitor Cap/Seal	X	X
Electrical Testing, $T_A = 25^\circ C$, T_{min}, T_{max}	X	X
Stabilization Bake 24 hrs. at +150°C, Method 1008	X	X
Temperature Cycle, Method 1010, Test Condition C, 10 Cycles, -65°C to +150°C	X	X
Constant Acceleration, Method 2001, Test Condition E, Y1 plane 30,000G	X	X



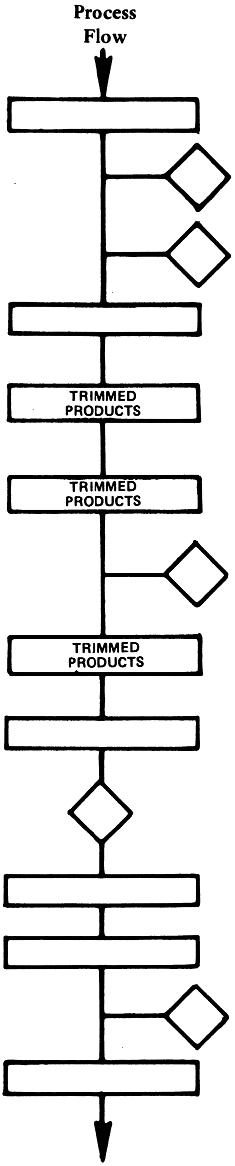
Operation Description	Bipolar Integrated Circuits	CMOS Integrated Circuits
Fine Leak Test, Method 1014, Test Condition A	X	X
Gross Leak Test, Method 1014, Test Condition C	X	X
Q. C. Data Review	X	X
Pre-Burn-In Electrical Test (Optional)	X	X
Burn-In Test, Method 1015, 160 hrs. at 125°C	X	X
Final Electrical Test, $T_A = 25°C$, T_{min} and T_{max}	X	X
Brand and Cure	X	X
Monitor Brand	X	X
100% External Visual	X	X
Q. C. Lot Acceptance, Method 2009	X	X
Transfer to Bonded Stock	X	X
Ship to Customer	X	X

MIL-STD-883, METHOD 5008
PRODUCT FLOW HYBRID PRODUCTS

Process Flow

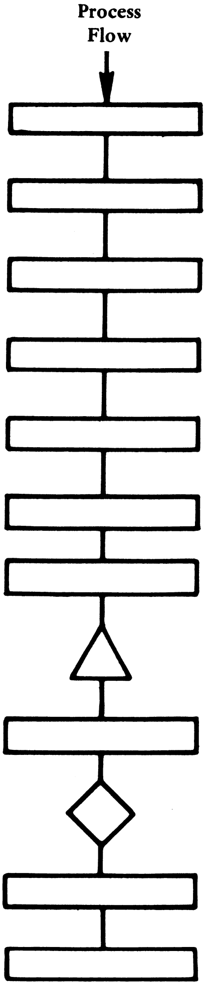


Operation Description	Microelectronics Division Suffix "883" Components	Computer Labs Division Suffix "B" or "883" Components
Direct Material, 100% Tested at Wafer Level	X	X
Q. C. Sample Inspection of Incoming Material	N/A	X
Kit Preparation and Issue	X	X
Thick Film Substrate/Package Preparation for Al or Au Wire Bonding	X	X
Kit Inspection	X	X
Remove Lead Frame	X	N/A
Adhesive Application	X	X
Die Attach	X	X
Q. C. Monitor	X	N/A
Adhesive Cure	X	X
Substrate Attach	X	X
Adhesive Cure	X	X
Q. C. Monitor	X	N/A



Operation Description	Microelectronics Division Suffix "883" Components	Computer Labs Division Suffix "B" or "883" Components
Wire Bond	X	X
Monitor Wire Bond	X	N/A
Pre-Cap Visual	N/A	X
Functional Test	X	X
Burn-In	X	N/A
Laser Trim	X	X
Q. C. Monitor (Trimmed Products)	X	X
Pre-Seal Functional Test	X	N/A
Pre-Seal Visual	X	N/A
Q. C. Pre-Seal Visual, Method 2017	X	X
Pre-Seal Bake	X	X
Seal	X	X
Q. C. Monitor	X	N/A
Stabilization Bake, Method 1008, 24 hrs. at +150°C, Condition C	X	N/A

Process Flow



Operation Description	Microelectronics Division Suffix "883" Components	Computer Labs Division Suffix "B" or "883" Components
Temperature Cycle, Method 1010, Test Condition C, 10 Cycles	X (-65°C to +150°C)	X (-55°C to +125°C)
Constant Acceleration, Method 2001, Y1 plane, per Applicable Device Specification	X	X
Fine Leak, Method 1014, Test Condition A or B	X	X
Gross Leak, Method 1014, Test Condition C	X	X
Operating Burn-In, Method 1015, 160 hrs. at +125°C	X	X (At Max Operating Temperature)
Final Electrical Tests	X	X
Brand and Cure	X	X
External Visual, Method 2009	X	X
Pack	X	X
Outgoing Q. A. Lot Acceptance	X	N/A
Transfer to Bonded Stock	X	X
Ship to Customer	X	X

The products listed in the following tables meet the requirements of MIL-STD-883, Methods 5004 and 5008, Class B. The tables only include products described in this catalog, other products are available. Please contact your local salesman for information.

BIPOLAR INTEGRATED CIRCUITS PROCESSED TO MIL-STD-883, METHOD 5004, CLASS B

AD503SH/883B
AD504SH/883B
AD506SH/883B
AD507SH/883B
AD509SH/883B
AD510SH/883B

AD517SH/883B
AD518SH/883B
AD521SD/883B
AD524SD/883B
AD532SH/883B
AD533SD/883B

AD533SH/883B
AD534SD/883B
AD534SH/883B
AD534TD/883B
AD534TH/883B
AD536ASD/883B

AD536ASH/883B
AD537SD/883B
AD537SH/883B
AD539SD/883B
AD542SH/883B
AD544SH/883B

AD547SH/883B
AD558SD/883B
AD558TD/883B
AD561SD/883B
AD561TD/883B
AD562SD/BCD/883B

AD562SD/BIN/883B
AD563SD/BCD/883B
AD563SD/BIN/883B
AD563TD/BCD/883B
AD563TD/BIN/883B
AD565ASD/883B

AD565ATD/883B
AD565SD/883B
AD565TD/883B
AD566ASD/883B
AD566ATD/883B
AD566SD/883B

AD566TD/883B
AD570SD/883B
AD571SD/883B
AD573SD/883B
AD574ASD/883B
AD574ATD/883B

AD574AUD/883B
AD580SH/883B
AD580TH/883B
AD580UH/883B
AD581SH/883B
AD581TH/883B

AD581UH/883B
AD582SD/883B
AD582SH/883B
AD584SH/883B
AD584TH/883B
AD589SH/883B

AD589TH/883B
AD589UH/883B
AD590JF/883B
AD590JH/883B
AD590KF/883B
AD590KH/883B

AD590LF/883B
AD590LH/883B
AD590MF/883B
AD590MH/883B
AD642SH/883B
AD644SH/883B

AD647SH/883B
AD650SD/883B
AD673SD/883B
AD741SH/883B
AD1508-8D/883B
AD1508-9D/883B

AD DAC08AD/883B
AD DAC08D/883B
AD OP-07AH/883B
AD OP-07H/883B
ADVFC32SD/883B
ADVFC32SH/883B

CMOS INTEGRATED CIRCUITS PROCESSED TO MIL-STD-883, METHOD 5004, CLASS B

AD7111TD/883B
AD7111UD/883B
AD7118TD/883B
AD7118UD/883B
AD7501SD/883B
AD7502SD/883B

AD7503SD/883B
AD7506SD/883B
AD7506TD/883B
AD7507SD/883B
AD7507TD/883B
AD7510DISD/883B

AD7511DISD/883B
AD7511DITD/883B
AD7512DISD/883B
AD7512DITD/883B
AD7520SD/883B
AD7520TD/883B

AD7520UD/883B
AD7521SD/883B
AD7521TD/883B
AD7521UD/883B
AD7522SD/883B
AD7522TD/883B

AD7522UD/883B
AD7524SD/883B
AD7524TD/883B
AD7524UD/883B
AD7525TD/883B
AD7525UD/883B

AD7527GUD/883B
AD7527TD/883B
AD7527UD/883B
AD7528SD/883B
AD7528TD/883B
AD7528UD/883B

AD7533SD/883B
AD7533TD/883B
AD7533UD/883B
AD7541SD/883B
AD7541TD/883B
AD7542SD/883B

AD7542TD/883B
AD7543SD/883B
AD7543TD/883B
AD7544GTD/883B
AD7544SD/883B
AD7544TD/883B

AD7545GUD/883B
AD7545SD/883B
AD7545TD/883B
AD7545UD/883B
AD7574SD/883B
AD7574TD/883B

ADG200AA/883B
ADG201AP/883B

HYBRID CIRCUITS, MANUFACTURED AT THE MICROELECTRONICS DIVISION, PROCESSED TO MIL-STD-883, METHOD 5008

AD346SD/883B
AD362SD/883B
AD363SD/883B
AD364SD/883B
AD364TD/883B
AD370SD/883B

AD371SD/883B
AD380SH/883B
AD381SH/883B
AD382SH/883B
AD390SD/883B
AD522SD/883B

AD572SD/883B
AD579TD/883B
AD579ZTD/883B
AD2700SD/883B
AD2700UD/883B
AD2701SD/883B

AD2701UD/883B
AD2702SD/883B
AD2702UD/883B
AD3554SH/883B
AD3860SD/883B
AD5201TD/883B

AD5202TD/883B
AD5204TD/883B
AD5205TD/883B
AD5211TD/883B
AD5212TD/883B
AD5214TD/883B

AD5215TD/883B
AD5240SD/883B
AD5240ZSD/883B
AD ADC85S-10/883B
AD ADC85S-12/883B
AD ADC85SZ-10/883B

AD ADC85SZ-12/883B
AD DAC85MIL-CBI-I/883B
AD DAC85MIL-CBI-V/883B
AD DAC87-CBI-I/883B
AD DAC87-CBI-V/883B

HYBRID CIRCUITS, MANUFACTURED AT THE COMPUTER LABS DIVISION, PROCESSED TO MIL-STD-883, METHOD 5008

ADLH0032G/883
ADLH0033G/883
ADSHC-85ET/883
HAS-0802MB
HAS-1002MB
HAS-1202MB

HDD-0810MB
HDD-0810CMB
HDD-1015MB
HDD-1015CMB
HDD-1206SM/883
HDG-0405/883

HDG-0605/883
HDG-0805/883
HDH-0802MB
HDH-1003MB
HDH-1205MB
HDS-0810EMB

HDS-0820MB
HDS-1015EMB
HDS-1025MB
HDS-1240EMB
HDS-1250AB
HOS-050AB

HOS-050B
HOS-100SH/883
HTC-0300MB
HTS-0025MB

Package Information

Page

2-Pin Packages
H2A 20–2
F2A 20–2

3-Pin Packages
TO-5 20–2
TO-52 20–2

8-Pin Packages
TO-99 20–3
H08A (TO-99 Style) 20–3
H08B (TO-99 Style) 20–3
H08C (TO-3 Style) 20–3
N8A 20–3

10-Pin Package
TO-100 20–3

12-Pin Package
H12A (TO-8 Style) 20–3

14-Pin Packages
D14A 20–4
D14B 20–4
N14A 20–4
N14B 20–4
Q14A 20–4
HY14A 20–5
HY14B 20–5
HY14C 20–5
HY14D 20–5

16-Pin Packages
D16A 20–6
D16B 20–6
N16A 20–6
N16B 20–6
Q16A 20–6
Q16B 20–6

18-Pin Packages
D18A 20–7
D18B 20–7
N18A 20–7
N18B 20–7
Q18A 20–7
HY18A 20–8

Page

20-Pin Packages
D20A 20–8
D20B 20–8
N20A 20–9
N20B 20–9
Q20B 20–9
HY20A 20–9

24-Pin Packages
D24A 20–10
N24A 20–10
HY24A 20–10
HY24B 20–10
HY24C 20–11
HY24D 20–11
HY24E 20–11
HY24G 20–11

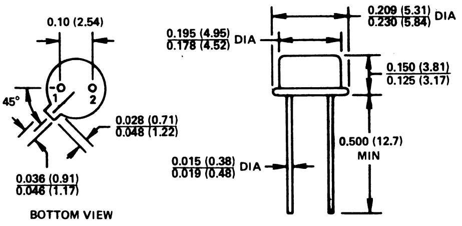
28-Pin Packages
D28A 20–12
D28B 20–12
N28A 20–12
HY28A 20–13
HY28B 20–13

32-Pin Packages
HY32A 20–13
HY32C 20–13
HY32D 20–14
HY32E 20–14
HY32F 20–14
HY32G 20–14
HY32H 20–15

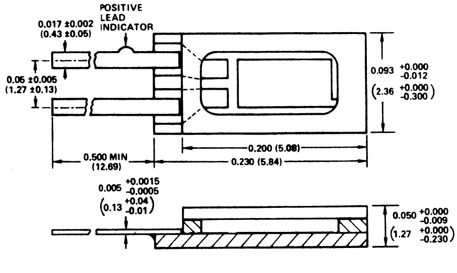
40-Pin Packages
D40A 20–15
N40A 20–15

2-PIN PACKAGES

H2A
2-Lead Metal Can Package

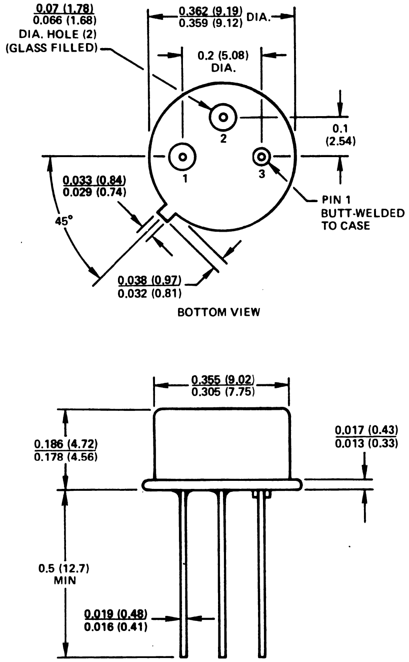


F2A
2-Lead Flat Package

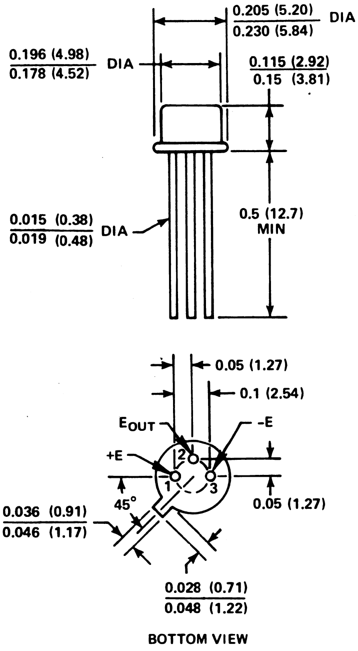


3-PIN PACKAGES

TO-5 Package



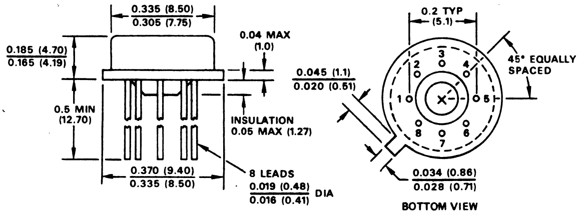
TO-52 Package



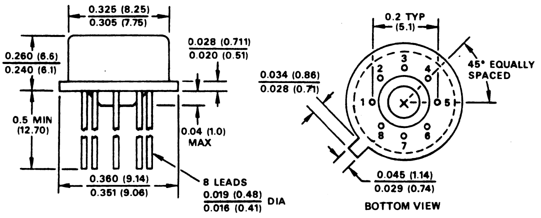
Dimensions shown in inches and (mm).
Lead No. 1 Identified by Dot or Notch.

8-PIN PACKAGES

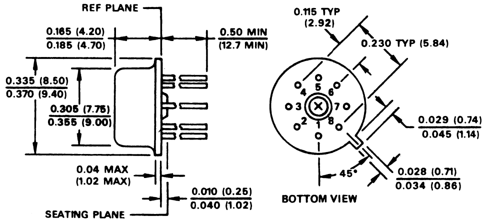
TO-99 Package



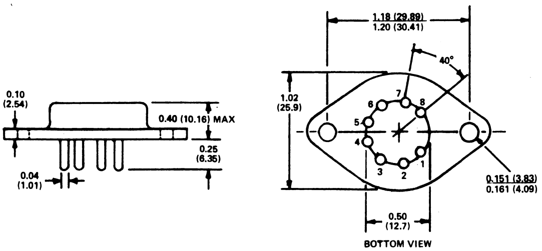
H08A Package (TO-99 Style)
(JEDEC REF MO-002AB)



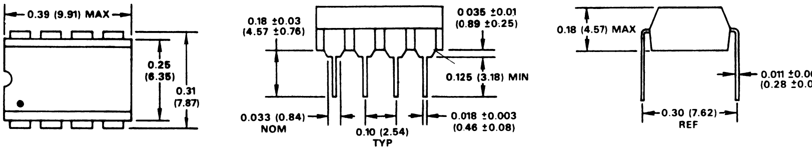
H08B Package (TO-99 Style)
(JEDEC REF MO-006AH)



H08C Package (TO-3 Style)

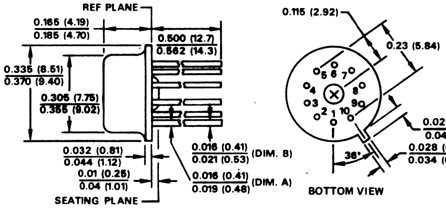


N8A Package



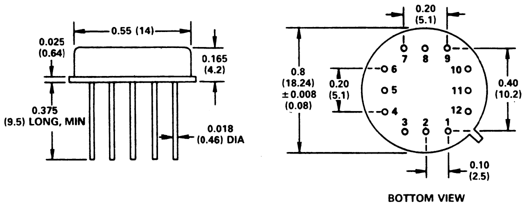
10-PIN PACKAGE

TO-100 Package



12-PIN PACKAGE

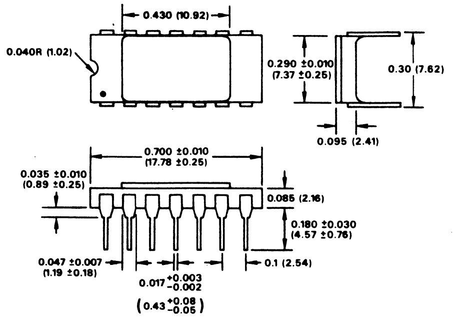
H12A
12-Lead Metal Can Package
(TO-8 Style)



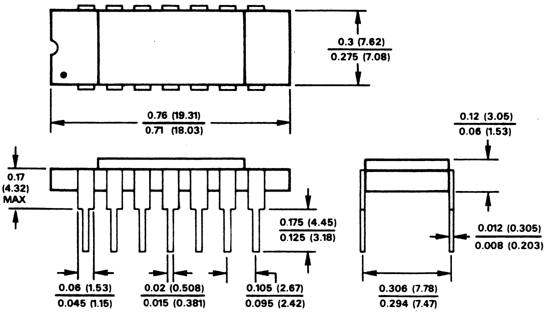
Dimensions shown in inches and (mm).
Lead No. 1 Identified by Dot or Notch.

14-PIN PACKAGES

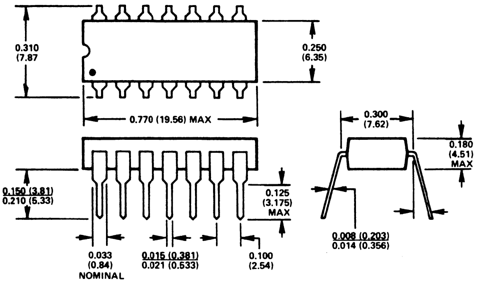
D14A
14-Lead Ceramic Package



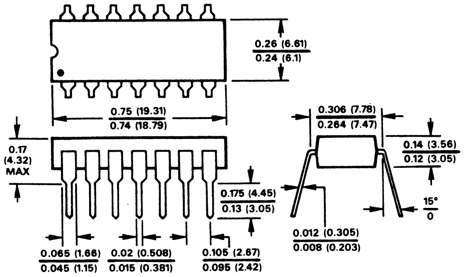
D14B
14-Lead Ceramic DIP Package



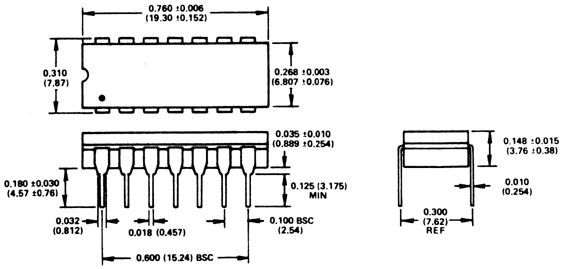
N14A
14-Pin Plastic DIP Package



N14B
14-Pin Plastic Package



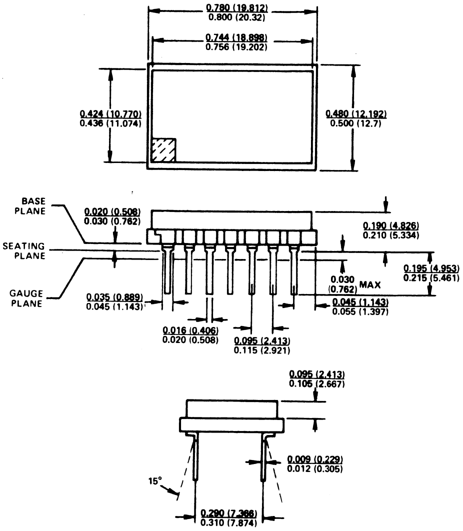
Q14A
14-Pin CERDIP Package



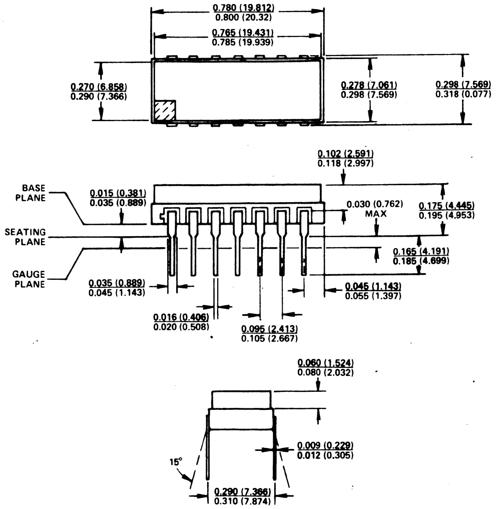
Dimensions shown in inches and (mm).
Lead No. 1 Identified by Dot or Notch.

14-PIN PACKAGES
(Continued)

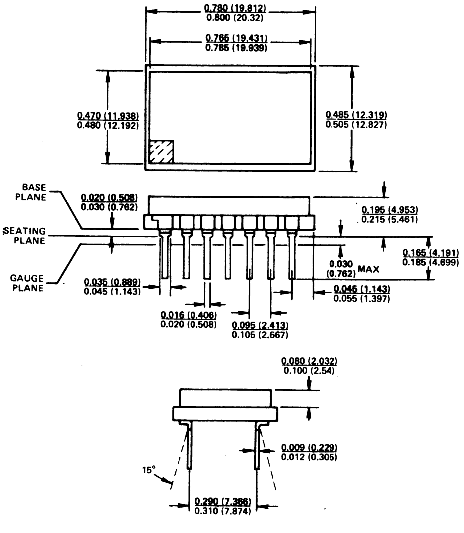
HY14A
14-Pin Hybrid Package



HY14B
14-Pin Hybrid Package



HY14C
14-Pin Hybrid Package



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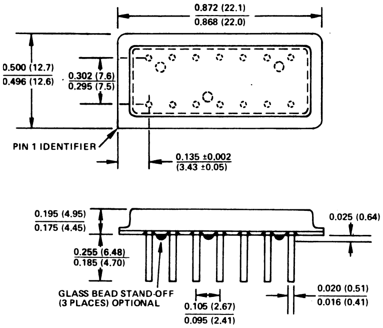

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Lead No. 1 Identified by Dot or Notch.

16-PIN PACKAGES

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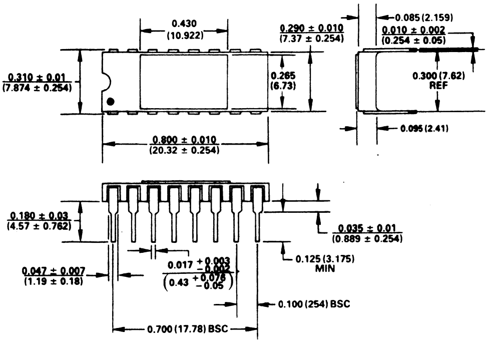

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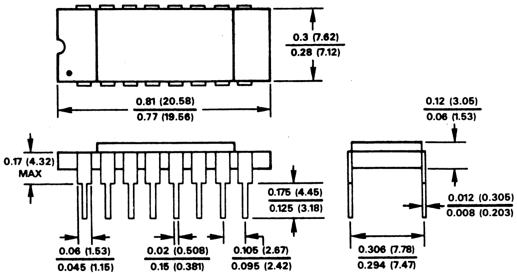

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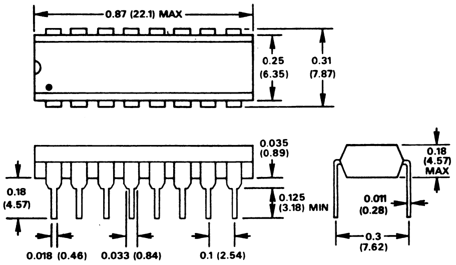

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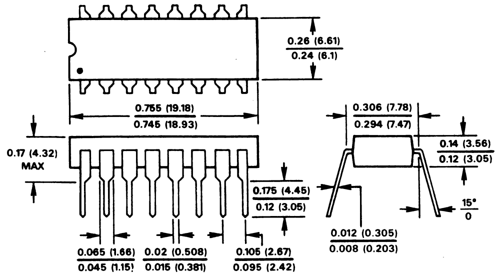

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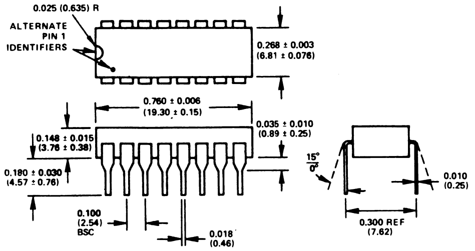

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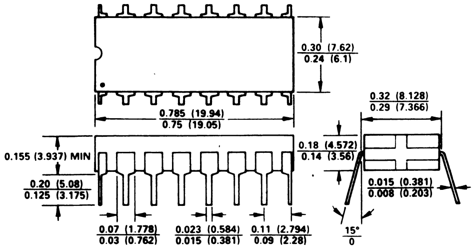

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18-PIN PACKAGES

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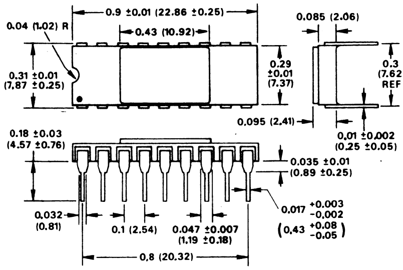

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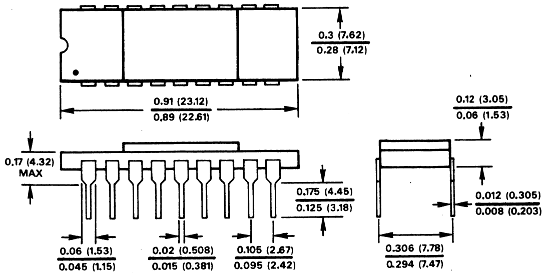

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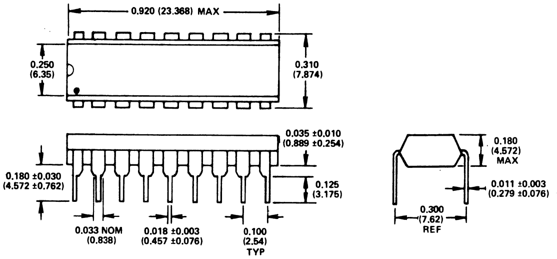

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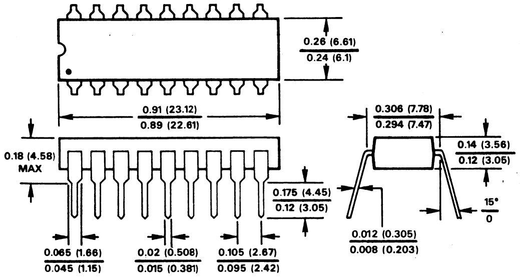

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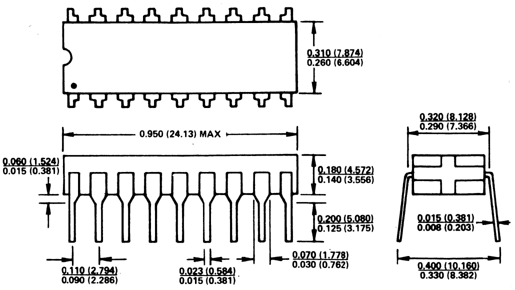

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Lead No. 1 Identified by Dot or Notch.

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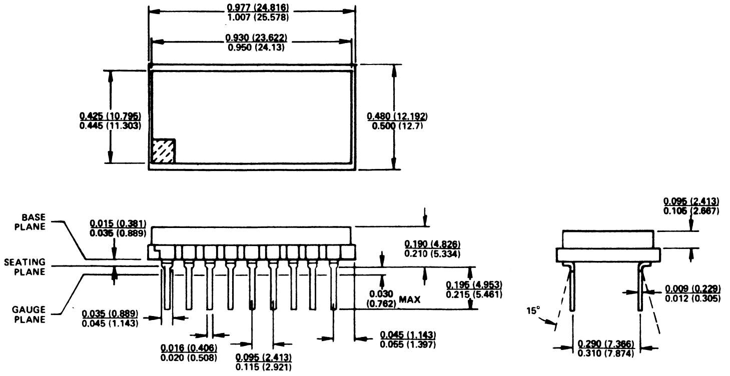

20-PIN PACKAGES

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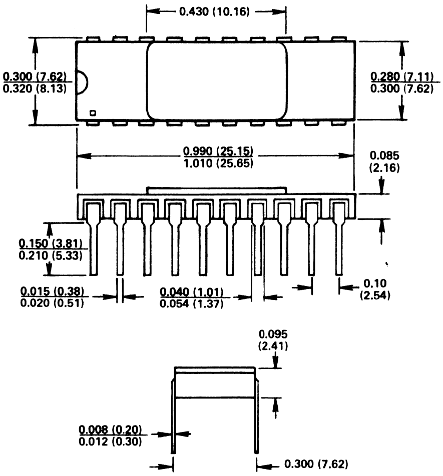

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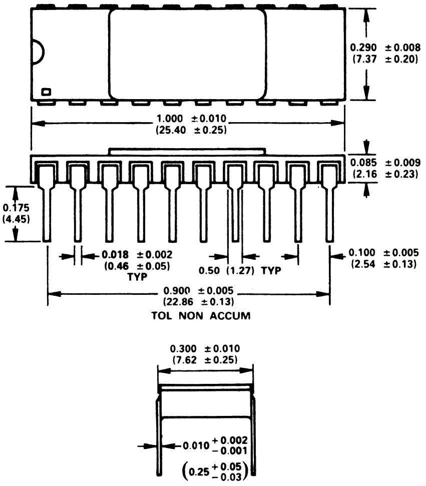

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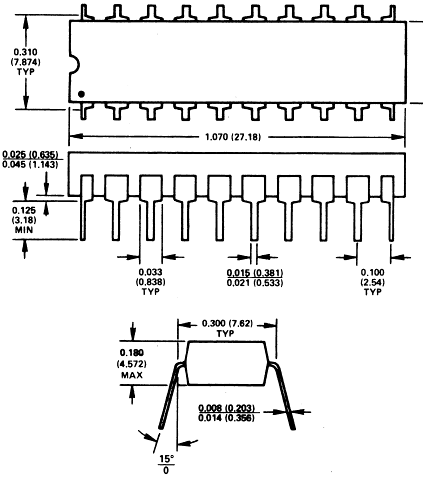

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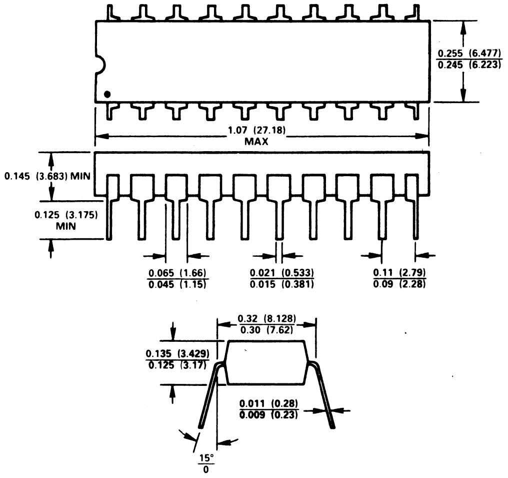

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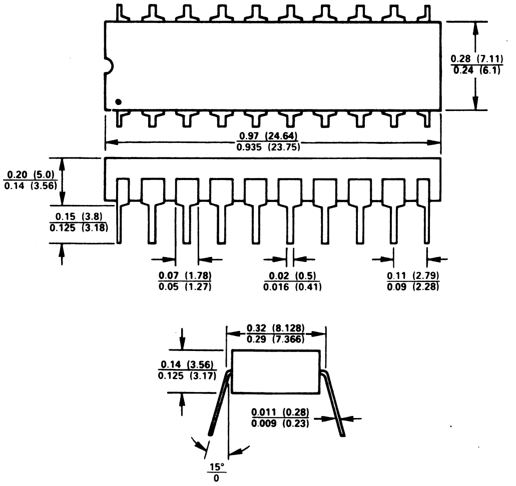

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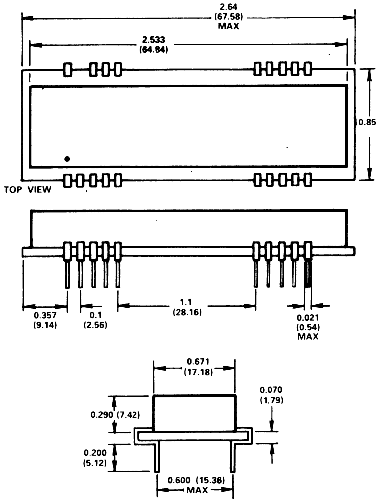

RECOMMENDED MATING SOCKET: AUGAT NO. 240-AG39D (TO PRESERVE THE HIGH CMV INTEGRITY OF THE AD293/AD294 REMOVE ALL UNUSED SOCKET PINS.)

Dimensions shown in inches and (mm).
Lead No. 1 Identified by Dot or Notch.

24-PIN PACKAGES

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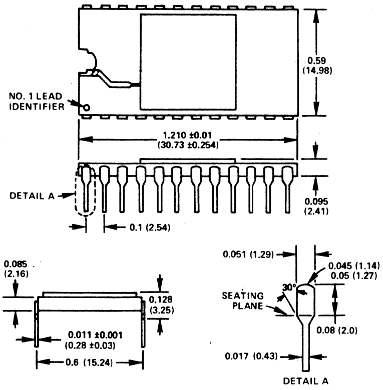
24-Lead Ceramic DIP Package



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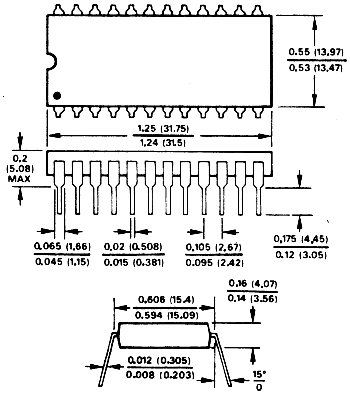

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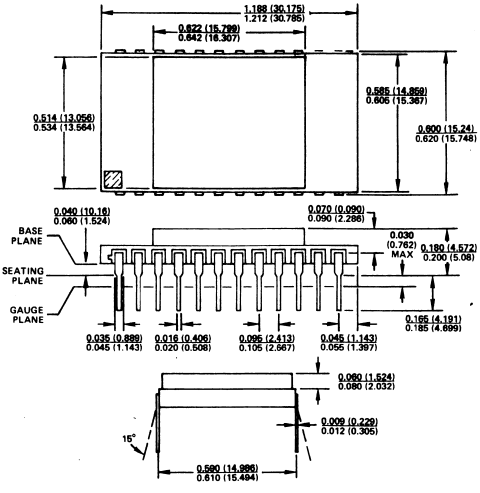

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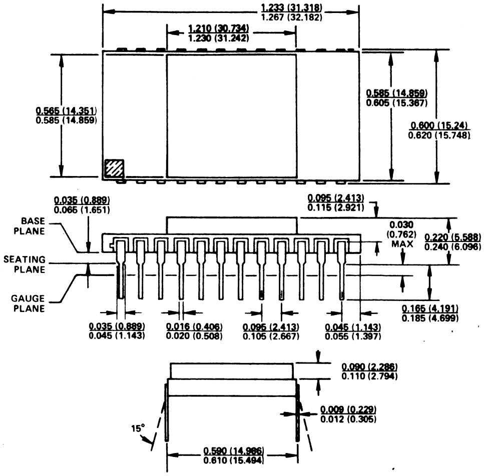

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Lead No. 1 Identified by Dot or Notch.

24-PIN PACKAGES

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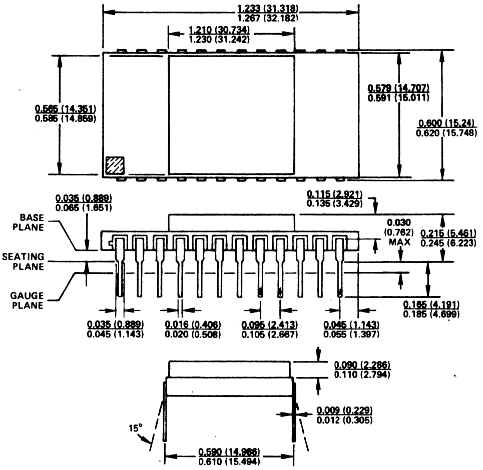

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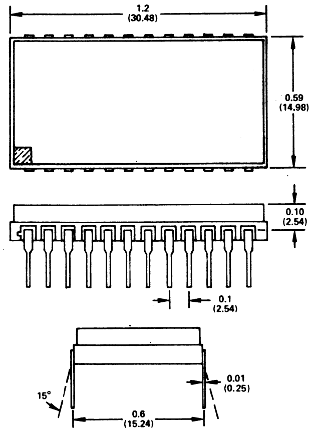

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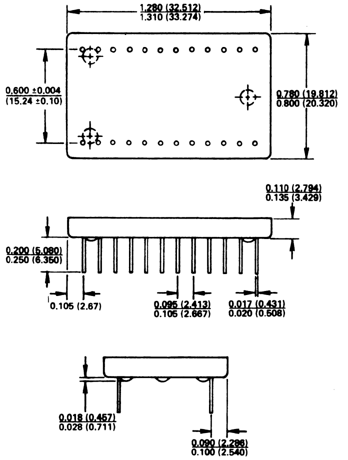

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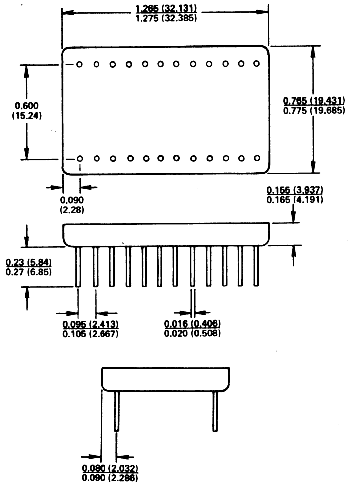

Dimensions shown in inches and (mm).
Lead No. 1 Identified by Dot or Notch.

28-PIN PACKAGES

D28A
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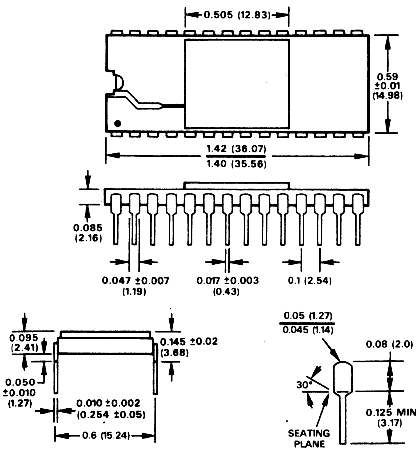

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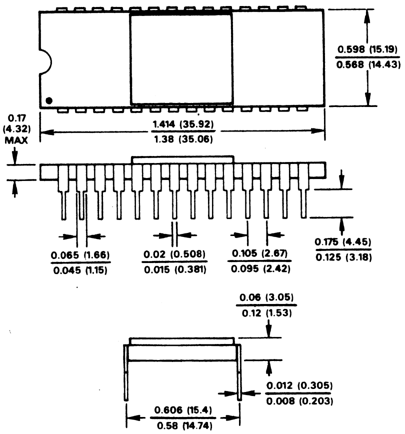

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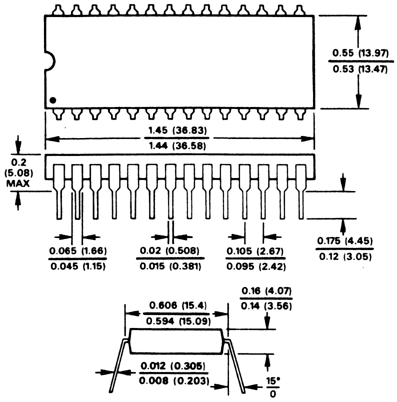

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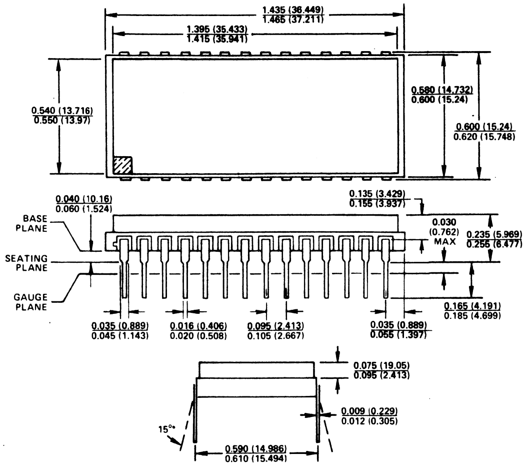

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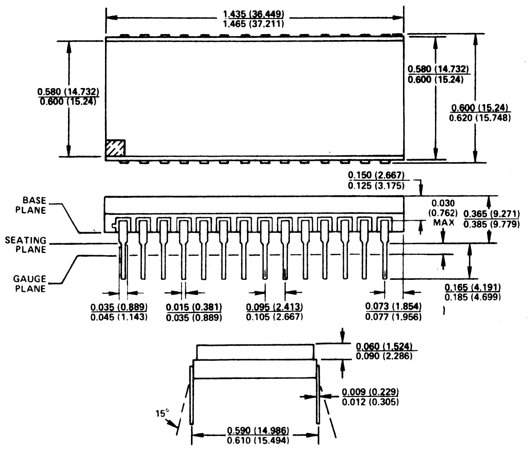

32-PIN PACKAGES

HY32A
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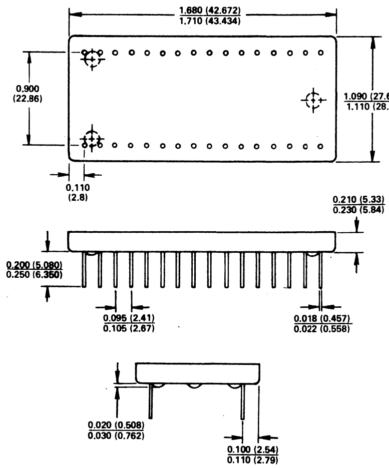

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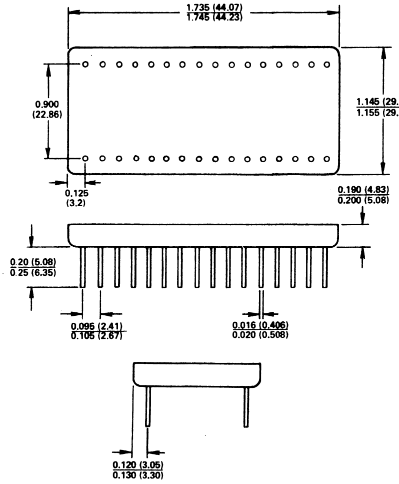

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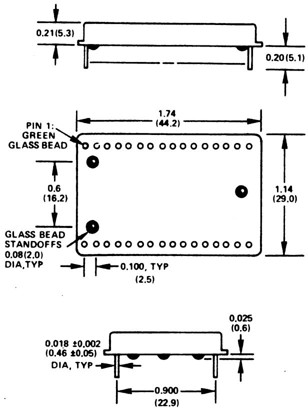

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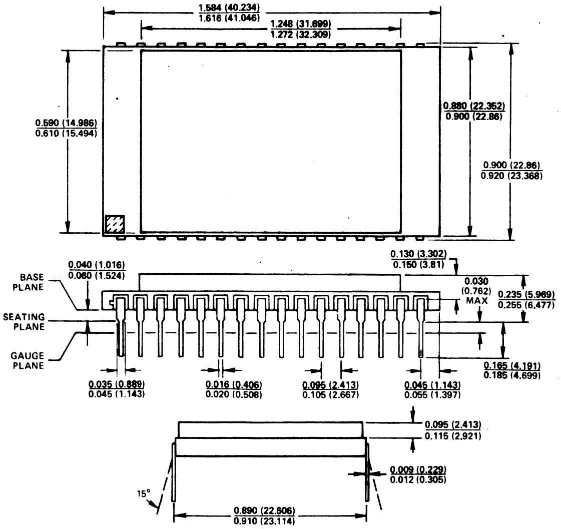

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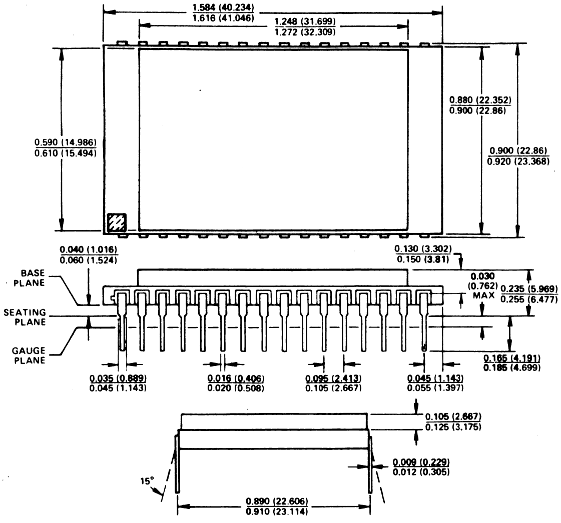

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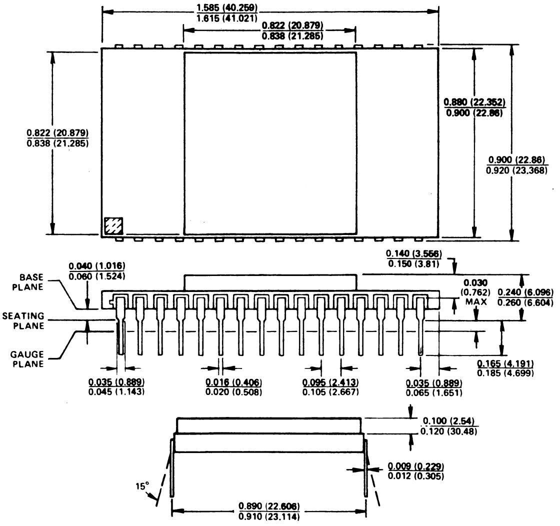

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32-PIN PACKAGES
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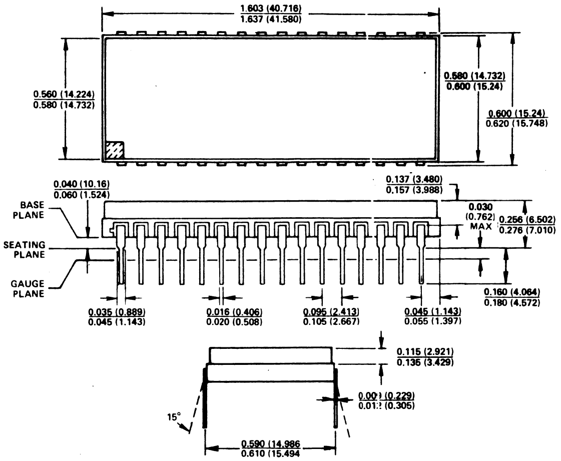

40-PIN PACKAGES

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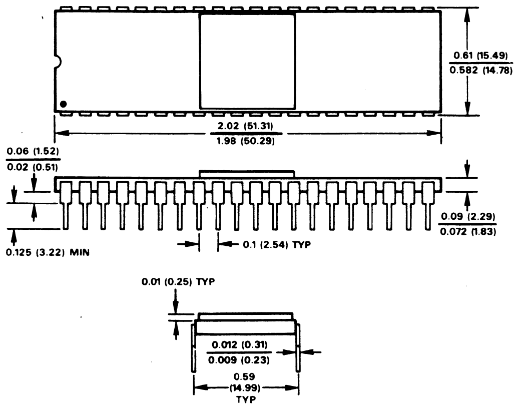

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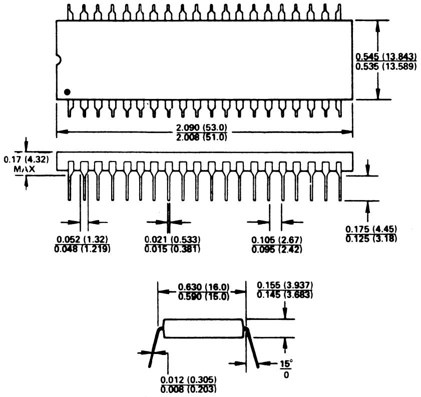

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Application Notes

Page

How to Select Operational Amplifiers 21-3

How to Test Basic Operational Amplifier Parameters 21-9

An I.C. Amplifier Users' Guide to Decoupling, Grounding, and Making Things Go Right For a Change 21-13

A User's Guide to IC Instrumentation Amplifiers 21-21

Interfacing the AD558 DACPORT^{TM} to Microprocessors 21-31

Gain Error and Gain Temperature Coefficient of CMOS Multiplying DACs 21-37

CMOS DACs in the Voltage-Switching Mode Can Work from a Single Supply, Including Output Op Amp, For Fast Response, No Offset-Induced Nonlinearity 21-41

Methods for Generating Complex Wafeforms and Vectors Using Multiplying D/A Converters 21-43

Behind the Switch Symbol: Use CMOS Analog Switches More Effectively When You Consider Them as Circuits 21-49

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How to Select Operational Amplifiers

INTRODUCTION

In selecting the right device for a specific application, you should have clearly in mind your design objectives and a firm understanding of what published specifications mean. Beyond this, you should detail the significant variables that are pertinent to your application. The purpose of this section is to put these many decision factors into perspective to help you make the most meaningful buying decisions.

To properly choose an operational amplifier for any given set of requirements, the designer must have:

1. *A complete definition of the design objectives.*
Signal levels, accuracy desired, bandwidth requirements, circuit impedance, environmental conditions and several other factors must be well defined before selection can be effectively undertaken.

2. *Firm understanding of what the manufacturer means by the numbers published for the parameters.*
Frequently, any two manufacturers may have comparable published specifications, which may have been arrived at using differing measurement techniques. This creates a pitfall in op amp selection. To avoid these difficulties, the designer must know what the published specifications mean and how these parameters are measured. He then must be able to translate these published specifications in terms meaningful to his design requirements. In the following discussion, Analog Devices provides the designer: 1) a checklist which he can apply to his application to assure that all significant factors are taken into account; 2) meaningful definitions for each of our published specifications; and 3) illustrations of how the requirements of his design are translated in terms of these specifications to help make an effective and economical choice.

APPLICATION CHECKLIST

By way of an application checklist, the designer will need to account for the following:

Character of the application: The character of the application (inverter, follower, differential amplifier, etc.) will often influence the choice of amplifier. Chopper stabilized amplifiers, for example, are not generally applicable where differential inputs are required.

Accurate description of the input signal: It is extremely important that the input signal be thoroughly characterized. Is the input a voltage source or current source? Range of amplitude? Source impedance? Time/frequency characteristics?

Environmental conditions: What is the maximum range of temperature, time, and supply voltage over which the circuits must operate (to the required accuracy) without readjustment?

Accuracy desired: The accuracy requirement determines the extent to which the foregoing considerations are critical, and ultimately points the way to a device (or series of devices) which are acceptable. Accuracy must, of course, be defined in terms meaningful to the application with regard to bandwidth, dc offset, and other parameters.

SELECTION PROCESS

In general, the objective of amplifier selection should be to choose the least expensive device which will meet the physical, electrical, and environmental requirements imposed by the application. This suggests that a "General Purpose" amplifier will be the best choice in all applications where the desired performance requirements can be met. Where this is not possible, it is generally because of limitations encountered in two areas – bandwidth requirements, and/or offset and drift parameters.

To make it easier to relate bandwidth requirements with the drift and offset characteristics, a capsule view of bandwidth considerations precedes the dc discussions below. The reader is then returned to an expanded discussion of gain-bandwidth considerations.

Gain Bandwidth Considerations, A Capsule View

Although all selection criteria must be met simultaneously, determination of the bandwidth requirements is a logical starting point because:

A) If dc information is not of interest, a suitable blocking capacitor can usually be connected at the amplifier input and all of the "drift" specifications may be ignored, and

B) Where high frequency (>10MHz) characteristics are of primary importance, the choice will be limited to those amplifiers designated "Wide Bandwidth/Fast Settling."

Where dc information is required and where frequency requirements are relatively modest (full power response below 100kHz, unity gain of less than 1.5MHz) other criteria will probably influence the final choice. It is important, however, to choose an amplifier with which an adequate value of loop gain is assured (at the maximum frequency of interest) to obtain the desired accuracy. Loop gain is the excess of open loop gain over closed loop gain, and is responsible for the diminishing error due to fluctuations in the open loop gain due to time, temperature, etc. Typically, a loop gain of 100 will yield an error of no more than 1%, 0.1% from loop gain of 1000, etc. Where undistorted response is required, the specifications for full linear response and slewing rate should be chosen such that they are not exceeded at the highest frequency of operation.

Offset and Drift Considerations

In the majority of op-amp applications, final selection is determined by the dc offset and drift characteristics. To undertake amplifier selection in these cases, it is necessary to translate the requirements listed above as follows. (It is assumed that bandwidth requirements have been established at this point.)

1. *What input impedance must the circuit present to the signal source?* This depends primarily on the source impedance, R_S, and the amount of loading error which is acceptable. Most amplifier circuits are designed around either the inverting or noninverting circuit of Figure 1. The choice is often made between the two to accommodate the impedance requirement. Input impedance for the inverting circuit is approximately equal to the summing impedance, R_i and the upper limit on the magnitude of R_i is determined by the allowable drift error because of input bias current as discussed below. The noninverting circuit offers inherently higher input impedance than the inverting circuit (due to "bootstrapping" feedback) and in this case input impedance is approximately equal to the common mode impedance of the amplifier R_{CM}.

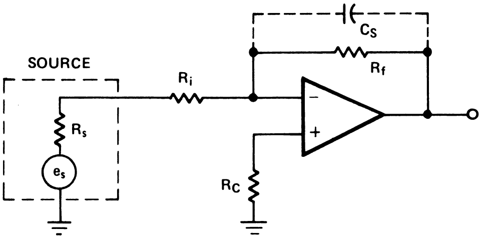
2. *How much drift error can be tolerated?* The question is related to the input signal level, e_S, and the required accuracy. For example, to amplify or otherwise manipulate a dc input signal of one volt with an accuracy of 0.1%, the offset drift error, V_d, must be one millivolt or less. (This assumes that other sources of error such as input loading, noise and gain error have already been allowed for.) By the same reasoning, the allowable drift error for a 1 volt signal and 0.01% accuracy would be 100μV.

When this has been defined, the allowable limits of offset voltage (e_{os}), bias current (i_b), and difference current can be calculated by the equations of Figure 1.

Figure 1 gives the equations which relate offset voltage (e_{os}), bias current (i_b), difference current (i_d) and the external circuit impedances to the drift error, V_d, for both the inverting and the noninverting circuits. From these equations it can be seen how the input impedance requirements of the foregoing paragraphs are related to the drift error.

For example, in the case of the inverting circuit, an offset error voltage, i_bR_i, is generated by the bias current flowing through the summing impedance. This error increases for increasing R_i. Since R_i also sets the input impedance, there is a conflict between high input impedance and low offset errors. Likewise, for a given offset error, higher values for R_i can be used with an amplifier which has lower bias current.

Where it will otherwise function properly, the noninverting circuit generally makes a better choice for high input impedance circuits. Also, for the same source and input impedance requirement, a given amplifier will generate lower offset errors for the noninverting circuit than for the inverting circuit. This is so because the bias current flows only through R_s for the noninverter and this will always be less than the input impedance, R_i, of the inverter. Input imped-



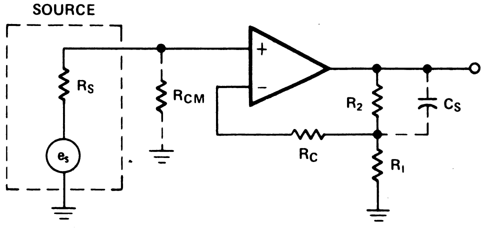
$$e_o = \frac{R_f}{R_i}\Big[\underbrace{e_s}_{\text{Signal}} + \underbrace{e_{os}\left(\frac{R_f+R_i}{R_f}\right) + I_b\,R_i}_{\text{Input Drift Error } = V_d}\Big] \quad \begin{array}{l}\text{For } R_C = 0\\ \text{and } R_S << R_i\end{array}$$

$$e_o = \frac{R_f}{R_i}\Big[\underbrace{e_s}_{\text{Signal}} + \underbrace{e_{os}\,\frac{R_f+R_i}{R_f} + i_d\,R_i}_{\text{Input Drift Error } = V_d}\Big] \quad \begin{array}{l}\text{For } R_C = R_i\,R_f/R_i + R_f\\ \text{and } R_S << R_i\end{array}$$

Input Impedance $R_{IN} \approx R_i$

$$\%\ \text{Drift Error} = \frac{100V_d}{e_s}$$

Figure 1A. Inverting Configuration



$$e_o = \frac{R_2 + R_i}{R_i}\Big[\underbrace{e_s}_{\text{Signal}} + \underbrace{e_{os} + i_b\,R_s}_{\text{Drift Error } = V_d}\Big] \ \text{for } R_C = 0$$

$$e_o = \frac{R_2 + R_i}{R_i}\Big[\underbrace{e_s}_{\text{Signal}} + \underbrace{e_{os} + i_d\,R_s}_{\text{Drift Error } = V_d}\Big] \ \text{for } R_C = R_s \quad \frac{R_i\,R_2}{R_i + R_2}$$

Input Impedance $R_{IN} \approx R_{CM}$

$$\%\ \text{Drift Error} = \frac{100V_d}{e_s}$$

Figure 1B. Noninverting Configuration

ance of the noninverter (approximately R_{CM}) is typically 10^7 ohms even for the least expensive bipolar amplifiers and up to 10^{11} ohms for FET types.

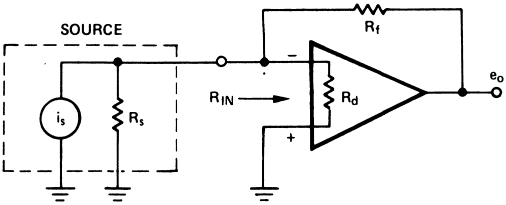
Unfortunately, however, the noninverting configuration can not always be used since it will not perform many circuit functions such as integration or summation. A further limitation occurs in high accuracy applications, where common mode errors may rule out this circuit configuration.

Initial offsets can usually be zeroed at room temperature so that only the maximum temperature excursion (ΔT) from +25°C need be considered. For example, over the range of -25°C to +85°C, the maximum temperature excursion (ΔT) from +25°C would be 60°C. As a practical matter, offset errors due to supply voltage and time drift can generally be neglected since errors due to temperature drift are usually much greater.

Current Amplifier Considerations

Before leaving the subject of offset errors, we shall discuss briefly the current amplifier configuration which is shown in Figure 2A. The obvious approach to measuring current is to develop a voltage drop across a load resistor, R_f, and to measure this potential with a high impedance amplifier as shown in Figure 2B.

This approach has several disadvantages as compared to the circuit of Figure 2A. First the noninverting amplifier introduces common mode errors which do not occur for Figure 2A. Second, an ideal current meter would have zero impedance whereas, R_f in Figure 2B may become very large since this resistor determines the sensitivity of the measurement. Third, the changes of input impedance, R_{CM}, for the noninverting amplifier with temperature will cause variable loading on R_f and hence a change in sensitivity.

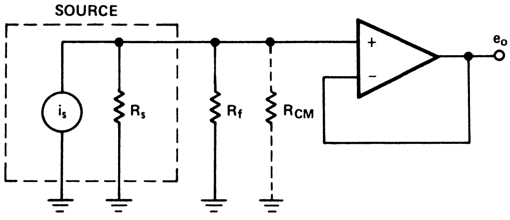


$$e_o = -R_f \left[\underbrace{i_s}_{\text{Signal}} + \underbrace{e_{os} \left(\frac{R_f + R_s}{R_s R_f} \right) + i_b}_{\text{Drift error} = I\epsilon} \right]$$

$$\text{Input Impedance } R_{IN} = \left(\frac{R_f R_d}{R_f + R_d} \right) \left(\frac{1}{1 + A\beta} \right)$$

$$\text{where } 1/\beta = 1 + \frac{R_f (R_s + R_d)}{R_s R_d} \quad \% \text{ Drift Error} = \frac{100\, I\epsilon}{i_s}$$

Figure 2A. Current Amplifier



$$e_o = \underbrace{R_f i_s}_{\text{Signal}} + \underbrace{e_{os} + i_b R_f}_{\text{Drift Error} = V_d} \text{ for } R_s > R_f$$

$$\text{Input Impedance } R_{IN} \approx R_f$$

$$\% \text{ Drift Error} = \frac{100\, V_d}{R_f i_s}$$

Figure 2B. Voltage Amplifier With Sampling Resistor

The current amplifier of Figure 2A circumvents all of these difficulties and approaches an ideal current meter; that is, there is essentially no voltage drop across the measuring circuit, since with enough open loop gain, A, the input impedance R_{IN} becomes very small.

In selecting a current amplifier, the most important consideration is current noise, and bias current drift. Measuring accuracy is largely the ratio of current noise and drift to signal current, i_s. To obtain the drift of error current I_ϵ referred to the input, use the following expression.

$$\Delta I_\epsilon = \left[\frac{\Delta e_{os}}{\Delta T} \left(\frac{R_f + R_s}{R_f R_s} \right) + \frac{\Delta i_B}{\Delta T} \right] \Delta T$$

Now, to make a proper selection you must pick an amplifier with an error current, I_ϵ, over the operating temperature which is small compared to the signal current, i_s. Do not overlook current noise which may be more important than current drift in many applications.

Gain Bandwidth Considerations, Expanded Discussion

From the previous discussion, it is apparent that most general purpose operational amplifiers will usually give adequate performance for the dc and audio frequency range applications. However, to obtain unity gain bandwidth above 2MHz, full power response above 20kHz and slewing rate above 6V/μs, in general, requires special design techniques. All amplifiers with wideband, fast response characteristics have been listed in the wide bandwidth group to simplify the selection for higher frequency applications.

One factor often overlooked is that stray capacitance and impedance levels of the external feedback circuit can be the major limitation in high frequency applications. For example, in Figure 1A, if R_f were one megohm and stray capacitance, C_s, were one picofarad then the closed loop bandwidth would be limited to 160kHz ($1/(2\pi R_F C_S)$) regardless of how fast the amplifier is. Moreover, output slewing rate will be limited by how fast C_S can be charged which in trun is related to signal level, e_s, and input impedance, R_i, by $de_o/dt = -e_s/R_iC_s$. For these reasons it is usually not possible to obtain both fast response and high input impedance for an inverting circuit since both R_i and R_f must be large to obtain high input impedance.

Another advantage of the noninverting circuit (Figure 1B) is that input impedance, being determined by potentiometric feedback, does not depend on the impedance levels for R_1 and R_2. Therefore, a low impedance can be used for R_2 so that stray capacitance of C_S will not limit the circuit's bandwidth. In this case the minimum value for R_2 is constrained only by the output current rating of the amplifier. Again the trade-off between the frequency response and input impedance of the inverting and noninverting circuits must be evaluated in light of the common mode rejection error introduced by the noninverter.

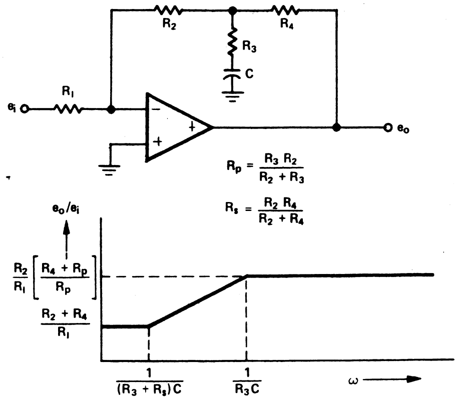


Figure 3. DC Feedback Minimizes Output Offset for AC Applications

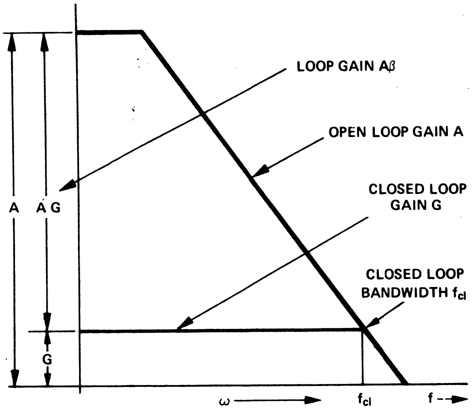


Figure 4. Closed Loop Bandwidth and Loop Gain

In the past, many wideband amplifiers, especially chopper stabilized units, did not offer fast response on the positive input and therefore were restricted to use in inverting circuits. However, new FET amplifiers from Analog Devices are available to meet the needs for high speed performance for either configuration.

For greater emphasis wideband applications can be separated into two categories – steady state and transient. Since the amplifier requirements for the two are somewhat different, these categories will be discussed separately.

A. Steady State Applications

Steady state applications involve amplifying or otherwise manipulating *continuous* sinusoidal, complex or random waveforms. In these applications the significant issues in choosing an amplifier are as follows:

1. *Is dc coupling required?* If dc information is of no consequence, then the offset drift errors are not usually important and a capacitor can be used if necessary to block the output dc offset. Your only concern here is that dc offset at the output does not become so large, as might be the case with a high gain stage, that the output is saturated or the dynamic swing for ac signals is limited. One way to circumvent the latter problem is to use feedback to limit the gain at dc as shown in Figure 3. The gain of these circuits can be small at dc but large at high frequencies.

2. *What closed loop gain and bandwidth are required?* Closed loop gain, G, is dictated by the application. To a first approximation the intersection of the open and closed loop gain curves in Figure 4 gives the closed loop bandwidth, f_{cl} (−3dB). For high gain, wideband requirements, it may be necessary, or more economical, to use two amplifiers in cascade, each at lower gain.

3. *What loop gain is required or alternatively what gain stability, output impedance and/or linearity are necessary?* The available loop gain at a particular frequency or over a range of frequencies is very often more important than closed loop bandwidth in selecting an amplifier. Loop gain as illustrated in Figure 4, is defined as the difference, in dB, or as the ratio, arithmetically, of the open to closed loop gain ($A\beta = A/G$). You will find in most of the equations defining the closed loop characteristic of a feedback amplifier that the loop gain ($A\beta$) is the determining factor in performance. Some of the more notable examples of this point are as follows:

a. Closed loop gain stability = $\Delta G/G$
$\Delta G/G = (\Delta A/A)\ [1/(1 + A\beta)]$ where $\Delta A/A$ is the open loop gain stability, usually about 1%/°C.

b. Closed loop output impedance = $Z_{ocl} = Z_o/(1 + A\beta)$, where Z_o is the open loop output impedance, usually 200 to 5000 ohms.

c. Closed loop nonlinearity = $L_{cl} = L_{ol}/(1 + A\beta)$, where L_{ol} is the open loop linearity, usually less than 5%.

Loop gain of 100, or 40dB, is adequate for most applications and this is readily achievable at dc and low frequencies. But note that loop gain decreases with increasing frequency which makes it difficult to obtain large loop gains at high frequencies. For this reason it may be necessary to use a 10MHz unity gain amplifier in order to obtain adequate feedback over a 10kHz bandwidth.

4. *What full power response and/or slew rate are required?* You should examine your expected output waveform and select an amplifier whose slewing rate exceeds the maximum rate of change of output signal. For a sinusoidal waveform with a peak voltage output equal to the rated amplifier output the frequency should not exceed f_p, the full power response of the amplifier. As the output signal voltage is reduced below the rated output voltage, the usable maximum frequency can be extended proportionately. If you do not observe these restrictions you will get distortion and unexpected dc offsets at the output of the amplifier.

There are many monolithic amplifier designs available today whose frequency response is not a simple 6dB roll-off and which may be shaped with external RC components for improved performance. Using feed-forward or phase lag compensation networks, gain-bandwidth product and/or full power response may be shaped to meet varying design requirements. Most discrete op amps offer the stable 6dB roll-off with specified unity gain-bandwidth and slew rate thereby limiting maximum speed and response to those published specifications.

B. Transient Applications

In applications such as A/D and D/A converters and pulse amplifiers, the *transient response* of the wideband amplifier is generally more important than the *gain bandwidth* characteristic described above. Slewing rate, overload recovery and settling time are the specifications which determine the transient response.

When applying the high frequency amplifier, it is important to understand how amplifier performance is affected by component selection as well as impedance levels used around the amplifier.

Settling Time

The time and frequency response of a linear, bilateral network or amplifier are related by well known mathematics. For example, the step response for a well behaved, linear, 6dB/octave amplifier with a closed loop bandwidth of ω_{cl} is shown in Figure 5.

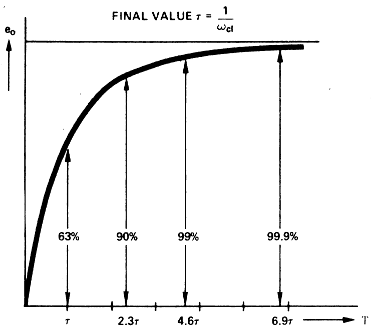


Figure 5. Step Response for Linear 6dB/Octave Amplifier

To a first approximation, the curve in Figure 5 can be used to relate settling time to closed loop bandwidth of Figure 4. *Settling time* is defined as the time elapsed from the application of a perfect step input to the time when the amplifier output has entered and remained within a specified error band symmetrical about the final value (Figure 6). Settling time therefore includes the time required for the amplifier to slew from the initial value, recover from slew rate limited overload, and settle to a given error in the linear range.

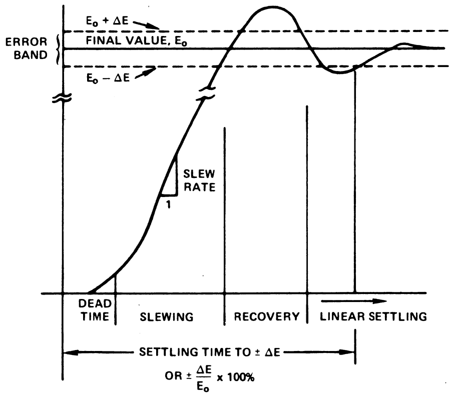


Figure 6. Typical Settling Time Characteristics

However, the approximation soon breaks down since settling time is determined by a combination of amplifier characteristics (both linear and nonlinear) and because it is a closed loop parameter. Therefore, it cannot be readily predicted from the open loop specifications such as slew rate, small signal bandwidth, etc.

Analog Devices specifies settling time for the condition of unity gain, relatively low impedance levels, and no capacitive loading. A full-scale step input is used to determine settling time and the step is generally unipolar – i.e.: from zero to plus or minus full scale. The settling time indicated is generally the longest time resulting from a step of either polarity and is given as a percentage of the full scale step transition.

Settling time is a nonlinear function. It varies with the input signal level and it is greatly affected by impedances external to the amplifier. The nonlinear dependence of settling time on these two parameters can be demonstrated by an examination of experimental data from Analog Devices' wide bandwidth AD544 op amp.

Settling Time vs. Signal Swing

The curves in Figure 7 illustrate the AD544 settling time error versus input signal level. These "V" curves are useful as a design aid for bracketing settling time versus step input level.

Because of nonlinear factors, extrapolation of settling times from one set of conditions to another becomes very difficult, if not impossible. This point becomes very apparent, in Figure 7, when reviewing settling time as a function of input signal swing. Using this measurement technique, the settling time error voltage, measured at point V, is equal to one-half of the null voltage between the input signal and the output signal.

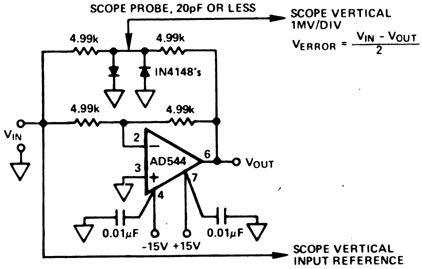


Figure 7A. Settling Time Test Circuit

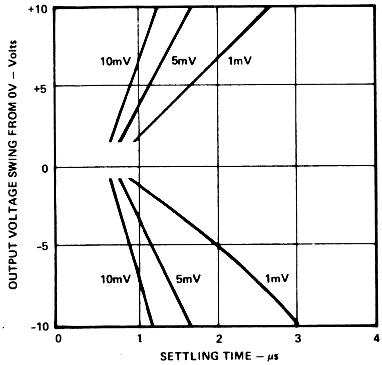


Figure 7B. Output Settling Time vs. Output Swing and Error

ERRORS DUE TO NOISE

A major criterion in the selection of an amplifier for low level signals is the amplifier input noise, since this is usually the limiting factor on system resolution. In the general case, amplifier noise can be characterized by a voltage source in series with the summing junction and a current source in parallel with the summing junction. Whenever high source impedance is encountered, current noise flowing through the source impedance will appear as an additional voltage noise, combining with the amplifier voltage noise. The sum of these noise sources will then be amplified along with the desired signal. For this reason, selection of a particular amplifier must consider both the amplifier noise performance as well as the source impedance.

Consideration must also be given to noise sources other than the amplifier whenever determining total system noise. RF noise may be fed into an amplifier through any connecting wire, including power supply and output leads. Adequate shielding and low-pass filters on all incoming leads will usually prevent noise pick-up.

Thermal noise is generated in any conductor or resistor as a result of thermal agitation of the electrons. This noise voltage source, sometimes referred to as "Johnson Noise", is generated in the resistive component of any impedance and has a value:

$$e_n = \sqrt{4KTBR}$$

where e_n = the rms value of the noise voltage

K = Boltzman's Constant (1.38 x 10^{23} joules/°K)

T = absolute temperature of the resistance, °K

B = the bandwidth in which the noise is measured

Since noise is related to the bandwidth over which the measurement is made, no noise specification is meaningful unless the bandwidth for the specification is given. Although the Thermal Noise equation may appear unwieldly for practical noise calculations, all that is required to enable rapid approximations is to apply a few simple rules of thumb.

Rules of Thumb

(1) Remember that a 100kΩ resistor generates 40nV rms in a 1Hz bandwidth. The noise voltages generated by other values of resistances in other bandwidths can be calculated by remembering that the noise is proportional to the square root of the resistance and the bandwidth; i.e.

$$e_n\,(\text{rms}) = (40\text{nV}/\sqrt{\text{Hz}})\left(\sqrt{\frac{R}{100\text{k}\Omega}\,(\text{BW})}\right)$$

(2) To convert the rms noise to a p-p value, a conversion factor of 6.6µV p-p/µV rms is applied for less than 0.1% probability of noise peaks exceeding calculated limits.

(3) The total rms noise contribution due to several noise sources is determined by the square root of the sum of the squares:

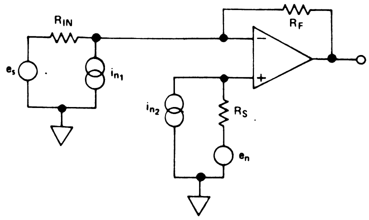
$$e_t = \sqrt{e_a{}^2 + e_b{}^2 + e_c{}^2 + \ldots e_n{}^2}$$

If any noise source is less than a third of another, it may be neglected. The resulting error will be approximately 5%.

(4) Restricting the bandwidth of a system to the minimum usable and using the lowest impedances possible are ways to reduce noise.

DESIGN EXAMPLE

Figure 8 illustrates a typical circuit with noise calculations shown for each noise source. The total of the noise sources is obtained by adding each of the individual sources in a rms fashion.



COMPONENT	CAUSE	OUTPUT CONTRIBUTION
R_{IN}	Johnson Noise	$\sqrt{4KTBR_{IN}}\,(R_F/R_{IN})$
R_S	Johnson Noise	$\sqrt{4KTBR_S}\,(R_F/R_{IN}+1)$
R_F	Johnson Noise	$\sqrt{4KTBR_F}$
i_{n_1}	Amp. Current Noise	$i_{n_1} R_F$
i_{n_2}	Amp. Current Noise	$(i_{n_2} R_S)\,(R_F/R_{IN}+1)$
e_n	Amp. Voltage Noise	$e_n\,(R_F/R_{IN}+1)$

$$\text{TOTAL NOISE} = \sqrt{(e_{R_{IN}}\,G)^2 + [e_{R_S}\,(G+1)]^2 + e^2_{R_F} + [(i_{n_1}\,R_F)^2] + [(i_{n_2}\,R_S)\,(G+1)]^2 + [e_n\,(G+1)]^2}$$

Figure 8. Noise Components

ANALOG DEVICES

APPLICATION NOTE

How to Test Basic Operational Amplifier Parameters

THE REAL OP AMP

Input Imperfections

The characteristics of op amps are, of course, considerably more complicated than can be shown in Figure 1. The real op amp has a number of sources of error which must be tested independently to determine the true quality of the device. The active errors at the input can be modeled as a dc current source (I_B) and a series dc voltage source (V_{OS}). An impedance (Z_{IN} Diff) appears between the inputs, and another (Z_{INCM}) appears between the inputs and ground. These impedances usually consist of a resistance and capacitance in parallel, and the finite Z_{CM} will introduce errors due to common-mode input voltages.

There are two additional input error sources. In addition to the dc voltage and current sources, small ac sources representing the noise components must be included in the model.

Output Obstacles

The output side of the model is also nonideal. First, an output impedance, R_O, is added in series with the voltage source. The "A" term (infinite in the ideal model) is both finite and a function of frequency in a real amplifier A'(s). It is also obvious that the output voltage and current capabilities of a real op amp are bounded.

The real amplifier, thus, can be modeled as shown below.

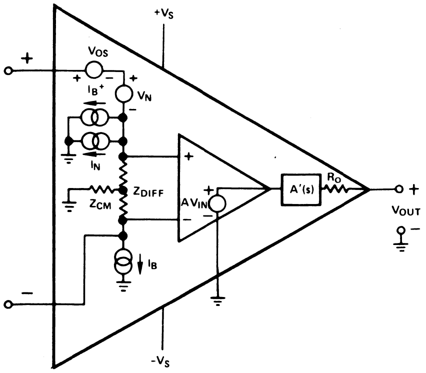


Figure 1. Real Op Amp

OP AMP SPECIFICATIONS

Offset Voltage

Each of these nonideal specifications should be examined in some detail. Consider first the dc errors. Offset voltage is the result of a mismatch in the base-emitter voltages of the differential input transistors (or gate-source voltage mismatch in FET-input amplifiers). This offset voltage is indistinguishable from an input signal as far as the amplifier is concerned. Usually this offset can be trimmed to zero by the user by means of an external potentiometer, which adjusts the balance of the operating currents in the input stage until the V_{BE}'s (or V_{GS}'s) are equal. Of course, this trim will be effective only at one temperature, since offset voltage changes as a function of temperature.

Many circuits exist for testing offset voltage. If V_{OS} is redefined as the voltage at the op amp input which will drive the output to zero in an open-loop circuit, a servo loop can be built around the device under test to determine that voltage. In the circuit shown below, a second amplifier is used to provide feedback. This feedback amplifier must have very high gain and low offset. In operation, the control voltage, V_C, is set to zero. This forces the output of the device under test (D.U.T.) to also go to zero, because no dc current can flow through the amplifier's feedback capacitor. Since the output of the D.U.T. will only go to zero when a voltage equal to its input offset voltage is applied to its input, then V_A must equal V_{OS}. Thus, the output of the feedback amplifier is equal to $V_{OS} \times (1 + R_F/100\Omega)$.

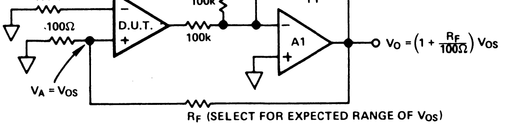


Figure 2. Op Amp Offset Voltage Test Circuit

An alternate method for offset voltage measurement can also be used. This alternate circuit is simpler to build and is only slightly less accurate. If it is assumed that V_{OS} can be modeled as a source connected in series with one input, configuring the amplifier for a fairly high closed-loop gain will allow reasonably accurate measurement of offset voltage with an inexpensive voltmeter.

In order to maintain accuracy in this measurement, R_{IN} should be low enough that I_{OS} flowing through R_{IN} is at least ten times lower than the expected value of V_{OS}. R_C causes an equal voltage to be developed at each input due to I_B. This common-mode voltage effect can be neglected due to the common mode rejection of the op amp. Reasonable values for R_{IN}, R_C, and R_{FB} are 100Ω, 100Ω, and 9.9kΩ, respectively.

Another error arises in this circuit due to the finite open loop gain of the amplifier. Assuming a test circuit gain of 100, the amplifier must have a dc open-loop gain of at least 10,000 for a 1% accurate V_{OS} measurement.

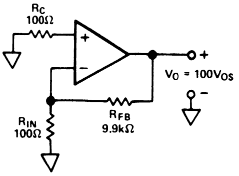


Figure 3. Simple V_{OS} Test Circuit

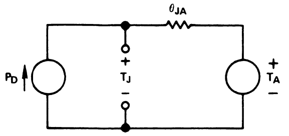
Input Bias Current

Another dc error term is the input bias current. As a consequence of the practical characteristics of transistors, base current must be supplied to the input transistors to bias them into their active operating region. This current must also return to its originating point through some dc path. Thus operational amplifiers cannot be used with input signal sources which are not referred to the same power source as the amplifier. It is possible to reduce bias current-induced errors by providing a source (other than the signal path) which can leak this current.

In many applications, the errors due to bias current are actually less annoying than the errors caused by the mismatch of the bias circuits of the two inputs. This difference between the bias currents is called the input offset current, and is usually specified along with the bias current.

Input currents, like input offset voltage, vary as a function of temperature. In the case of a bipolar-input amplifier, bias current decreases at elevated temperature. This is because the transistors' β increases, and since the emitter current is constant, the base current decreases. In the case of a FET-input amplifier, the bias current is due to JFET gate leakage, which is in reality a reverse-biased junction leakage current. Such currents have the characteristic of doubling for every 10°C rise in junction temperature.

It is important to consider the test conditions under which bias current is specified, particularly in the case of a FET-input op amp. Some manufacturers specify bias current at a junction temperature of 25°C. This corresponds roughly to the bias current immediately after power is applied to the amplifier. Unfortunately most circuits are not operated in a pulsed mode, and the effects of component self-heating must be considered. This effect is, in many cases, not trivial. For example, an amplifier which draws 5mA of supply current from ±15V supplies dissipates 150mW. The thermal resistance from junction to ambient for an 8-lead IC package is typically 150°C/W. This means that the junction temperature of the amplifier in question will be 22.5°C above ambient temperature, and the bias current will be over four times as high as a specification based on 25°C junction temperature.



θ_{JA} = 150°C/W FOR TO-99 TYPE PACKAGES
= 155°C/W FOR EPOXY MINI-DIP
= 100°C/W FOR 14/16 PIN CERAMIC DIP

Figure 4. Thermal Circuit Model for IC Op Amp

Consider an op amp specified for 50pA I_B at T_J = 25°C. If the amplifier draws 5mA from ±15V, as in the previous example,

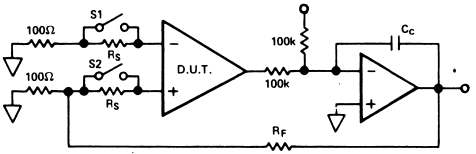
$$P_D = 30V \times 5mA = 150mW$$

$$T_J = T_A + (150mW \times 150°C/W)$$

$$= 25°C + 22.5°C$$

Therefore, I_B will be four times higher than the specification.

Bias current can be measured with essentially the same method used to measure offset voltage. The difference is that a large resistance is inserted in series with the input under test, creating an additional offset voltage equal to $I_B \times R_S$. Assuming the actual V_{OS} has been measured and recorded, the change in apparent V_{OS} due to the change in R_S can be determined and I_B easily computed. Offset current is tested by computing the difference between the bias current on the inverting input and the bias current on the noninverting input.



R_S >>> 100Ω
S_1 IS CLOSED TO TEST I_{B+}
S_2 IS CLOSED TO TEST I_{B-}
BOTH CLOSED TO TEST V_{OS}
BOTH OPEN TO TEST I_{OS}

$$V_O = \left(1 + \frac{R_F}{100\Omega}\right)(V_{OS}) + \left(1 + \frac{R_F}{100\Omega}\right)(I_{B+} R_S) - \left(1 + \frac{R_F}{100\Omega}\right)(I_{B-} R_S)$$

Figure 5. Bias/Offset Current Test Circuit

Open Loop Voltage Gain

Another op amp parameter which distinguishes a real amplifier from an ideal amplifier is open-loop gain. In the ideal op amp model, open loop gain is assumed to be infinite. The same assumption is also sometimes made when dealing with real amplifiers.

Open-loop gain of an operational amplifier is an interesting parameter to attempt to measure. It is generally not practical to measure open loop gain directly by applying a signal at the input and observing the output change. However, by using the device under test inside a feedback loop, it is possible to measure the change in input voltage required to produce a known change in output voltage.

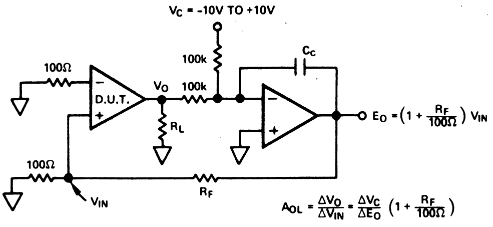


Figure 6. Open Loop Gain Test Circuit

In this circuit, the control voltage, V_C, is varied from $-10V$ to $+10V$, causing the D.U.T. output, V_O, to vary from $+10V$ to $-10V$. The D.U.T. output is varied by a change in V_{IN} produced by the second amplifier. Since V_{IN} is attenuated from E_O by the $R_F/100\Omega$ voltage divider, E_O is easily measured, and open-loop gain can readily be computed.

Frequency Response

Open-loop gain versus frequency is another difficult-to-test specification. Bandwidth is usually specified in terms of gain-bandwidth product or unity-gain small signal bandwidth. It is assumed that the amplifier under test has an open-loop gain versus frequency plot which decreases with a −20dB/decade slope. It is therefore possible to measure the open-loop gain at some known frequency and predict the frequency at which the open-loop gain will be unity.

In the circuit shown, the D.U.T. dc output is held to 0V by V_C and the integrator amplifier. A low amplitude 10kHz ac input signal is applied to the D.U.T. Since the integrator has very low gain at 10kHz, the D.U.T. is effectively running open-loop for the ac signal. The ac output from the D.U.T. can be measured and the gain at 10kHz can be computed. For example, a 741-type amplifier has an open loop gain of approximately 100k at 10kHz. Thus, an easily generated 100mV input at the D.U.T. input will produce an easily measured 10V output. This corresponds to a 1MHz gain-bandwidth product.

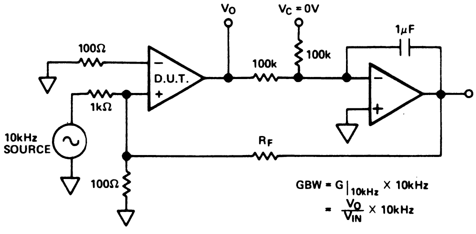
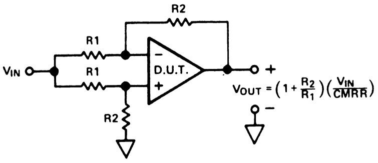


Figure 7. Gain-Bandwidth Product Test Circuit

Common-Mode Rejection Ratio

The ideal operational amplifier is a pure differential amplifier and is insensitive to the absolute voltage on the inputs with respect to ground. The real amplifier has several nonideal characteristics associated with input levels. First, of course, is the allowable range of input voltage. Most IC op amps will only operate when the voltage on the input terminal is within the range bounded by the supply voltages. The second, and perhaps more subtle, characteristic is the common-mode rejection ratio (CMRR). CMRR is defined as the ratio of the change in common mode to the resulting change in input offset voltage. It is often convenient to specify this parameter logarithmically in dB: CMR = 20 log (CMRR).

Common-mode rejection can be measured several ways. One method uses four precision resistors to configure the op amp as a subtractor amplifier. The disadvantage inherent in this circuit is that the ratio match of the resistors also determines the subtractor's CMRR. A mismatch of 0.1% between resistor pairs will result in a CMR of only 60dB. Since most amplifiers exhibit CMR in excess of 80dB (some as high as 120dB), it is clear that this circuit is only marginally useful.



RESISTORS MUST MATCH WITHIN 1ppm (0.0001%) IN ORDER TO MEASURE CMR>100dB

Figure 8. Simple CMR Test Circuit

A better circuit uses the same technique used for measuring offset voltage with one exception. Rather than applying a fixed zero volt input to the D.U.T. operating on ±15V supplies, the same input is applied to the D.U.T. with asymmetrical power supplies, such as +5V and −25V. The output of the amplifier is forced to remain centered between the supplies and the input voltage to the D.U.T. which forces this to occur is measured.

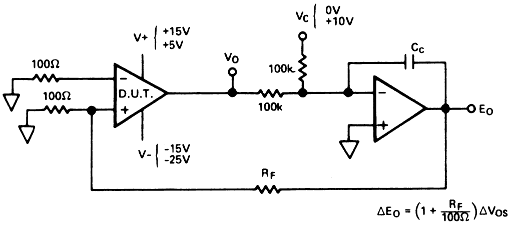


Figure 9. Common-Mode Rejection Test Circuit

The change in V_{OS} can be readily translated into CMR. If this 10V change in CMV creates a 1mV change in V_{OS}, the CMRR is 10,000 and the CMR is 80dB.

An I.C. Amplifier Users' Guide To Decoupling, Grounding, And Making Things Go Right For A Change

by Paul Brokaw

"There once was a breathy baboon
Who always breathed down a bassoon,
For he said "It appears
that in billions of years
I shall certainly hit on a tune"
(Sir Arthur Eddington)

This quotation seemed a proper note with which to begin on a subject which has made monkeys of most of us at one time or another. The struggle to find a suitable configuration for system power, ground, and signal returns too frequently degenerates into a frustrating glitch hunt. While a strictly experimental approach can be used to solve simple problems, a little forethought can often prevent serious problems and provide a plan of attack if some judicious tinkering is later required.

The subject is so fragmented that a completely general treatment is too difficult for me to tackle. Therefore, I'd like to state one general principle and then look a bit more narrowly at the subject of decoupling and grounding as it relates to integrated circuit amplifiers.

. . . Principle: Think—where the currents will flow.

I suppose this seems pretty obvious, but all of us tend to think of the currents we're interested in as flowing "out" of some place and "through" some other place but often neglect to worry how the current will find its way back to its source. One tends to act as if all "ground" or "supply voltage" points are equivalent and neglect (for as long as possible) the fact that they are parts of a network of conductors through which currents flow and develop finite voltages.

In order to do some advance planning it's important to consider where the currents originate and to where they will return and to determine the effects of the resulting voltage drops. This in turn requires some minimum amount of understanding of what goes on inside the circuits being decoupled and grounded. This information may be lacking or difficult to interpret when integrated circuits are part of the design.

Operational amplifiers are one of the most widely used linear I.C.'s, and fortunately most of them fall into a few classes, so far as the problems of power and grounding are concerned. Although the configuration of a system may pose formidable problems of decoupling and signal returns, some basic methods to handle many of these problems can be developed from a look at op-amps.

OP AMPS HAVE FOUR TERMINALS:

A casual look through almost any operational amplifier text might leave the reader with the impression that an ideal op-amp has three terminals: a pair of differential inputs and an output as shown in Figure 1. A quick review of fundamentals, however, shows that this can't be the case. If the amplifier has an output voltage it must be measured with respect to some point . . . a point to which the amplifier has a reference. Since the ideal op-amp has infinite common mode rejection, the inputs are ruled out as that reference so that there must be a fourth amplifier terminal. Another way of looking at it is that if the amplifier is to supply output current to a load, that current must get into the amplifier somewhere. Ideally, no input current flows, so again the conclusion is that a fourth terminal is required.

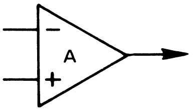


Figure 1. Conventional "Three Terminal" Op Amp

A common practice is to say, or indicate in a diagram, that this fourth terminal is "ground." Well, without getting into a discussion of what "ground" may be we can observe that most integrated circuit op-amps (and a lot of the modular ones as well) don't have a "ground" terminal. With these circuits the fourth terminal is one or both of the power supply terminals. There's a temptation here to lump together both supply voltages with the ubiquitous ground. And, to the extent that the supply lines really do present a low impedance at all frequencies within the amplifier bandwidth, this is probably reasonable. When the impedance requirement isn't satisfied, however, the door is left open to a variety of problems including noise, poor transient response, and oscillation.

DIFFERENTIAL TO SINGLE-ENDED CONVERSION:

One fundamental requirement of a simple op-amp is that an applied signal which is fully differential at the input must be converted to a single-ended output. Single ended, that is, with respect to the often neglected fourth terminal. To see how this can lead to difficulties, take a look at Figure 2.

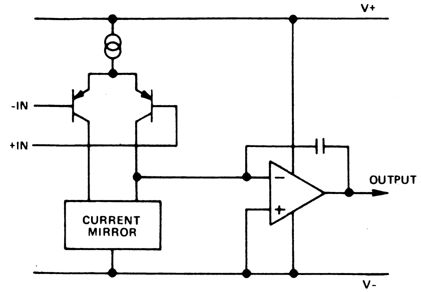


Figure 2. Simplified "Real" Op Amp

The signal flow illustrated by Figure 2 is used in several popular integrated circuit families. Details vary, but, the basic signal path is the same as the 101, 741, 748, 777, 4136, 503, 515, and other integrated circuit amplifiers. The circuit first transforms a differential input voltage into a differential current. This input stage function is represented by PNP transistors in Figure 2. The current is then converted from differential to single-ended form by a current mirror which is connected to the negative supply rail. The output from the current mirror drives a voltage amplifier and power output stage which is connected as an integrator. The integrator controls the open-loop frequency response, and its capacitor may be added externally, as in the 101, or may be self-contained, as in the 741. Most descriptions of this simplified model don't emphasize that the integrator has, of course, a differential input. It's biased positive by a couple of base emitter voltages, but, the non-inverting integrator input is referred to the negative supply.

It should be apparent that most of the voltage difference between the amplifier output and the negative supply appears across the compensation capacitor. If the negative supply voltage is changed abruptly the integrator amplifier will *force* the output to follow the change. When the entire amplifier is in a closed loop configuration the resulting error signal at its input will tend to restore the output, but, the recovery will be limited by the slew rate of the amplifier. As a result, an amplifier of this type may have outstanding low frequency power supply rejection, but, the negative supply rejection is fundamentally limited at high frequencies. Since it is the feedback signal to the input that causes the output to be restored, the negative supply rejection will approach zero for signals at frequencies above the *closed loop* bandwidth. This means that high-speed, high-level circuits can "talk to" low-level circuits through the common impedance of the negative supply line.

Note that the problem with these amplifiers is associated with the negative supply terminal. Positive supply rejection may also deteriorate with increasing frequency, but, the effect is less severe. Typically, small transients on the positive supply have only a minor effect on the signal output. The difference between these sensitivities can result in an apparent asymmetry in the amplifier transient response. If the amplifier is driven to produce a positive voltage swing across its rated load it will draw a current pulse from the positive supply. The pulse may result in a supply voltage transient, but, the positive supply rejection will minimize the effect on the amplifier output signal. In the opposite case, a negative output signal will extract a current from the negative supply. If this pulse results in a "glitch" on the buss, the poor negative supply rejection will result in a similar "glitch" at the amplifier output. While a positive pulse test may give the amplifier transient response, a negative pulse test may actually give you a pretty good look at your negative supply line transient response, instead of the amplifier response!

Remember that the impulse response of the power supply itself is not what is likely to appear at the amplifier. Thirty or forty centimeters of wire can act like a high Q inductor to add a high-frequency component to the normally overdamped supply response. A decoupling capacitor near the amplifier won't always cure the problem either, since the supply must be decoupled *to* somewhere. If the decoupled current flows through a long path, it can still produce an undesirable glitch.

Figure 3 illustrates three possible configurations for negative supply decoupling. In 3a the dotted line shows the negative signal current path through the decoupling and along the ground line. If the load "ground" and decoupled "ground" actually join at the power supply the "glitch" on the ground lines is similar to the "glitch" on the negative supply buss. Depending upon how the feedback and signal sources are "grounded" the effective disturbance *caused* by the decoupling capacitor may be larger than the disturbance which it was intended to prevent. Figure 3b shows how the decoupling capacitor can be used to minimize disturbance of V— and ground busses. The high-frequency component of the load current is confined to a loop which doesn't include any part of the ground path. If the capacitor is of sufficient size and quality, it will minimize the glitch on the negative supply without disturbing input or output signal paths. When the load situation is more complex, as in 3c, a little more thought is required. If the amplifier is driving a load that goes to a virtual ground, the actual load current does not return to ground. Rather, it must be supplied by the amplifier creating the virtual ground as shown in the figure. In this case, decoupling the negative supply of the first amplifier to the positive supply of the second amplifier closes the fast signal current loop without disturbing ground or signal paths. Of course, it's still important to provide a low impedance path from "ground" to V— for the second amplifier to avoid disturbing the input reference.

The key to understanding decoupling circuits is to note where the actual load and signal currents will flow. The key to optimizing the circuit is to bypass these currents around ground and other signal paths. Note, that as in figure 3a, "single point grounding" may be an oversimplified solution to a complex problem.

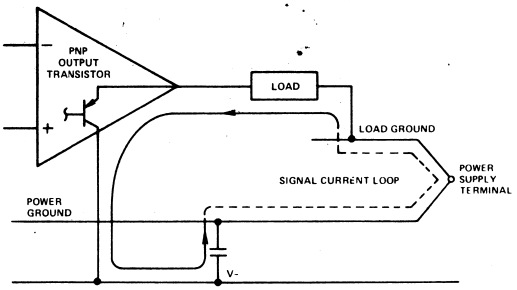


Figure 3a. Decoupling for Negative Supply Ineffective

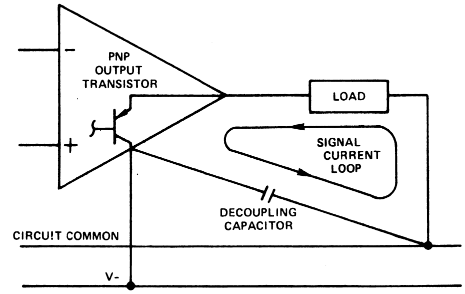


Figure 3b. Decoupling Negative Supply Optimized for "Grounded" Load

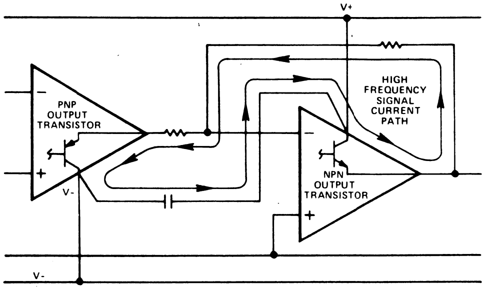


Figure 3c. Decoupling Negative Supply Optimized for "Virtual Ground" Load

Figure 3b and 3c have been simplified for illustrative purposes. When an entire circuit is considered conflicts frequently arise. For example, several amplifiers may be powered from the same supply, and an individual decoupling capacitor is required for each. In a gross sense the decoupling capacitors are all paralleled. In fact, however, the inductance of the interconnecting power and ground lines convert this harmless-looking arrangement into a complex L-C network that often rings like the "Avon Lady". In circuits handling fast signal wavefronts, decoupling networks paralleled by more than a few centimeters of wire generally mean trouble. Figure 4 shows how small resistors can be added to lower the Q of the undesired resonant circuits. The resistors can generally be tolerated since they convert a bad high-frequency jingle to a small damped signal at the op amp supply terminal. The residual has larger *low frequency* components, but, these can be handled by the op-amp supply rejection.

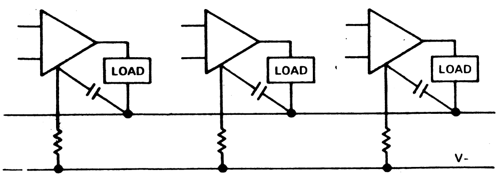


Figure 4. Damping Parallel Decoupling Resonances

FREQUENCY STABILITY:

There's a temptation to forget about decoupling the negative supply when the system is intended to handle only low-frequency signals. Granted that decoupling may not be required to handle low-frequency signals, but it may still be required for frequency stability of the op-amps.

Figure 5 is a more-detailed version of Figure 2 showing the output stage of the I.C. separated from the integrator (since this is the usual arrangement) and showing the negative power supply and wiring impedance lumped together as a single constant. The amplifier is connected as a unity gain follower. This makes a closed-loop path from the amplifier output through the differential input to the integrator input. There is a second feedback path from the collector of the output PNP transistor back to the other integrator input. The net input to the integrator is the difference of the signals through these two paths. At low frequencies this is a net, negative feedback. The high-frequency feedback depends upon both the load reactance and the reactance of the V− supply.

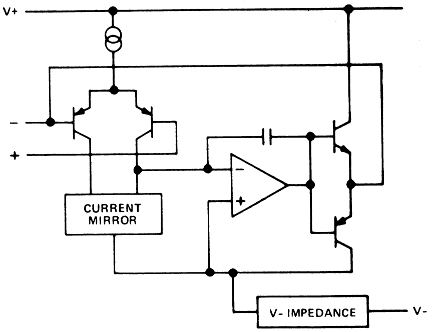


Figure 5. Instability Can Result from Neglecting Decoupling

When the supply lead reactance is inductive, it tends to destabilize the integrator. This situation is aggravated by a capacitive load on the amplifier. Although it's difficult to predict under exactly what circumstances the circuit will become unstable, it's generally wise to decouple the negative supply if there is any substantial lead inductance in the V− lead *or* in the common return to the load and amplifier input signal source. If the decoupling is to be effective, of course, it must be with respect to the *actual* signal returns, rather than to some vague "ground" connection.

POSITIVE SUPPLY DECOUPLING:

Up to this point we haven't considered decoupling the positive supply line, and with amplifiers typified by Figures 2 and 5 there may be no need to. On the other hand, there are a number of integrated circuit amplifiers which refer the compensating integrator to the positive supply. Among these are the 108, 504, and 510 families. When these circuits are used, it's the positive supply which requires most attention. The considerations and techniques described for the class of circuits shown in Figure 2 apply equally to this second class, but, should be applied to the positive supply rather than the negative.

FEED-FORWARD:

A technique which is most frequently used to improve bandwidth is called feed-forward. Generally, feed-forward is used to bypass an amplifier or level translator stage which has poor high frequency response. Figure 6 illustrates how this may be done. Each of the amplifiers shown is really a subcircuit, usually a single stage, in the overall amplifier. In the illustration, the input stage converts the differential input to a single-ended signal. The signal drives an intermediate stage (which in practice often includes level translator circuitry) which has low-frequency gain, but, limited bandwidth. The output of this stage drives an integrator-amplifier and output stage. The overall compensation capacitor feeds back to the input of the second stage and includes it in the integrator loop. The compromises necessary to obtain gain and level translation in the intermediate stage often limit its bandwidth and slow down the available integrator response. A feed-forward capacitor permits high-frequency signals to bypass this stage. As a result, the overall amplifier combines the low-frequency gain available from 3 stages with the improved frequency response available from a 2-stage amplifier. The feed-forward capacitor also feeds back to the non-inverting input of the intermediate stage. Note that the second stage is not an integrator, as it may appear at first glance, but actually has a positive feedback connection. Fed-forward amplifiers must be carefully designed to avoid internal oscillations resulting from this connection. Improper decoupling can upset this plan and permit this loop to oscillate.

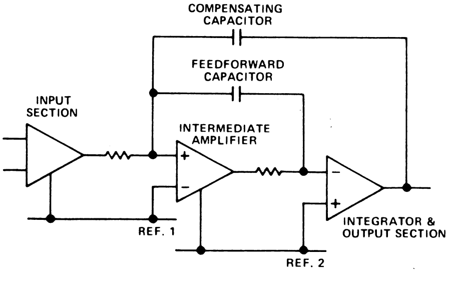


Figure 6. Fast Fed-Forward Amplifier

Note that the internal input stages are shown as being referred to separated reference points. Ideally, these will be the same reference so far as signals are concerned, although they may differ in bias level. In practice this may not be the case. Examples of fed-forward amplifiers are the AD518, the AD118, and the OP-05. In these amplifiers, signal Reference 1 is the positive supply, while signal Reference 2 is the negative supply. Signals appearing between the positive and negative supply terminals are effectively inserted inside the integrator loop!

Obviously, while feed-forward is a valuable tool for the high-speed amplifier designer, it poses special problems in application. A thoughtful approach to decoupling is required to maximize bandwidth and minimize noise, error, and the likelihood of oscillation.

Some fed-forward amplifiers have other arrangements, which include the "ground" terminal in inverting only amplifiers. Almost without exception, however, signals between some combination of the supply terminals get "inside" the amplifier. It is vital to proper operation that the involved supply terminals present a common low impedance at high frequencies. Many high-speed modular amplifiers include appropriate capacitive decoupling within the amplifier, but, with I.C. op amps this is impossible. The user must take care to provide a cleanly decoupled supply for fed-forward amplifiers. Figure 7 shows a decoupling method which may be applied to the AD518 as well as to other fast fed-forward amplifiers such as the 118. One capacitor is used to provide a low-impedance path between the supply terminals at high frequencies. The resistor in the V+ lead insures that noise on the supply lines will be rejected *and* prevents the establishment of resonances with other decoupling circuits. The second capacitor decouples the low side of the integrator to the load.

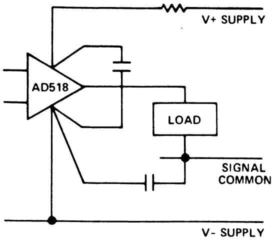


Figure 7. Decoupling for a Fed-Forward Amplifier

Alternatives include a resistor in both supply leads and/or decoupling from V+ to the load. In principle, the positive and negative supply should be tied in a "tight knot" with the signal return. To the extent that this cannot be done, there is a slight advantage to favoring the negative supply due to the high frequency limitations of PNP transistors used in junction-isolated I.C.'s.

OTHER COMPENSATION:

While most integrated circuit amplifiers use one of the three compensation schemes already described, a significant fraction use some other plan. The 725 type amplifiers combine a V− referred integrator with a network which the manufacturers recommend to be connected from signal ground to the integrator input. This makes the circuit extremely liable to pick up noise between V− and ground. In many circumstances it may be wiser to connect the external compensation to the negative supply, rather than to signal ground.

One more class of amplifiers is typified by the Analog Devices AD507 and AD509. In these circuits, a single capacitor may be used to induce a dominant pole of response without resorting to an integrator connection. The high-frequency response of the amplifier will appear with respect to the "ground" end of the compensation capacitor. In these amplifiers a small internal capacitance is connected between V+ and the compensation point. Unity gain compensation can be added in parallel and the pin-out is arranged to make this simple. The free end of the compensation capacitor can also be connected either to V− or signal common. It is extremely important that the signal common and the compensation connect directly or through a low-impedance decoupling.

Although the main signal path of these amplifiers can be compensated in a variety of ways, some care is required to insure the stability of internal structures. It's always wise to use extra care in decoupling wideband amplifiers to avoid problems with the output stage and other subcircuits which are similar to the main integrator problem illustrated by Figure 5. An effective compensation and decoupling circuit for the AD509 is shown in Figure 8. This arrangement is similar to Figure 7, and one of these two circuits is likely to be suitable for many types of wideband amplifier. Depending upon the power distribution, a small (10Ω to 50Ω) resistor may be appropriate in both of the supply leads to reduce power lead resonance and interference both to and from circuits sharing the power supply.

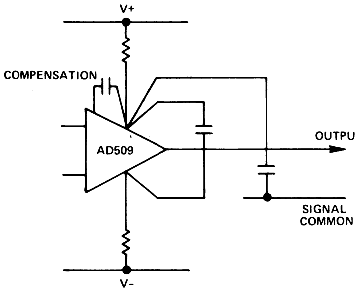


Figure 8. Decoupling a Wideband Amplifier

GROUNDING ERRORS:

Ground in most electronic equipment is not an actual connection to earth ground, but a common connection to which signals and power are referred. It is frequently immaterial to the function of the equipment whether or not the point actually connects to earth ground. I myself prefer some distinguishing name or names for these common points to emphasize that they must be *made* common. The term "ground" too often seems to be associated with a sort of cure-all concept, like snake oil, money or motherhood. If you're one of those who regards ground with the same sort of irrational reverence that you hold for your mother, remember that while you can always trust your mother, you should *never* trust your "ground." Examine and think about it.

It's important to have a look at the currents which flow in the ground circuit. Allowing these currents to share a path with a low-level signal may result in trouble. Figure 9 illustrates how careless grounding can degrade the performance of a simple amplifier. The amplifier drives a load which is represented by the load resistor. The load current comes from the power supply and is controlled by the amplifier as it amplifies the input signal. This current must return to the supply by some path; suppose that points A and B are alternative power supply "ground" connections. Assuming that the figure represents the proper topology or ordering of connections along the "ground" bus, connecting the supply at A will cause the load current to share a segment of wire with the input signal connection. Fifteen centimeters of number 22 wire in this path will present about 8 milliohms of resistance to the load current. With a 2k load, a 10-volt output signal will result in about 40 microvolts between the points marked "ΔV." This signal acts in series with the non-inverting input and can result in significant errors. For example, the typical gain of an AD510 amplifier is 8 million so that only $1\frac{1}{4}\mu V$ of input signal is required to produce a 10 volt output. The $40\mu V$ ground error signal will result in a 32 times increase in the circuit gain error! This degradation could easily be the most serious error in a high-gain precision application. Moreover, the error represents positive feedback so that the circuit will latch up or oscillate for large closed-loop gains with R_f/R_i greater than about 250k.

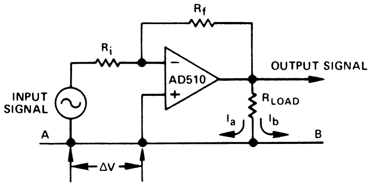


Figure 9. Proper Choice of Power Connections Minimizes Problems

Reconnecting the power supply to point B will correct the problem by eliminating the common impedance feedback connection. In a real system, the problem may be more complex. The input signal source, which is represented as floating in Figure 9, may also produce a current which must return to the power supply. With the supply at point B, any current which flows in additional loads (other than R_i) may interfere with the operation of the amplifier shown. Figure 10 illustrates how amplifiers can be cascaded and still drive auxiliary loads without common impedance coupling. The output currents flow through the auxiliary loads and back to the power supply through power common. The currents in the input and feedback resistors are supplied from

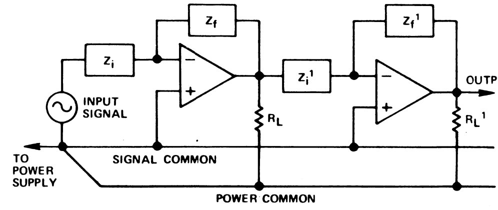


Figure 10. Minimizing Common Impedence Coupling

the power supply by way of the amplifiers as previously illustrated in Figure 3c. The only current flowing in signal common is the amplifier's input current, and its effect is generally negligibly small.

Having given an example of a simple "grounding error" and its solution, I will now get back on my soap box and say that grounding errors result from neglect based on the assumption that a ground, is a ground, is a ground. *Some* impedance will be present in any interconnection path, and its effect should be considered in the overall design of a system. Quantitative approaches are quite useful in specialized applications. In fast TTL and ECL logic circuitry the characteristic impedance of interconnections is controlled so that proper terminations can reduce problems. In RF circuitry the unavoidable impedances are taken into account and incorporated into the design of the circuit. With op-amp circuitry, however, impedance levels do not lend themselves to transmission line theory, and the power and ground impedances are difficult to control or analyze. The most expedient procedure, short of difficult and restrictive quantitative analysis, seems to be to arrange the unavoidable impedances so as to minimize their effects and arrange the circuitry to overcome the effects. Figures 9 and 10 illustrate the sort of simple considerations which can substantially reduce practical ground problems. Figure 11 illustrates how circuitry can be used to reduce the effect of ground problems which can't be corrected by topological tricks.

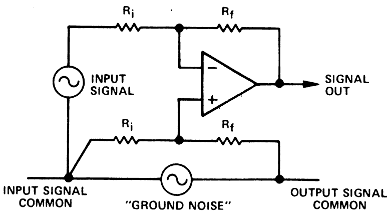


Figure 11. Subtractor Amplifier Rejects Common Mode Noise

GETTING AROUND THE PROBLEM:

In Figure 11 a subtractor circuit is used to amplify a normal mode input signal and reject a ground noise signal which is common to both sides of the input signal. This scheme uses the common-mode rejection of the amplifier to reduce the noise component while amplifying the desired signal. An important aspect of this arrangement, which is often overlooked, is that the amplifier should be powered with respect to the *output* signal common. If its power pins are exposed to the high-frequency noise of the input common, the compensation capacitor will direct the noise right to the output and defeat the purpose of the subtractor. It's just this kind of effect which makes it important to use care in grounding and decoupling. A subtractor or dynamic bridge, like Figure 11, will be ineffective in correcting a grounding problem if the amplifier itself is carelessly decoupled. In general, an op-amp should be decoupled to the point which is the reference for measuring or using its output signal. In "single-ended" systems it should also be decoupled to the input signal return as well. When it is impossible to satisfy both these requirements at once, there's a high probability of either a noise or oscillation problem or both. Frequently the difficulty can be resolved with a subtractor, like Figure 11, where a network like the single-ended feedback network (which needn't be all resistive) joins the input and output signal reference points and provides a "clean" reference point for the non-inverting input of the amplifier.

A problem with the subtractor is that it uses a balanced bridge to reject the common mode signal between the input and output reference points. The arms of the network must be carefully balanced, since to the extent they don't match, the unwanted signal will be amplified. Although even a poorly matched network will probably eliminate oscillation problems, noise rejection will suffer in direct proportion to any mismatches. An easier way to reject large "ground noise" signals is to use a true instrumentation amplifier.

INSTRUMENTATION AMPLIFIERS:

A true instrumentation amplifier has a very visible "fourth terminal." The output signal is developed with respect to a well defined reference point which is usually a "free" terminal that may be tied to the output signal common. The instrumentation amplifier also differs from an op amp in that the gain is fixed and well defined, but there is no feedback network coupling input and output circuits. Figure 12 shows how an instrumentation amplifier can be used to translate a signal from one "ground reference" to another. The normal mode input signal is developed with respect to one reference point which may be common to its generating circuits. The signal is to be used by a system which has an interfering signal between its own common and the signal source. The instrumentation amplifier has a high impedance differential input to which the desired signal is applied. Its high common mode rejection eliminates the unwanted signal and translates the desired signal to the output reference point. Unlike the dynamic bridge circuit, the gain and common mode rejection don't depend on a network connecting the input and output circuits. The gain is set, in Figure 12, by the ratio of a pair of resistors which are connected inside the amplifier. The amplifier has a very high input impedance, so that gain and common mode rejection are not greatly affected by variations or unbalance in source impedance.

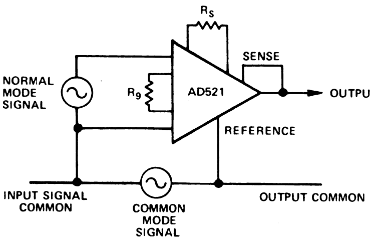


Figure 12. Applying an In-Amp

Since instrumentation amplifiers have a reference or "ground" terminal, they have the potential to be free of the power supply sensitivities of op amps. In practice, however, most instrumentation amplifiers have internal frequency compensation which is referred to the power supply. In the case of the AD521, the compensation integrator is referred to the negative supply terminal. The decoupling of this terminal is particularly important, and it should be decoupled with respect to the output reference terminal, or actually to the point to which this terminal refers. The AD520 instrumentation amplifier, on the other hand, has an internal integrator which is referred to the positive supply terminal. For best results both the V+ and V− terminals should be decoupled to the output reference point.

THE "OTHER" INPUT:

Most I.C. op-amps and in-amps include offset voltage nulling terminals. These terminals generally have a small voltage on them and by loading the terminals with a potentiometer the amplifier offset voltage can be adjusted. While their impedance level is much lower than the normal input, the null terminals can act as another differential input to the amplifier. Although the null terminals aren't generally looked at as inputs, most amplifiers are quite sensitive to signals applied here. For example, in 741 family amplifiers the output voltage gain from the null terminals is greater than the gain from the normal input!

An illustration of the type of problems that can arise with the "other" input is shown in Figure 13. The figure is an op-amp circuit with some of the offset null detail shown.

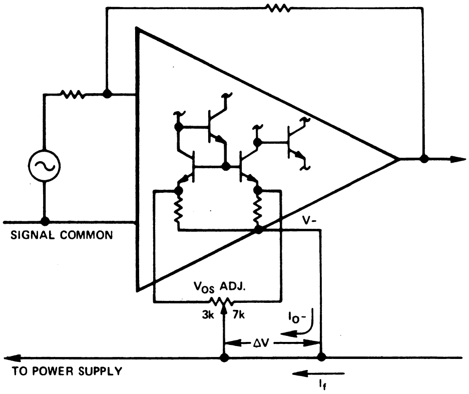


Figure 13. Details of V_{OS} Nulling – the "Other" Input

As it's drawn, the V_{OS} null pot wiper connects to a point along a V− "clothesline" which carries both the return current from the amplifier and currents from other circuits back to the power supply. These currents will develop a small voltage, ΔV, along the conductor between the amplifier V− terminal and the null pot wiper. If the null pot is set on center, the equal halves will form a balanced bridge with the resistors inside the amplifier. The effect of the voltage generated along the wire is balanced at the V_{OS} terminals and will have little effect on the amplifier output. On the other hand, if the null pot is unbalanced, to correct an amplifier offset, the bridge will no longer balance. In this case voltages developed along the "clothesline" will result in a difference voltage at the V_{OS} terminals. For instance, suppose that a 10k null pot balances out the op amp offset when it is set with 3k and 7k branches as shown in the figure. In a 741 the internal resistors are about 1k so that the difference signal at the V_{OS} terminals will be about 1/8 ΔV. The gain from these terminals is about twice the gain from the normal input, so that the disturbance acts as if it were an input signal of about 1/4 ΔV. Using the same assumptions as in the discussion of Figure 9. the current I_{O-} will result in a 10 microvolt input error signal. In this case, however, the error will appear *only* when the amplifier load current comes from the negative supply. When the load is driven positive the error will disappear. As a result, the V_{OS} input signal will result in distortion rather than a simple gain error!

An additional problem is created by I_f, a current returning to the power supply from other circuits. The current from other circuits is not generally related to the op amp signal, and the voltage developed by it will manifest itself as noise. This signal at the null terminals can easily be the dominant noise in the system. A few milliamps of V− current through a few centimeters of wire can result in interference which is orders of magnitude larger than the inherent input noise of the amplifier. The remedy is to make the connection from the null pot wiper direct to the V− pin of the amplifier, as shown in Figure 14. Some amplifiers such as the AD504 and AD510 refer to the null offset terminals to V+. Obviously, the pot wiper should go to the V+ terminal of this type of amplifier. It's important to connect the line directly to the op amp terminal so as to minimize the common impedance shared by the op amp current and the null pot connection.

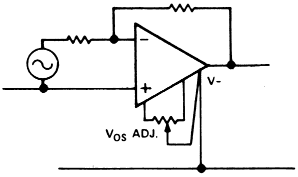


Figure 14. Connecting the Null Pot for Trouble Free Operation

The considerations for op-amp null pots also apply to the similar trimmers on almost all types of integrated circuits. For example, the AD521 In-Amp null terminals exhibit a gain of about 30 to the output. Although this is much less than in the case of most op-amps, it still warrants care in controlling the null pot wiper return. Table 1 lists the integrated circuits manufactured by Analog Devices, including some popular second-source families, and indicates how internal conversions from differential to single ended are referred. That is, the signals are made to appear with respect to the terminal(s) listed.

	Internal Integrator Referred to:	Comments
AD502	V-	
AD503	V-	
AD504	V+	External Cap
AD506	V-	
AD507	–	External Cap to Signal Common or V+
AD509	–	External Cap to Signal Common or V+
AD510	V+	
AD511	V-	
AD512	V-	
	V-, -in	External Caps, Optional Feedforward to -in
AD514	V-	
AD515	V-	
AD517	V+	
AD518	V+, V-	Internal Feedforward Cap V+ to V- and Integrator to Output
AD520	V+, V-	Internal Integrator Refers to V+, Internal Input Stage Cap Refers to V-, External Output Caps Refer to V+ and Common
AD521	V-	Output Amplifier Integrator Refers to V-
AD522	V+, V-	Input Amplifier Refers to V+ Output Amplifier Refers to V-
AD523	V-	
AD528	V+, V-	Internal Feedforward Cap V+ to V- and Integrator to Output
AD530	V+	Multiplier Output Amplifier Integrator Refers to V+
AD531	V+	Multiplier Output Amplifier Integrator Refers to V+
AD532	V+	Multiplier Output Amplifier Integrator Refers to V+
AD533	V+	Multiplier Output Amplifier Integrator Refers to V+
AD534	V-	Output Amplifier
AD535	V-	Output Amplifier
AD536A	V-, V+, Common	External Integrator to V+, Internal Feedforward V- to Common
AD537	V-	Internal Buffer Amp
AD540	V-	
AD542	V-	
AD544	V-	
AD545	V-	
AD559	V-, Common	DAC Control Loop Integrator Referred Between V- and Common
AD561	V-, Common	DAC Control Loop Integrator and Ref. Amp Refer to Common Ref. Bias Amp Refers to V-
AD562	V-	DAC Control Loop Integrator Referred to V-. Reference Input Common to Control Loop Isolated from DAC Output Common
AD563	V-	DAC Control Loop Integrator Referred to V-. Reference Input Common to Control Loop Isolated from DAC Output Common
AD565	V-	DAC Control Loop Integrator Referred to V-. Reference Input Common to Control Loop Isolated from DAC Output Common
AD566	V-	DAC Control Loop Integrator Referred to V-, Reference Input Common to Control Loop Isolated from DAC Output Common
AD580	V-	
AD581	V-	
AD582	V-	
AD584	V-	
AD101A	V-	External Cap (Includes AD201A, AD301A, etc.)
AD108	V+	External Cap (Includes AD208, AD308, etc.)
AD741	V-	Internal Cap (Includes 741J, K, L, etc.)

TABLE 1

This collection of examples won't solve all your potential grounding problems. I hope that it will give you some good ideas about how to prevent some of them, and it should also give you some of the "inside story" on I.C.'s which you can put to work in very practical ways. There is no general grounding method which will prevent all possible problems. The only generally applicable rule is attention to detail, and remember that you can always trust your mother, but. . .

ANALOG DEVICES **APPLICATION NOTE**

A User's Guide
to
IC Instrumentation Amplifiers

by Jeffrey R. Riskin
Manager of Microcircuits Applications Engineering

INTRODUCTION

It is traditional to begin a discussion of instrumentation amplifiers by saying that an IA is not an operational amplifier. As obvious as this statement is to the informed user, and as awkward as a description by exclusion may be, such an approach is inevitable and perhaps necessary. When an engineer needs a signal conditioning gain block, the first thought that springs to mind is the nearly ultimate flexibility provided by the currently available assortment of low-cost IC op amps. It may well be that an op amp will suffice as an element in a given gain block, but in demanding applications, op amp circuitry will often require extensive and expensive additional circuit elements, specialized manufacturing and/or test instrumentation together with highly skilled personnel to make it all work. The purpose of this article is to explain when and where an instrumentation amplifier may best be employed and where its unique virtues give it an advantage over the more flexible op amp.

WHAT IS AN INSTRUMENTATION AMPLIFIER?

An instrumentation amplifier is a precision differential voltage gain device that is optimized for operation in an environment hostile to precision measurement. The real world is characterized by deviations from the ideal; temperature fluctuates, electrical noise exists, and voltage drops caused by current through the resistance of leads from remote locations are dictated by the laws of physics. Furthermore, real transducers rarely exhibit zero output impedance and nice neat zero-to-ten-volt ranges. Induced, leaked or coupled electrical interference (noise) is always present to some extent. In brief, even the best "cookbook" must be taken with a grain of salt.

Instrumentation amplifiers are intended to be used whenever acquisition of a useful signal is difficult. IA's must have extremely high input impedances because source impedances may be high and/or unbalanced. Bias and offset currents are low and relatively stable so that the source impedance need not be constant. Balanced differential inputs are provided so that the signal source may be referenced to any reasonable level independent of the IA output load reference. Common mode rejection, a measure of input balance, is very high so that noise pickup and ground drops, characteristic of remote sensor applications, are minimized.

Care is taken to provide high, well-characterized stability of critical parameters under varying conditions, such as changing temperatures and supply voltages. Finally, all components that are critical to the performance of the IA are internal to the device (with the exception of a single gain-determining resistor or resistor-pair). The manufacturer may then optimize, characterize and guarantee the specifications, while the user may in turn depend on a certain level of performance without having to provide his own precision application components or design expertise.

The precision of an IA is provided at the expense of flexibility. By committing to the one specific task of amplifying voltage, the IA manufacturer may optimize performance in this area. An IA is not intended to perform integration, differentiation, rectification, or any other non-voltage-gain function; although possible with an IA, these tasks are best left to operational amplifiers.

To put an instrumentation amplifier to work, the potential user does not require an intimate knowledge of its internal construction. Figure 1, a functional diagram of a basic IA, provides sufficient information for many applications.

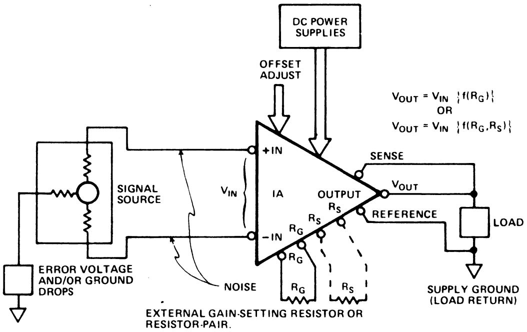

DC POWER SUPPLIES
OFFSET ADJUST
$V_{OUT} = V_{IN} \{f(R_G)\}$
OR
$V_{OUT} = V_{IN} \{f(R_G, R_S)\}$
+IN
SENSE
SIGNAL SOURCE
V_{IN}
IA
OUTPUT
V_{OUT}
R_S
R_S
R_G
REFERENCE
LOAD
−IN
R_G
ERROR VOLTAGE AND/OR GROUND DROPS
NOISE
R_G
R_S
SUPPLY GROUND (LOAD RETURN)
EXTERNAL GAIN-SETTING RESISTOR OR RESISTOR-PAIR.

Figure 1. Basic Instrumentation Amplifier Functional Diagram

The two inputs shown permit direct interface to "floating" signal sources. The IA, being truly differential, detects only the difference in voltage between its inputs; any common-mode signals (signals present on both inputs), such as noise and voltage drops in ground lines, are subtracted and cancelled at the inputs before amplification takes place.*

A single resistor or resistor-pair is used to program the IA for the desired gain. The manufacturer will provide a transfer function or gain equation that allows the user to calculate the required values of resistance for a given gain. Special requirements for that resistor or resistors, if any, are also spelled out by the manufacturer.

The output is single-ended and is designed to drive ground-referenced loads as normally found in measurement equipment. The load reference is common to the power supply return although careful consideration must be given to the overall grounding system (more on that later).

Of course, power must be supplied to the IA; as with op amps, this is normally a differential balanced voltage that may be varied over a specified range.

Most instrumentation amplifiers provide some means of adjusting offset voltage (that dc error voltage present at the output when both inputs are grounded). This adjustment is usually made by varying the setting of an external potentiometer. Sense and reference terminals allow remote sensing of output voltage so that effects of IR drops and ground drops may be minimized. For low current non-remote loads, the sense terminal may be tied directly to the output while the reference terminal may be tied to power supply common. There are other uses for sense and reference that will be discussed in the applications section of this article.

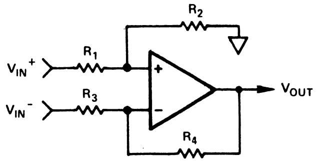
INSIDE AN INSTRUMENTATION AMPLIFIER

While there are many ways of designing an instrumentation amplifier, most such designs can be classified into one of two categories. The most common configuration consists of a number of interconnected operational amplifiers and a precision resistor network. This technique is popular in modular and hybrid instrumentation amplifiers where most practical designs utilize a minimum number of components. Examples are the modular Analog Devices model 605 and hybrid AD522 IA's.

In the other category are designs that, instead of employing op amps, use fundamental active-circuit elements, such as differential circuits and controlled current sources and reflectors; this eliminates all unnecessary or redundant features and tends to minimize active device (transistor) count and decrease the dependence upon accurate resistor matching. This technique is most often employed in the design of monolithic IA's where cost is inversely proportional to chip size. Examples are the monolithic Analog Devices AD520 and AD521 IC IA's. Some older modular IA's (such as the Analog Devices models 602 & 603) also use this technique because suitably precise IC op amps have only recently become readily available. Newer modular IA's may also use this technique because nonlinearity tends to be lower at high gains, although some sacrifice of linearity may exist at lower gains. Examples are the Analog Devices models 606 & 610.

Op Amp Based IA's

The most simple (and crude) method of implementing a differential gain block with op amps is shown in Figure 2.



$$V_{OUT} = V_{IN}^+ \left(\frac{R_2}{R_1 + R_2}\right)\left(\frac{R_3 + R_4}{R_3}\right) - V_{IN}^- \left(\frac{R_4}{R_3}\right)$$

Figure 2. Differential Input Voltage Gain Block (Simple Subtractor)

In this circuit, an expressions for V_{OUT} can be derived by superposition.

The output for V_{IN}^+ (V_{IN}^- grounded) is:

$$V_{O_1} = V_{IN}^+ \left(\frac{R_2}{R_1 + R_2}\right)\left(\frac{R_3 + R_4}{R_3}\right) \qquad (1)$$

The output for V_{IN}^- (V_{IN}^+ grounded) is:

$$V_{O_2} = -V_{IN}^- \left(\frac{R_4}{R_3}\right) \qquad (2)$$

By superposition:

$$\begin{aligned} V_O &= V_{O_1} + V_{O_2} \\ &= V_{IN}^+ \left(\frac{R_2}{R_1 + R_2}\right)\left(\frac{R_3 + R_4}{R_3}\right) - V_{IN}^- \left(\frac{R_4}{R_3}\right) \end{aligned} \qquad (3)$$

If $R_2 = R_4$, $R_1 = R_3$:

$$V_O = \left(V_{IN}^+ - V_{IN}^-\right) \frac{R_4}{R_3} \qquad (4)$$

Thus, we have created a simple differential voltage amplifier. The input impedances, however, are low and unequal. Furthermore, all 4 resistors have to be carefully ratio-matched to maintain good common mode rejection:

$$\begin{aligned} V_{OUT\,CM} &= V_{OUT} \text{ for } V_{IN}^+ = V_{IN}^- \\ &= V_{IN} \left[\left(\frac{R_2}{R_1 + R_2}\right)\left(\frac{R_3 + R_4}{R_3}\right) - \left(\frac{R_4}{R_3}\right)\right] \end{aligned} \qquad (5)$$

If we are looking for a gain of 1, all resistors will be equal. For a 0.1% mismatch in just one of the resistors:

$$R_1 = R_3 = R_4 = R$$

$$R_2 = 0.999R$$

$$\begin{aligned} V_{O\,CM} &= V_{IN} \left[\left(\frac{0.999R}{1.999R}\right)\left(\frac{2R}{R}\right) - \left(\frac{R}{R}\right)\right] \\ &= 0.0005 V_{IN} \end{aligned} \qquad (6)$$

$$CMR = 66dB$$

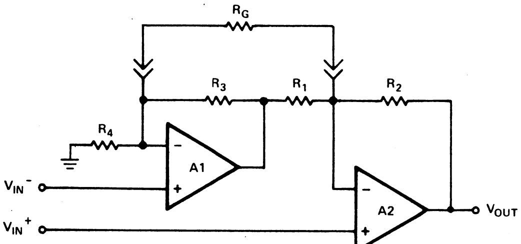
(Note that if the source resistance is not low and balanced, gain and CMR will be further degraded.)

---

*For applications involving extremely high common-mode voltages, or requiring complete galvanic isolation, *isolation amplifiers* should be used. Analog Devices manufactures a complete line of single and multi-channel isolators.

Considering what is available in the way of reasonably priced standard resistors, one can hardly expect to improve upon this mediocre level of performance. Considering the several serious drawbacks, it is not surprising that this configuration is not used in true instrumentation amplifier designs.

The two-amplifier approach shown in Figure 3 overcomes some of the weaknesses inherent in the simple subtractor of Figure 2.



IF $\frac{R_2}{R_1} = \frac{R_4}{R_3}$, $V_{IN} = V_{IN}^+ - V_{IN}^-$

$\frac{V_{OUT}}{V_{IN}} = 1 + \frac{R_2}{R_1} + \frac{2R_2}{R_G}$

Figure 3. "Two-Amplifier" Instrumentation Amplifier

Input resistance is high, thus permitting the signal sources to have unbalanced, non-zero output impedance. Furthermore, gain may be changed by switching only one resistor thus allowing CMR to remain constant once initial trimming is accomplished. (CMR is still dependent upon the ratio-matching of four resistors.) The major disadvantage to this design is that the common mode voltage input range is a function of gain and can thus be very poor. By referring to Figure 3, it can be seen that A1 is called upon to amplify a common mode signal by the ratio $(R_3 + R_4)/R_4$; this could lead to saturation of A1 thus leaving no "headroom" to amplify the differential signal of interest. A few modules and hybrids use this configuration because of its simplicity, but it is not optimal.

The most popular configuration for op-amp based instrumentation amplifiers is shown in Figure 4:

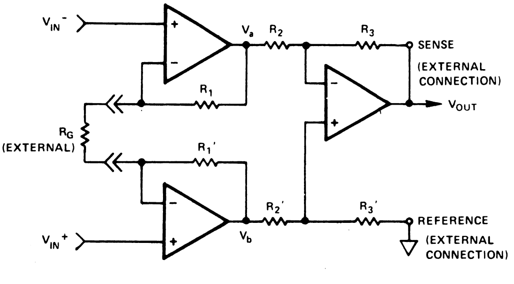


Figure 4. "Classic" 3 Op Amp Instrumentation Amplifier

The transfer function of this circuit can be calculated by superposition.

For $V_{IN}^+ = 0$

$$V_a = V_{IN}^- \left(\frac{R_1 + R_G}{R_G}\right) \tag{7}$$

$$V_b = V_{IN}^- \left(\frac{R_1'}{R_G}\right) \tag{8}$$

For $V_{IN}^- = 0$

$$V_a = V_{IN}^+ \left(\frac{R_1}{R_G}\right) \tag{9}$$

$$V_b = V_{IN}^+ \left(\frac{R_1' + R_G}{R_G}\right) \tag{10}$$

$$\therefore \quad V_a = V_{IN}^- \left(\frac{R_1 + R_G}{R_G}\right) - V_{IN}^+ \left(\frac{R_1}{R_2}\right) \tag{11}$$

$$\text{and } V_b = V_{IN}^+ \left(\frac{R_1' + R_G}{R_G}\right) - V_{IN}^- \left(\frac{R_1'}{R_G}\right) \tag{12}$$

$$V_{OUT} = -\left(\frac{R_3}{R_2}\right) V_a + V_b \left(\frac{R_3'}{R_2' + R_3'}\right) \left(\frac{R_3 + R_2}{R_2}\right) \tag{13}$$

If $R_3 = R_3'$, $R_2 = R_2'$, and $R_1 = R_1'$

$$V_{OUT} = (V_b - V_a) \left(\frac{R_3}{R_2}\right) \tag{14}$$

substituting for V_b and V_a and simplifying

$$V_{OUT} = (V_{IN}^+ - V_{IN}^-) \left(\frac{2R_1}{R_G} + 1\right) \left(\frac{R_3}{R_2}\right) \tag{15}$$

In this configuration, gain accuracy and CMR still depends upon the ratio-matching of R_2, R_2', R_3 and R_3'. It can be shown, however, that CMR does *not* depend on the matching of R_1 and R_1'.

$$V_{CM\ OUT} = (V_a - V_b) = V_{IN}^+ \left(\frac{R_1 + R_G}{R_G}\right) - V_{IN}^- \left(\frac{R_1}{R_G}\right) - V_{IN}^- \left(\frac{R_1' + R_G}{R_G}\right) + V_{IN}^+ \left(\frac{R_1'}{R_G}\right) \tag{16}$$

but $V_{CM\ IN} = V_{IN}^+ = V_{IN}^-$

$$V_{CM\ OUT} = V_{CM\ IN} \left[\frac{R_1 + R_G}{R_G} - \frac{R_1}{R_G} - \frac{R_1' + R_G}{R_G} + \frac{R_1'}{R_G}\right] \tag{17}$$

$$= V_{CM\ IN} \left[\frac{R_1}{R_G} - \frac{R_1}{R_G} + 1 - \frac{R_1'}{R_G} + \frac{R_1'}{R_G} - 1\right] \tag{18}$$

$$= V_{CM\ IN} \left[0\right]$$

$$= 0$$

Therefore, in theory at least, the user may take as much gain in the front end as he wishes (as determined by R_G) without increasing the common mode error signal. Thus, CMRR will theoretically increase in direct proportion to gain, a very useful property. Furthermore, common-mode signals are only amplified by a factor of 1 regardless of gain because no common-mode voltage will appear across R_G, hence, no common-mode current will flow in it (the input terminals of an op-amp operating normally will have no significant potential difference between them). This means that large common-mode signals may be handled independent of gain.

Finally, because of the symmetry of this configuration, first order common-mode error sources in the input amplifiers, if they track, tend to be cancelled out by the output stage subtractor. These features explain the popularity of this IA design technique; examples include the Analog Devices module model 605 and the hybrid AD522. Both of these products are characterized by their extremely high precision.

IA's of this type may use either FET or Bipolar input operational amplifiers. FET input devices have very low bias currents and are well-suited for use with very high source impedances. FET input op amps, however, generally have poorer CMR than bipolar amplifiers due to non-geometry related mis-matches. (In other words, matching of FET's is largely a function of process control; matching bipolar transistors is less process dependent.) This will manifest itself in lower linearity and CMR for large input voltages. Furthermore, these mis-matches usually cause larger input offset voltage drifts. For these reasons, Analog Devices instrumentation amplifiers use bipolar input stages thus sacrificing low bias currents to achieve high linearity and CMR along with low input offset voltage drift. As technology develops, FET input IA's may become more viable.

Dedicated Design IA's

The second category of IA design is based on minimum active device count; a virtue for monolithic IC circuits. The basic schematic for such a design is shown in Figure 5.

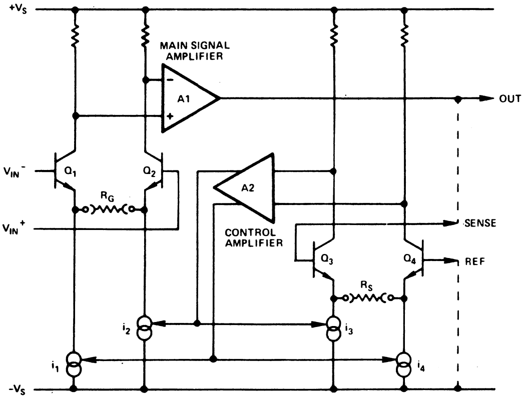


Figure 5. Typical IC IA Basic Schematic

Forward gain is provided by the input differential stage Q_1 and Q_2 whose current gain (transconductance) is $1/R_G$ (amps/volt) and the main signal amplifier A_1 which senses differences in input stage collector currents. When the output is connected back to sense (with reference grounded) differential stage Q_3 and Q_4 acts as a feedback error-sensing amplifier with a transconductance of $1/R_S$ (amps/volt). A_2 senses the collector current imbalance in that stage.

When a differential voltage is applied to the inputs, the collector currents of Q_1 and Q_2 tend to become unbalanced by $(V_{IN}^+ - V_{IN}^-)/R_G$. This is sensed by A_1 which develops an error voltage between the sense and reference points. This, in turn, tries to unbalance the collector currents in Q_3 and Q_4 by $(V_{SENSE} - V_{REF})/R_S$. That unbalance is sensed by A_2 which then adjusts I_3 and I_4 to equalize the collector currents in Q_3 and Q_4 $(I_4 - I_3 = (V_S - V_R)/R_S)$. A_2 simultaneously adjusts I_1 and I_2 such that $I_1 - I_2 = I_4 - I_3$. Balance is reached when:

$$\frac{V_S - V_R}{(I_4 - I_3)\,R_S} = \frac{V_1 - V_2}{(I_1 - I_2)\,R_G} \qquad (19)$$

$$\text{if } \frac{V_S - V_R}{V_1 - V_2} = \frac{V_{OUT}}{V_{IN}} = \text{Gain} \qquad (20)$$

and $I_4 - I_3 = I_1 - I_2$

$$\text{Gain} = \frac{R_{SCALE}}{R_{GAIN}} \qquad (21)$$

It is apparent from this analysis that the requirement for carefully matched resistors changes to a requirement for carefully matched active devices. In IC technology, this is possible by utilization of precision photographic techniques along with careful design layout and well-controlled processing. The result is a good trade-off between high performance and low cost.

This design configuration describes the Analog Devices AD520, the industry's first monolithic IC IA. The AD521 is a second-generation monolithic IA offering improved performance at a reduced cost.*

INSTRUMENTATION AMPLIFIER SPECIFICATIONS

To successfully apply any electronic component, a full understanding of its specifications is required. That is to say, the numbers contained in a spec sheet are of little value if the user doesn't have a clear picture of what each spec means. In this section, a typical instrumentation amplifier specification sheet will be reviewed. Each individual specification will be discussed in terms of how it is measured and what error it might contribute to the overall performance of the circuit. In some cases, a given specification may not affect a particular application; the more common situations of this type will be discussed.

Table 1 is the specification sheet for the Analog Devices AD522 instrumentation amplifier, chosen for its rather complete characterization and its varity of available versions.

At the top of the spec sheet is the statement that the listed specs are typical @ $V_S = \pm 15V$, $R_L = 2k\Omega$ and $T_A = +25^\circ C$ unless otherwise specified. This tells the user that these are the normal operating conditions under which the device is tested. Deviations from these conditions might degrade (or improve) performance. When deviations from the "normal" conditions are likely (such as a change in temperature) the significant effects are usually indicated within the specs. This statement also tells us that all numbers are typical unless noted; "typical" means that the manufacturers characterization process has shown this number to be average, but individual devices may vary.

Specifications not discussed in detail are self-explanatory and require only a basic knowledge of electronic measurements. Those specs do not apply uniquely to instrumentation amplifiers.

Gain

These specs relate to the transfer function of the device.

$$\text{Gain Equation: } G = 1 + \frac{2(10^5)}{R_G} \qquad (22)$$

To select an R_G for a given gain, solve the equation for R_G

$$\text{(in ohms): } R_G = \frac{200{,}000}{G - 1} \qquad (23)$$

---

*The AD521 data sheet, available from Analog Devices, offers a complete circuit description along with specifications and applications of this versatile device.

TABLE 1
AD522 SPECIFICATIONS

(Typical @ $+V_S = \pm 15V$, $R_L = 2k\Omega$ & $T_A = +25^\circ C$ unless otherwise specified)

MODEL	AD522A	AD522B	AD522S
GAIN			
Gain Equation	$1 + \frac{2(10^5)}{R_G}$	*	*
Gain Range	1 to 1000	*	*
Equation Error			
G = 1	0.2% max	0.05% max	**
G = 1000	1.0% max	0.2% max	**
Nonlinearity, max			
G = 1	0.005% of F.S. (±10V)	0.001%	**
G = 10	0.006% of F.S. (±10V)	0.0025%	**
G = 100	0.01% of F.S. (±10V)	0.005%	**
Gain vs. Temp, max			
G = 1	2ppm/°C (1ppm/°C typ)	*	*
G = 1000	50ppm/°C (25ppm/°C typ)	*	*
OUTPUT CHARACTERISTICS			
Output Rating	±10V @ 5mA min	*	*
DYNAMIC RESPONSE			
Small Signal (-3dB)			
G = 1	300kHz	*	*
G = 100	3kHz	*	*
Full Power GBW	1.5kHz	*	*
Slew Rate	0.1V/µs	*	*
Settling Time to 0.1%, G = 100	0.5ms	*	*
to 0.01%, G = 100	5ms	*	*
to 0.01%, G = 10	2ms	*	*
to 0.01%, G = 1	0.5ms	*	*
VOLTAGE OFFSET			
Offsets Referred to Input			
Initial Offset Voltage (adj. to 0)			
G = 1	±400µV max (±200µV typ)	±200µV max (±100µV typ)	±200µV max (±100µV typ)
vs. Temperature, max			
G = 1	±50µV/°C(±10µV/°C typ)	±25µV/°C(±5µV/°C typ)	±100µV/°C(±10µV/°C typ)
G = 1000	±6µV/°C	±2µV/°C	±6µV/°C
1<G<1000	$\pm\left(\frac{50}{G} + 6\right)\mu V/^\circ C$	$\pm\left(\frac{25}{G} + 2\right)\mu V/^\circ C$	$\pm\left(\frac{100}{G} + 6\right)\mu V/^\circ C$
vs. Supply, max			
G = 1	±20µV/%	*	*
G = 1000	±0.2µV/%	*	*
INPUT CURRENTS			
Input Bias Current			
Initial max, +25°C	±25nA	±15nA	±25nA
vs. Temperature	±100pA/°C	±50pA/°C	±100pA/°C
Input Offset Current			
Initial max, +25°C	±20nA	±10nA	±20nA
vs. Temperature	±100pA/°C	±50pA/°C	±100pA/°C
INPUT			
Input Impedance			
Differential	$10^9\Omega$	*	*
Common Mode	$10^9\Omega$	*	*
Input Voltage Range			
Minimum Differential Input	±10V	*	*
Maximum Differential Input	±20V	*	*
Maximum Common Mode Linear	±10V	*	*
Maximum Common Mode Input	±15V	*	*
Common Mode Rejection			
Min @ ±10V, 1kΩ Source Imbalance			
G = 1 (dc to 30Hz)	75dB (90dB typ)	80dB (100dB typ)	75dB (90dB typ)
G = 10 (dc to 10Hz)	90dB (100dB typ)	95dB (110dB typ)	90dB (110dB typ)
G = 100 (dc to 3Hz)	100dB (110dB typ)	100dB (120dB typ)	100dB (120dB typ)
G = 1000 (dc to 1Hz)	100dB (120dB typ)	110dB (>120dB typ)	100dB (>120dB typ)
G = 1 to 1000 (dc to 60Hz)	75dB (88dB typ)	80dB (88dB typ)	*
NOISE			
Voltage Noise, RTI			
0.1Hz to 100Hz (p-p)			
G = 1	15µV	*	*
G = 1000	1.5µV	*	*
10Hz to 10kHz (rms)			
G = 1	15µV	*	*
TEMPERATURE RANGE			
Specified Performance	-25°C to +85°C	*	-55°C to +125°C
Operating	-55°C to +125°C	*	*
Storage	-65°C to +150°C	*	*
POWER SUPPLY			
Power Supply Range	±(5 to 18)V	*	*
Quiescent Current, max @ ±15V	±10mA	±8mA	±8mA

*Specifications same as AD522A **Specifications same as AD522B Specifications subject to change without notice.

For example:

$$G = 1 \quad : R_G = \infty \text{ (open circuit)}$$
$$G = 10 \quad : R_G = 22{,}222\Omega$$
$$G = 100 \quad : R_G = 2020.2\Omega$$
$$G = 1000 : R_G = 200.20\Omega$$

Of course the user must provide a very clean circuit board to realize an accurate gain of 1 since 200MΩ leakage resistance will cause a gain error or 0.1%.

Gain Range
Specified at 1 to 1000, this device may (and in fact will) work at higher gains, but the manufacturer will not promise any particular level of performance. In practice, noise and drift may make higher gains impractical for this device.

Equation Error
The number given by this specification describes maximum deviation from the gain equation. The user can trim the gain (above unity) or can compensate elsewhere in his design. If his data is eventually digitized and fed to an "intelligent system" (such as a microprocessor), he might be able to correct for gain errors by measuring a reference and multiplying by a constant.

Nonlinearity
Nonlinearity is defined as the deviation from a straight line on the plot of output versus input. Figure 6a shows the transfer function of a device with exaggerated nonlinearity. The magnitude of this error can be calculated thus:

$$\text{N. L.} = \left[\frac{\text{Actual Output - Calculated Output}}{\text{Rated Full-Scale Output Range}} \right]$$

To confuse matters, this deviation can be specified relative to *any* straight line or to a specific straight line. There are two commonly-used methods of specifying this ideal straight line relative to the performance of a precision measurement device.

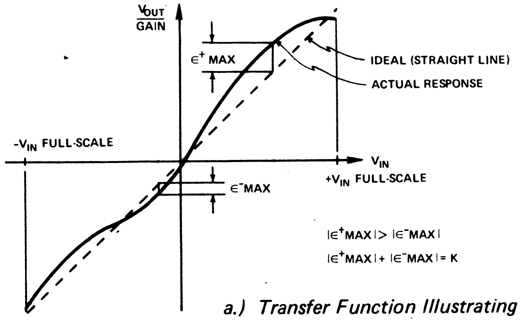
The "Best Straight Line" method of nonlinearity specification consists of measuring the peak positive and negative deviations and adjusting the slope of the device transfer function (by adjusting the gain and offset) so that these maximum positive and negative errors are equal. This method yields the best specifications but is difficult to implement in that it requires that the user examine the entire output signal range to determine these maximum positive and negative deviations. The results of a best-straight-line calibration is shown by the transfer function of Figure 6b.

The "End-Point" method of specifying nonlinearity requires that the user perform his offset and/or gain calibrations at the extremes of the output range. This is much easier to implement but may result in nonlinearity errors of up to twice these attained with best-straight-line techniques. This worst case will occur when the transfer function is "bowed" in one direction only. Figure 8c shows the results of end-point calibration.

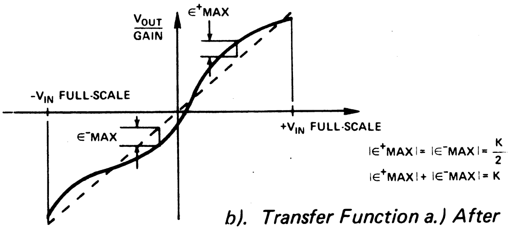
Most linear devices, such as instrumentation amplifiers, are specified for best-straight-line linearity. The user must take this into consideration when evaluating the error budget for his application.

Regardless of the method used to specify nonlinearity, the errors thus created are irreducible. That is to say that these errors are neither fixed nor proportional to input or output voltage and can not be reduced by adjustment.

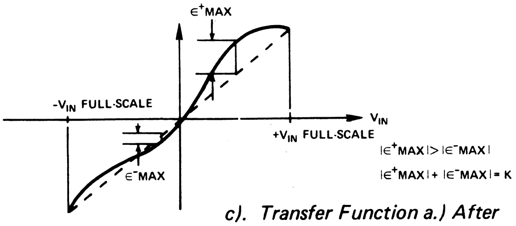
Referring to the AD522 specifications, the larger number at G = 100 indicates that in the AD522, nonlinearity increases with gain.



a.) Transfer Function Illustrating Exaggerated Nonlinearity



b). Transfer Function a.) After Calibration by Best-Straight-Line Method



c). Transfer Function a.) After Calibration by End-Point Method

Figure 6. Nonlinear Transfer Function

Gain vs. Temperature
These numbers give both maximum and typical deviations from the gain equation as a function of temperature. An intelligent system can correct for this with an "auto-gain" cycle (measure a reference and re-normalize).

Settling Time
Settling time is defined as that length of time required for the output voltage to approach and remain within a certain tolerance of its final value. It is usually specified for a fast full scale input step and includes output slewing time. Since several factors contribute to the overall settling time, fast settling to 0.1% doesn't necessarily mean proportionally fast-settling to 0.01%. In addition, settling time is not necessarily a function of gain. Some of the contributing factors

include slew rate limiting, under-damping (ringing) and thermal gradients ("long tails").

Voltage Offset

Voltage offset specifications are often considered a figure of merit for instrumentation amplifiers. While initial offset may be adjusted to zero, shifts in offset voltage could cause errors. Intelligent systems can often correct for this factor with an auto-zero cycle, but there are many small-signal high-gain applications that don't have this capability.

Voltage offset and offset drift comprise two components each; input and output offset and offset drift. Input offset is that component of offset that is directly proportional to gain, i.e., input offset as measured at the output at G = 100 is 100 times greater than at G = 1. Output offset is independent of gain. At low gains, output offset drift is dominant, while at high gains input offset drift dominates. Therefore, the output offset voltage drift is normally specified as drift at G = 1 (where input effects are insignificant), while input offset voltage drift is given by drift specification at a high gain (where output offset effects are negligible). All input-related numbers are referred to the input (RTI) which is to say that the effect on the output is "G" times larger. Voltage offset vs. power supply is also specified at one or more gain settings and is also RTI.

Input Bias Currents

Input bias currents are those currents necessary to bias the input transistors of a dc amplifier. FET input devices have lower bias currents, but those currents increase dramatically with temperature, doubling approximately every 11°C. Since bias currents can be considered as a source of voltage offset (when multiplied by source resistance), the change in bias currents is of more concern than the magnitude of the bias currents. Input offset current is the difference between the two input bias currents.

Although instrumentation amplifiers have differential inputs, there must be a return path for the bias currents. If this is not provided, those currents will charge stray capacitances, causing the output to drift uncontrollably or to saturate. Therefore, when amplifying "floating" input sources such as transformers and thermocouples, as well as ac-coupled sources, there must still be a dc path from each input to ground.

Common-Mode Rejection

Common-mode rejection is a measure of the change in output voltage when both inputs are changed equal amounts. These specifications are usually given for a full-range input voltage change and a specified source imbalance. "Common-mode rejection ratio" (CMRR) is a ratio expression while "common-mode rejection" (CMR) is the logarithm of that ratio. For example, a CMRR of 10,000 corresponds to a CMR of 80dB.

In most IA's the CMRR increases with gain. This is because most designs have a front-end configuration that does not amplify common-mode signals. Since the standard for CMRR specifications is referred to the output (RTO), a gain for differential signals in the total absence of gain for common-mode output signals will yield a 1-to-1 improvement of CMRR with gain. This means that the common-mode output error signal will not increase with gain, it does not mean that it decreases with gain! At higher gains, however, amplifier bandwidth decreases. Since differences in phase-shift through the differential input stage will show up as a common-mode error, CMRR becomes more frequency dependent at high gains.

Error Budget Analysis

To illustrate how instrumentation amplifier specifications are applied, we will now examine a typical case where an AD522 is required to amplify the output of an unbalanced transducer.

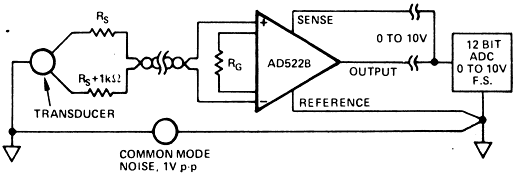


Figure 7. Typical AD522B Application

Figure 7 shows a differential transducer, unbalanced by 1kΩ, supplying a 0 to 1 volt signal to a remotely located AD522B. The output of the IA feeds a 12 bit A to D converter with a 0 to 10 volt input voltage range. There is 1 volt of peak-to-peak 0 to 10Hz noise on the ground return appearing as a common-mode signal at the inputs of the IA. The operating temperature range is -25°C to +85°C; calibration is performed at +25°C.

The input signal must be amplified by a factor of 10 in order to utilize the full resolution of the A to D converter. Solving the gain equation for G = 10 gives a value of 22.22kΩ for R_G.

Table 2 lists all applicable error sources and their corresponding effects on accuracy. Initial errors are defined as those errors that can be reduced to a negligible amount by performance of an initial calibration.

Reducible errors include these initial errors along with other errors that occur during normal operation that may be corrected by an adaptive or "intelligent" system. For example, changes in gain or offset may be measured during an auto-zero/auto-gain cycle by measuring two known voltages (a precision reference and ground, for example). This is a common practice in computer or processor-controlled equipment.

Irreducible errors are errors which can not be readily corrected either at initial calibration or in use. It could be argued that an array of precision references would permit a software linearity correction, but in most applications that would be unrealistically cumbersome.

The total error "as built" is approximately 5540ppm or 0.55%. If an initial calibration is performed, this number is reduced by 2210ppm to 3330ppm = 0.33%. Note that 3000ppm of this is gain drift.

In many applications, differential linearity and resolution are of prime importance. This would be so in cases where the absolute value of a variable is less important than changes in value. In these applications, only the irreducible errors (57.8ppm = 0.006%) are significant. Furthermore, if a system has an intelligent processor monitoring the A to D output, the addition of a auto-gain/auto-zero cycle will remove all reducible errors and may eliminate the requirement for initial calibration. This will also reduce errors to 0.006%.

In the above example, the system can justifiably make use of a 13 bit A to D converter for its differential linearity and

TABLE 2
AD522B ERRORS

Error Source	AD522B Specs	Calculation	Initial Effects on Accuracy (May be Calibrated)	Reducible Effects on Accuracy (Correctable by "Intelligent" System)	Irreducible Effects on Accuracy
Gain Error	±0.2%	±0.2% = ±2000ppm	±2000ppm	±2000ppm	–
Gain Instability	±50ppm/°C	(±50ppm)(85°C -25°C) = ±3000ppm	–	±3000ppm	–
Gain Nonlinearity	±0.0025%	±0.0025% = ±25ppm	–	–	±25ppm
Offset Voltage	±200µV, RTI	±200µV/1V = ±200ppm	±200ppm	±200ppm	–
Offset Voltage Drift	±4.5µV/°C	(4.5µV/°C)(85°C -25°C) = 270µV/1V = 270ppm	–	±270ppm	–
Offset Current	±10nA	[±10nA][1kΩ] = ±10µV = ±10ppm	±10ppm	±10ppm	–
Offset Current Drift	±50pA/°C	[±50pA][85°C -25°C][1kΩ] = ±3µV = ±3ppm	–	±3ppm	–
Common Mode Rejection	95dB	-95dB = 20 log ϵ ϵ = 0.0000178 = 17.8ppm	–	–	±17.8ppm
Noise	15µV p-p (0.1Hz to 100Hz)	15µV/1V = 15ppm	–	–	±15ppm
Totals			2210ppm	5483ppm	57.8ppm

resolution. Dynamic range exceeds 84dB (14 bits). Absolute accuracy depends on calibration and system interaction capabilities; it might be as good as the resolution (0.006%) or as poor as the initial accuracy (0.55%).

INSTRUMENTATION AMPLIFIER APPLICATIONS

General Considerations

Whenever a precision high-gain device—such as an instrumentation amplifier—is used, certain precautions apply. Obviously, it is wise to have a clean layout, short wire runs where possible and a carefully considered grounding scheme. Figure 8 shows a well-thought out approach to IA interconnection.

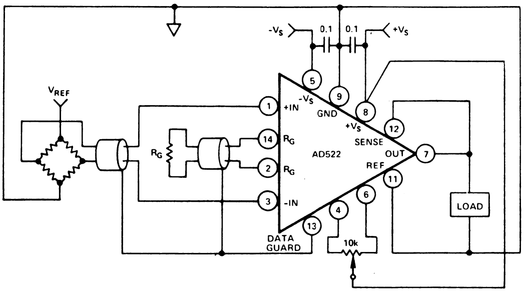


Figure 8. AD522 Interconnection

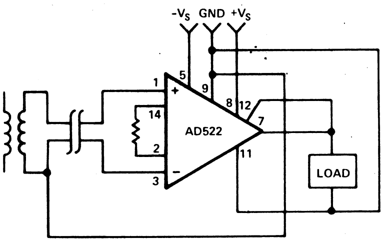
A properly designed instrumentation amplifier exhibits low sensitivity to power supply variations; the AD522, for example, shows an RTI offset variation of only 0.2µV per percent of power supply change at G = 1000. At increasing frequencies, however, this rejection factor will degrade as internal capacitances permit more power supply noise to find its way into the signal path. This effect can be minimized by bypassing the power supplies, as close to the IA as possible, with 0.1µF ceramic disc capacitors. Larger tantalum capacitors would be effective against lower frequency variations, but a competent IA is capable of rejecting most of these slower changes.

The offset adjustment pot usually affects the balance of the high gain differential input stage. Short wire runs to this pot will minimize injection of noise into a sensitive location.

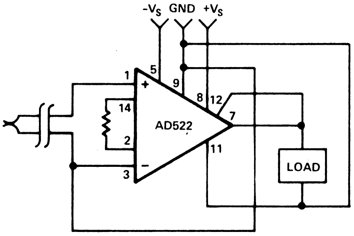
The gain-determining resistor, R_G, is often remotely located for purposes of gain switching. A well-designed IA will tolerate this to a certain extent, but stray capacitances and wiring inductance may disturb the frequency compensation of the device. Sometimes it becomes necessary to install a series RC right at the R_G terminals of the IA to add a compensating zero to correct for LC resonances caused by stray inductances and capacitances. This lead compensation may improve stability at the cost of a peak in the frequency response curve at the high end. Unfortunately, this compensation, if required, depends on the individual application and is usually determined experimentally.

Most IA's are provided with "sense" and "reference" outputs. While there are several interesting uses for these features (to be discussed later), the most basic application is remote load sensing. This essentially puts the IR drops "inside the loop" of the IA and is most useful when driving remote and/or heavy loads or when the load ground is not firmly "anchored" to the power supply returns.

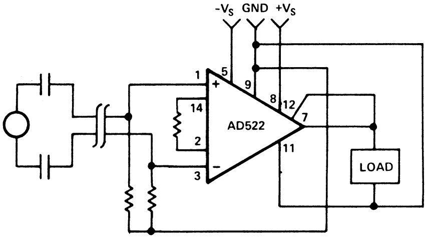
Grounding is a topic worthy of its own application note (see "An IC Amplifier User's Guide to Decoupling, Grounds, etc." by A. P. Brokaw). In the case of instrumentation amplifiers, the main thing to remember is that all signal and power returns must eventually have a direct or indirect common point. Direct coupling of IA inputs make it necessary to provide signal ground returns for input amplifier bias currents. Figure 8 shows a direct connection. If a "floating" source or ac coupling is used, indirect returns similar to those shown in Figure 9 must be provided.



a). Transformer Coupled



b). Thermocouple



c). AC Coupled

Figure 9. Indirect Ground Returns for "Floating" Transducers

Signals from remote transducers are often transmitted to the IA through shielded cables. While this may well serve to reduce noise pick-up, the distributed RC's in such cabling can cause differential phase shifts in those lines. When ac common-mode signals are present, these phase shifts will reduce common-mode rejection. The same effect will occur with remote R_G's located at the end of shielded cables. If the shields could be driven by the common-mode signal, the cable capacitance could be "boot-strapped" thus making the capacitance effectively zero for common-mode signals. The data guard output of the AD522 provides the common-mode component of the input signals and can be used to drive the shields of coaxial input cables and increase ac CMR. Figure 8 illustrates this connection; if not used, the data guard should be left unconnected.

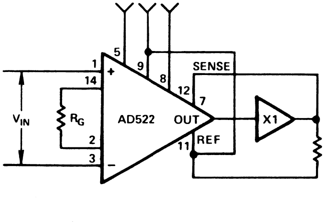


Figure 10. Current-Booster Output

Boosted Output

In the previous section, use of the sense terminal for remote load sensing was discussed. Another use of that terminal is illustrated in Figure 10.

Typically, IC instrumentation amplifiers are rated for a full ±10 volt output swing into 2kΩ. In some applications, however, the need exists to drive more current into heavier loads. Figure 10 shows how a high-current booster may be connected "inside the loop" of an instrumentation amplifier to provide the required current boost without significantly degrading overall performance. Nonlinearities, offset and gain inaccuracies of the buffer are minimized by the loop gain of the IA output amplifier. Offset drift of the buffer is similarly reduced.

Offset Load

The reference terminal may be used to offset the output by up to ±10V. This is useful when the load is "floating" or does not share a ground with the rest of the system. It also provides a direct means of injecting a precise offset.

Two caveats apply to the use of the reference pin. When the IA is of the three-amplifier configuration shown in Figure 4 (as is the AD522), it is necessary that nearly zero impedance be presented to the reference terminal. It can be shown that any significant resistance from the reference terminal to ground increases the gain of the non-inverting signal path thereby upsetting the common-mode rejection of the IA. An operational amplifier may be used to provide that low impedance reference point as shown in Figure 11. The input offset voltage characteristics of that amplifier will add directly to the offset voltage performance of the IA.

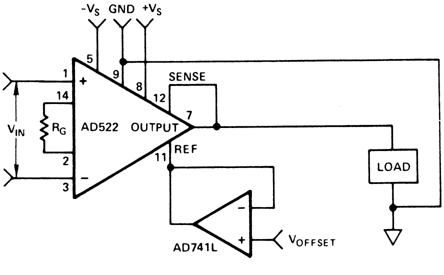


Figure 11. Use of Reference Terminal to Provide Output Offset

The other precaution is more obvious. The output voltage range of an IA is clearly specified; if that range is mostly used up by offset at the reference terminal not much range is left for the signal. In other words, the sum of the offset and signal may not exceed the specified output voltage range of the IA.

CMR Trim

The effect of resistance in the reference termination may be used to advantage. A short-term CMR improvement can be realized with the circuit shown in Figure 12.

While applying a low-frequency 20 volt peak-to-peak input signal to both inputs, the pot should be adjusted for an output null. In many cases this adjustment will not improve matters on a long-term basis since the common-mode rejection of the device is determined by the long-term stability of internal components (which will drift regardless of what happens externally).

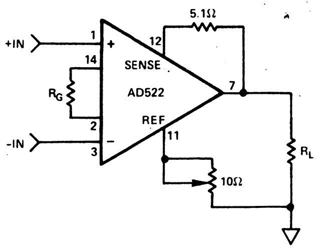
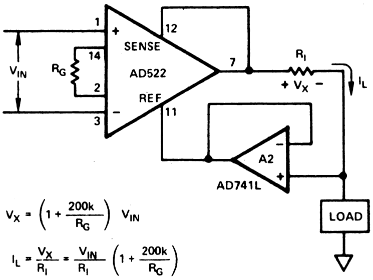


Figure 12. Common Mode Rejection Trim

Controlled Currents

An instrumentation amplifier can be turned into a voltage-to-current converter by taking advantage of the sense and reference terminals as shown in Figure 13.



$$V_X = \left(1 + \frac{200k}{R_G}\right) V_{IN}$$

$$I_L = \frac{V_X}{R_I} = \frac{V_{IN}}{R_I}\left(1 + \frac{200k}{R_G}\right)$$

Figure 13. Voltage-To-Current Converter

By establishing a reference at the "low" side of a current setting resistor, an output current may be defined as a function of input voltage, gain and the value of that resistor. Since only a small current is demanded at the input of the buffer amplifier A_2, the forced current I_L will largely flow through the load. Offset and drift specifications of A_2 must be added to the output offset and drift specifications of the IA.

CONCLUSIONS

Thus characterized, the instrumentation amplifier stands ready to take its place in the Grand Order of Things. The preliminary contention that an IA is not a special sort of operational amplifier should now be obvious. Its versatility is limited in scope but its applications are limited only by the imagination of the potential user. As a precision linear device, an IA is qualified mainly by its specifications, a full understanding of which is necessary to successfully use it to advantage. Analog Devices, as a long time supplier of components for precision measurement applications, offers a full spectrum of instrumentation amplifiers in modular, hybrid and monolithic IC form, each ideally suited to particular applications. We hope that this article will help clarify the issues involved and will aid in the selection of a suitable device for a particular application.

ANALOG DEVICES

APPLICATION NOTE

Interfacing the AD558 DACPORT™ to Microprocessors

by Doug Grant

The AD558 represents a major breakthrough in monolithic DAC technology. It is a true complete 8-bit unit including reference, output amplifier, and data latch on a single chip designed to operate from a single positive power supply. Figure 1 shows the block diagram of the device. The internal reference is a 1.2 volt bandgap type. The actual digital-to-analog conversion is accomplished by means of eight PNP current switches driving a precision thin-film R/2R ladder network to produce a direct unbuffered 0 to 400 millivolt analog signal. The high-speed output amplifier provides pin-selectable output scales of 0 to 2.56 volts and 0 to 10.00 volts. Settling time of the voltage output is typically 700 nanoseconds for a full-scale step, and the resistive pulldown output stage with a proprietary anti-saturation driver provides single-supply operation.

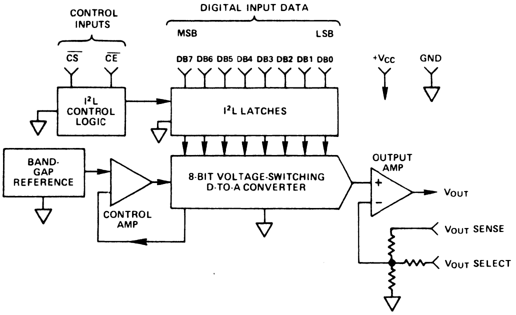


Figure 1. AD558 Functional Block Diagram

The PNP current switches are driven from the outputs of the octal data latch. This latch is fabricated using Analog Devices' linear-compatible-I^2L technology. This process provides a dense, low-power logic family which can be produced without compromising the linear components necessary for converter design.

The latch is operated from two TTL-compatible control signals, $\overline{CS}$ and $\overline{CE}$. Figure 2 shows the truth table for the latch. The $\overline{CS}$ and $\overline{CE}$ inputs are interchangeable, and the latch is transparent when both $\overline{CS}$ and $\overline{CE}$ are low. When either control input returns high, the eight-bit data word is latched and the analog output is unaffected by further activity on the data lines. This latch permits simple interface to many popular microprocessors, as will be shown in the remainder of this application note.

Input Data	$\overline{CE}$	$\overline{CS}$	DAC Data	Latch Condition
0	0	0	0	"transparent"
1	0	0	1	"transparent"
0	↑	0	0	latching
1	↑	0	1	latching
0	0	↑	0	latching
1	0	↑	1	latching
X	1	X	previous data	latched
X	X	1	previous data	latched

Notes: X = Does not matter

↑ = Logic Threshold at Positive-Going Transition

Figure 2. AD558 Control Logic Truth Table

GENERAL CONCEPTS

While microprocessor control signals vary widely from one architecture to the next, two conditions must be signalled to the AD558. First, the processor must indicate which memory (or I/O) location is being operated upon. An address decoder is used to provide a unique signal for each distinct address. This signal is normally applied to $\overline{CS}$ (Chip Select). Depending on system complexity, this decoding may range from direct connection to an address line to a complete decoding of all memory locations. The second signal necessary is an indication of whether the data on the bus is flowing from processor to memory (WRITE) or from memory to processor (READ). In the case of a DAC, where data is flowing from the processor, a WRITE signal is used. This signal is normally applied to the DACPORT $\overline{CE}$ (Chip Enable).

8080A Interface

The 8080A microprocessor provides two possible methods of sending data to an AD558 or other I/O port: memory-mapped or isolated I/O. Both types are useful and will be examined. In memory-mapped I/O, the I/O devices are treated as part of the memory array. This allows the full range of memory reference instructions and addressing modes to be used to manipulate the data.

DACPORT is a trademark of Analog Devices, Inc.

The isolated I/O technique treats the I/O devices as separate system elements, accessed by READ and WRITE signals distinct from the memory READ and WRITE signals. In the 8080A, while there are 64K memory locations, there are only 256 dedicated I/O addresses. This permits simpler address decoding in some systems. The primary disadvantage of isolated I/O is that all data must pass through the accumulator. Direct transfer of data from a register (or memory) to an I/O device is not possible.

READ and WRITE signals for memory and I/O are available on the 8080A data bus at the beginning of each machine cycle and are latched externally. The latch function can be accomplished with dedicated chips such as the 8228 (see Figure 3) or a few packages of random logic (Figure 4). If an active low decoded address signal is applied to pin 10 of the AD558 ($\overline{CS}$) and the $\overline{MEMW}$ (or $\overline{OUT}$) is applied to pin 9 ($\overline{CE}$), the data will be latched and the analog output updated whenever the processor writes into the chosen address.

If, for example, a previous subroutine has generated a byte of data to be sent to the DAC, and returned this byte in the B register, a simple routine such as:

```
MOV A, B
OUT F1
```

will send the data to an AD558 residing at I/O address F1. If memory-mapped I/O is used instead, the move to the accumulator is unnecessary, and the code becomes simply:

```
LXI H, (16 BIT DAC ADDRESS)
MOV M, B
```

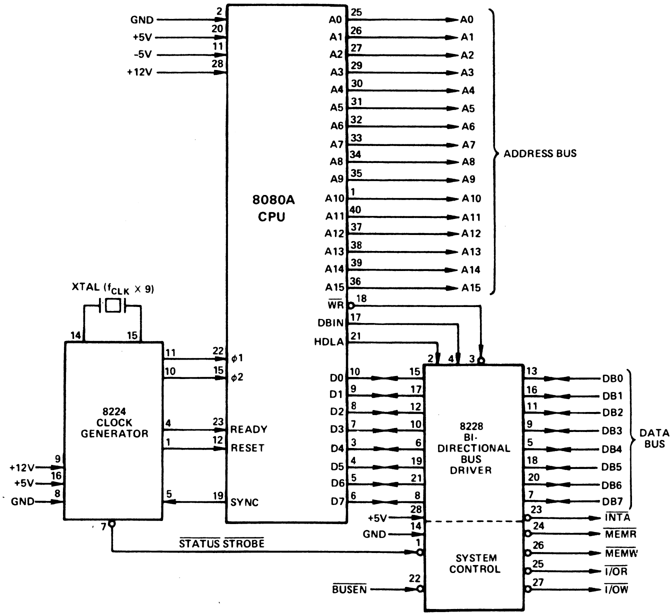


Figure 3. Control Signal Generation with 8228 System Controller

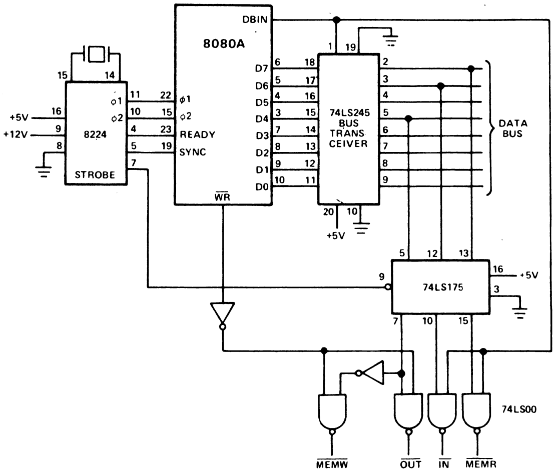


Figure 4. Control Signal Generation with Standard Logic

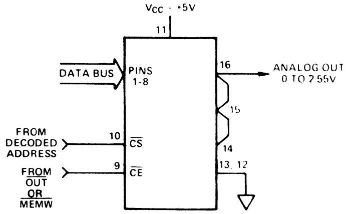


Figure 5. Control Signal Connections to AD558

8085A Interface

The 8085A is a somewhat improved version of the 8080A. It includes an on-chip clock generator requiring only a crystal (or LC or RC tuned circuit) to establish the oscillator frequency. In addition to more flexible interrupt handling capability, higher speed, and on-chip serial I/O capability, the 8085A operates from a single 5 volt power supply. Since a complete family of 8085A compatible peripheral components and memory devices are also available for single-supply operation, it is unnecessary and inconvenient to add a negative power supply to a system just to support a DAC. For this reason, the AD558 with its single power requirement is clearly the best choice for an analog output port.

The 8085A uses a multiplexed Address/Data bus, which contains the lower 8 bits of the desired address during the first clock cycle of a machine cycle. The ALE signal is used to latch the lower half of the address. For the second and third clock cycles, the bus contains the data word.

As with the 8080A, there are two possible I/O techniques: isolated and memory-mapped. Since the upper and lower 8 bits of the address are identical in I/O operations, it is not necessary to latch the lower 8 bits and decode all 16. The IO/$\overline{M}$ signal can be used in the address decoder to signify that the address on the bus is an I/O address, not a memory location. The active low decoded address can then be applied to the AD558 $\overline{CS}$.

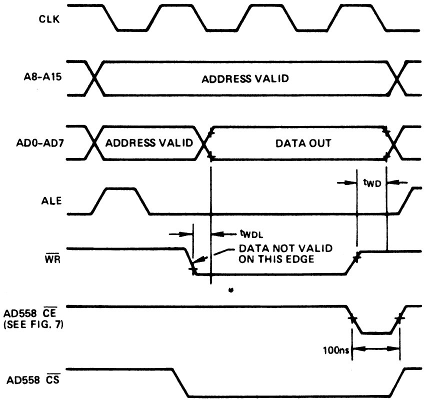


Figure 6. 8085A – AD558 Timing Diagram

The address decoding for memory-mapped I/O is slightly more complex since the total 16-bit address must be dealt with. System complexity will dictate exactly how many distinct addresses must be decoded, and in smaller systems it may be possible to locate an AD558 in a large block of otherwise vacant locations. Of course, memory-mapped I/O allows the full range of memory reference instructions to be used, while isolated I/O requires data to pass through the accumulator before being sent to the DAC.

Data validity is a subtle point when considering memory-mapped I/O, where the DAC appears as a write-only-memory. When writing to a RAM, it is permissible to have bad data on the bus during the WRITE cycle (as long as it becomes valid by the end of the operation), since the outside world is not affected by this data. However, unstable data during writes to a DAC can cause observable (and usually undesirable) activity on the output. Thus, WRITE timing for a particular processor must be closely examined to determine data validity.

The $\overline{CE}$ input of the AD558 can be driven directly from the $\overline{WR}$ of the 8085A, even though the data bus is not stable until 40 nanoseconds after the falling edge of $\overline{WR}$. Since the AD558 internal circuitry does not respond to pulses less than 60 nanoseconds wide on the data inputs, any invalid data during this 40 nanosecond period does not produce an erroneous output.

In the case of an 8085A with a heavily-loaded bus, t_{WDL} may be extended long enough to cause bad data to reach the AD558 and produce an incorrect analog output. If this temporary anomaly can be tolerated, then $\overline{WR}$ can be used to provide the DACPORT's $\overline{CE}$ input. If the output glitch is undesirable, the circuits of Figure 7 will provide valid signals for $\overline{CE}$.

Systems using the 5MHz 8085A-2 can use $\overline{WR}$ directly for $\overline{CE}$, since t_{WDL} is only 20 nanoseconds maximum. Furthermore, since t_{WD} is only 60 nanoseconds, the one-shot method shown in Figure 7a does not apply.

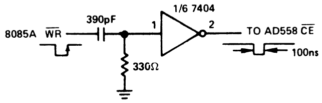


Figure 7a. AD558 $\overline{CE}$ Generated from 8085A $\overline{WR}$ Rising Edge

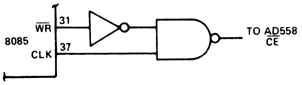


Figure 7b. $\overline{CE}$ Generated from $\overline{WR}$ and $\overline{CLK}$

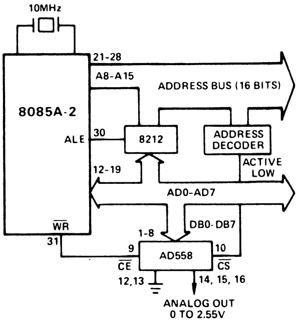


Figure 8. AD558 – 8085A Interface

8048/8748 Interface

The 8048 series of single-chip microcomputers offers two methods of I/O interfacing. The first is a modified version of the isolated I/O described for the 8080A. It differs in that the 8048 contains two decoded and latched I/O ports on the chip. The instructions OUTL P1,A and OUTL P2,A perform the functions of sending the accumulator contents to PORT 1 or PORT 2, respectively. The AD558 can reside directly on either port if pins 9 and 10 are hard-wired to a logic 0*. In this mode, the internal latch appears transparent, and activity on the data inputs causes the DAC output to change. Figure 9 shows a typical connection scheme.

*The technique of hard-wiring $\overline{CS}$ and $\overline{CE}$ low can be used with other single-chip microcomputers (such as the 6801, 3870, 6500/1, PIC1650) which feature built-in latched I/O ports. The 8048 is chosen as a representative example. The AD558 can also be used in this mode in non-μP applications.

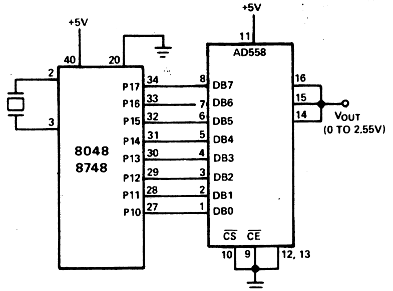


Figure 9. AD558 Connected to Dedicated I/O Port of 8048 Microcomputer

A second method of interface is necessary in 8048-based systems with more than two I/O devices. The 8048 BUS port allows system memory and I/O expansion, with the RD and WR signals controlling data flow on this bus. During a WRITE to external memory (or memory-mapped I/O devices) the falling edge of ALE latches the address from the bus. The decoded address (active low) is then applied to CS of the AD558. Since this control scheme is very similar to 8085 operation, many 8085 system components may be used. However, as with the 8085, when the WR of the 8048 goes low, data is not yet valid on the bus. The falling edge of WR occurs at least 200 nanoseconds before data is valid. The rising edge of WR should be used to trigger a one-shot whose low-going output drives the CE of the AD558.

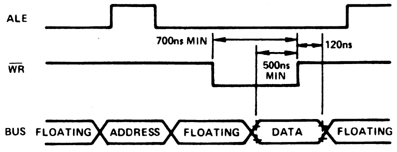


Figure 10. 8048 Timing for External Memory Write

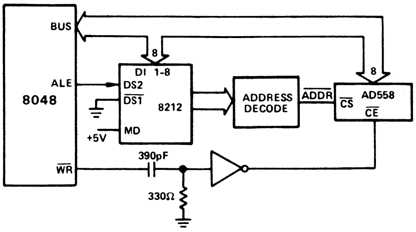


Figure 11. AD558 as External Data Memory

In this external memory mode, data is sent from the accumulator to the external memory using MOVX @ Rr, A instructions. These instructions use the RAM pointer registers R0 and R1 to point to one of 256 external memory addresses. Figures 10 and 11 demonstrate this operating mode.

6800/650X Series Interface*

The 6800 microprocessor family has only one method of data exchange to peripheral devices: memory mapping. Thus it is possible to use any address in the full 64K memory space for I/O devices. Since the address bus of the 6800 is three-state, a signal called VMA is provided to indicate that the bus contains a valid memory address. This signal normally used as a part of the address decoding logic to prevent inadvertent writes to memory at times when the address bus is being controlled by an external device (such as a DMA controller).

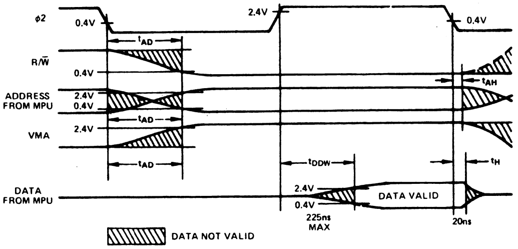


Figure 12. 6800 System Write Timing

Read/Write signaling is accomplished by use of two signals, R/W and φ2. The state of R/W during the up time of φ2 (E on 6802) determines whether a Read or Write is in progress. This requires validity of both W and φ2 rather than simply a WR to operate the AD558 CE input. To further complicate matters, Figure 12 shows that there is a period of time when all control signals are valid, but data is *not*. In systems where spurious outputs can be tolerated (such as de-glitched systems or systems unable to respond to sub-microsecond pulses) the control signal connection scheme of Figure 13a is sufficient.

This scheme produces a CS signal for the AD558 when VMA, φ2 and A15 are all high. The R/W signal is used for CE.

The circuit of Figure 13b uses a 74LS221 dual one-shot triggered by φ2 and W validity to produce the delayed pulse necessary to operate the AD558 CE input. This delayed pulse allows only valid data into the AD558 data latch.

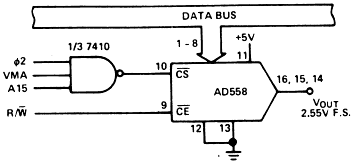


Figure 13a. Simple 6800 Interface

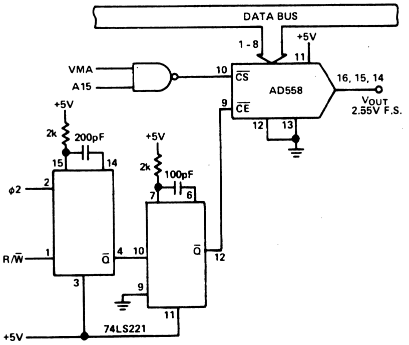


Figure 13b. Glitch-Free 6800 Interface

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*Although this discussion will refer to 6800 control signals, the 650X series bus architecture is similar (with the exception of VMA which is not available on the 650X). For example, t_{DDW} (see Figure 12) is 200 nanoseconds max on the 650X.

Z80 Interface

The Z80 processor uses an instruction set which includes all the 8080A instructions as well as several other operations. It operates from a single +5 volt supply; therefore Z80-based systems do not generally have negative power supplies available to power a DAC. The AD558 is thus well suited to serve as an analog output port for such a system.

As with the 8080A, both isolated and memory-mapped I/O are possible. The isolated I/O instructions are more flexible than the 8080A IN and OUT instructions. For example, there are a total of 12 output instructions including transfers of entire blocks of register indirect addressed data and transfers of data from any internal register to a register indirect addressed I/O port.

Output signaling is accomplished with a $\overline{WR}$ signal, while $\overline{IORQ}$ and $\overline{MREQ}$ indicate whether the address on the bus is an I/O or memory address. (Note that during I/O operations only the lower 8 address bits are valid).

Timing on the Z80 is particularly convenient for AD558 interfacing, since the data bus is stable and contains valid information while $\overline{WR}$ is low. The low time of $\overline{WR}$ is 220 nanoseconds minimum for memory writes on the higher-speed Z80A, and 470 nanoseconds minimum during I/O writes. Therefore, $\overline{WR}$ can be applied directly to $\overline{CE}$.

Address decoding can be as simple or complex as the system requirements dictate. In the simplest case, shown in Figure 14, the inverse of A15 is used for the AD558 $\overline{CS}$ signal.

Complex systems might decode more address bits to further partition the memory space or use $\overline{IORQ}$ instead of $\overline{MREQ}$ to accomplish accumulator I/O.

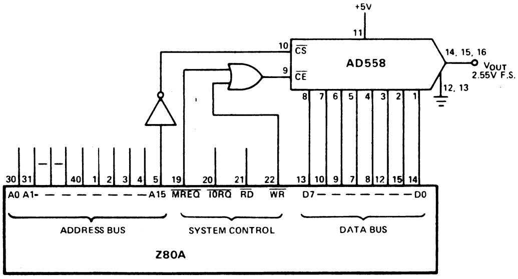


Figure 14. Z80A – AD558 Interface

1802 Interface

The 1802 CMOS microprocessor is used extensively in applications where low power consumption is critical. Many of these systems use a single supply (usually 5 volts), which makes the AD558 an ideal analog output port.

The 1802, like the 8080 series, features both accumulator and memory-mapped I/O formats. Accumulator I/O addresses appear on the N0, N1, and N2 lines with the $\overline{MRD}$ (memory read) signal indicating direction of data flow. This allows direct addressing of 14 I/O devices (device address 0 is not valid). In systems where more than 14 I/O devices are used, or where decoding of the N lines is undesirable, memory-mapped I/O is also possible. Address information on the 1802 appears on the address bus in two parts: the high-order 8 bits appear first and are latched with the falling edge of the TPA clock; the low order byte of address information then appears. The active low signal which indicates presence of the chosen address can be applied directly to the AD558 $\overline{CS}$ input. The DACPORT $\overline{CE}$ input is operated by the 1802 $\overline{MWR}$ signal. Fortunately the data is stable on the bus during the low time of $\overline{MWR}$. Figure 15 shows a generalized configuration for locating a DACPORT in the 1802 memory space.

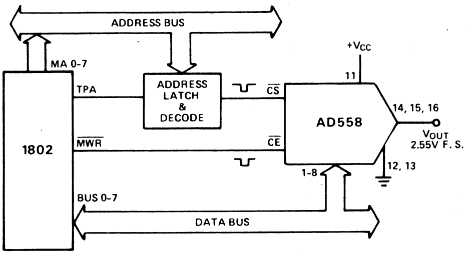


Figure 15. 1802 – DACPORT Connection

APPLICATIONS

The AD558 DACPORT can be used in any system which requires an analog output from a microprocessor bus. Several applications follow which demonstrate the capabilities of the device.

Ramp Generation

Systems such as vector graphic displays and digitally-swept VCO's require digitally-controlled analog voltage ramps. Such ramps are easily generated by an AD558 driven by a relatively simple software routine. The 8080A subroutine below accepts input arguments of initial and final ramp value in the B and C registers, and timing between steps in the D register. It is assumed that the HL register pair points to the DACPORT address when the subroutine is called. Ramp time is variable from 51 microseconds to 3.87 milliseconds per point, corresponding to full-scale sweep times of 13 milliseconds to 0.992 seconds, respectively, when this program is executed at 1MHz.

```
RAMP:    MOV A, B
         MOV M, A
         INR B
         MOV E, D
LOOP:    DCR E
         JNZ LOOP
         CMP C
         JNZ RAMP
         RET
```

Analog-To-Digital Conversion

The process of A-to-D conversion often involves comparing the (unknown) analog input signal to the output of a DAC controlled by some algorithm. Examples include the staircase or single-ramp ADC which uses a counter-driven DAC and a comparator. When the comparator detects that the DAC output has exceeded the analog input, the counter is stopped and the digital value can be read. A similar example is the tracking ADC, where the counter used is an up/down type, with its direction controlled by the comparator.

These ADC types are usually implemented in hardware using standard MSI logic, low-cost IC comparators, and DACs. The counting (or other) algorithm can just as easily be performed in software in a microprocessor system if the DAC is easily interfaced. The AD558 DACPORT offers convenient digital interfacing for such applications. Furthermore, the internal output amplifier can be operated open-loop to perform the comparator function directly.

Figure 16 shows the circuit diagram for the software-controlled ADC. The internal gain-setting resistors are used to attenuate the 10V full-scale input signal to a 0 to 400 millivolt scale and present approximately a 40kΩ load resistance to the analog input. The open-loop output amplifier slews in several tens of microseconds since it is not optimally compensated for comparator operation. The NPN buffer provides adequate current sink capability for the LSTTL tri-state buffer. It is also possible to substitute a CMOS tri-state driven directly from the DACPORT output. As shown, the DAC appears to the microprocessor as a memory location which accepts an 8-bit data word and when read back uses the LSB state to determine whether the processor's guess was higher or lower than the value of the analog input signal.

The successive-approximation algorithm is a popular method for accomplishing A to D conversion. It has the advantages of fixed conversion time regardless of analog input signal magnitude and reasonably fast conversion times. The algorithm consists of testing the MSB (most-significant-bit) to determine whether the signal resides above or below mid-scale. The result of this test determines whether the MSB should be kept or dropped. If it is kept, the next test is whether the signal is above or below 3/4 of full scale; if the MSB was dropped, the test is done at 1/4 full scale. This process repeats until all eight bits have been exercised.

The following 22 line 8080-language subroutine performs the successive-approximation algorithm with the circuit shown in Figure 16. The routine assumes that the HL register pair points to the DAC location. the conversion result is returned in the accumulator, and the conversion cycle executes in approximately 2.5 milliseconds on a 1MHz 8080A.

```
START:   PUSH B        ; SAVE B + C
         LXI B, 8000H  ; CLEAR C
                       ; SET MSB IN B
         MOV A, B      ; AND ACC.
TRY:     ADD C         ; ADD PARTIAL ANSWER
         MOV M, A      ; SEND TO DACPORT
         MVI A, ODH    ; SET UP DELAY FOR
LOOP:    DCR A         ; COMPARATOR TO SETTLE.
         JNZ LOOP      ; 200 MICROSECONDS USED
                       ; HERE
         MOV A, M      ; READ COMPARATOR
                       ; OUTPUT
         ANI 01H       ; MASK ALL BUT LSB
         JZ NEXTRY     ; IF ZERO, GUESS IS TOO
                       ; HIGH
         MOV A, B      ; SO DROP BIT, OTHERWISE,
         ADD C         ; ADD THAT BIT TO OLD
                       ; PARTIAL
         MOV C, A      ; ANSWER AND STORE IN C.
NEXTRY:  MOV A, B      ; GET LAST BIT TRIED +
                       ; MOVE RIGHT
         RAR           ; IF IT WAS LSB
         JC DONE       ; THEN EXIT
         MOV B, A      ; IF NOT, GO BACK
         JMP TRY       ; AND TRY IT.

DONE:    MOV A, C      ; WHEN DONE PUT
         POP B         ; ANSWER IN A
         RET           ; RESTORE BC AND EXIT
```

8080-Language successive-approximation subroutine.

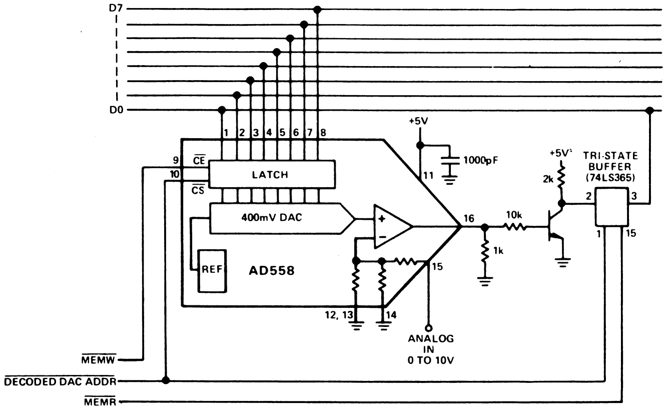


Figure 16. Software-Controlled ADC Using DACPORT Output Amplifier as Comparator

ANALOG DEVICES

APPLICATION NOTE

Gain Error and Gain Temperature Coefficient of CMOS Multiplying DACs

by Phil Burton

INTRODUCTION

This note is intended to provide an insight into factors which affect the "gain" of CMOS multiplying D/A converters. The emphasis is on developing an understanding of the phenomena involved and in creating rules of thumb and criteria which are easy to apply. The mathematical relationships which are derived are approximate and usually give worst case values which are worse than those that one might reasonably expect to occur. Almost every circuit application has its own unique set of parameters and clearly it is not possible to cover every eventuality. But, hopefully, with the information contained in this note, engineers will be in a position to assess the importance of related parameters for themselves.

GAIN ERROR AND GAIN TEMPERATURE COEFFICIENT

An ideal 12-bit D/A converter has full scale output voltage of

$$\left\{ \frac{4095}{4096} \cdot V_{REF} \right\} \text{ Volts}$$

In practice the full-scale output voltage can differ from this and the transfer relationship V_{OUT}/V_{REF}, commonly called ***"gain"***, is specified as having a "gain error" of ±x%. This means that the full scale output voltage can deviate by up to ±x% from the ideal output voltage.

Gain is also specified as having a gain temperature coefficient. For most modern CMOS DACs the "gain tempco" is of the order of ±5ppm/°C. This gives the worst case variation in gain of the D/A converter with temperature due to differences of temperature coefficients between the feedback resistor and the R/2R converter. The gain tempco varies with temperature and the specified worst case value usually applies to a 10°C segment of the operating temperature range. For a temperature variation of 100°C (+25°C to +125°C) the average temperature coefficient is generally a good deal less (better than ±3ppm/°C) than the specified worst case value. However, for the sake of simplicity and worst case analysis it is often convenient to assume that the specified worst case temperature coefficient applies over the whole temperature range.

GAIN TRIM CIRCUIT—THEORETICAL CONSIDERATIONS

Imperfection in "gain" is due to inevitable manufacturing tolerances in the process used to fabricate the resistors. The gain (or full scale value) may be restored to the ideal value by using a fixed resistor and a trim resistor as shown in the generalized circuit of Figure 1. Note that it is preferable to use a "select on test" fixed resistor in place of potentiometer R1 where possible—more about this later.

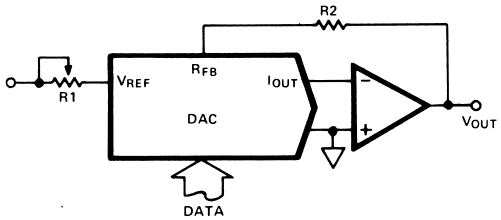


Figure 1. Generalized Gain Trim Arrangement for CMOS Multiplying D/A Converters

The maximum required value of R1 and R2 may be determined by using equations (1) and (2) given below where R_{DAC} is the input resistance of the R-2R ladder (i.e., the input resistance at the reference input of the D/A converter), $R_{DAC\ max}$ is the maximum specified value of R_{DAC} and x is the gain error in %.

$$R_{1\ max} = \frac{2\,|x|\,R_{DAC\ max}}{100} \tag{1}$$

$$R_{2\ max} = \frac{|x|\,R_{DAC\ max}}{100} = \frac{R_{1\ max}}{2} \tag{2}$$

The full scale output (or gain) of a D/A converter varies with temperature because of the temperature coefficients of the D/A converter itself and the temperature coefficients of the additional components (R1 and R2 and the op-amp) used to realize the circuit. The temperature coefficients of the R-2R ladder and the feedback resistor are around -300ppm/°C but they are carefully designed to track each other to better than ±5ppm/°C, so that the overall gain temperature coefficient is better than ±5ppm/°C. It may be shown that the additional temperature coefficients (tempco) introduced into the circuit of Figure 1 by R1 and R2 are approximately given by:-

$$\text{Additional Tempco due to } R_1 = -\frac{R_1}{R_{DAC}}(\gamma_1 - \varsigma) \qquad (3)$$

$$\text{Additional Tempco due to } R_2 = +\frac{R_2}{R_{DAC}}(\gamma_2 - \varsigma) \qquad (4)$$

ς is the temperature coefficient of the D/A converter resistor material, expressed in ppm/°C units.

$\gamma 1$ and $\gamma 2$ are the temperature coefficients of R_1 and R_2 respectively, expressed in ppm/°C units.

From equations (3) and (4) it will be observed that the *additional* temperature coefficients are at a maximum when R_{DAC} is at a minimum, i.e., $R_{DAC\ min}$. By substituting equations (1) and (2) into equations (3) and (4) we obtain equations (5) and (6) which give the worst case (i.e., maximum) additional temperature coefficients due to R1 and R2. Note that these equations are expressed in terms of data which is directly available from the manufacturer's data sheet; in fact, the value -

$$\frac{|x| R_{DAC\ max}}{R_{DAC\ min}}$$

is a simple figure of merit for assessing potential D/A converter temperature coefficients.

$$\text{Worst case additional tempco due to } R_1 = \frac{-2\,|x| R_{DAC\ max}}{100 R_{DAC\ min}}(\gamma_1 - \varsigma) \qquad (5)$$

$$\text{Worst case additional tempco due to } R_2 = \frac{+\,|x| R_{DAC\ max}}{100 R_{DAC\ min}}(\gamma_2 - \varsigma) \qquad (6)$$

IMPLICATIONS OF COMPONENT TEMPERATURE COEFFICIENTS ON THE DESIGN AND SPECIFICATION OF D/A CONVERTERS

From equations (3) and (4) it can be seen that if R1 and R2 have the same temperature coefficient, then the overall additional (circuit) temperature coefficient is given by

$$\frac{R_2 - R_1}{R_{DAC}} \cdot (\gamma - \varsigma)\,.$$

If the D/A converter has no gain error then R2 = R1 and there is no additional temperature coefficient due to R1 and R2. Clearly then R1 and R2 should preferably be the same type of resistor with the same temperature coefficient. Hence, it is always best to use a "select on test" fixed resistor for R1. The temperature coefficient of potentiometers usually varies with setting, so that it is difficult to match potentiometer temperature coefficients to that of fixed resistors. Figure 2 shows a distribution of gain error for a batch of AD7542 12-bit D/A converters. The average gain error is zero, so that the average temperature coefficient of applications circuits will be zero. This is of little comfort to the worst case applications circuit designer, but a necessary consideration of the IC designer.

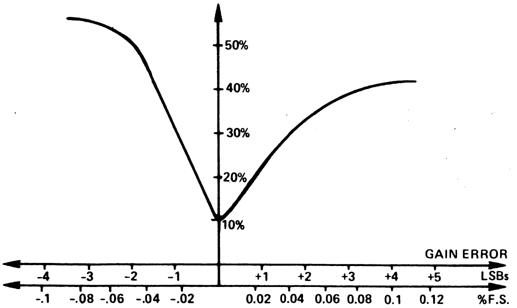


Figure 2. Cumulative Distribution of Gain Error for One Batch of AD7542s (All Grades)

An alternative strategy for the IC manufacturer would be to design and specify the D/A converter so that its gain error is always in one direction (as opposed to plus and minus) and the average gain error is centered some distance from zero. This has the advantage that R2 (or R1 depending on the direction of skew) could be omitted from circuit. However, R1 will always have a finite value and there will always be an additional temperature coefficient due to the gain trim circuit. Since precision resistor temperature coefficients are usually positive and the D/A converter resistor temperature coefficient is negative, the two will add (see equation 5) to give a significant temperature coefficient overall.

A better approach to minimizing additional temperature coefficients due to gain trim components is to improve the figure of merit

$$\frac{|x| R_{DAC\ max}}{R_{DAC\ min}}$$

and, if possible, to improve the temperature coefficient of the resistors used to manufacture the D/A converter. Unfortunately, it is not possible to change ς without changing other critical resistor parameters and the designer is left with the option of reducing the specified gain error spread x and minimizing the spread of R_{DAC} values. Recognizing this requirement, Analog Devices has introduced a "G" selection on gain error (x) for some of its more recent D/A converter products. "G" selected products have a specified gain error at 25°C of not more than plus or minus 1LSB (least significant bit). This represents more than a twelve fold improvement in the figure of merit. For many applications such a tight gain-error specification will be sufficient to eliminate any requirement for gain trimming, but where gain trims are still used, the additional temperature coefficients introduced by the very small values of R1 and R2 required for "G" selected parts will be so small as to be negligible. This is considered in more detail in the next section.

It is also possible to select R_{DAC} to a narrower spread of values, and to improve the figure of merit even more. However, the net improvement in gain temperature coefficient which results from such a selection is difficult to justify on a commerical basis.

PRACTICAL EFFECTS OF COMPONENT TEMPERATURE COEFFICIENTS

Table 1 shown on next page summarizes the worst case component gain drifts over a 100°C range for the AD7542TD, AD7542GTD, 12-bit D/A converters and the AD7527UD and AD7527GUD 10-bit D/A converters. In drawing up this table it has been assumed that precision wire-wound resisors with a temperature coefficient of +50ppm/°C have been used for R1 and R2. The actual values of R1 and R2 are given in this table. R_{DAC} temperature coefficient has been assumed to be -300ppm/°C.

It will be seen that for the "G" selected parts, the worst case additional temperature coefficient due to R1 and R2 is so small as to be negligible compared with the worst case 5ppm/°C temperature coefficient of gain error for the D/A converter itself.

LEAKAGE CURRENT EFFECTS ON GAIN

This note is primarily intended to cover the effects of external gain trim resistors on overall gain temperature coefficient.

However, it is worth noting that apparent gain shifts with temperature can be caused by op amp offset and bias current drifts, changes in V_{REF} and by D/A converter leakage currents at the I_{OUT} terminal of Figure 1.

The I_{OUT} leakage current effect on gain is negligible at 25°C, but at higher temperatures it can have some effect. Leakage current has two components:-

1. Leakage from the V_{DD} supply to the I_{OUT} terminal. This is more or less independent of input code.
2. Leakage from the R-2R ladder through off-switches. This leakage is a maximum for all zeros at the input because all switches are off, and is a minimum with all ones at the input, i.e., all switches on.

Usually the two components of leakage current are roughly equal, but this depends a great deal upon circuit design and layout, fabrication process, and temperature. Leakage from the V_{DD} supply produces a constant shift on the D/A converter transfer function as depicted in Figure 3—the magnitude of the shift is exaggerated in the diagram to make it clearer. Leakage from the R-2R ladder produces a rotation of the D/A transfer function as shown in Figure 4. The magnitude and direction of rotation due to leakage across "Off Switches" is determined by V_{REF} as shown.

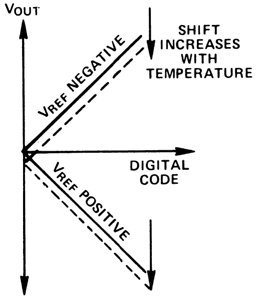


Figure 3. Graph Showing Shift of DAC Transfer Function Due to Leakage From V_{DD}

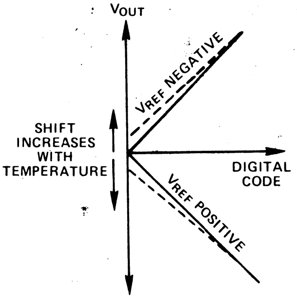


Figure 4. Graph Showing Effect of Off-Switch Leakage on DAC Transfer Function

Leakage current effects on gain error are usually only of significance at operating temperatures above 100°C where the worst case error voltages due to leakage current begins to become comparable to 1LSB worth of current. The user should be aware of leakage current effects because they have often in the past, been erroneously interpreted as being due to gain trim components.

Some electrical cleaning solvents, used to wash printed circuit boards after soldering, leave a slightly conductive film on the components after drying. These films introduce leakage paths from V_{DD}, V_{REF} and other pins to I_{OUT} of the D/A converter and the effect can be similar to that due to leakage effects in the converter chip itself. The user should ensure that such films do not occur during the manufacturing processes for any precision analog circuits.

SPECIAL CASES OF LEAKAGE CURRENT EFFECTS

(a) $\underline{V_{REF} = -10V}$

With a negative reference voltage the two leakage effects shown in Figures 3 and 4 tend to cancel each other at zero output, and give a net decrease in gain at full scale. The gain trim resistors R1 and R2, on the other hand, introduce a positive temperature coefficient of gain (i.e., increase in gain) so that the combined result of all these effects is to reduce the gain variation with temperature.

(b) $\underline{V_{REF} = +10V}$

For a positive reference voltage the two leakage effects add to each other and add to any positive gain temperature coefficient due to R1 and R2. The combined result is a positive increase in the gain temperatue coefficient due to all three effects. Positive reference applications, therefore, suffer more gain variation with temperature than negative reference applications.

SUMMARY

This text has been concerned with factors which cause the gain of CMOS multiplying D/A converters to vary with temperature.

The primary factors are:-

1. Gain temperature coefficient of the D/A converter itself.
2. Gain temperature coefficient due to the gain trim resistors R1 and R2.
3. Gain shift due to leakage from V_{DD}.
4. Offset shift due to leakage across off switches.

The additional gain temperature coefficient due to R1 and R2 is minimized by using the same type of resistor for R1 and R2 and by minimizing the specified maximum gain error of the D/A converter.

Leakage currents can produce gain errors. Applications using negative reference voltages are less sensitive to temperature variations than positive reference applications.

	Specified Values				**Trim Values**		**Worst Case Additional Gain Tempco Due to R_1 & R_2 ppm/°C**	**Worst Case Full Scale Gain Shift Over 100°C Due to R_1 and R_2**	
Part Number	**$R_{DAC\ max}$ kΩ**	**$R_{DAC\ min}$ kΩ**	**Worst Case Gain Tempco (ppm/°C)**	**Worst Case Untrimmed Gain Error at +25°C**	**R1 Ω**	**R2 Ω**		**LSBs**	**%**
AD7542TD	25	8	5	±0.3% (±12LSB)	150	75	3.28	1.34	0.033
AD7542GTD	25	8	5	±0.0244% (±1LSB)	12.4	6.2	0.27	0.11	0.0027
AD7527UD	20	7	5	±0.49% (±5LSB)	196	98	4.9	0.5	0.049
AD7527GUD	20	7	5	±0.098% (±1LSB)	40	20	1.0	0.1	0.01

Note: AD7542 is a 12-bit D/A converter.
AD7527 is a 10-bit D/A converter.

Table 1. Worst Case Full Scale Gain Error Due to Gain Trim Components R1 and R2 for a Selection of D/A Converters

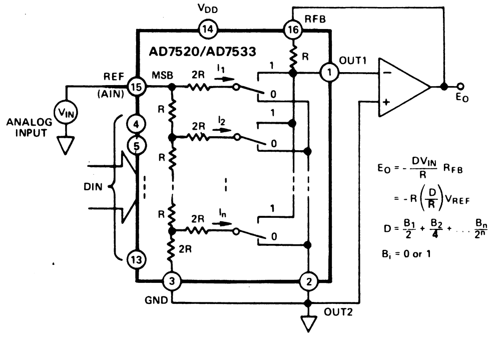
ANALOG
DEVICES

APPLICATION NOTE

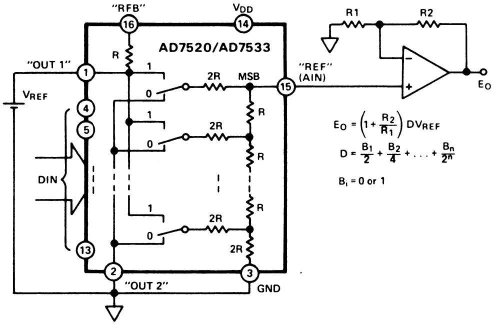
CMOS DACs in the Voltage-Switching Mode Can Work from a Single Supply, Including Output Op Amp, For Fast Response, No Offset-Induced Nonlinearity

by Steve Stephenson

The versatile R-2R ladder attenuator can be used as either a voltage or a current source, and it may be used in either a current-steering or a voltage-switching mode.[1] Figure 1a shows the familiar connection of a CMOS d/a converter, such as the 10-bit AD7520, in the current-steering mode; Figure 1b shows how the DAC can be connected for voltage switching by reversing the roles of the MSB node (REF/AIN) and the active switch bus (OUT1).


VDD
14
16
RFB
AD7520/AD7533
R
1
OUT1
REF
(AIN)
15
MSB
2R
I_1
0
1
V_{IN}
ANALOG INPUT
4
5
R
2R
I_2
DIN
R
2R
I_n
2R
13
3
2
GND
OUT2
Eo
$E_O = -\frac{DV_{IN}}{R} R_{FB}$
$= -R\left(\frac{D}{R}\right)V_{REF}$
$D = \frac{B_1}{2} + \frac{B_2}{4} + \dots \frac{B_n}{2^n}$
$B_i = 0$ or 1

(a). Current-Steering Mode


"RFB"
16
VDD
14
R1
R2
AD7520/AD7533
R
"OUT 1"
1
2R
MSB
"REF" (AIN)
15
VREF
0
1
4
5
R
2R
R
DIN
R
2R
2R
13
2
"OUT 2"
3
GND
Eo
$E_O = \left(1 + \frac{R_2}{R_1}\right) DV_{REF}$
$D = \frac{B_1}{2} + \frac{B_2}{4} + \dots + \frac{B_n}{2^n}$
$B_i = 0$ or 1

(b). Voltage-Switching Mode

Figure 1. CMOS DAC Connected for Different Operating Modes

CURRENT STEERING

In the current-steering mode, since the OUT2 terminal is at ground potential, the operational amplifier maintains OUT1 at the same voltage (virtual ground), and the binary-weighted currents through the 2R switch legs are independent of switch position. As commented upon in an earlier article,[2] the output capacitance and resistance (as seen by the amplifier's input) vary as functions of the input digital code. This makes the feedback-circuit's *noise gain* dependent on the code. The variation of resistance can cause the linearity to be affected if the amplifier has sufficient offset voltage. The variation of the output time-constant means that feedback compensation can, at best, only be a compromise. To ensure circuit stability for all codes, overcompensation (and consequent reduced bandwidth and increased settling time) is required.

There is also some charge injection from the gate of the switch, via the inherent capacitance between the gate and channel of the FET switch. This charge must take the lowest-impedance path to ground, in this case through the virtual ground of the amplifier. At major code-changes, output glitches may be significant.

VOLTAGE SWITCHING

In the voltage-switching mode, the constant resistance at the amplifier input eliminates the problems caused by modulation of the amplifier's offset voltage. In addition, the switch capacitance is remote from the amplifier, and the charge is shunted to the input source or to ground. Furthermore, the output capacitance of the network is considerably lower. All of this results in cleaner and faster response of the circuit to code changes.

As an additional important feature, the system's output voltage is of the same polarity as the reference voltage; as will be seen, this makes it possible to *operate the DAC and its amplifier from a single-polarity supply*. Finally, only a single amplifier is required for bipolar digital operation, using offset binary or (with the MSB complemented) 2's complement coding.

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[1] Examples of current steering and voltage switching may be seen in the *Analog-Digital Conversion Notes* (Analog Devices, 1977, ed by D. Sheingold, available at $5.95 postpaid), pages 116–117 and pp. 133–138.

[2] "Analog Signal-Handling for High Speed and Accuracy," by A. Paul Brokaw, *Analog Dialogue* 11-2 (1977), pages 10–16.

Reprinted from Analog Dialogue 14-1, 1980.

The configuration has a few minor disadvantages. Since the ON resistance of the FET switch increases the applied drain-source voltage approaches the value of the gate-drive voltage, and significant values of R_{ON} cause the division of voltage to depart from the ideal, large values of reference voltage will produce nonlinear performance.[3] However, for values of reference voltage less than +3.5V and V_{DD} = +15V, the 10-bit DACs in the AD7500 series will retain their linearity. The 12-bit DACs will maintain 11-bit accuracy over temperature when employing a +2.5V reference (eg., the AD580).

While the current-steering mode permits input voltages of either polarity and allows the circuit to function as a digitally controlled potentiometer (and as a four-quadrant multiplier), the voltage-switching mode permits only a single polarity of input (positive with respect to common).

CIRCUIT POSSIBILITIES

Single Supply, Unbuffered. In Figure 2, the circuit of Figure 1b, without a buffer, is implemented with an AD584 as an adjustable reference. Settling time of better than 1µs was observed, with overall conversion linearity to 10 bits, using a 3.5V (max) reference voltage. Although the network can be loaded resistively, buffering is preferred, since the different temperature sensitivities of an external load resistance and the ladder resistance will result in a temperature-sensitive scale factor.

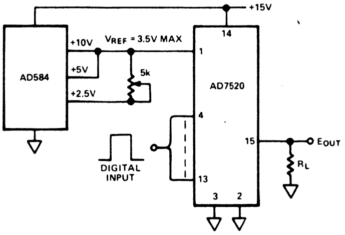


Figure 2. Single-Supply DAC with AD584 Reference, Unbuffered Output

Single Supply, Buffered. In Figure 3, the DAC and the CMOS op amp are both powered from a single +15V supply. With this circuit, 10-bit linearity and good gain-temperature coefficient (since there are no external resistors sharing current with the ladder) were achieved over ambient temperatures up to 125°C. With a single-supply operational amplifier, offset is difficult to remove completely; therefore, some offset may have to be tolerated, usually amounting to less than one-half LSB at 3.5V reference. The observed settling time under these conditions, governed by the amplifier's performance, was found to be better than 2µs to one-half LSB.

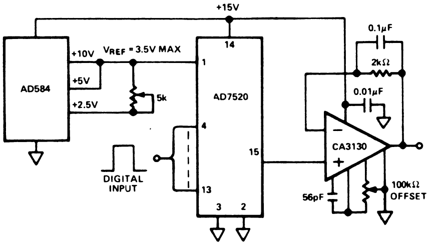


Figure 3. Single-Supply DAC, Buffered Output

Shorter Voltage-Settling Times. Figure 4 shows a circuit in which the voltage-switched mode is employed to obtain a *current* output, by connection of the ladder output directly to the summing point of the output amplifer. This connection provides the *fastest response* (settling time of the order of 900ns was observed): however, the gain tempco is poor, because the external feedback resistance cannot be expected to track the network's resistance variation with temperature.

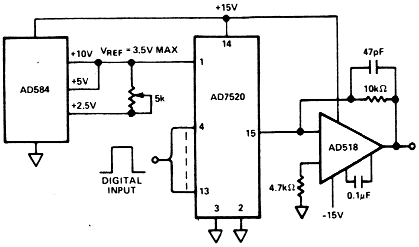
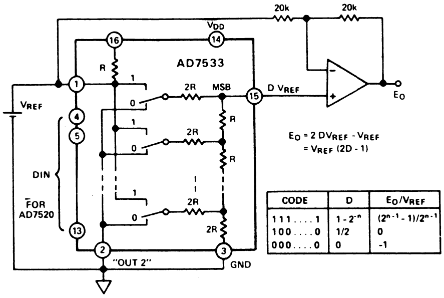


Figure 4. Increased Speed DAC

Simplified Bipolar Operation. Figure 5 shows how the voltage switched mode simplifies the conversion of bipolar digital signals.[4] The output voltage from the ladder is applied at the amplifier's positive input, as in Figure 1b; the reference is connected to the inverting input via a resistance equal to the feedback resistance. Thus, the output of the ladder has a gain of 2, and the reference has a gain of −1; as the equation and the table show, this provides conventional offset-binary response, but *with a single amplifier*, instead of the two called for in the current-steering mode.



$$E_O = 2\,DV_{REF} - V_{REF} = V_{REF}\,(2D - 1)$$

CODE	D	E_O/V_{REF}
111 1	$1-2^{-n}$	$(2^{n-1}-1)/2^{n-1}$
100 0	1/2	0
000 0	0	-1

Figure 5. Connection for Bipolar Operation. If V_{REF} is Provided by the 2.5V AD580, Nominal Output Swing is ±2.5V

SUMMARY

Using the techniques described here, Analog Devices CMOS d/a converters in the series AD7520, AD7521, AD7522, AD7523, AD7524, AD7530, AD7531 and AD7533 may all be made to operate in the voltage-switching mode with their published specified linearity. System benefits include the possibility of single-supply operation, increased speed, freedom from offset-voltage modulation, and more-economical digital bipolar operation.

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[3] *Application Guide to CMOS Multiplying D/A Converters,* Analog Devices, 1978.

[4] "An Unusual Circuit Configuration Improves CMOS-MDAC Performance," by N. Sevastopoulos *et al EDN* Magazine, March 5, 1979, pp. 77–82.

ANALOG DEVICES

APPLICATION NOTE

Methods For Generating Complex Waveforms and Vectors Using Multiplying D/A Converters

by Phil Burton

Complex analog waveforms are used in a variety of equipment. They can define a process temperature profile, be used to generate high resolution graphics either on a CRT or X–Y plotter, or form the basis of a speech synthesizer. There are as many solutions to the problem of waveform generation as there are applications. This note describes some common methods for generating complex waveforms using CMOS multiplying D/A converters. The applications bias, is towards graphics displays because most engineers will understand the applications but designers of other equipment will immediately recognize the relevance of the various techniques to their own particular problem. The treatment is mostly in block diagram form with the emphasis on a systems approach rather than detailed circuit design. The implications of the various methods of interfacing D/A converters to computer systems are also covered with regard to the hardware and software requirements of the system.

STAIRCASE WAVEFORM SYNTHESIS

Figure 1 shows a simplified waveform generator consisting of a DAC driven from a ROM look-up table, and a counter which provides sequential addresses for the ROM. The frequency of the generated waveform is determined by the clock rate of the counter and the number of memory words used to define the waveform.

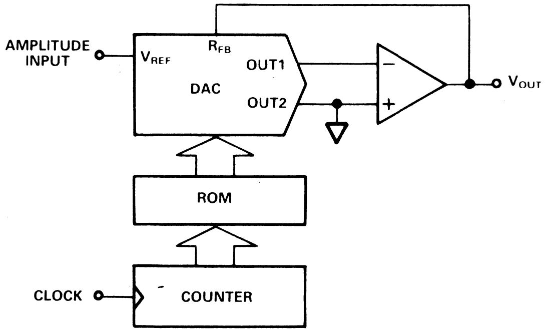


Figure 1. Simple ROM Waveform Generator

If the waveform is symmetric as in a sinusoid, then the size of the ROM can be reduced by only coding one quadrant and using digital arithmetic on the output and input of the ROM to generate the words for the other three quadrants.

When a ROM contains the values of sin θ for $0<\theta<90$ then the values for the other three quadrants can be computed as follows:

For $90 < \theta < 180°$ $\sin\theta = \sin(180-\theta)$
For $180 < \theta < 270°$ $\sin\theta = \sin(\theta-180)$
For $270 < \theta < 360°$ $\sin\theta = \sin(360-\theta)$

Suppose θ is represented by a 10-bit binary number to cover the range 0 to 360°, then the two most significant digits of θ will determine the quadrant of operation. Furthermore the most significant digit will determine the sign of sin θ and the second most significant digit will determine whether the remainder of the number is to be used as it stands, or substracted from the binary equivalent of 180°. Note that 180° in our chosen 10-bit notation is 10,0000,0000 and 2's complement subtraction is achieved by complementing the number and adding 1. Complementation can be achieved by exclusive–OR gates. Figure 2 shows in block diagram form a high resolution sine-wave synthesizer using a one quadrant look-up table.

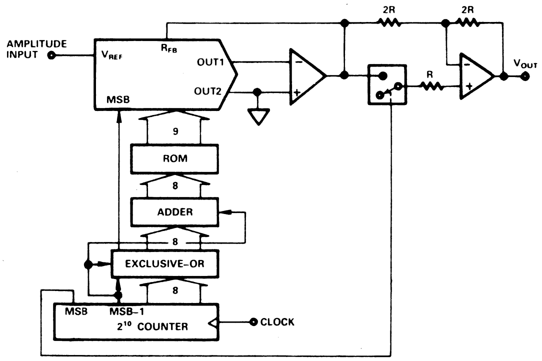


Figure 2. Block Diagram of Sinusoid Generator

The 10-bit D/A converter is operated with sign plus magnitude coding, the most significant bit of the 10-bit word being fed to the sign switch. The second MSB of the 10-bit word, representing θ, determines whether the remaining bits are complemented or not using the exclusive OR gates, and it also provides the +1 required for 2's complemented subtraction. The eight-bit word from the adder is fed to the ROM look-up table which provides the appropriate digital word to the D/A converter.

If the addresses to the ROM are generated by a counter, the adder and exclusive OR circuits can be dispensed with by using a counter which alternately counts up to 1111,1111 and then counts down to 0000,0000. An additional flip-flop is required to generate the sign. This method is described on page 27 of "Application Guide to CMOS Multiplying D/A Converters" available from Analog Devices.

Sinusoid generators such as the one described above have been used in radar displays (A Scopes) and Synchro to Digital Converters. In both of these applications the ease with which the reference voltage V_{REF} can be varied, to change the magnitude of $\sin\theta$ is a distinct advantage. This results directly from the multiplying properties of CMOS multiplying D/A converters. Some of the disadvantages of the approach described above are the relatively low frequencies that can be generated with any precision, and the presence of quantisizing noise due to the output being defined in discrete steps. Also, the D/A converter has a relatively long settling time (2μs approximately), so that the output waveform contains glitches at every change of digital input.

BASIC INTERPOLATION METHOD FOR WAVEFORM GENERATION

If the staircase method of waveform generation was used to draw a sawtooth on a X–Y plotter then the drawn waveform would have a staircase appearance due to the discrete output steps available from the D/A converter. Clearly such an appearance is not desirable and consequently analog graphic output systems have adopted an interpolative method of generating waveforms. Not only does this method give a cleaner looking waveform, but it also allows a much higher frequency of operation, and reduces to a minimum the number of digital words necessary to define a waveform.

An interpolative method uses two D/A converters to generate a waveform–one to define the starting point and another to define the finishing point. A straight line is drawn between the start and finish. Figure 3 shows a sinusoid drawn by an interpolative waveform generator, and the associated waveforms for the circuit of Figure 4.

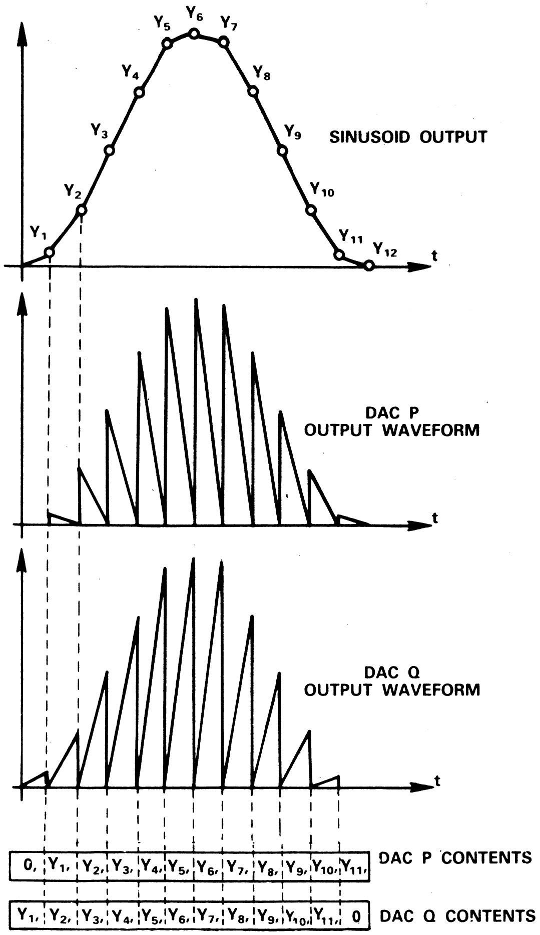


Figure 3. Synthesis of Sinusoid Using Circuit of Figure 4

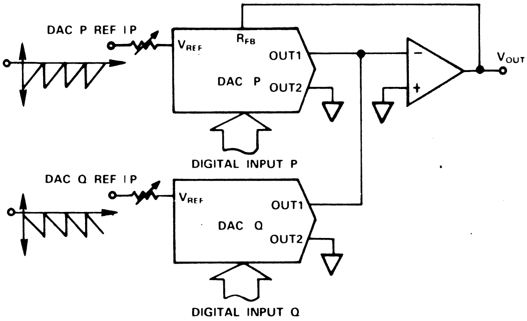


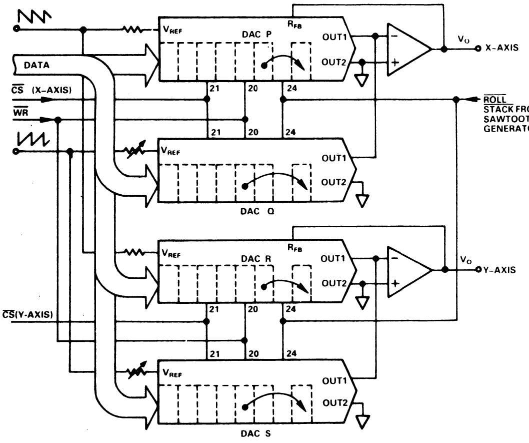
Figure 4. Elementary Interpolation Method

Figure 4 shows a simple interpolation scheme such as might be used to drive one axis of an X–Y plotter or a CRT graphics display. The digital inputs to DAC P define the starting point and DAC Q inputs define the finishing point of the straight line to be drawn. The reference input to DAC P consists of a positive going ramp which goes from $-V_{MAX}$ to 0 in time T. The reference to DAC Q is an equal but opposite ramp which goes from 0 to $-V_{MAX}$ during the same period T. The sum of the outputs of DAC P and DAC Q is given by:

$$V_{OUT} = N_p\left(V_{MAX} - \frac{V_{MAX}}{T}t\right) + N_q\left(\frac{V_{MAX}}{T}t\right)$$

$$= N_p V_{MAX} + (N_q - N_p)\frac{V_{MAX}}{T}t$$

which is a straight line between the two points defined by the binary number N_p in DAC P and the number N_q in DAC Q. For the next line to be drawn P is loaded with Q's value and Q is loaded with the new finishing point and the process is repeated. In drawing a number of points DAC P and DAC Q receive exactly the same binary input words except the DAC Q inputs are always one word in front of DAC P inputs. This suggests a FIFO (first-in, first-out) structure with DAC P being fed from the output end of the FIFO, and DAC Q being fed with the "next to the end" word of the FIFO. The FIFO has the additional advantage that a number of data points can be loaded into the FIFO by the main processor at one burst, and then the points can be clocked out of the FIFO at a rate determined by the repetition frequency of the reference sawtooth waveforms. This leads to very efficient software and minimizes the time the processor is tied up in I/O operations. Figure 5 shows a simplified graphic display system using the method described above. The main portion of the system is based on four AD7544s which are 12-bit D/A converters with integral 6-word FIFO registers. Each x coordinate is loaded by the computer to both x-axis DACs simultaneously, similarly for the y-axis DACs. This reduces the data transfer operation to one x and one y value per coordinate. DAC's Q and S are loaded from the next to the end word of the FIFO and DAC's P and R are loaded from the end word of the FIFO—this is shown in Figure 5 by the curved arrows. The DAC Register of the AD7544 can be loaded from either the top or next to top word of the FIFO. At the point when the data feeding the DACs is changed, the D/A outputs will exhibit some glitches, due to the settling time of the DAC and op amps, slew rate of the sawtooth, digital feedthrough, etc. During this update period, the CRT display should be blanked off. In electromechanical displays the transients are usually absorbed by the mechanical inertia of the system.



All D/A converters are AD7544.

The following pin connections have been omitted from all DACs in the above drawing to preserve clarity:

Pin 19	RESET	Normally connected to the system reset.
Pin 22	SFUL	Stack Full – indicates stack full to processor.
Pin 23	SAMT	Stack Almost Empty – used to interrupt the processor to load another burst of data to the FIFOs.
Pin 25	RLEN	Roll Enable – strapped low.
Pin 26	LDAC	Load DAC – strapped high. This makes the DAC register transparent.
Pin 27	W1/W2	Selects top or next or top word of stack. DAC's P&R have this pin strapped high, DAC's Q&S have it strapped low.

Figure 5. Simplified Graphic Display System

IMPROVED INTERPOLATION METHOD FOR WAVEFORM GENERATION

In the scheme of section "Basic Interpolation Method for Waveform Generation", converter P always holds the starting value of the vector and converter Q the finishing value. Unwanted transients occur each time the digital values to the D/A converters are updated. These transients can be overcome by continuously alternating the roles of converters P and Q. In Figure 3 note that each digital value is first subjected to a positive going ramp in DAC Q and then subjected to a negative going ramp in DAC P. Instead of feeding each digital word to DAC Q and then one sawtooth later to DAC P, each word can be input to a single DAC and a triangle wave is now applied to the reference of the DAC. Figure 6 shows a circuit to achieve this together with the two reference waveforms for converters P and Q and the successive data words applied to P and Q. *Note in particular that the data words applied to the D/A converters are updated when the D/A reference input is zero.* This avoids most of the slew rate and settling time problems of the circuit of Figure 4, although there will still be a small glitch at the output of the D/A converter due to digital feedthrough. When using AD7544s, the effective memory capacity at the FIFO is doubled because there is no duplication of memory contents.

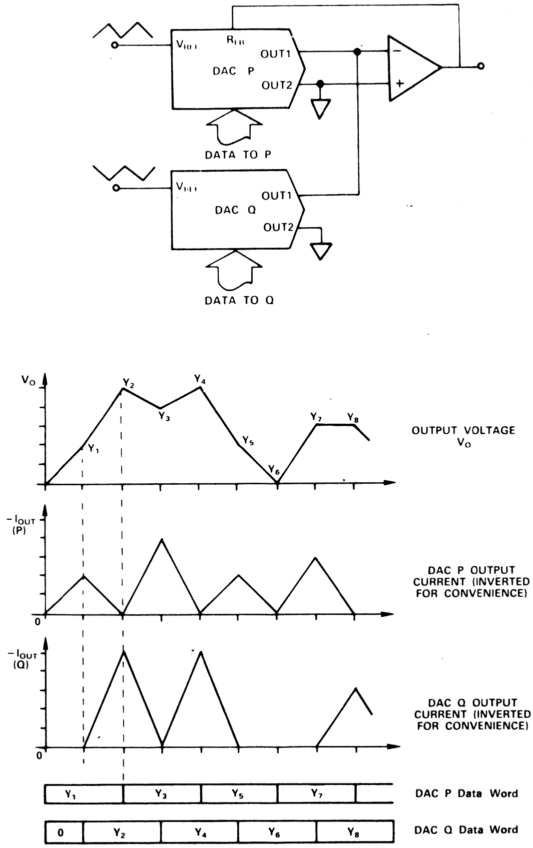


Figure 6. Improved Interpolation Method and Waveform

This improved method is particularly suitable for continuous waveform generation because there are no significant transients (or blanking periods) in the signal.

TRIANGLE AND SAWTOOTH WAVEFORM GENERATION

The triangle and sawtooth reference waveforms required for the circuits of sections "Basic Interpolation Method for Waveform Generation" and "Improved Interpolation Method for Waveform Generation" can, in some applications, be fixed frequency waveforms. However, in graphic display systems, this would allocate exactly the same time for each drawn vector. A short vector would take just as long a time to draw as a long vector, with the result that a CRT display would exhibit uneven brightness and an X–Y plotter would have to be restricted to drawing each vector at the time taken to traverse a full axis. Clearly a better solution for vectors drawn on a CRT would be to scale the waveform ramp rate in accordance with the length of the vector to be drawn. A long vector would be drawn using a slow ramp and a short one by a much faster ramp. For electromechanical X–Y plotters, the ramp rate would be determined by whichever axis has the greatest distance to travel. Figure 7 shows a simple circuit for generating programmable sawtooth waveforms suitable for the interpolation method described in section "Basic Interpolation Method for Waveform Generation". The circuit consists of a resetable integrator (A1), the ramp rate of which is determined by a D/A converter. A comparator determines when the ramp has reached its maximum value, and the output of the comparator is used to reset the integrator and to trigger a one-shot for blanking the screen during the reset period of the sawtooth and the settling time of the D/A converter. The output of the comparator is also used to clock the FIFOs associated with each D/A converter, so as to load the next vector coordinates to the DACs. Amplifier A2 provides the inverse sawtooth waveform which drives the reference input of DAC Q in Figure 4.

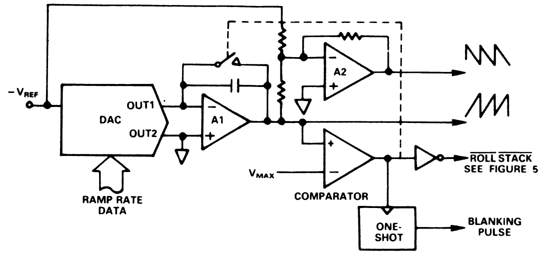


Figure 7. Simplified Sawtooth Generator

Figure 8 shows a programmable triangle waveform generator, which uses two D/A converters, one to determine the upward ramp and another to determine the downward ramp. The integrator A1 has two input resistors and switch S1 switches between the two D/A converters to provide the up and down ramps. The digital inputs to the D/A converters are changed during the half cycle when the converter output is not being used to drive the integrator. This allows the D/A converters adequate time to settle before its output is switched to the integrator.

Switch S1 is a two pole, N-Channel changeover switch such as normally used for the switches in a CMOS D/A converter. This type of switch ensures that the two D/A converter outputs see a constant load impedance, thereby preventing load induced glitches; it also provides a fast changeover for the integrator inputs. The switches can be formed from CD4016s or alternatively an AD7201 can be used which incorporates 5 changeover switches with resistors in one package. Amplifier A2 provides the inverse triangle waveform. Comparators A3 and A4 are used to detect the peak and the trough of the triangle waveform, and to generate the clock signals for the FIFOs feeding the D/A converters.

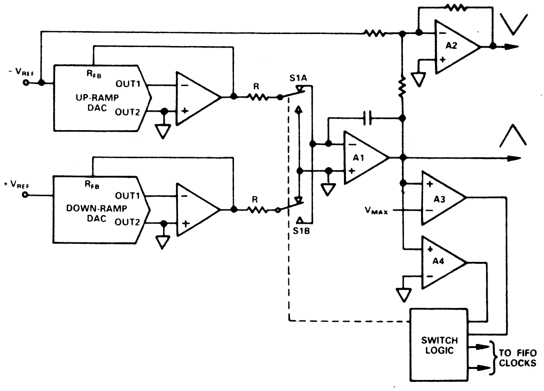


Figure 8. Programmable Triangle Waveform Generator

A COMPLETE GRAPHICS GENERATOR

Figure 9 shows a complete simplified schematic of a graphics vector generator using triangle waveforms (i.e., the scheme of section "Triangle and Sawtooth Waveform Generation"). All the D/A converters are AD7544's. DAC 1 is the odd-coordinate x-axis DAC and DAC 3 is the odd-coordinate y-axis DAC. Together DAC 1 and DAC 3 define the points $(x_1,y_1)(x_3,y_3)$ etc.; DAC 2 and DAC 4 are the x and y even-coordinate DACs respectively. DAC 5 defines the upward ramp of the triangle, from the integrator and DAC 6 defines the downward ramp. The 6-word on-chip FIFOs of the AD7544 enable 12 full vectors to be stored by the system.

The vector generator is entirely self-clocking and its effective "clock rate" is determined by the ramp-rates of the triangle wave generator (i.e., by the length of the vectors to be drawn). In operation the vector coordinates are loaded to the DAC's FIFOs by a burst of data words from the system's computer and the graphics generator clocks the data through the FIFOs to the DACs under its own control. When only one word of data remains in a FIFO, the AD7544 generates an "almost empty" signal which is used to interrupt the main processor and initiate the transfer of another block of data coordinates to the graphics circuit.

An undrawn line (i.e., beam blanked) is encoded as a full-scale value to the inputs of DAC 5 or DAC 6. Comparators

A5 and A6 detect a full-scale output and their outputs are used to provide the blanking pulse to the display. In CRT graphics an undrawn line will always be generated at maximum velocity, thus the blanking encoding information scheme is consistent with practice. The circuit is designed so that drawn lines are always drawn with a ramp rate much lower than defined by the full scale output of the DAC.

For electromechanical plotters the situtation is not quite so simple and the problem of undrawn lines has to be solved either by a separate FIFO to store pen lift signals, or by encoding an undrawn line as an ordinary line which is followed by a line of zero length drawn at maximum velocity. Comparators A5 and A6 and DAC 5 and DAC 6 give not only the ramp rate for the line to be plotted, but also the rate for the next line to be plotted (once the DAC has settled). If a comparator detects that the *next* line is to be plotted at maximum rate (a speed which is never used for a genuine drawn line), then the output of the comparator can be used to supply pen-lift signal for the current line. Once this undrawn line has been completed, the next line, which has the maximum ramp rate information in its DAC will simply cause the pen to remain in the same position–hence an undrawn line from one point to another could be created. This pen lift scheme is not shown in Figure 9, but it is a relatively simple matter to modify Figure 9 as discussed above.

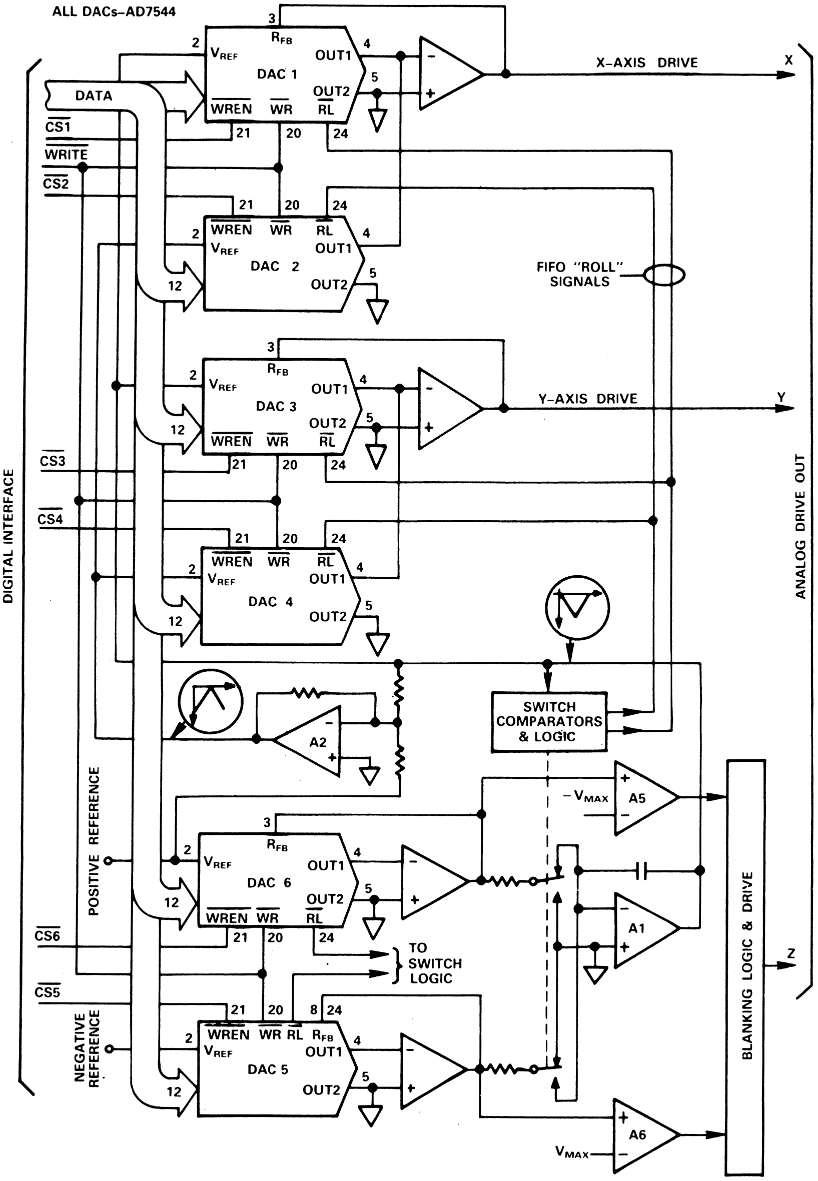


Figure 9. Simplified Graphics Generator Using Triangle Waves

THE PROCESSOR INTERFACE

As mentioned in the section "Triangle and Sawtooth Waveform Generation", the graphics system of Figure 8 is an asynchronous, self-clocking scheme. The on-chip FIFOs of the AD7544 provide a perfect interface between the high speed synchronous processor and the asynchronous graphics circuit. The FIFOs are self-clocking and generate "almost empty" and "full" signals so that the processor can be interrupted when more coordinates are required, and can signal when a full set of coordinates have been received. The design of the full digital interface between processor and graphics circuit is beyond the scope of this article. It is no simple matter to connect six 12-bit D/A converters to a high-speed microprocessor bus without incurring unwanted digital cross talk. It is preferable that the 12-bit bus feeding the graphics circuit should have its own set of data bus buffers which are only enabled when data is being transferred to the FIFOs. At all other times the bus to the converters should be tied to a logic high or a logic low. If the graphics circuit is being fed from an 8-bit data bus, the 8-bit data latch necessary to reassemble the 12-bit word for the FIFOs can also be used as part of the computer data bus to graphics data bus buffer suggested above. Very careful ground management should be used, with the graphics circuit having its own digital and analog grounds tied back to the "quiet point".

COMPUTING THE TRIANGLE RAMP DATA

The ramp rate of the triangle (or sawtooth) waveform is variously related to the distance between the two points to be drawn. For electromechanical plotters it is only necessary to ascertain which axis has to move the furthest and then scale the distance moved according to the equation.

$$\text{Ramp DAC data} = \text{Constant} \times \frac{1}{\text{Distance Moved}}$$

Calculating reciprocal of the distance moved is usually done in the microcomputer since electromechanical plotters are relatively slow and there is adequate time to make the calculation. Note, however, that if a DAC is connected as the feedback resistor of an inverting amplifier, the amplifier output voltage is proportional to the reciprocal of the digital code at the DAC inputs (see page 26 of "CMOS D/A Converter Application Guide"). This could be used as an analog "reciprocal taker" and scaler to ease the software burden on the microcomputer.

In CRT displays the ramp data is directly proportional to the distance along the vector, i.e., $\sqrt{(\Delta x)^2 + (\Delta y)^2}$ and it is difficult to solve such an equation at high speed. Fortunately it is not necessary to encode the CRT intensity information to a high degree of resolution and a lookup table method can be used. Addresses for the lookup table are generated by combining say the top 4-bits of Δx with the top 4-bits of Δy to create an 8-bit address for the intensity lookup table.

An alternative high speed method for evaluating either $1/x$ or $\sqrt{x^2 + y^2}$ is to use a logarithmic number scheme such as the FOCUS number scheme in reference 1. The FOCUS scheme makes it possible to do multiplication, division, addition and subtraction by the use of only addition and subtraction and lookup tables. A D/A converter (AD7118) is now available which accepts numbers encoded according to the FOCUS scheme and delivers a proportional linear output current. Such a converter could be used for DAC 5 and DAC 6 in Figure 8, although the AD7118 does not have an integral FIFO.

SUMMARY

This paper have been deliberately brief. It is intended to stimulate ideas rather than give definitive circuit designs. As mentioned in the introduction, the treatment has centered on the design of graphics displays. This was done because a graphics display is something with which most engineers are familiar. However, graphics has the added complication that two channels of waveforms (x and y) are required whereas many applications, e.g., speech synthesis, only requires one channel. Fortunately most designers are experts at simplifying circuits. Graphic output from computers is becoming increasingly important; it is hoped that this article stimulates more engineers to design their own circuits.

REFERENCE

A. D. Edgar and S. C. Lee, "FOCUS" Microcomputer Number System, ":Commun. Ass. Comput. Mach. Vol 22, No. 3 p.p. 166–177. March 1979.

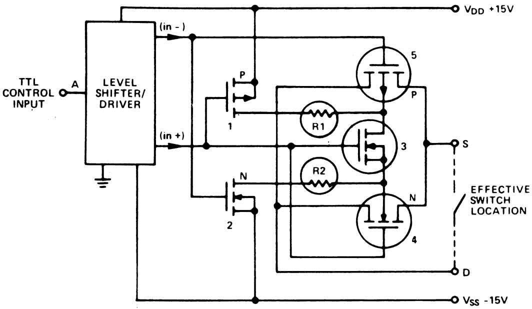
Behind the Switch Symbol: Use CMOS Analog Switches More Effectively When You Consider Them as Circuits

by Jerry Whitmore

CMOS analog switches are widely used to make or break circuits in such applications as multiplexing and function switching. Ideally, they have zero resistance when closed, infinite resistance when open, no leakage, instantaneous glitch-free response, and no parasitic capacitance. While these assumptions are reasonably valid for low-frequency applications at moderate impedance levels, the good designer will always challenge them, to establish what errors may be introduced and even to determine whether the circuit configuration is viable.

SWITCH CIRCUITS

Figure 1 is a reasonable approximation of the circuitry in a single-pole dielectrically isolated CMOS switch (e.g., AD7510DI or AD7590DI series).The dielectric isolation makes possible protection against latchup and overvoltage to ±25V beyond the supplies. Note that, for one polarity, conduction is via an N-channel FET; for the other polarity, it is via a P-channel FET. The two types are not perfectly symmetrical.



NOTE. CIRCLED DEVICES IN SEPARATE ISOLATED POCKETS.

Figure 1. Typical Output Switch Circuitry of the AD7590DI Series

Figure 2 is an equivalent circuit of a pair of adjacent switches. The parameters are defined in Table 1. There are three principal categories of error one should be concerned about: low-frequency errors due to resistances and current leakage (switch open or closed), high-frequency and signal-transient errors due to stray capacitances (switch open or closed) and dynamic errors due to switching transients while the state of the switch is changing. Because of the present limitations of space, we shall for now consider just the first category, since it answers the most urgent question, "How well does the switch actually work for low-frequency signals?"

C_{DS}	Open-switch capacitance
C_S,C_D	Source, drain capacitance
R_{ON}	Series on resistance
S,D	Source, drain; electrically interchangeable
C_{SS},C_{DD}	Capacitance between any two corresponding switch terminals
I_{LKG}	Leakage current of back-gate diode

Table 1. Nomenclature

Although the leakage currents of the P- and N-channel transistors (devices 4 and 5 in Figure 1) might appear to tend to cancel, they don't, since the P channel is three times larger than the N channel. Because of the size mismatch of the reverse-biased source-or-drain-to-back-gate diodes, plus the differing lot-to-lot variations in breakdown voltage of the diodes, it is difficult to predict leakage or its tempco. However, maximum values at 25°C and over temperature are specified and 100% tested.

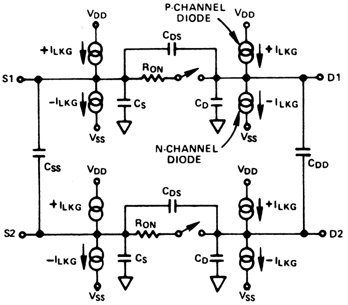
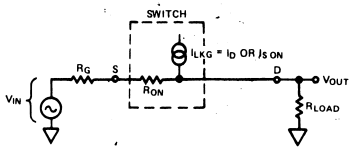


Figure 2. Equivalent Circuit of a Pair of Adjacent Switches

Figure 3 shows the factors affecting dc performance for the *on* switch condition and how the various parameters affect the output voltage. Figure 4 shows typical curves of R_{ON}, as they appear on the product data sheet. They indi-

Reprinted from Analog Dialogue 15-2, 1981.

cate how R_{ON}, is affected, as a function of input voltage, by supply voltages and by temperature. R_{ON} is lower and less signal-dependent at the higher supply voltages and lower temperatures.

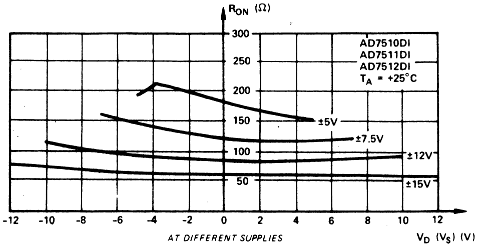


$$V_{OUT} = V_{IN}\left[\frac{R_{LOAD}}{R_G + R_{ON} + R_{LOAD}}\right] + I_{LKG}\left[\frac{R_{LOAD}(R_{ON} + R_G)}{R_G + R_{ON} + R_{LOAD}}\right]$$

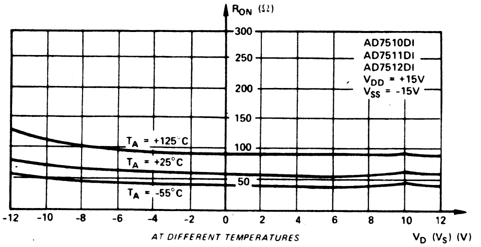
If $R_G \to 0$,

$$V_{OUT} = V_{IN}\left[\frac{R_{LOAD}}{R_{LOAD} + R_{ON}}\right] + I_{LKG}\left[\frac{R_{LOAD}\,R_{ON}}{R_{LOAD} + R_{ON}}\right]$$

Figure 3. Effective Circuit of Switch in the ON Condition



a. *R_{ON} vs. V_D (V_S), as a Function of + V_{DD}, (– V_{SS})*



b. *R_{ON} vs. V_D (V_S), as a Function of Temperature*

Figure 4. R_{ON} vs. Input Voltage as a Function of Supply Voltage and Temperature

How to minimize the influence of variable R_{ON} on circuit accuracy: Figure 5 shows a problem circuit–an inverting amplifier with four switched inputs. R_{ON}, in series with the 10-kilohm input resistor, affects the circuit gain. Even if it is compensated for at one level of supply voltage and analog input voltage, the input's variations will cause the gain to change and degrade the gain accuracy.

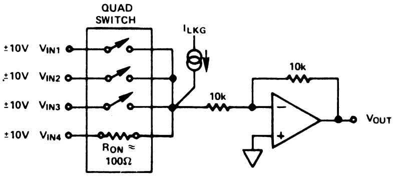


Figure 5. Unity-Gain Inverter with Switched Input

The most obvious solution–if the amplifier doesn't have to invert or act as a precision attenuator–is to use the amplifier in a noninverting mode, as shown in Figure 6. Since there are no resistors in series, there is no effect on gain.

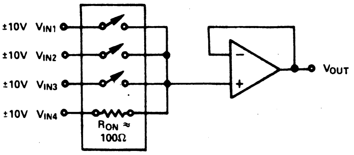


Figure 6. Noninverting Solution

Another solution (Figure 7) is to connect the quad switch at the amplifier's summing point. Then the switch sees only millivolts–rather than volts–of signal variation, minimizing the variation of R_{ON} with signal. This solution can impair bandwidth, since capacitance C_S may require a capacitor in parallel with the feedback resistor for compensation. Also, I_{LKG}, flowing through the feedback resistor, may cause significant error, depending on the accuracy requirements. ($\Delta V_{OUT} = I_{LKG} \times R_F$).

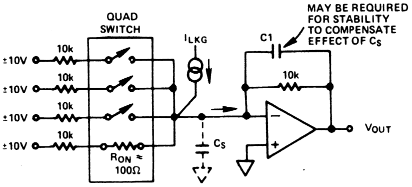


Figure 7. Connecting Switch at the Summing Point

Another possible solution is to use larger values of input and feedback resistance (Figure 8). Then the ΔR_{ON} variations will be small compared to the 1-megohm load. However, bandwidth will be affected by the larger R-C time constants.

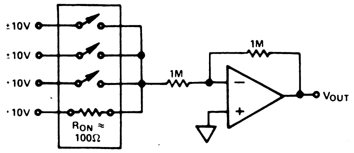


Figure 8. Using Larger Values of Resistance

Figures 7 and 8 do not compensate for the effects of variation of R_{ON} with temperature. A circuit that provides good compensation (Figure 9) uses one of the switches, wired *on*, in series with the feedback resistor. Its R_{ON} will tend to track that of the other switches on the same substrate with temperature; thus the feedback and input resistances will tend to track quite well, keeping the gain constant.

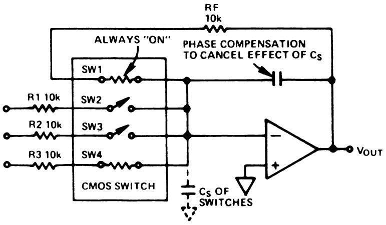


Figure 9. Switch in Series with Feedback Resistor to Compensate Gain

The principal dc effect in the switch *off* condition is that of I_{LKG} ($I_{D\ OFF}$ or $I_{S\ OFF}$), which will bias the output of a circuit by $I_{LKG} \times R_L$. Polarity of the error is determined by the dominant leakage polarity of a given switch.

Contents of Volume II

	SECTION
General Information	1
Comprehensive Index to Both Volumes	2
Ordering Guide	3
Operational Amplifiers	4
Isolation Amplifiers	5
Analog Multipliers/Dividers	6
RMS-to-DC Converters	7
Log-Antilog Amplifiers	8
Transducers & Signal Conditioners	9
Digital-to-Analog Converters	10
Analog-to-Digital Converters	11
Voltage-Frequency Converters	12
Synchro & Resolver Converters	13
Sample/Track-Hold Amplifiers	14
Data-Acquisition Subsystems	15
Digital Panel Instruments	16
Microcomputer Analog I/O Subsystems	17
μMAC Measurement-and-Control Subsystems	18
MACSYM Measurement & Control Systems	19
Linear-IC Test Systems	20
AC/DC and DC/DC Power Supplies	21

Selection Guides for Product Categories Not Included in This Volume

SIGNAL CONDITIONERS

		CURRENT (4 TO 20mA) OUT							
		I TO I	V TO I		TRANSMITTERS				
		2B24	2B20	2B22	2B52	2B53	2B57	2B58	2B59
Input Sensor	Thermocouple				●	●			
	RTD[1]							●	●
	AD590/AC2626 Temperature Sensor						●		
	Resistance Bridge								
Input Signal	Millivolts				●	●			
	Volts		●	●					
	4 to 20mA	●							
Output	0 to ±5V								
	0 to ±10V								
	0 to 20mA		●						
	4 to 20mA	●	●	●	●	●	●	●	●
	10 to 50mA	●							
	±15V Power								
Special Features	Transducer Excitation						●	●	●
	Open Input Detection				●	●	●		
	Cold Junction Compensation				●	●			
	Input/Output Isolation	●		●	●				
	Channel to Channel Isolation								
	Signal Filter				●	●	●		
	Linearization							●	
	Common Mode Rejection >140dB				●				
Power Required	Loop Powered	●		●[2]	●	●	●	●	●
	+14V to +32V		●	●					
	±15V								
	115V 60Hz Line								
Mechanical	Module		●	●			●		●
	Metal Case	●			●	●	●	●	
	Input Screw Terminals	●			●	●		●	
	Output Screw Terminals	●			●	●		●	
	#22 AWG Input/Output Leads								●
Volume II Page		9-25	9-9	9-13	9-35	9-35	9-47	9-51	9-53

[1] Resistance Temperature Detector.
[2] Provides 4 to 20mA out or may modulate Loop Power.

		VOLTAGE OUT							
		MILLIVOLTS IN							
		SINGLE-CHANNEL			MULTI-CHANNEL				
		2B30	2B31	2B50	2B34	2B54	2B55	2B56	2B35
Input Sensor	Thermocouple			●		●			
	RTD[1]				●				
	AD590/AC2626 Temperature Sensor								
	Resistance Bridge		●		●				
Input Signal	Millivolts	●	●	●	●	●			
	Volts						●	●	
	Line Power								●
Output	0 to ±5V			●	●	●	●		
	0 to ±10V	●	●					●	
	0.1 to 10mA								●
	4 to 20mA								
	10 to 50mA								
	±15V Power								●
Special Features	Transducer Excitation		●		●[1]				●
	Open Input Detection			●		●	●		
	Cold Junction Compensation			●				●	
	Input/Output Isolation			●		●	●		●
	Channel to Channel Isolation					●	●		
	Signal Filter	●	●	●	●	●	●		
	Linearization								
	Common Mode Rejection >140dB	●	●	●		●	●		
Power Required	Loop Powered								
	+14V to +32V								
	±15V	●	●	●	●	●	●	●	
	115V 60Hz Line								●
Mechanical	Module	●	●	●	●	●	●	●	●
	Metal Case								
	Input Screw Terminals			●					
	Output Screw Terminals								
	#22 AWG Input/Output Leads								
Volume II Page		9-19	9-19	9-31	9-25	9-37	9-37	9-43	9-29

[1] Resistance Temperature Detector.

DIGITAL PANEL INSTRUMENTS

For the purpose of selection, the instruments in this section are divided into three classes, each having its own Selection Guide:

1. 3- to 4 3/4-digit panel meters for general applications, powered by dc voltage furnished by the user's instrumentation-system +5V logic supply
2. 3- to 4 3/4-digit panel meters for general applications, powered by ac line voltage, and including multi-channel scanning and true-rms types
3. Single- and scanning multi-channel digital temperature meters for measurements with thermocouples, RTDs, thermistors, and AD590 semiconductor temperature sensors

The Selection Guides permit all the devices in each class to be compared in terms of their salient features, to narrow the field of choice to one or two devices, for which page locations are given. The data sheets in this Volume have technical

(continued on the next page)

		LOGIC (+5V) POWERED DIGITAL PANEL METERS						
		AD2026-1	AD2006D	AD2010	AD2021	AD2004	AD2027	AD2028
Digits; F.S. Range	3; -99 to +999mV	●						
	3½; ±199.9mV			●	●			
	±1.999V		●		●			
	±19.99V				●			
	4½; ±1.9999V					●	●	
	±19.999V						●	
	4¾; ±3.9999V							●
	±39.999V							●
Input Type	Ltd. Differential	●		●	●		●	●
	Differential		●					
	Floating					●		
Data Outputs		N/A						
	Character Serial				●		●	●
	Parallel BCD		●				●	●
	Parallel BCD Latched			●		●		
Display Type	LED	●		●	●	●	●	●
	Beckman		●					
Display Size		0.5/13	0.55/14	0.27/7	0.5/13	0.27/7	0.43/11	0.43/11
Case Depth[1] in/mm		0.65/17	4.08/104	0.84/21	1.31/33	2.52/64	4.08/104	4.08/104
Volume II Page		16-41	16-15	16-23	16-31	16-13	16-33	16-37

[1] All logic powered DPMs use industry standard case with 3.175" X 1.810" (80.65 X 45.97mm) cutout. All ac-powered DPMs except AD2006 use industry standard case with 3.930" X 1.682" (99.82 X 42.72mm) cutout. AD2006 uses same case as logic powered DPMS.

descriptions, specifications, and in many cases, applications information. Complete data sheets for most of these instruments, with further information on application and use of the products, are available upon request. General information on digital panel instruments can be found in the pages that follow the Selection Guides.

For temperature instrumentation, there are a number of other products dedicated to temperature measurement, included in this Databook, that may be of interest. They are to be found in these sections: Transducers & Signal Conditioners, μMAC-4000 Intelligent Measurement-and-Control Subsystems, and MACSYM. Power supplies for excitation of system-powered panel instruments may be found in the Power Supply section.

Finally, in the Synchro & Resolver Conversion section, there are the benchtop API1620 and API1718 Angle Position Indicators, which accept synchro or resolver input, convert to digital, and provide a 5-digit numerical LED display of the angle, and a 5-decade BCD or 16-bit binary data output.

		AC-POWERED DIGITAL PANEL METERS							
		AD2026-2	AD2006	AD2009	AD2016	AD2033[1]	AD2024	AD2025	AD2037
6-Channel Scanning									●
Digits; F.S. Range	3; -99 to +999mV	●							
	3½; ±199.9mV			●	●	●[1]			●
	±1.999V		●	●	●	●[1]			●
	±19.99V			●	●	●[1]			
	199.9V					●[1]			
	600V					●[1]			
	4½; ±1.9999V						●		
	±19.999V						●		
	4¾; ±3.9999V							●	
	±39.999V							●	
Input Type	Single Ended			●					
	Ltd. Differential				●		●	●	
	Differential		●						●
	Floating	●				●			●
	True RMS					●			
Data Outputs		N/A							
	Character Serial				●	●	●	●	
	Parallel BCD		●	●	●	●	●	●	
	Parallel BCD Latched								●
Display Type	LED	●			●	●	●	●	●
	Beckman		●	●					
Display Size		0.5/13	0.55/14	0.55/14	0.5/13	0.5/13	0.43/11	0.43/11	0.5/13
Case Depth[2] in/mm		2.44/63	4.08/104	4.15/105	4.15/112	4.48/114	4.48/114	4.48/114	5.80/147
Volume II Page		16-41	16-15	16-19	16-27	16-43	16-33	16-37	16-49

[1] Full scale inputs when reading out in dB are 500mV, 5V, 50V, 500V and 625V rms.

[2] All logic powered DPMs use industry standard case with 3.175" X 1.810" (80.65 X 45.97mm) cutout. All ac-powered DPMs except AD2006 use industry standard case with 3.930" X 1.682" (99.82 X 42.72mm) cutout. AD2006 uses same case as logic powered DPMs.

			DIGITAL TEMPERATURE METERS					
			AD2036	AD2037	AD2038	AD2040	AD2050	AD2051
Input	Number of Channels	1				●	●	●
		6	●	●	●			
Sensor (Determines Temperature Range)	Thermocouple Type	Switch Selected						●
		User Specified	●				●	
		J, K, T	●				●	●
		E, R, S					●	●
	AD590 (-55°C to +150°C)				●	●		
	RTD			●				
	Thermistor			●				
Features	Self-Calibration						●	●
	Cold-Junction Compensation		●				●	●
	Linearization		●				●	●
	Isolation		●	●	●		●[1]	●[1]
Readout	Digits	3+, 2-				●		
		3½	●	●	●		●	●
	LED Display Height	0.5", 13mm	●	●	●	●		
		0.56", 14.3mm					●	●
Digital Data Output	Isolated Parallel BCD		●	●	●			
	7-Bit Character-Serial ASCII						●	●
Analog Output	Voltage		●	●	●		●	●
	4-to-20mA Current Loop						●	●
Power Supply	AC Line		●	●	●		●	●
	DC	+7V to +15V					●	●
		+5V				●		
Volume II Page			16-47	16-49	16-49	16-51	16-55	16-55

[1] AC line-operated versions.

MICROCOMPUTER ANALOG I/O SUBSYSTEMS

Analog Devices Real-Time Interface (RTI) products provide a direct memory-mapped interface between popular microcomputers and analog input and output signals. Each RTI board is electrically and mechanically compatible with the bus it is designed to interface with. No additional interface logic or power are required for the board, which plugs directly into the microcomputer card cage.

As the Selection Guide indicates, there are Input-only, Output-only, and—in most cases—Input/Output cards available for each bus type. Within each card family, there are optional features available to provide a close fit to the individual user's application.

The Selection Guide provides selection information in capsule form, permitting card types to be matched to desired features. Additional information and complete specifications are provided on the individual card or family data sheets.

		MICROCOMPUTER BUS COMPATIBILITY									
		INTEL NATIONAL MULTIBUS$^{\mathrm{TM}}$						PRO-LOG MOSTEK STD BUS			
		RTI-1200-001	RTI-1200-004	RTI-1200-011	RTI-1200-014	RTI-1201	RTI-1202	RTI-1225	RTI-1226	RTI-1260	RTI-1262
Board Type	Input	●		●			●		●	●	
	Input/Output		●		●			●			
	Output					●					●
Channel Capacity	Input (Single ended/ differential)	16/8	16/8	32/16	32/16		16/8	16/8	16/8	32/16	
	Output		2		2	4		2			4
Input Resolution	10 Bits							●	●		
	12 Bits	●	●	●	●		●			●	
Output Resolution	8 Bits							●			
	12 Bits		●		●	●					●
Additional Features											
DC/DC Converter		●	●	●	●	●	●	●	●	●	●
Software PGA Gains of 1, 2, 4, 8V/V		●	●	●	●						
Resistor PGA Gains of 1 to 1000V/V							●			●	
4-20mA Output			●		●	●					●
Digital Output Drivers		●	●	●	●	●					
Volume II Page		17-5	17-5	17-5	17-5	17-7	17-9	17-11	17-11	17-19	17-19

MULTIBUS is a trademark of Intel Corporation.

(continued on the next page)

		MICROCOMPUTER BUS COMPATIBILITY									
		MOTOROLA MICROMODULE BUS			TEXAS INSTRUMENT TM990 BUS				DEC LSI BUS		
		RTI-1230	RTI-1231	RTI-1232	RTI-1240	RTI-1241	RTI-1242	RTI-1243	RTI-1250	RTI-1251	RTI-1252
Board Type	Input	●			●				●		
	Input/Output		●			●				●	
	Output			●			●	●			●
Channel Capacity	Input (Single ended/ differential)	32/16	32/16		32/16	32/16			32/16	16/8	
	Output		2	4		2	4	8		2	4
Input Resolution	10 Bits										
	12 Bits	●	●		●	●			●	●	
Output Resolution	8 Bits										
	12 Bits		●	●			●	●		●	●
Additional Features											
DC/DC Converter		●	●	●	●	●	●	●	●	●	●
Software PGA											
Gains of 1, 2, 4, 8V/V		●	●		●	●			●		
Resistor PGA											
Gains of 1 to 1000V/V		●			●	●			●	●	
4-20mA Output				●		●					
Digital Output Drivers				●			●	●			●
Volume II Page		17-13	17-13	17-13	17-15	17-15	17-15	17-15	17-17	17-17	17-17

AC/DC AND DC/DC POWER SUPPLIES

MODULAR AC/DC POWER SUPPLIES

SPECIFICATIONS (typical @ +25°C and 115V ac 60Hz unless otherwise noted)

	Type	Model	Output Voltage Volts	Output Current mA	Line Reg. Max %	Load Reg. Max %	Output Voltage Error Max	Ripple & Noise mV rms Max	Dimensions Inches
PC Board Mounted	Dual Output	915	±15	±25	0.2	0.2	±1%	1	3.5×2.5×0.875
		904	±15	±50	0.02	0.02	±200mV −0mV	0.5	3.5×2.5×0.875
		902	±15	±100	0.02	0.02	+300mV −0mV	0.5	3.5×2.5×1.25
		902-2	±15	±100	0.02	0.02	+300mV −0mV	0.5	3.5×2.5×0.875
		920	±15	±200	0.02	0.02	+300mV −0mV	0.5	3.5×2.5×1.25
		925	±15	±350	0.02	0.02	±1%	0.5	3.5×2.5×1.62
		921	±12	±240	0.02	0.02	+300mV −0mV	0.5	3.5×2.5×1.25
	Single Output	906	5	250	0.02	0.04	±1	1	3.5×2.5×0.875
		903	5	500	0.02	0.04	±1	1	3.5×2.5×1.25
		905	5	1000	0.02	0.05	±1	1	3.5×2.5×1.25
		922	5	2000	0.02	0.05	±1	1	3.5×2.5×1.62
		•928	5	3000	0.05	0.10	±2	5 (typ)	3.5×2.5×1.25
	Triple Output	923	±15	±100	0.02	0.02	±1	0.5	3.5×2.5×1.25
			+5	500	0.02	0.05	±1	0.5	
		•926	±15	±150	0.02	0.02	±2	0.5 (typ)	3.5×2.5×1.62
			+5	300	0.02	0.10	±2	1.0 (typ)	
		•927	±15	±150	0.02	0.02	±2	0.5 (typ)	3.5×2.5×1.62
			+5	1000	0.02	0.10	±2	1.0 (typ)	
		2B35J	±15	±65	0.08	0.1	(−0, +300mV)	0.5	3.5×2.5×1.25
			+1 to +15*	125	0.08	0.1		0.25	
		2B35K	±15	±65	0.01	0.02	(−0, +300mV)	0.5	3.5×2.5×1.25
			+1 to +15*	125	0.01	0.02		0.25	
Chassis Mounted	Dual Output	952	±15	±100	0.05	0.05	±2	1	4.4×2.7×1.44
		970	±15	±200	0.05	0.05	±2	1	4.4×2.7×1.44
		973	±15	±350	0.05	0.05	±2	1	4.4×2.7×2.00
		975	±15	±500	0.05	0.05	±2	1	4.4×2.7×2.00
	Single Output	955	5	1000	0.05	0.15	±2	2	4.4×2.7×1.44
		•976	5	3000	0.05	0.10	±2	5 (typ)	4.75×2.7×2.00
	Triple Output	•972	±15	±150	0.02	0.02	±2	0.5 (typ)	4.75×2.7×1.45
			+5	300	0.02	0.10	±2	1.0 (typ)	
		•974	±15	±150	0.02	0.02	±2	0.5 (typ)	4.75×2.7×1.45
			+5	1000	0.02	0.10	±2	1.0 (typ)	

*Resistor Programmable

•New product since *1980 Data-Acquisition Components and Subsystems Catalog*

MODULAR DC/DC CONVERTERS

SPECIFICATIONS (typical @ +25°C over the full range of input voltages unless otherwise noted)

Model	Output Voltage Volts	Output Current mA	Input Voltage Volts	Input Voltage Range Volts	Input Current Full Load	Output Voltage Error Max	Temperature Coefficient /°C Max	Efficiency Full Load Min	Dimensions Inches
943	5	1000	5	4.65/5.5	1.52A	±1%	±0.02%	62%	2.0×2.0×0.375
•957*	5	100	5	4.5/5.5	200mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
•958	5	100	5	4.5/5.5	200mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
941	±12	±150	5	4.65/5.5	1.17A	±0.5%	±0.01%	58%	2.0×2.0×0.375
•959*	±12	±40	5	4.5/5.5	384mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
•960	±12	±40	5	4.5/5.5	384mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
•961*	±15	±33	5	4.5/5.5	396mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
•962	±15	±33	5	4.5/5.5	396mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
•963*	±15	±33	12V	10.8/13.2	165mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
•964	±15	±33	12V	10.8/13.2	165mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
•965	±15	±190	5V	4.65/5.5	1.7A	±1%	±0.005% (typ)	62% (typ)	2.0×2.0×0.38
•966	±15	±190	12V	11.2/13.2	710mA	±1%	±0.005% (typ)	62% (typ)	2.0×2.0×0.38
•967	±15	±190	24V	22.3/26.4	350mA	±1%	±0.005% (typ)	62% (typ)	2.0×2.0×0.38
•968	±15	±190	28V	26/30.8	300mA	±1%	±0.005% (typ)	62% (typ)	2.0×2.0×0.38
949	±15	±60**	5	4.65/5.5	0.6A	±2%	±0.03%	58%	2.0×1.0×0.375
940	±15	±150	5	4.65/5.5	1.35A	±0.5%	±0.01%	62%	2.0×2.0×0.375
953	±15	±150	12	11/13	0.6A	±0.5%	±0.01%	62%	2.0×2.0×0.375
945	±15	±150	28	23/31	250mA	±0.5%	±0.01%	61%	2.0×2.0×0.375
951	±15	±410	5	4.65/5.5	3.7A	±0.5%	±0.01%	62%	3.5×2.5×0.88

*Unfiltered Models

**Single-ended or unbalanced operation is permissible such that total output current load does not exceed a total of 120mA.

•New product since *1980 Data-Acquisition Components and Subsystems Catalog*

Product Families Not in this Databook (But Still Available)

The information published in this Databook is intended to assist the user in choosing components for the design of *new* equipment, using the most cost-effective products available from Analog Devices. The popular product types listed below may have been designed into your circuits in the past, but they are no longer likely to be the most economic choice for your new designs. Nevertheless, we recognize that it is often a wise choice to refrain from redesigning proven equipment, and we are continuing to make these products available for use in existing designs or in designs for which they are uniquely suitable. Data sheets on these products are available upon request.

AD108/208/308
AD108A/208A/308A
AD111/211/311
AD351
AD502
AD511
AD512
AD514
AD520
AD523
AD528
AD530
AD531
AD559
AD801
AD2003
AD2008
AD2020
AD2022
AD2023
AD3900 Series
AD7513
AD7519
AD7570
AD7583
ADC-QM
ADC-QU
ADC-8S
ADC-10Z
ADC-12QZ
ADC-14I/17I
ADC-16Q
ADC1100
ADC1102
ADC1103
ADC1105
ADC1109
ADC1111
ADC1133
B100
BDM1615/1616/1617
DAC-M
DAC-QG
DAC-QM
DAC-QS
DAC-QZ
DAC-10DF
DAC-10Z
DAC1009
DAC1118
DAC1125
DAC1132
DAC1137
DAS1150
DAS1151
DGM1040
MDA-F
MDA-10Z
RTI-1220
RTI-1221
SCDX1623
SCM1677
SDC1604
SHA-1A
SHA-2A
SHA-3
SHA-4
SHA-5
SHA-1114
SHA-1134
SMC1007
SMX1004
SMX2607
SRX1005
SRX2605
STX1003
STX2603
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956

Substitution Guide for Product Families No Longer Available

The products listed in the left-hand column are no longer available from Analog Devices. In many cases, comparable functions and performance may be obtained with newer models, but–as a rule–they are not directly interchangeable. The closest recommended Analog Devices equivalent, physically and electrically, is listed in the right-hand column. If no equivalent is listed, or for further information, get in touch with Analog Devices.

Model	**Closest Recommended Equivalent**	**Model**	**Closest Recommended Equivalent**
AD501	AD511	107	118
AD505	AD509	108	52
AD508	AD517	110	48
AD513	AD503	111	AD308
AD516	AD506	114	119
AD550	None	115	43
AD551	None	120	50
AD553	None	142	48
AD555	AD7519	143	52
AD810-813	None	149	50
AD814-816	None	153	AD517
AD818	None	161	165
AD820-822	None	163	165
AD830-833	None	170	171
AD835-839	None	220	234
AD840-842	None	231	233
AD7516	AD7510DI	274J	284J
ADC1121	AD7550	279	286J
ADM501	ADM501/506	280	281
ADP501	ADP511	282J	292A
DAC-10H	DAC-10Z	283J	292A
DAC1112	DAC12QS	301 (module)	52
DAC1122	AD7541	302	310 (module)
IDC1703	IRDC1730/1731	350	None
MDA-LB	None	427	424
MDA-LD	None	602J10	AD612
MDA-UB	None	602J100	AD612
MDA-UD	None	602K100	AD612
MDA-8H	MDA-10Z	603	AD612
MDA-10H	MDA-10Z	901	904
MDA-11MF	AD7521	907	921
SERDEX	µMAC-4000	908	921
SHA-6	SHA1144	909	921
SSCT1621	None	931	None
TSDC1608-1611	TSL1612	932	None
2N3954	None	933	None
2N5900	None	935	None
41	AD515	948	947
47	48	971	921
101 (module)	45		
102	48		
106	118		

Analog Devices provides a wide array of FREE technical publications. These include data sheets for all products, catalogs, Application Notes and Guides, and two serial publications: *Analog Productlog*, a digest of new-product information, and *Analog Dialogue*, our technical journal, with in-depth discussions of products, technologies, and applications.

In addition to the free publications, three technical handbooks, a set of *Analog-Digital Conversion Notes*, and *Synchro and Resolver Conversion*, published at the end of 1980, are available at reasonable cost.

A brief description of this literature appears below. If you would like copies, or if you want to receive *Analog Productlog* and *Analog Dialogue*, please get in touch with Analog Devices or your nearby sales office.

CATALOGS

DATA ACQUISITION PRODUCTS DATABOOK (this book)
Two volumes of data sheets for all Analog Devices ICs, hybrids, modules, and subsystems recommended for new designs.

1981-1982 SHORT–FORM GUIDE to Electronic Products for Precision Measurement & Control
A 48-page catalog of all ADI Products.

APPLICATION NOTES AND GUIDES

ISOLATION AND INSTRUMENTATION AMPLIFIER DESIGNERS GUIDE
This guide explains, in detail, the differences between isolation and instrumentation amplifiers, and the applications for which each type is optimized (24 pages).

MULTIPLIER (Analog) APPLICATION GUIDE
Over 30 workable applications for the ubiquitous multiplier. Circuits, specifications and theory (50 pages).

APPLICATION GUIDE TO CMOS MULTIPLYING D TO A CONVERTERS
This 44-page guide includes detailed information on the internal design and successful application of CMOS MDACs. Typical circuits discussed include measurement, function generation, programmable filters, and audio control.

IC VOLTAGE TO FREQUENCY CONVERTER APPLICATION NOTES
Twenty-four pages of V to F converter applications.

A USER'S GUIDE TO IC INSTRUMENTATION AMPLIFIERS
Application note tells how they work, explains their specifications and provides an example of error budget computation (12 pages).

AN IC AMPLIFIER USER'S GUIDE TO DECOUPLING, GROUNDING, AND MAKING THINGS GO RIGHT FOR A CHANGE (8 pages)
A down-to-earth application note on the often ignored topic of ground management in combined analog and digital systems.

TRANSDUCER INTERFACING HANDBOOK
Isolation and Instrumentation Amplifiers Designers Guide
DESIGNER'S GUIDE TO HIGH RESOLUTION PRODUCTS
ANALOG DEVICES
1981-1982 SHORT FORM GUIDE
nonlinear circuits handbook

UNDERSTANDING HIGH SPEED (Video) A/D CONVERTER SPECIFICATIONS
A sixteen-page profusely illustrated application note.

DESIGNER'S GUIDE TO HIGH-RESOLUTION PRODUCTS
20-page brochure describes how to use 14-, 16-, and 18-bit Data Converters and where to apply them.

MACSYM SYSTEM NOTES:
Multitasking, RS-232 Interface, and P-I-D Control Loops

BOOKS

SYNCHRO & RESOLVER CONVERSION (1980)
Edited by Geoffrey Boyes
Everything you need to know about interfacing synchros, resolvers, and Inductosyns™ to digital and analog circuitry. $11.50

TRANSDUCER INTERFACING HANDBOOK (1980)
A Guide to Analog Signal Conditioning
Edited by D.H. Sheingold
A book for the electronic engineer who must interface temperature, pressure, force, level or flow transducers to electronics, these 260 pages tell how transducers work–as circuit elements–and how to connect them to electronic circuits for effective processing of their signals. Hardcover $14.50

MICROPROCESSOR SYSTEMS HANDBOOK (1977)
by Dr. D. Philip Burton and Dr. A. L. Dexter
Two hundred pages of concise explanation of microprocessor hardware and software, and how to interface to A/D and D/A converters. Hardcover $9.50

ANALOG-DIGITAL CONVERSION NOTES (1977)
Edited by D.H. Sheingold
A 250-page guide to A/D and D/A converters and their applications, illustrated by more than 275 diagrams and tables. $5.95

NONLINEAR CIRCUITS HANDBOOK (1974)
Edited by D. H. Sheingold
A 540-page guide to multiplying and dividing, squaring and rooting, rms-to-dc conversion, and multifunction modules with 325 illustrations. Principles, circuitry, performance, specifications, testing, and application of these devices. $5.95

Worldwide Service Directory

North America

Alabama	(205) 536-1506	(B)
Alaska	*(617) 329-4700	(B)
	*(714) 842-1717	(B)
Arizona	*(714) 842-1717	(B)
	(602) 949-0048	(C)
Arkansas	*(214) 231-5094	(B)
	*(713) 664-6704	(C)
	*(713) 664-5866	(S)
California	*(714) 842-1717	(B)
	*(408) 947-0633	(B)
Colorado	*(714) 842-1717	(B)
	(303) 443-5337	(C)
Connecticut	*(617) 329-4700	(B)
	(516) 673-1900	(C)
Delaware	*(215) 643-7790	(B)
Florida	(305) 855-0843	(B)
Georgia	(404) 476-3107	(B)
Hawaii	*(714) 842-1717	(B)
Idaho	*(206) 251-9950	(C)
	(303) 443-5337	(C)
	(206) 451-8223	(S)
Illinois	*(312) 653-5000	(B)
	(312) 446-9085	(C)
Indiana	*(312) 653-5000	(B)
	(317) 244-7867	(C)
Iowa	*(312) 653-5000	(B)
	(312) 446-9085	(C)
Kansas	*(312) 653-5000	(B)
	(913) 888-3330	(C)
	(913) 649-6996	(S)
Kentucky	*(312) 653-5000	(B)
	(317) 244-7867	(C)
	(513) 426-5551	(C)
Louisiana	*(713) 664-6704	(C)
	*(713) 664-5866	(S)
Maine	*(617) 329-4700	(B)
Maryland	*(215) 643-7790	(B)
	(301) 799-7490	(C)
	(301) 788-2380	(S)
Massachusetts	*(617) 329-4700	(B)
Michigan	*(312) 653-5000	(B)
	*(313) 644-1866	(S)
	(313) 882-1717	(C)
Minnesota	*(312) 653-5000	(B)
	(612) 835-2414	(C)
Mississippi	(205) 536-1506	(B)
Missouri	*(312) 653-5000	(B)
	(314) 725-5361	(C)
	(314) 878-5042	(S)
Montana	*(714) 842-1717	(B)
	(303) 443-5337	(C)
Nebraska	*(312) 653-5000	(B)
	(913) 888-3330	(C)
Nevada	*(408) 947-0633	(B)
	*(714) 842-1717	(B)
	(505) 262-1416	(B)
New Hampshire	*(617) 329-4700	(B)
New Jersey	*(617) 329-4700	(B)
	*(215) 643-7790	(B)
	*(201) 967-1126	(S)
	(516) 673-1900	(C)
New Mexico	(505) 262-1416	(B)
New York	*(617) 329-4700	(B)
	*(201) 967-1126	(S)
	(516) 673-1900	(C)
	(315) 454-9314	(C)
	(800) 962-5701	(C)
North Carolina	(919) 273-3040	(C)
	(919) 373-0380	(S)
North Dakota	*(312) 653-5000	(B)
	(612) 835-2414	(C)
Ohio	*(614) 764-8795	(C)
	*(216) 531-9455	(S)
	*(614) 764-8870	(S)
	(216) 321-3328	(C)
	(513) 426-5551	(C)
Oklahoma	*(214) 231-5094	(B)
	*(713) 664-6704	(C)
Oregon	*(206) 251-9550	(C)
	(503) 641-4463	(S)
Pennsylvania	*(215) 643-7790	(B)
	*(614) 764-8795	(C)
	*(216) 531-9455	(S)
	(412) 487-3801	(C)
Rhode Island	*(617) 329-4700	(B)
South Carolina	(919) 273-3040	(C)
	(803) 254-1971	(S)
South Dakota	*(312) 653-5000	(B)
	(612) 835-2414	(C)
Tennessee	(205) 536-1506	(B)
Texas	*(214) 231-5094	(B)
	*(713) 664-6704	(C)
	*(713) 664-5866	(S)
Utah	*(714) 842-1717	(B)
	(801) 268-8707	(C)
Vermont	*(617) 329-4700	(B)
Virginia	(301) 799-7490	(C)
	(804) 276-3979	(S)
Washington	*(206) 251-9550	(C)
	(206) 451-8223	(S)
West Virginia	*(614) 764-8795	(C)
	(412) 487-3801	(C)
	(804) 276-3979	(S)
Wisconsin	*(312) 653-5000	(B)
	(414) 784-7736	(C)
Wyoming	*(714) 842-1717	(B)
	(303) 443-5337	(C)
Puerto Rico	*(617) 329-4700	(B)
	(305) 855-0843	(S)
Canada	(416) 625-7752	(B)
	(613) 722-7667	(B)
	(514) 694-5343	(B)
	(604) 984-4141	(B)
Mexico	*(617) 329-4700	(B)

International

Argentina	37-9890	(C)
Australia	02/43 93288	(B)
	580 74 44	(B)
Austria	235-5550	(B)
Belgium	*031/37 48 03	(B)
Brazil	230-0277	(C)
CMEA COUNTRIES	*022/31 57 60 (Switzerland)	(B)
	0222/859304 (Austria)	(C)
Denmark	*02/84 58 00	(B)
Finland	90-738265	(B)
France	*01-687-3411	(B)
	*76 22 21 90	(B)
	*61 40 85 62	(B)
	*33 26 07 61	(B)
Holland	*016/20-51080	(B)
Hong Kong	*(617) 329-4700 (U.S.A.)	(B)
India	664850	(B)
Ireland	*01 941 0466 (United Kingdom)	(B)
Israel	*052-28995	(B)
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